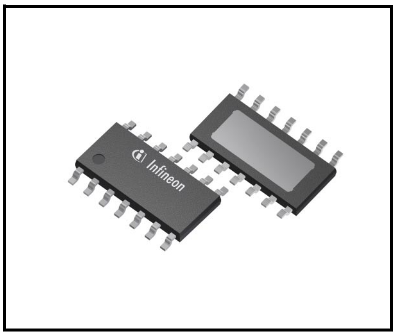
PROFET™ + 24V

BTT6080-1ERL

Smart High-Side Power Switch Single Channel, 80 mΩ

AEC Qualified RoHS ISO 26262 ready

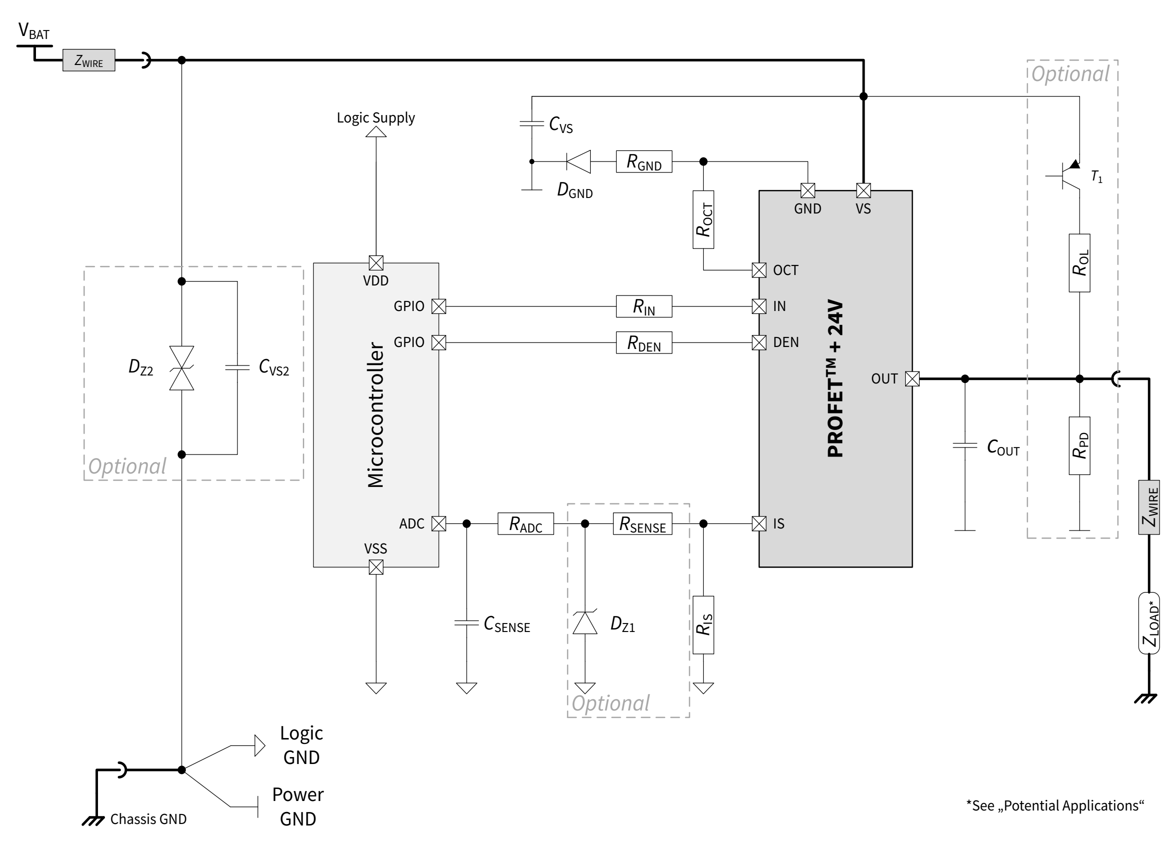
Package	PG-TDSO-14
Marking	6080-1ERL



1 Overview

Potential applications

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Suitable for driving electronic loads (e.g. radar, camera modules)
- Suitable for 12 V and 24 V truck and transportation system
- Protection of system supply
- Main switch for ECU power supply



Application Diagram with BTT6080-1ERL

Basic Features

- Adjustable current limitation with OCT-pin
- One channel device
- Very low stand-by current
- 3.3 V and 5 V compatible logic inputs
- Electrostatic discharge protection (ESD)
- Optimized electromagnetic compatibility
- Logic ground independent from load ground
- Very low power DMOS leakage current in OFF state
- Green product (RoHS compliant) and AEC qualified

Description

The BTT6080-1ERL is a 80 mΩ single channel Smart High-Side Power Switch, embedded in a PG-TDSO-14, Exposed Pad package, providing protective functions and diagnosis. The power transistor is built by an N-channel vertical power MOSFET with charge pump. The device offers an adjustable current limitation to offer higher reliability for protecting the system.

Table 1 Product Summary

Parameter	Symbol	Value
Nominal operating voltage range	V_{NOM}	8 V ... 36 V
Maximum supply voltage	$V_{\mathrm{S(LD)}}$	65 V
Maximum ON state resistance at T_{J} = 150°C	$R_{\mathrm{DS(ON)}}$	150 mΩ
Nominal load current	$I_{\mathrm{L(NOM)}}$	2.5 A
Typical current sense ratio	k_{ILIS}	1250
Adjustable current limitation	I_{LIM}	0.81 A to 5.56 A
Maximum standby current with load at T_{J} = 25°C	$I_{\mathrm{S(OFF)}}$	0.5 µA

Diagnostic Functions

- Proportional load current sense
- Open load in ON and OFF
- Short circuit to battery and ground
- Overtemperature, Stable diagnostic signal during short circuit
- Enhanced k_{ILIS} dependency with temperature and load current

Protection Functions

- Stable behavior during undervoltage
- Reverse polarity protection with external components
- Secure load turn-off during loss of logic ground with external components
- Overtemperature protection with latch
- Overvoltage protection with external components
- Enhanced short circuit operation

2 Block Diagram

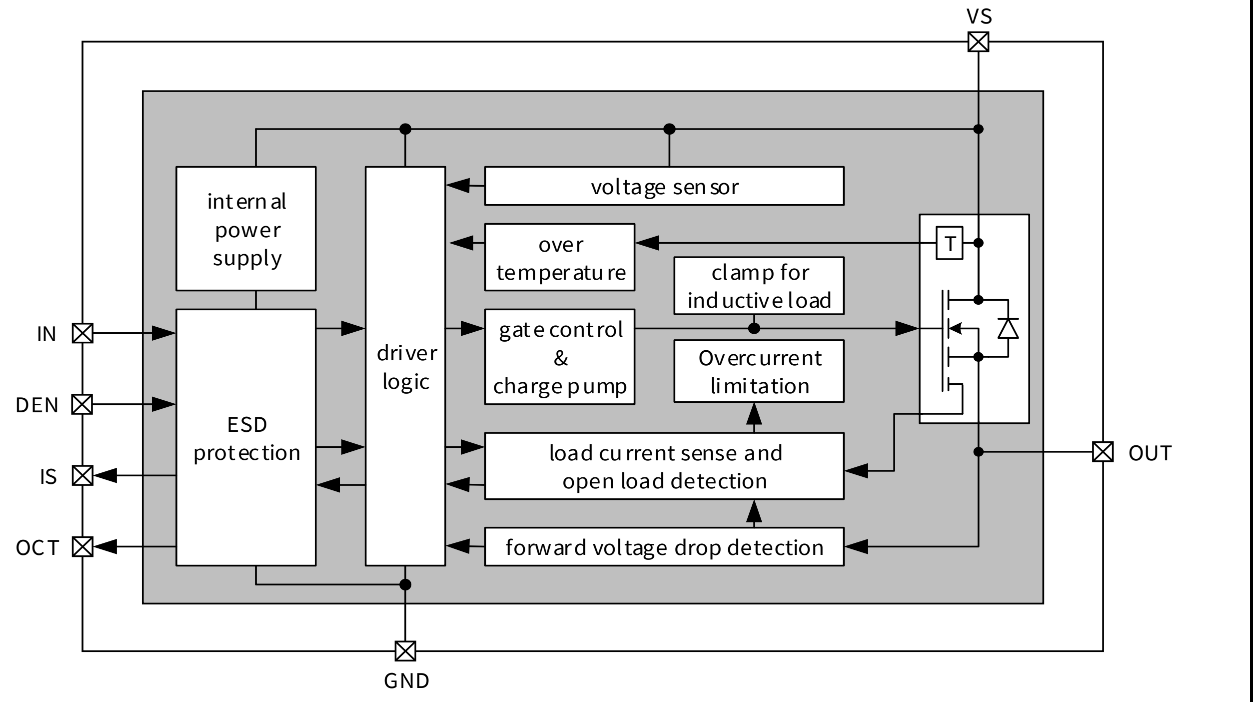


Figure 1 Block Diagram for the BTT6080-1ERL

3 Pin Configuration

3.1 Pin Assignment

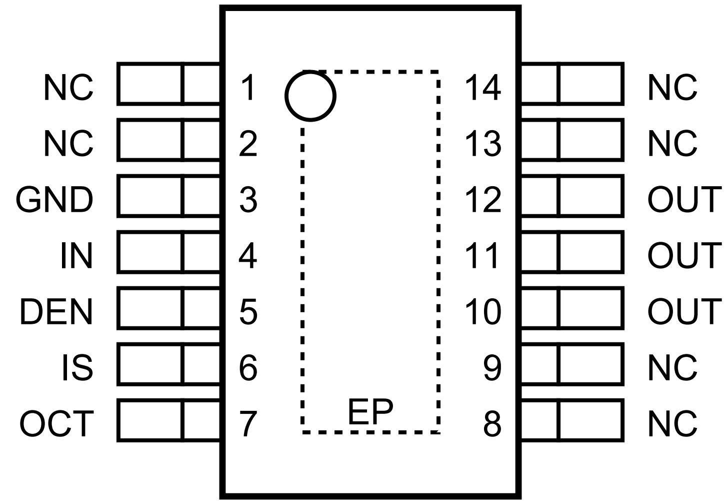


Figure 2 **Pin configuration PG-TDSO-14**

3.2 Pin Definitions and Functions

Table 2 **Pin Definitions and Functions**

Pin	Symbol	Function
Cooling Tab	VS	**Voltage supply;** Battery voltage
1, 2, 8, 9, 13, 14	NC	**Not connected;** No internal connection to the chip
3	GND	**Ground;** Ground connection
4	IN	**Input channel;** Input signal for channel activation
5	DEN	**Diagnostic enable;** Digital signal to enable/disable the diagnosis of the device
6	IS	**Sense;** Sense current of the selected channel
7	OCT	**Adjustable overcurrent threshold**; A resistor R_{OCT} needs to be connected between OCT pin and GND pin to adjust the overcurrent threshold. R_{OCT} resistor must be placed close to the OCT pin
10, 11, 12	OUT	**Output;** Protected high side power output channel[1]

[1] All output pins must be connected together on the PCB. All pins of the output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow

3.3 Voltage and Current Definition

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

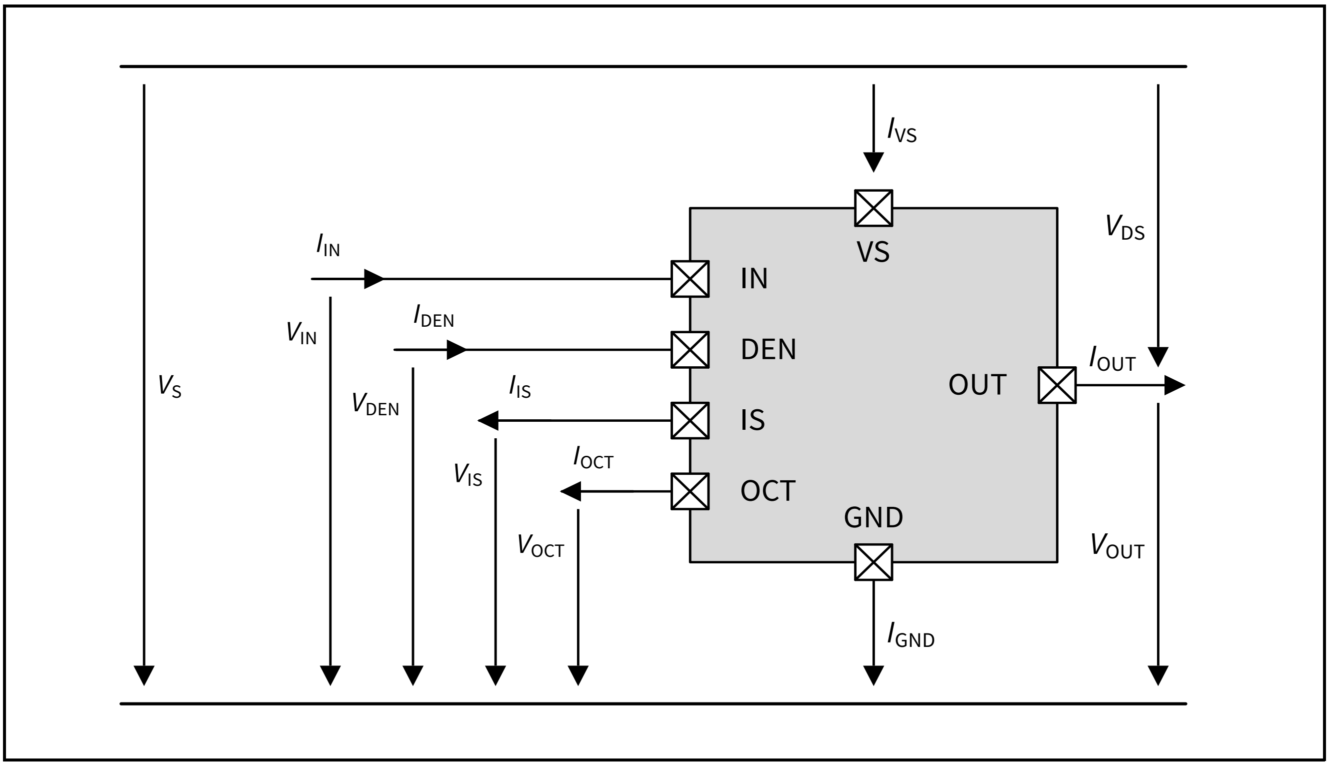


Figure 3 Voltage and Current Definition

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings[1)]

T_J = -40°C to +150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Supply voltage	V_S	-0.3	–	48	V	–	P_4.1.1
Reverse polarity voltage	$-V_{S(REV)}$	0	–	28	V	$t < 2$ min $T_A = 25°C$ $R_L \geq 25\ \Omega$ $R_{GND} = 150\ \Omega$	P_4.1.2
Supply voltage for short circuit protection	$V_{BAT(SC)}$	0	–	36	V	$R_{ECU} = 20\ m\Omega$ $R_{Cable} = 16\ m\Omega/m$ $L_{Cable} = 1\ \mu H/m$, $l = 0$ or 40 m See **Chapter 6** and **Figure 30**	P_4.1.3
Supply voltage for Load dump protection	$V_{S(LD)}$	–	–	65	V	[2)] $R_I = 2\ \Omega$ $R_L = 25\ \Omega$	P_4.1.12
Input Pins							
Voltage at INPUT pin	V_{IN}	-0.3	–	6 7	V	– t < 2 min	P_4.1.13
Current through INPUT pin	I_{IN}	-2	–	2	mA	–	P_4.1.14
Voltage at DEN pin	V_{DEN}	-0.3	–	6 7	V	– t < 2 min	P_4.1.15
Current through DEN pin	I_{DEN}	-2	–	2	mA	–	P_4.1.16
OCT Pin							
Voltage at OCT pin	V_{OCT}	-0.3	–	V_S	V	–	P_4.1.5
Current through OCT pin	I_{OCT}	-2	–	2	mA	–	P_4.1.6
Sense Pin							
Voltage at IS pin	V_{IS}	-0.3	–	V_S	V	–	P_4.1.19
Current through IS pin	I_{IS}	-25	–	50	mA	–	P_4.1.20
Power Stage							
Load current	$\| I_L \|$	–	–	$I_{L(LIM)}$	A	–	P_4.1.21
Power dissipation (DC)	P_{TOT}	–	–	1.6	W	$T = 85°C$ $T_J < 150°C$	P_4.1.22

Table 3 Absolute Maximum Ratings[1)]

T_J = -40°C to +150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Maximum energy dissipation Single pulse	E_{AS}	–	–	45	mJ	I_L = 2.5 A $T_{J(0)}$ = 150°C V_S = 28 V	P_4.1.23
Voltage at power transistor	V_{DS}	–	–	65	V	–	P_4.1.26
Current							
Current through ground pin	I_{GND}	-20 -200	–	20 20	mA	– t < 2 min	P_4.1.27
Temperature							
Junction temperature	T_J	-40	–	150	°C	–	P_4.1.28
Storage temperature	T_{STG}	-55	–	150	°C	–	P_4.1.30
ESD Susceptibility							
ESD susceptibility (all pins)	V_{ESD}	-2	–	2	kV	3) HBM	P_4.1.31
ESD susceptibility OUT Pin vs. GND and VS connected	V_{ESD}	-4	–	4	kV	3) HBM	P_4.1.32
ESD susceptibility	V_{ESD}	-500	–	500	V	4) CDM	P_4.1.33
ESD susceptibility pin (corner pins)	V_{ESD}	-750	–	750	V	4) CDM	P_4.1.34

1) Not subject to production test. Specified by design
2) $V_{S(LD)}$ is setup without the DUT connected to the generator per ISO 7637-1
3) ESD susceptibility, Human Body Model "HBM" according to AEC Q100-002
4) ESD susceptibility, Charged Device Model "CDM" according to AEC Q100-011

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 4 Functional Range T_J = -40°C to +150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating voltage	V_{NOM}	8	28	36	V	–	P_4.2.1
Extended operating voltage	$V_{S(OP)}$	5	–	48	V	[2] V_{IN} = 4.5 V R_L = 25 Ω V_{DS} < 0.5 V See **Figure 15**	P_4.2.2
Minimum functional supply voltage	$V_{S(OP)\_MIN}$	3.8	4.3	5	V	[1] V_{IN} = 4.5 V R_L = 25 Ω From I_{OUT} = 0 A to V_{DS} < 0.5 V; See **Figure 15**	P_4.2.3
Undervoltage shutdown	$V_{S(UV)}$	2.5	3.5	4.1	V	[1] V_{IN} = 4.5 V V_{DEN} = 0 V R_L = 25 Ω From V_{DS} < 1 V to I_{OUT} = 0 A See **Figure 15**	P_4.2.4
Undervoltage shutdown hysteresis	$V_{S(UV)\_HYS}$	–	850	–	mV	[2] –	P_4.2.13
Operating current channel active	I_{GND}	–	2.5	3.5	mA	V_{IN} = 5.5 V V_{DEN} = 5.5 V Device in $R_{DS(ON)}$ V_S = 36 V	P_4.2.5
Standby current for whole device with load (ambient)	$I_{S(OFF)}$	–	0.1	0.5	µA	[1] V_S = 36 V V_{OUT} = 0 V V_{IN} floating V_{DEN} floating T_J ≤ 85°C	P_4.2.7
Maximum standby current for whole device with load	$I_{S(OFF)\_150}$	–	3	15	µA	V_S = 36 V V_{OUT} = 0 V V_{IN} floating V_{DEN} floating T_J = 150°C	P_4.2.10
Standby current for whole device with load, diagnostic active	$I_{S(OFF\_DEN)}$	–	1.3	–	mA	[2] V_S = 36 V V_{OUT} = 0 V V_{IN} floating V_{DEN} = 5.5 V	P_4.2.8

1) Test at T_J = -40°C only
2) Not subject to production test. Specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Table 5 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	2.7	–	K/W	1)	P_4.3.1
Junction to ambient	R_{thJA}	–	29.5	–	K/W	1) 2)	P_4.3.2

1) Not subject to production test. Specified by design

2) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board with 1 W power dissipation at T_A=105°C ; The product (chip + package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 7 µm Cu, 2 x 35 µm Cu). Where applicable, a thermal via array under the exposed pad contacts the first inner copper layer. Please refer to **Figure 4**

4.3.1 PCB Set-up

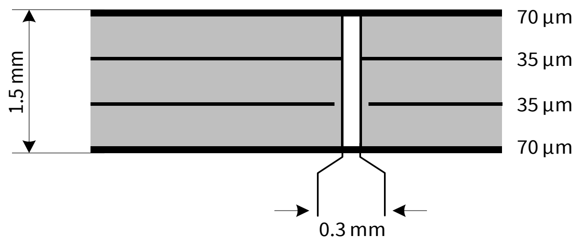


Figure 4 2s2p PCB Cross Section

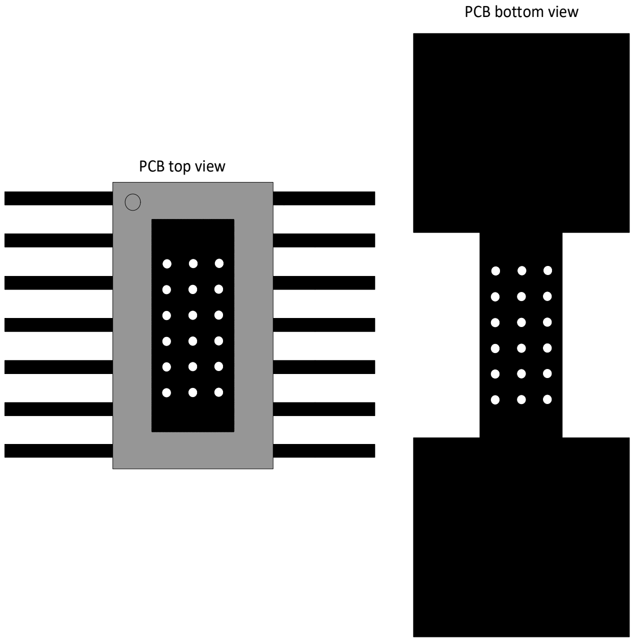


Figure 5 PC Board Top and Bottom View for Thermal Simulation with 600 mm² Cooling Area

4.3.2 Thermal Impedance

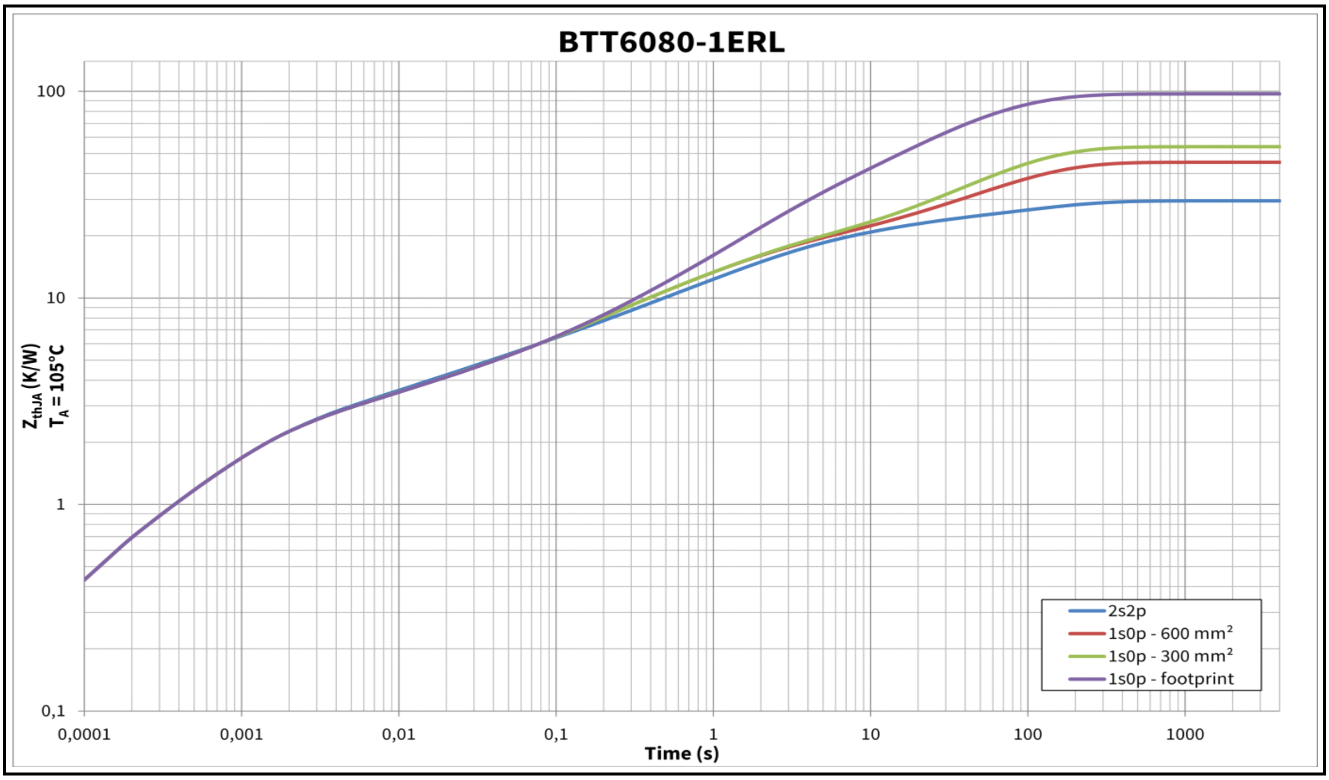


Figure 6 Typical Thermal Impedance. 2s2p set-up according Figure 4

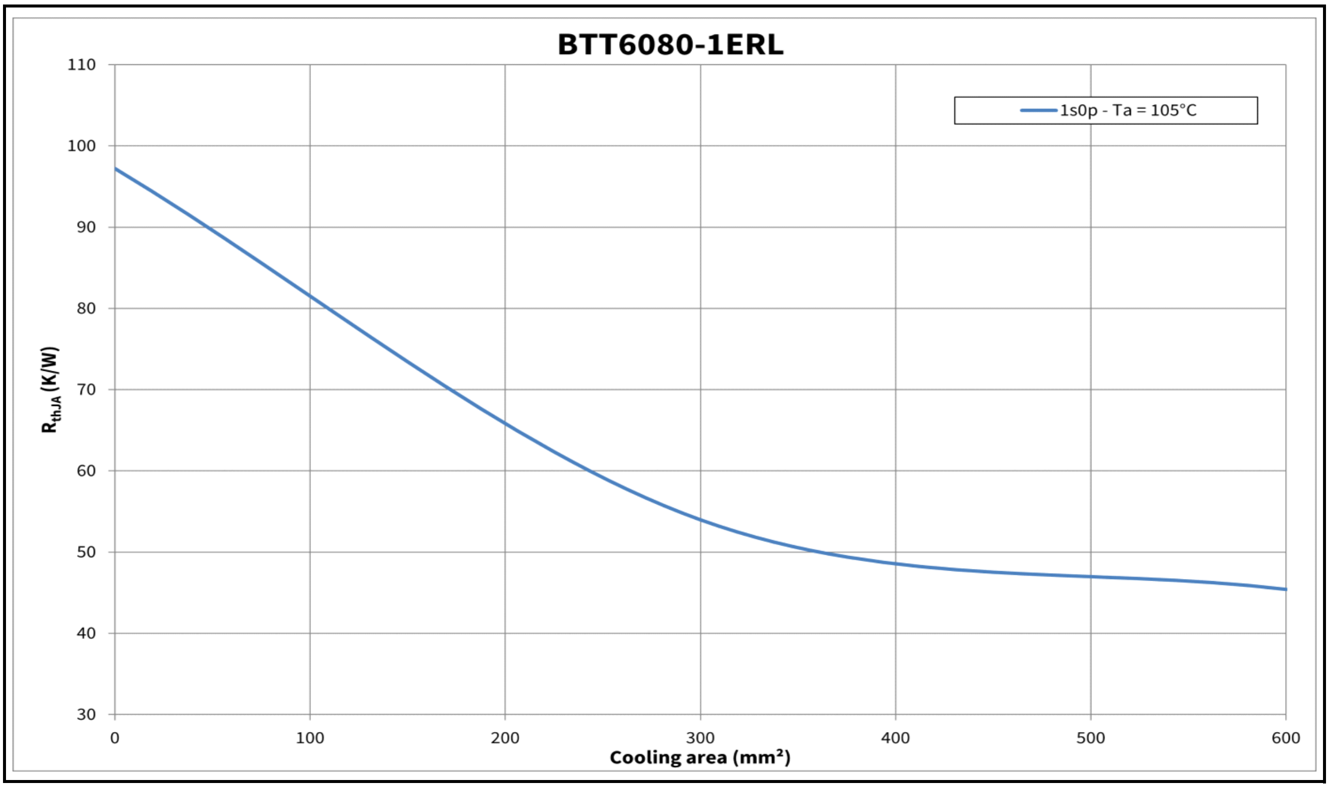


Figure 7 Typical Thermal Resistance. PCB set-up 1s0p

5 Power Stage

The power stage is built using an N-channel vertical power MOSFET (DMOS) with charge pump.

5.1 Output ON-State Resistance

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature T_J. **Figure 8** shows the dependencies in terms of temperature for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 6.4**.

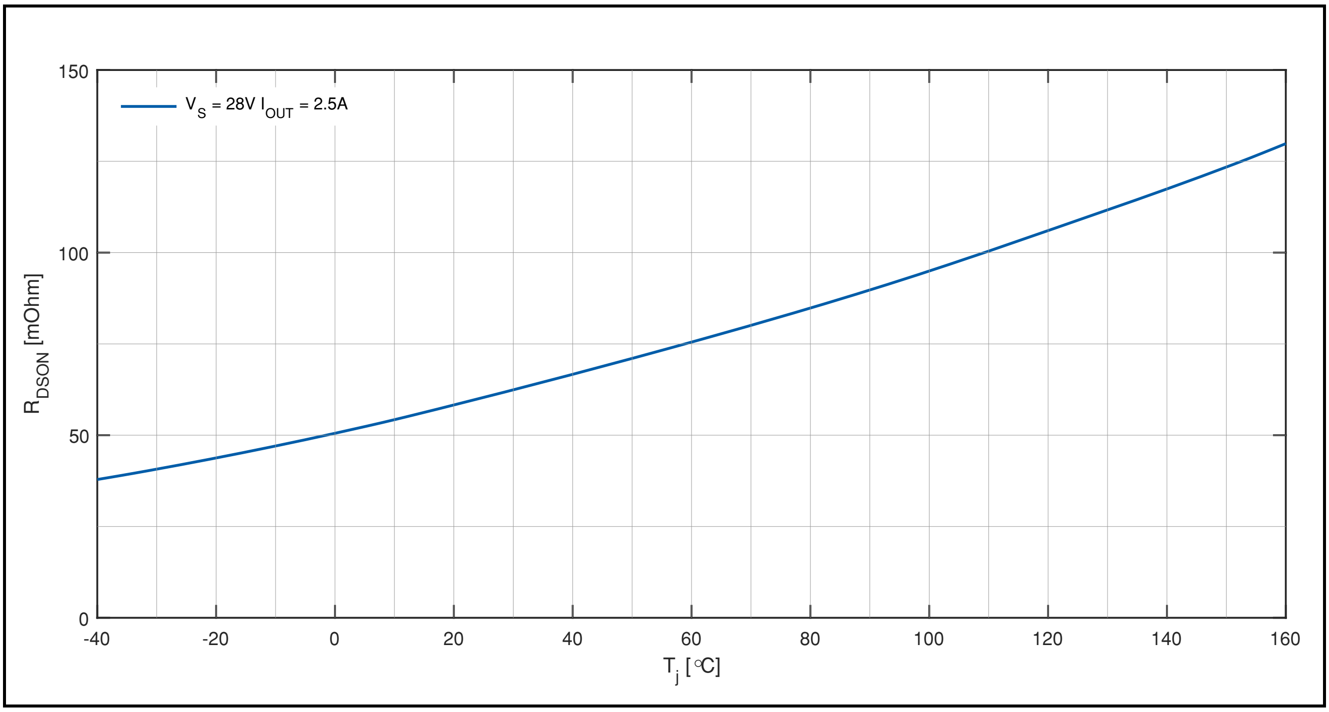


Figure 8 Typical ON-State Resistance

A “high” signal (see **Chapter 8**) at the input pin causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

5.2 Turn ON/OFF Characteristics with Resistive Load

Figure 9 shows the typical timing when switching a resistive load.

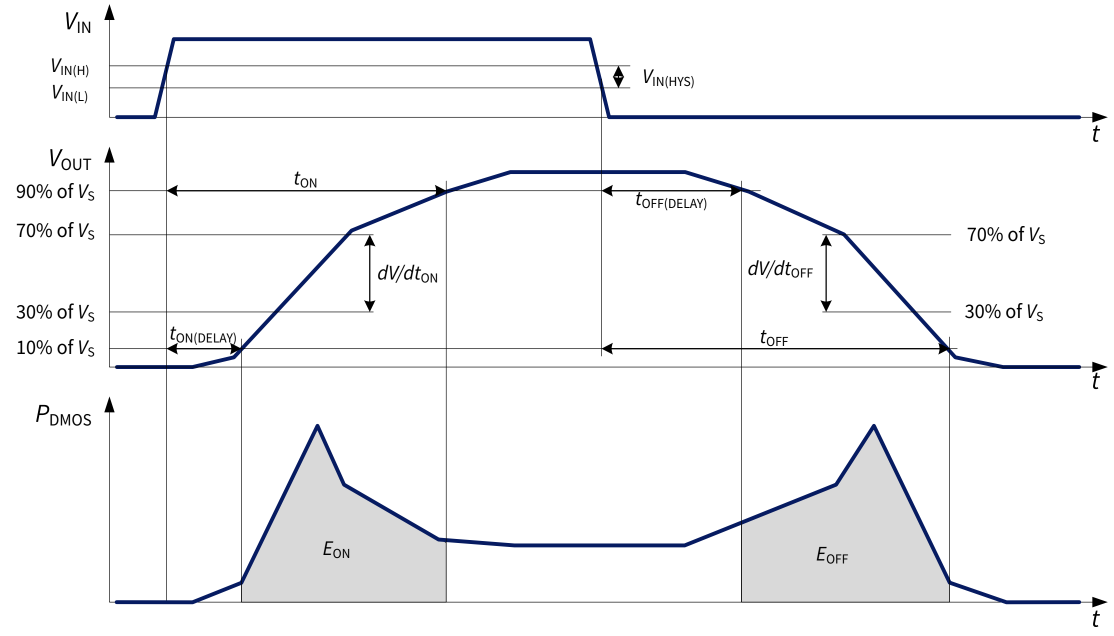


Figure 9 **Switching a Resistive Load Timing**

5.3 Inductive Load

5.3.1 Output Clamping

When switching OFF inductive loads with high side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device by avalanche due to high voltages, there is a voltage clamp mechanism $Z_{DS(AZ)}$ implemented that limits negative output voltage to a certain level (V_S - $V_{DS(AZ)}$). Please refer to **Figure 10** and **Figure 11** for details. Nevertheless, the maximum allowed load inductance is limited.

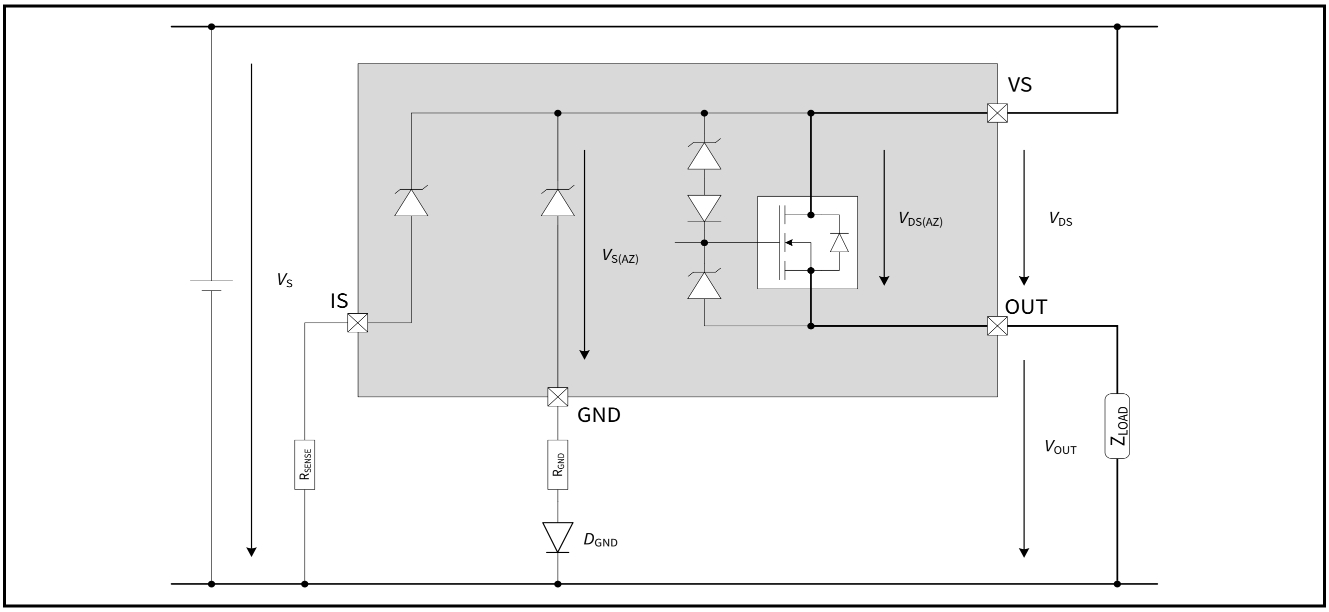


Figure 10 Output Clamp

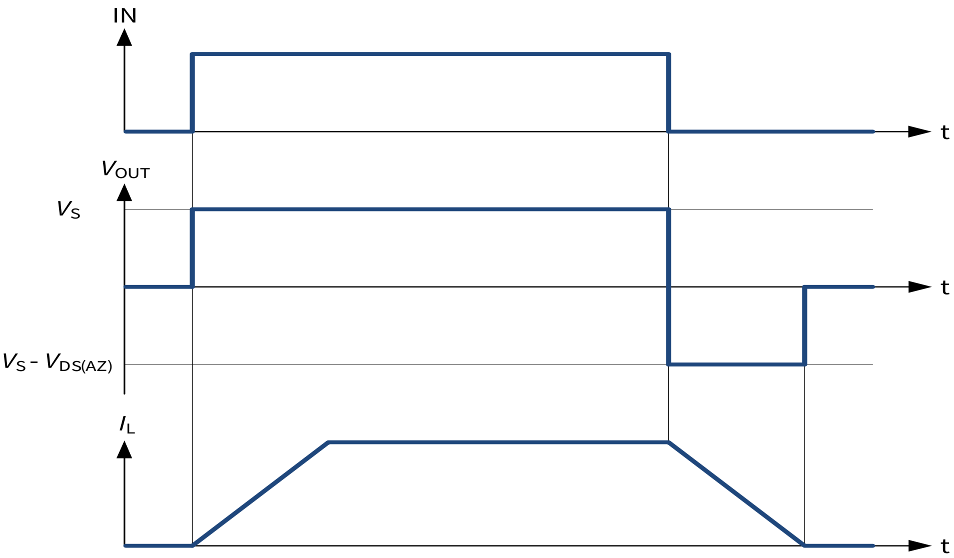


Figure 11 Switching an Inductive Load Timing

5.3.2 Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the BTT6080-1ERL. This energy can be calculated with following equation:

$$E = V_{\mathrm{DS(AZ)}} \cdot \frac{L}{R_{\mathrm{L}}} \cdot \left[\frac{V_{\mathrm{S}} - V_{\mathrm{DS(AZ)}}}{R_{\mathrm{L}}} \cdot \ln\left(1 - \frac{R_{\mathrm{L}} \cdot I_{\mathrm{L}}}{V_{\mathrm{S}} - V_{\mathrm{DS(AZ)}}}\right) + I_{\mathrm{L}}\right] \tag{5.1}$$

Following equation simplifies under the assumption of $R_{\mathrm{L}} = 0\ \Omega$.

$$E = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(1 - \frac{V_{\mathrm{S}}}{V_{\mathrm{S}} - V_{\mathrm{DS(AZ)}}}\right) \tag{5.2}$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 12** for the maximum allowed energy dissipation as a function of the load current.

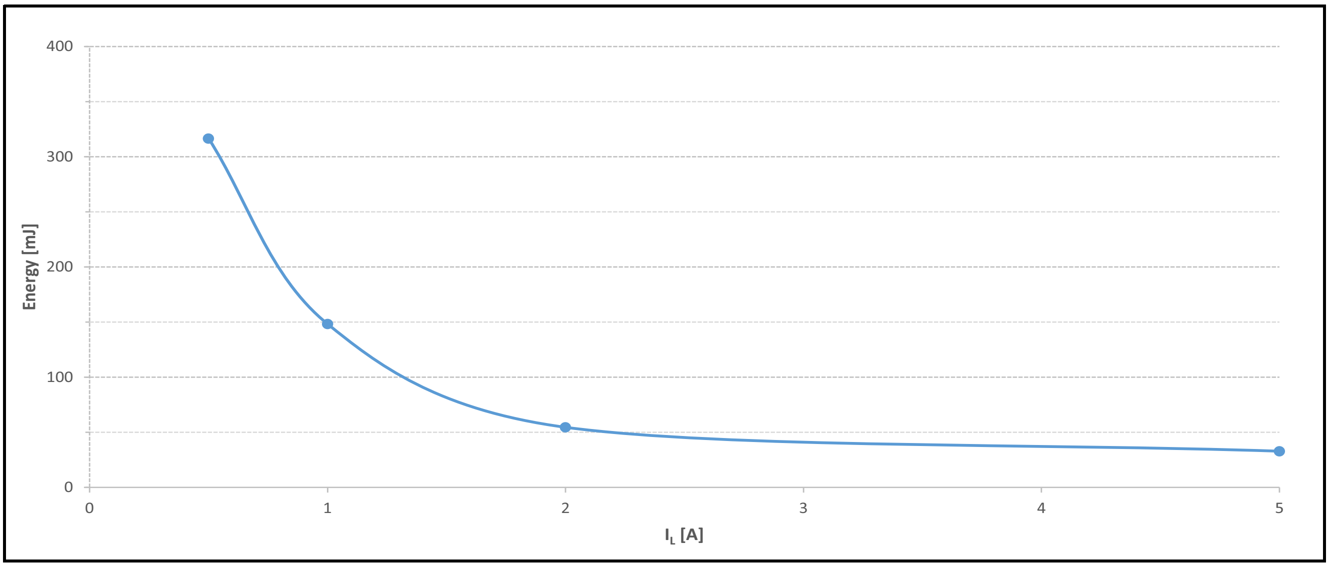


Figure 12 Maximum Energy Dissipation Single Pulse, $T_{\mathrm{J\_START}}$ = 150°C; V_{S} = 28 V

5.4 Inverse Current Capability

In case of inverse current, meaning a voltage V_{INV} at the OUTput higher than the supply voltage V_S, a current $I_{L(INV)}$ will flow from output to V_S pin via the body diode of the power transistor (please refer to **Figure 13**). The output stage follows the state of the IN pin, except if the IN pin goes from OFF to ON during inverse. In that particular case, the output stage is kept OFF until the inverse current disappears. Nevertheless, the current $I_{L(INV)}$ should not be higher than $I_{L(INV)}$. If the channel is OFF, the diagnostic will detect an open load at OFF. If the channel is ON, the diagnostic will detect open load at ON (the overtemperature signal is inhibited). At the appearance of V_{INV}, a parasitic diagnostic can be observed. After, the diagnosis is valid and reflects the output state. At V_{INV} vanishing, the diagnosis is valid and reflects the output state. During inverse current, no protection functions are available.

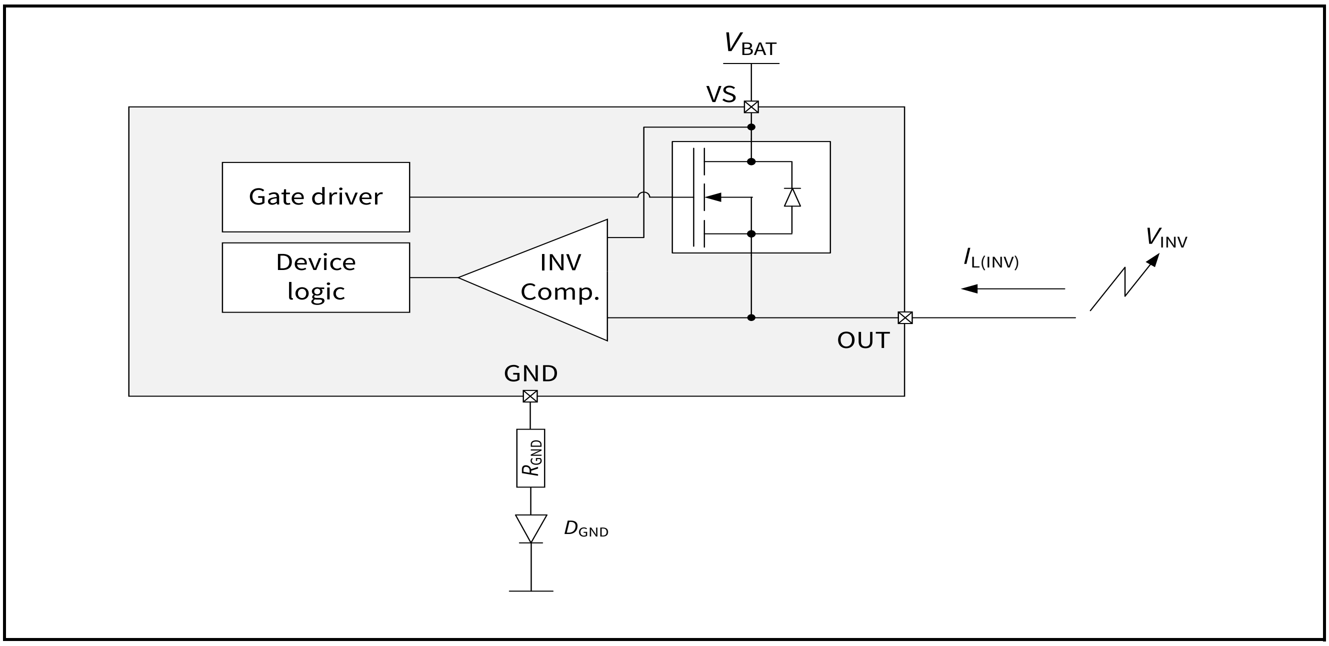


Figure 13 Inverse Current Circuitry

5.5 Electrical Characteristics Power Stage

Table 6 Electrical Characteristics: Power Stage

V_S = 8 V to 36 V, T_J = -40°C to +150°C (unless otherwise specified).
Typical values are given at V_S = 28 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ON-state resistance per channel	$R_{DS(ON)\_150}$	–	125	150	mΩ	I_L = 2.5 A V_{IN} = 4.5 V T_J = 150 °C See **Figure 8**	P_5.5.1
ON-state resistance per channel	$R_{DS(ON)\_25}$	–	75	–	mΩ	[1] T_J = 25 °C	P_5.5.21
Nominal load current	$I_{L(NOM)}$	–	2.5	–	A	[1] T_A = 85 °C T_J < 150 °C	P_5.5.2
I_{LIM} fraction to calculate the maximum application load current	$I_{LIM01\_fraction}$	–	–	0.70	–	[1][2] $I_{L(APP),MAX} = I_{LIM01\_fraction} \times I_{LIM}$ $0.81\ A \le I_{LIM} < 1.87\ A$	P_5.5.3
I_{LIM} fraction to calculate the maximum application load current	$I_{LIM02\_fraction}$	–	–	0.75	–	[1][2] $I_{L(APP),MAX} = I_{LIM02\_fraction} \times I_{LIM}$ $1.87\ A \le I_{LIM} < 2.30\ A$	P_5.5.22
I_{LIM} fraction to calculate the maximum application load current	$I_{LIM03\_fraction}$	–	–	0.80	–	[1][2] $I_{L(APP),MAX} = I_{LIM03\_fraction} \times I_{LIM}$ $2.30\ A \le I_{LIM} < 4.60\ A$	P_5.5.23
I_{LIM} fraction to calculate the maximum application load current	$I_{LIM04\_fraction}$	–	–	0.85	–	[1][2] $I_{L(APP),MAX} = I_{LIM04\_fraction} \times I_{LIM}$ $4.60\ A \le I_{LIM} \le 5.56\ A$	P_5.5.24
Output voltage drop limitation at small load currents	$V_{DS(NL)}$	–	12	25	mV	$I_L = I_{L0}$ = 50 mA	P_5.5.4
Drain to source clamping voltage $V_{DS(AZ)} = [V_S - V_{OUT}]$	$V_{DS(AZ)}$	65	70	75	V	I_{DS} = 20 mA See **Figure 11**	P_5.5.5
Output leakage current $T_J \le$ 85°C	$I_{L(OFF)}$	–	0.05	0.5	µA	[3] V_{IN} floating V_{OUT} = 0 V $T_J \le$ 85°C	P_5.5.6
Output leakage current T_J = 150°C	$I_{L(OFF)\_150}$	–	3	10	µA	V_{IN} floating V_{OUT} = 0 V T_J = 150°C	P_5.5.8

Table 6 Electrical Characteristics: Power Stage (cont'd)

V_S = 8 V to 36 V, T_J = -40°C to +150°C (unless otherwise specified).
Typical values are given at V_S = 28 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Inverse current capability	$I_{L(INV)}$	–	2.5	–	A	1) $V_S < V_{OUT}$ $T_J < 150°C$ $\Delta T_J \leq 80K$ See **Figure 13**	P_5.5.9
Slew rate 30% to 70% V_S	dV/dt_{ON}	0.3	0.8	1.4	V/µs	$R_L = 25\ \Omega$ $V_S = 28\ V$ $I_{OCT} = 97.84\ \mu A$ See **Figure 9**	P_5.5.11
Slew rate 70% to 30% V_S	$-dV/dt_{OFF}$	0.3	0.8	1.4	V/µs		P_5.5.12
Slew rate matching $dV/dt_{ON} - dV/dt_{OFF}$	$\Delta dV/dt$	-0.3	0	0.3	V/µs		P_5.5.13
Turn-ON time to $V_{OUT} = 90\%\ V_S$	t_{ON}	20	60	150	µs		P_5.5.14
Turn-OFF time to $V_{OUT} = 10\%\ V_S$	t_{OFF}	20	50	150	µs		P_5.5.15
Turn-ON / OFF matching $t_{OFF} - t_{ON}$	Δt_{SW}	-50	0	50	µs		P_5.5.16
Turn-ON time to $V_{OUT} = 10\%\ V_S$	t_{ON_delay}	–	30	70	µs		P_5.5.17
Turn-OFF time to $V_{OUT} = 90\%\ V_S$	t_{OFF_delay}	–	30	70	µs		P_5.5.18
Switch ON energy	E_{ON}	–	0.32	–	mJ	1) $R_L = 25\ \Omega$ $V_{OUT} = 90\%\ V_S$ $V_S = 36\ V$ $I_{OCT} = 97.84\ \mu A$	P_5.5.19
Switch OFF energy	E_{OFF}	–	0.30	–	mJ	1) $R_L = 25\ \Omega$ $V_{OUT} = 10\%\ V_S$ $V_S = 36\ V$ $I_{OCT} = 97.84\ \mu A$	P_5.5.20

1) Not subject to production test, specified by design

2) This parameter describes the safety margin between the adjustable current limitation and the expected load current of the application. This is essential to prevent the unintentional activation of the current limitation circuit during normal operation. Keep in mind that when designing a real-world application, thermal constraints can impact the maximum allowed current ($I_{L(APP)}$) to prevent overheating. This is particularly crucial when the current limit is set to high values and the ambient temperature (T_{AMB}) is elevated. To ensure reliable operation, it's essential to consider the thermal design of the application and the resulting thermal budget in order to not exceed the maximum allowed junction temperature (T_J) of 150°C.

3) Test at T_J = -40°C only

6 Protection Functions

The device provides integrated protection functions. These functions are designed to prevent the destruction of the IC from fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed for neither continuous nor repetitive operation.

6.1 Loss of Ground Protection

In case of loss of the module ground and the load remains connected to ground, the device protects itself by automatically turning OFF (when it was previously ON) or remains OFF, regardless of the voltage applied on IN pin.

In case of loss of device ground, it is recommended to use input resistors between the microcontroller and the BTT6080-1ERL to ensure switching OFF of the channel.

In case of loss of module or device ground, a current ($I_{OUT(GND)}$) can flow out of the DMOS. **Figure 14** sketches the situation.

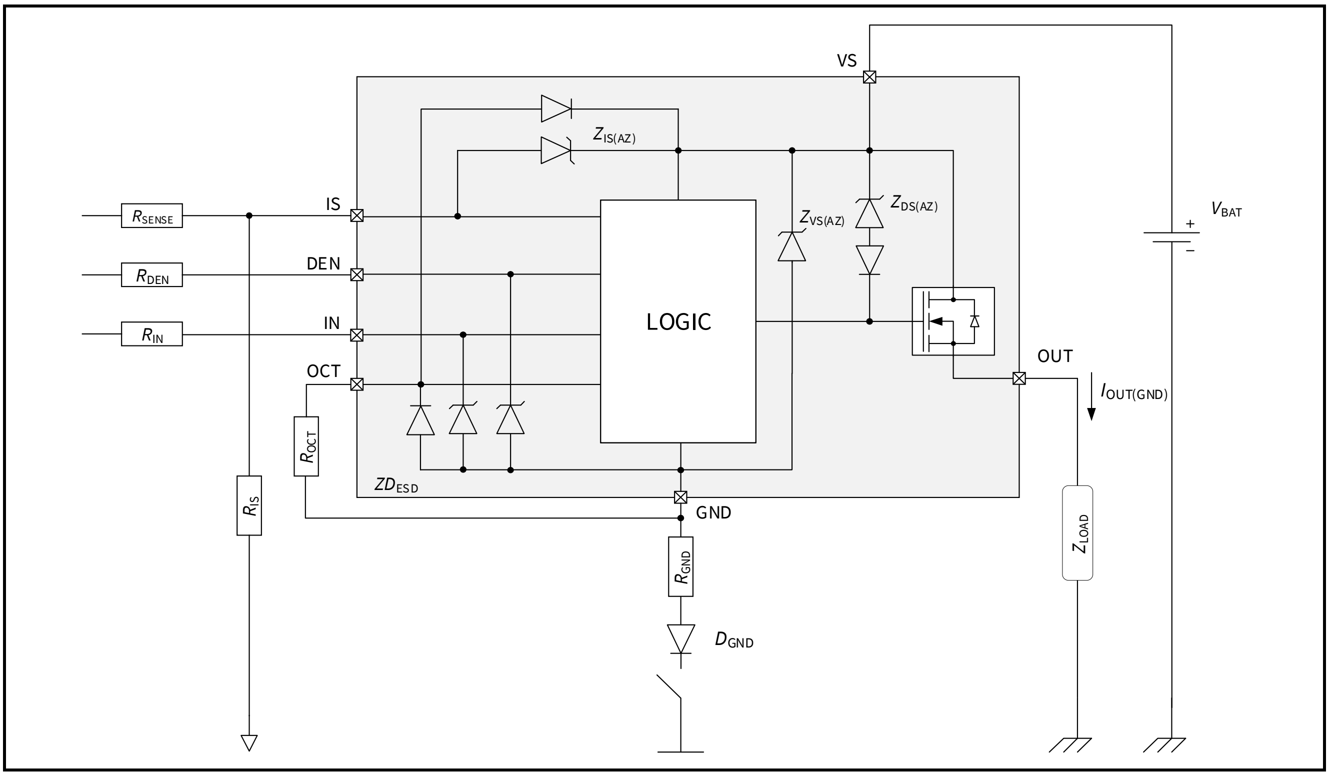


Figure 14 Loss of Ground Protection with External Components

6.2 Undervoltage Protection

Between $V_{S(UV)}$ and $V_{S(OP)}$, the under voltage mechanism is triggered. $V_{S(OP)}$ represents the minimum voltage where the switching ON and OFF can take place. $V_{S(UV)}$ represents the minimum voltage the switch can hold ON. If the supply voltage is below the undervoltage mechanism $V_{S(UV)}$, the device is OFF (turns OFF). As soon as the supply voltage is above the undervoltage mechanism $V_{S(OP)}$, then the device can be switched ON. When the switch is ON, protection functions are operational. Nevertheless, the diagnosis is not guaranteed until V_S is in the V_{NOM} range. **Figure 15** sketches the undervoltage mechanism.

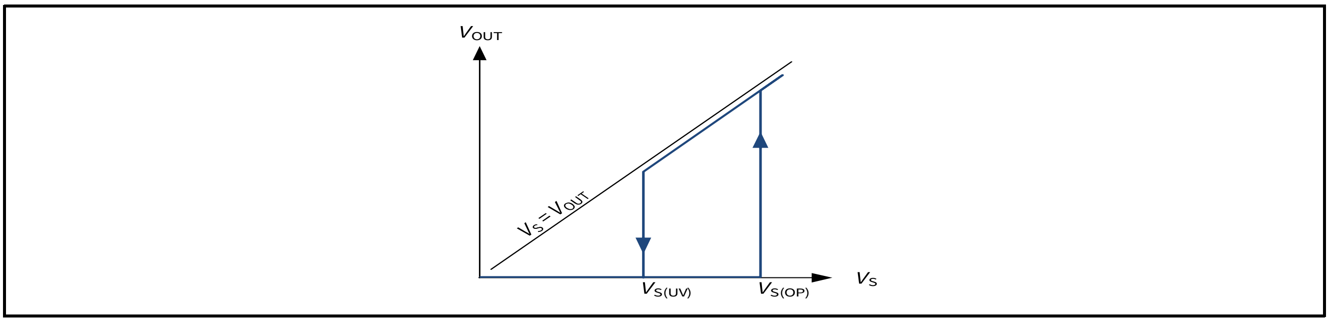


Figure 15 Undervoltage Behavior

6.3 Overvoltage Protection

There is an integrated clamp mechanism for overvoltage protection ($Z_{VS(AZ)}$). To guarantee this mechanism operates properly in the application, the current in the Zener diode has to be limited by a ground resistor. **Figure 16** shows a typical application to withstand overvoltage issues. In case of supply voltage higher than $V_{S(AZ)}$, the power transistor switches ON and the voltage across the logic section is clamped. As a result, the internal ground potential rises to V_S - $V_{S(AZ)}$. Due to the ESD Zener diodes, the potential at pin IN and DEN rises almost to that potential, depending on the impedance of the connected circuitry. In the case the device was ON, prior to overvoltage, the BTT6080-1ERL remains ON. In the case the BTT6080-1ERL was OFF, prior to overvoltage, the power transistor can be activated. In the case the supply voltage is in above $V_{BAT(SC)}$ and below $V_{DS(AZ)}$, the output transistor is still operational and follows the input. If the channel is in the ON state, parameters are no longer guaranteed and lifetime is reduced compared to the nominal supply voltage range. This especially impacts the short circuit robustness, as well as the maximum energy E_{AS} capability.

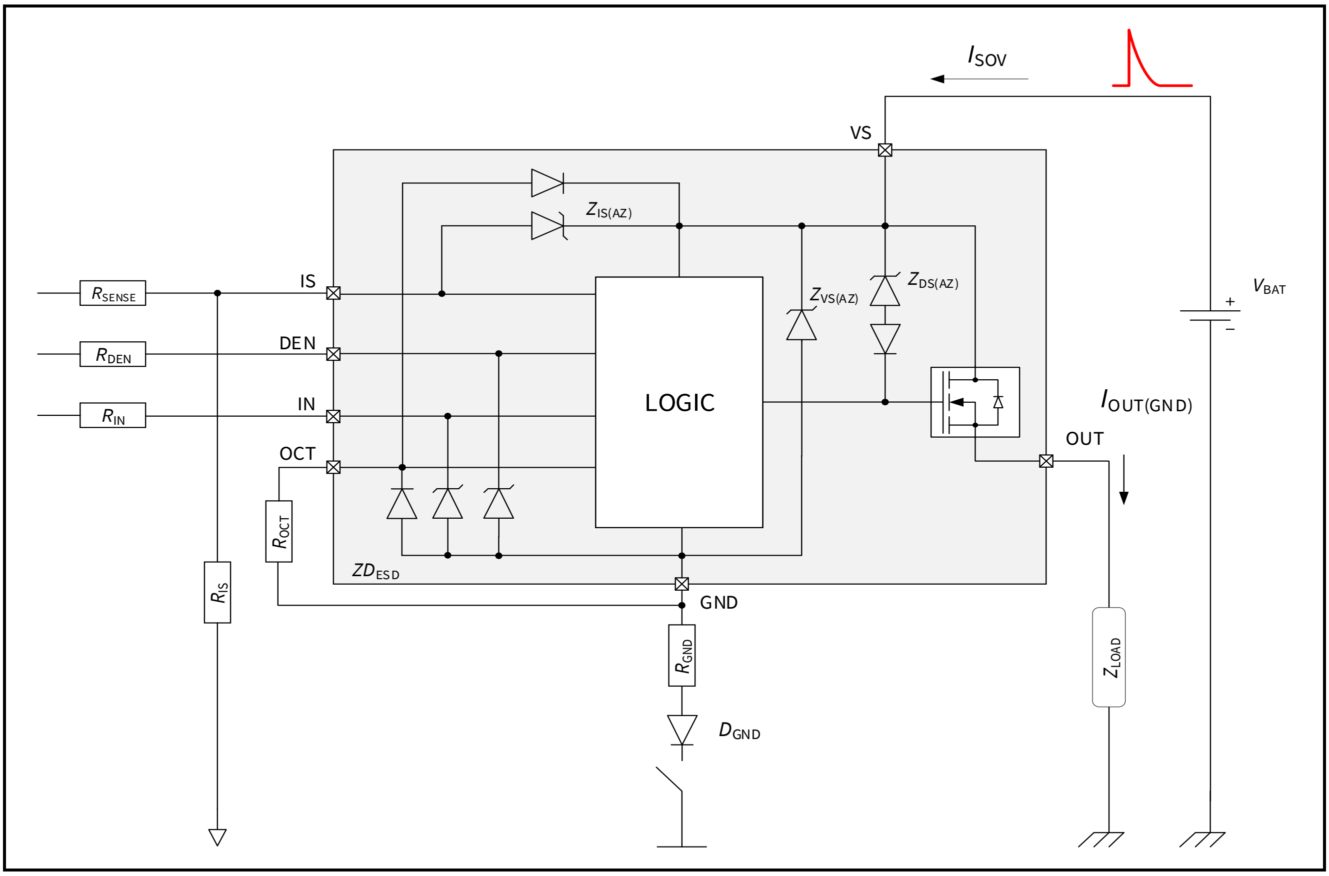


Figure 16 Overvoltage Protection with External Components

6.4 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode of the power DMOS causes power dissipation. The current in this intrinsic body diode is limited by the load itself. Additionally, the current into the ground path and the logic pins has to be limited to the maximum current described in **Chapter 4.1** with an external resistor. **Figure 17** shows a typical application. R_{GND} resistor is used to limit the current in the Zener protection of the device. Resistors R_{DEN} and R_{IN} are used to limit the current in the logic of the device and in the ESD protection stage. R_{SENSE} is used to limit the current in the sense transistor which behaves as a diode. The recommended value for $R_{DEN} = R_{IN} = R_{SENSE} = 10\ k\Omega$.

During reverse polarity, no protection functions are available.

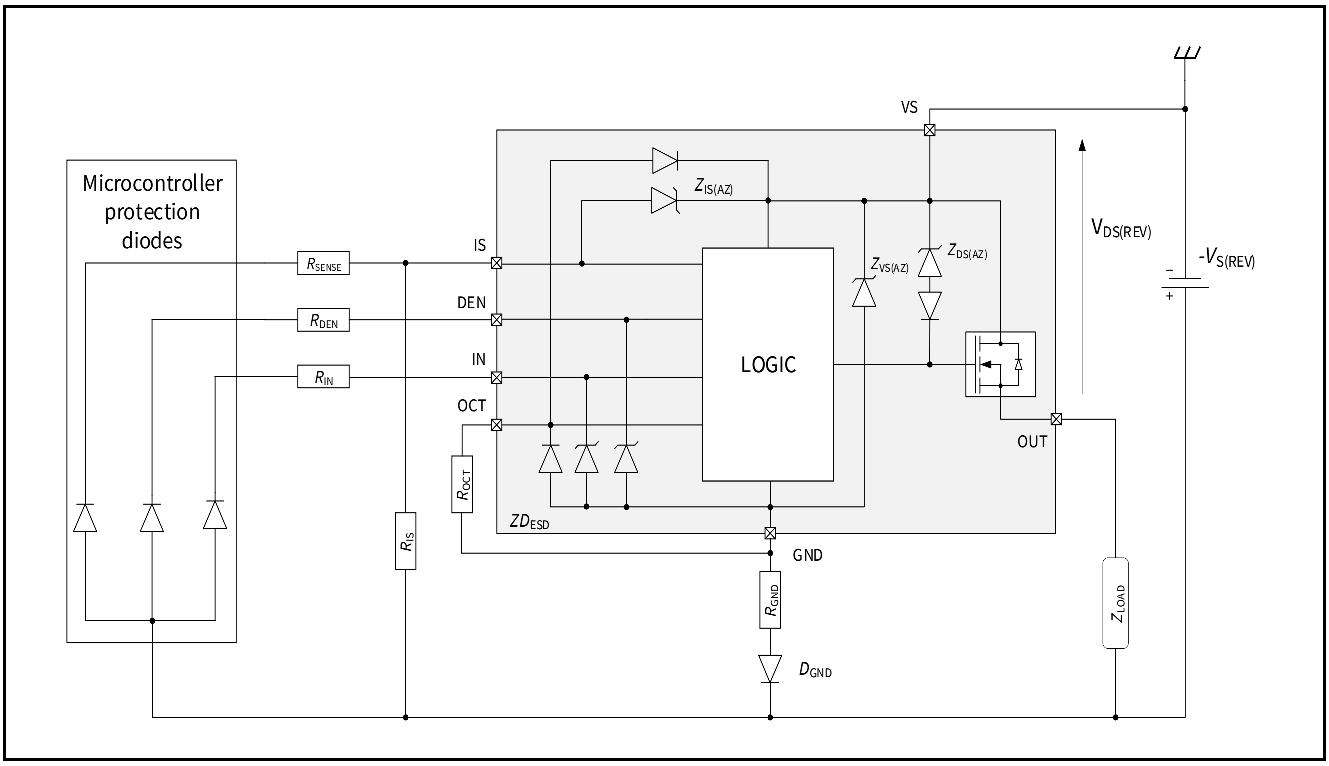


Figure 17 Reverse Polarity Protection with External Components

6.5 Overload Protection

In case of overload or short circuit to ground, the BTT6080-1ERL offers several protection mechanisms.

6.5.1 Adjustable Overcurrent Threshold

The BTT6080-1ERL is protected in case of overload and short circuit to ground.

The device offers an adjustable current limitation range from $I_{LIM,MIN}$ to $I_{LIM,MAX}$. This feature offers protection against overstress for the load as well as for the power output stage. The configured current threshold is independent of V_{DS} and T_J. In case of DMOS temperature increase exceeding the device safe operation environment, overtemperature and dynamic tempertature protection mechanism will be triggered as shown in **Figure 19**.

For the adjustment of the current threshold for the output channel, the following equation can be considered:

$$I_{LIM} = (k_{ILIOCT} \cdot I_{OCT}) + \Delta I_{LIM}, \tag{6.1}$$

where

$$I_{OCT} = (I_{LIM} - \Delta I_{LIM}) / k_{ILIOCT} \tag{6.2}$$

To select the proper resistor value R_{OCT} connected between the OCT pin and device ground, the following equation can be considered:

$$R_{OCT} = (V_{OCT} \cdot k_{ILIOCT}) / (I_{LIM} - \Delta I_{LIM}) \tag{6.3}$$

In case of an OCT pin short to ground with the current exceeding $I_{OCT(SHORT2GND)}$ the device will set the current limit value to $I_{LIMOCT(SHORT2GND)}$. The behavior of how I_{OCT} is related to I_{LIM} is described in **Figure 18**. However, due to the maximum rating of the allowed current through OCT pin I_{OCT}, it is not recommended to shorten the OCT pin to device GND. In the case of reverse battery condition, this could lead to violations of the maximum ratings, therefore I_{OCT} absolute maximum rating needs to be considered.

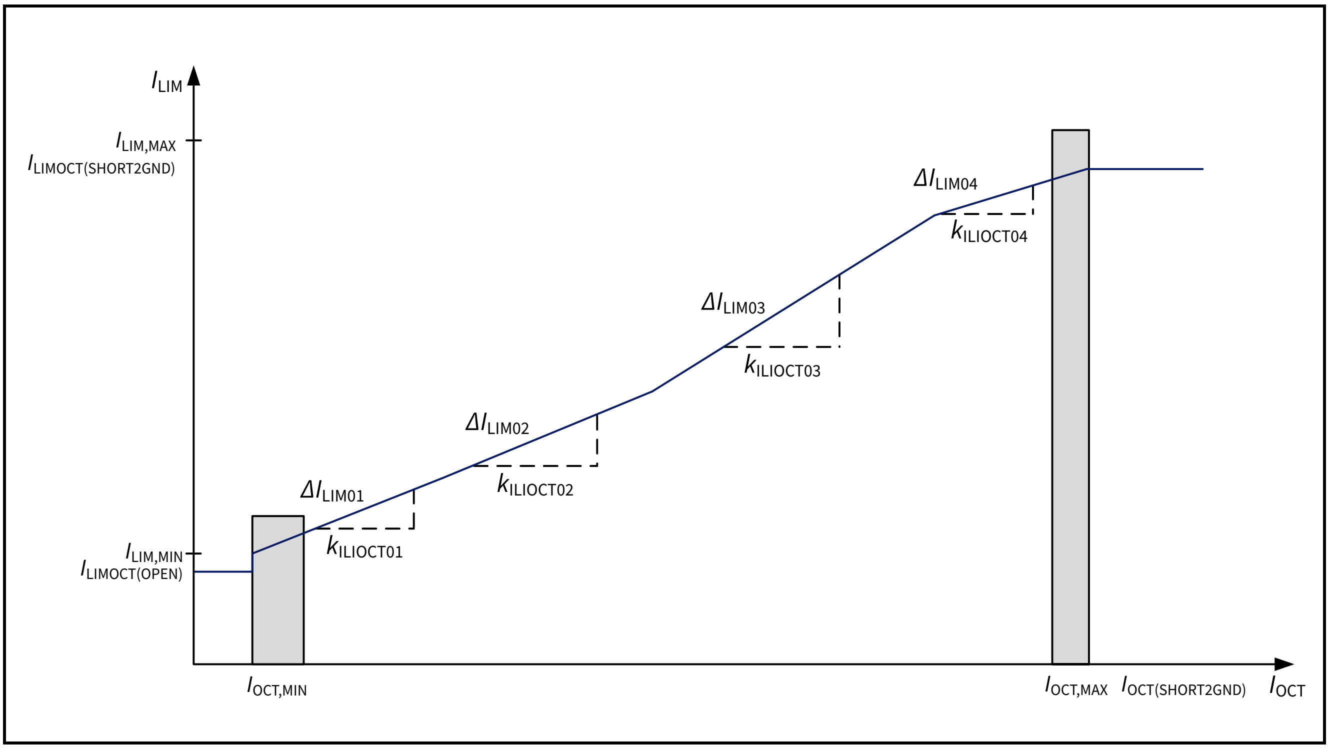


Figure 18 Adjustable overcurrent threshold behavior

When setting the required current limitation, make sure that there is a safety margin between the adjusted current limitation and the expected load current of the application. This is important to prevent unintentional activation of the current limitation circuit during normal operation. When the load current is close(r) to the adjusted current limitation threshold, the turn-on slew rate becomes slower, causing a longer t_{ON} timing, while the turn-off slew rate may become faster, resulting in a shorter t_{OFF} timing. Keeping this safety margin ensures that the influence of the current limitation threshold on switching times is moderate.

The maximum application load capability of the device at a certain current limitation threshold is given by the equation

$$I_{\mathrm{L(APP),MAX}} = I_{\mathrm{LIM0x\_fraction}} * I_{\mathrm{LIM}} \tag{6.4}$$

where x = 1 – 4 (see **Table 6**)

6.5.2 Overtemperature protection

The channel incorporates both an absolute ($T_{J(SC)}$) and a dynamic ($T_{J(SW)}$) temperature sensor. Activation of either sensor will cause the overheated channel to switch OFF to prevent destruction. The channel remains switched OFF even when the temperature has cooled down to an acceptable value (latch behavior). No retry strategy is implemented to switch ON the channel when the DMOS temperature has cooled down and only the IN pin signal toggling can re-activate the power stage. **Figure 19** depicts the behavior of the device during an overtemperature condition.

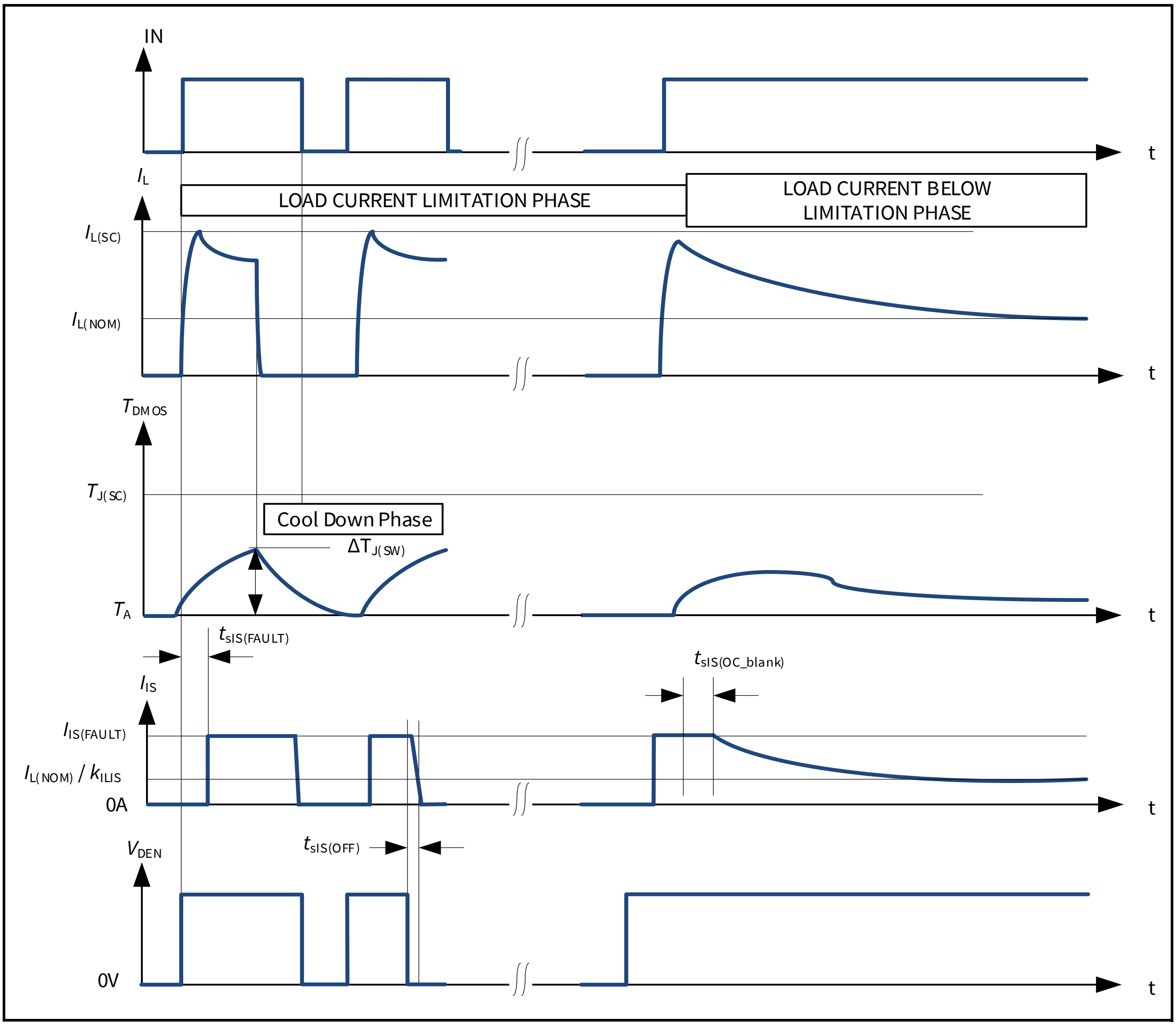


Figure 19 Overload Protection

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant and cannot be described.

6.6 Electrical Characteristics for the Protection Functions

Table 7 Electrical Characteristics: Protection

V_S = 8 V to 36 V, T_J = -40°C to +150°C (unless otherwise specified).
Typical values are given at V_S = 28 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Loss of Ground							
Output leakage current while GND disconnected	$I_{OUT(GND)}$	–	0.1	–	mA	[1] [2] V_S = 48 V See **Figure 14**	P_6.6.1
Reverse Polarity							
Drain source diode voltage during reverse polarity	$V_{DS(REV)}$	200	610	700	mV	I_L = - 5 A T_J = 150°C See **Figure 17**	P_6.6.2
Overvoltage							
Overvoltage protection	$V_{S(AZ)}$	65	70	75	V	I_{SOV} = 20 mA See **Figure 16**	P_6.6.3
Overload Condition							
Dynamic temperature increase while switching	$\Delta T_{J(SW)}$	–	80	–	K	[3] See **Figure 19**	P_6.6.8
Thermal shutdown temperature	$T_{J(SC)}$	150	170	200	°C	[3][4] See **Figure 19**	P_6.6.10
Thermal shutdown hysteresis	$\Delta T_{J(SC)}$	–	30	–	K	[3][4] See **Figure 19**	P_6.6.11
Adjustable overcurrent limitation accuracy (low)	$I_{LIM01(ACC)}$	-70.3%	–	70.3%	–	[2] 0.81 A ≤ I_{LIM} < 1.87 A V_{DS} = 5 V	P_6.6.9
Adjustable overcurrent limitation d-value (low)	ΔI_{LIM01}	–	0.58	–	A	[2] 0.81 A ≤ I_{LIM} < 1.87 A V_{DS} = 5 V	P_6.6.6
Adjustable overcurrent limitation k-factor (low)	$k_{ILIOCT01}$	–	33.4k	–	–	[2] 0.81 A ≤ I_{LIM} < 1.87 A V_{DS} = 5 V	P_6.6.7
Adjustable overcurrent limitation accuracy (medium1)	$I_{LIM02(ACC)}$	-40.2%	–	40.2%	–	[2] 1.87 A ≤ I_{LIM} < 2.30 A V_{DS} = 5 V	P_6.6.14
Adjustable overcurrent limitation d-value (medium1)	ΔI_{LIM02}	–	0.24	–	A	[2] 1.87 A ≤ I_{LIM} < 2.30 A V_{DS} = 5 V	P_6.6.15
Adjustable overcurrent limitation k-factor (medium1)	$k_{ILIOCT02}$	–	42.4k	–	–	[2] 1.87 A ≤ I_{LIM} < 2.30 A V_{DS} = 5 V	P_6.6.16

Table 7 Electrical Characteristics: Protection (cont'd)

V_S = 8 V to 36 V, T_J = -40°C to +150°C (unless otherwise specified).
Typical values are given at V_S = 28 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Adjustable overcurrent limitation accuracy (medium2)	$I_{LIM03(ACC)}$	-37.5%	–	37.5%	–	[2)] 2.30 A ≤ I_{LIM} < 4.60 A V_{DS} = 5 V	P_6.6.19
Adjustable overcurrent limitation d-value (medium2)	ΔI_{LIM03}	–	-0.58	–	A	[2)] 2.30 A ≤ I_{LIM} < 4.60 A V_{DS} = 5 V	P_6.6.20
Adjustable overcurrent limitation k-factor (medium2)	$k_{ILIOCT03}$	–	57.1k	–	–	[2)] 2.30 A ≤ I_{LIM} < 4.60 A V_{DS} = 5 V	P_6.6.21
Current limitation value in case OCT pin open	$I_{LIMOCT(OPEN)}$	–	0.75	–	A	[2)] $I_{OCT} \leq I_{OCT(OPEN)}$	P_6.6.24
Current limitation value in case OCT pin short to device ground	$I_{LIMOCT(SHORT2GND)}$	5.1	7.9	10.7	A	[2)] $I_{OCT} \geq I_{OCT(SHORT2GND)}$	P_6.6.25
Adjustable overcurrent limitation accuracy (high)	$I_{LIM04(ACC)}$	-48.1%	–	48.1%	–	[2)] 4.60 A ≤ I_{LIM} ≤ 5.56 A V_{DS} = 5 V	P_6.6.27
Adjustable overcurrent limitation d-value (high)	ΔI_{LIM04}	–	-6.46	–	A	[2)] 4.60 A ≤ I_{LIM} ≤ 5.56 A V_{DS} = 5 V	P_6.6.26
Adjustable overcurrent limitation k-factor (high)	$k_{ILIOCT04}$	–	122.9k	–	–	[2)] 4.60 A ≤ I_{LIM} ≤ 5.56 A V_{DS} = 5 V	P_6.6.28

1) All pins are disconnected except VS and OUT
2) Not subject to production test, specified by design
3) Functional test only
4) Test at T_J = +150°C only

7 Diagnostic Functions

For diagnosis purposes, the BTT6080-1ERL provides a combination of digital and analog information at pin IS. These signals are called SENSE. The current sense is enabled when DEN is activated (DEN pin is set to "high"). In case of disabled diagnostic (DEN is set to "low"), IS becomes high impedance.

7.1 IS Pin

The BTT6080-1ERL provides a SENSE current, I_{IS}, at IS pin as long as no “hard” failure mode occurs (short circuit to GND/OCT short circuit to GND/current limitation/overtemperature/excessive dynamic temperature increase or open load at OFF). IS current is a proportional signal to the load current (ratio $k_{ILIS} = I_L / I_{IS}$).

The complete IS pin and diagnostic mechanism is described on **Figure 20**. The accuracy of the sense current depends on temperature and load current. Due to the ESD protection, in connection to V_S, it is not recommended to share the IS pin with other devices if these devices are using a different battery feed. The consequence is that the unsupplied device would be supplied via the IS pin of the supplied device.

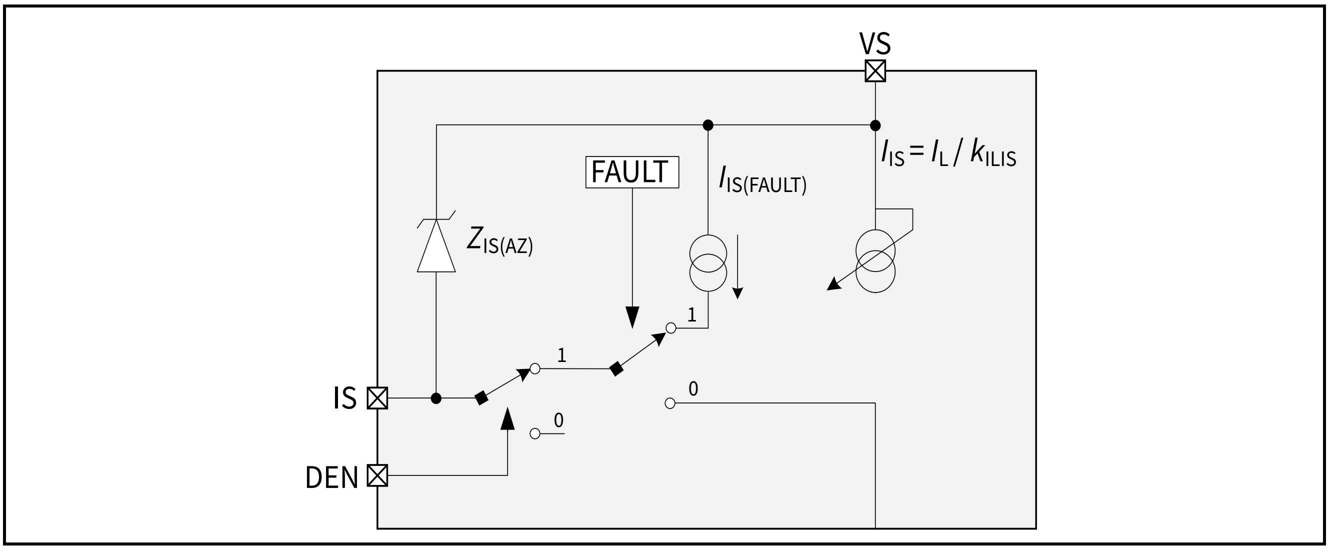


Figure 20 Diagnostic Block Diagram

7.2 SENSE Signal in Different Operating Modes

Table 8 gives a quick reference for the state of the IS pin during device operation.

Table 8 Sense Signal, Function of Operation Mode

Operation Mode	Input level	DEN	Output Level	Diagnostic Output
Normal operation	OFF	H	Z	Z
Short circuit to GND			~ GND	Z
Overtemperature			Z	Z
Short circuit to V_S			V_S	$I_{IS(FAULT)}$
Open Load			$< V_{OL(OFF)}$ $> V_{OL(OFF)}$ 1)	Z $I_{IS(FAULT)}$
Inverse current			$\sim V_{INV}$	$I_{IS(FAULT)}$
OCT-pin short circuit to GND			Z	$I_{IS(FAULT)}$
Normal operation	ON		$\sim V_S$	$I_{IS} = I_L / k_{ILIS}$
Current limitation			$< V_S$	$I_{IS(FAULT)}$
OCT-pin short circuit to GND			$\sim V_S$	$I_{IS} = I_L / k_{ILIS}$
Short circuit to GND			~ GND	$I_{IS(FAULT)}$
Overtemperature			Z	$I_{IS(FAULT)}$
Short circuit to V_S			V_S	$I_{IS} < I_L / k_{ILIS}$
Open Load			$\sim V_S$ 2)	$I_{IS} < I_{IS(OL)}$
Inverse current			$\sim V_{INV}$	$I_{IS} < I_{IS(OL)}$
Underload			$\sim V_S$ 3)	$I_{IS(OL)} < I_{IS} < I_{L / kILIS}$
Diagnostic Disabled	Don't care	L	Don't care	Z

1) With additional pull-up resistor

2) The output current has to be smaller than $I_{L(OL)}$

3) The output current has to be higher than $I_{L(OL)}$

7.3 SENSE Signal in the Nominal Current Range

Figure 21 and **Figure 23** show the current sense as a function of the load current in the power DMOS. Usually, a resistor R_{IS} is connected to the current sense IS pin. This resistor has to be higher than 560 Ω to limit the power losses in the sense circuitry. A typical value is 1.2 kΩ. The blue curve represents the ideal sense current, assuming an ideal k_{ILIS} factor value. The red curves show the accuracy the device provides across full temperature range, at a defined current.

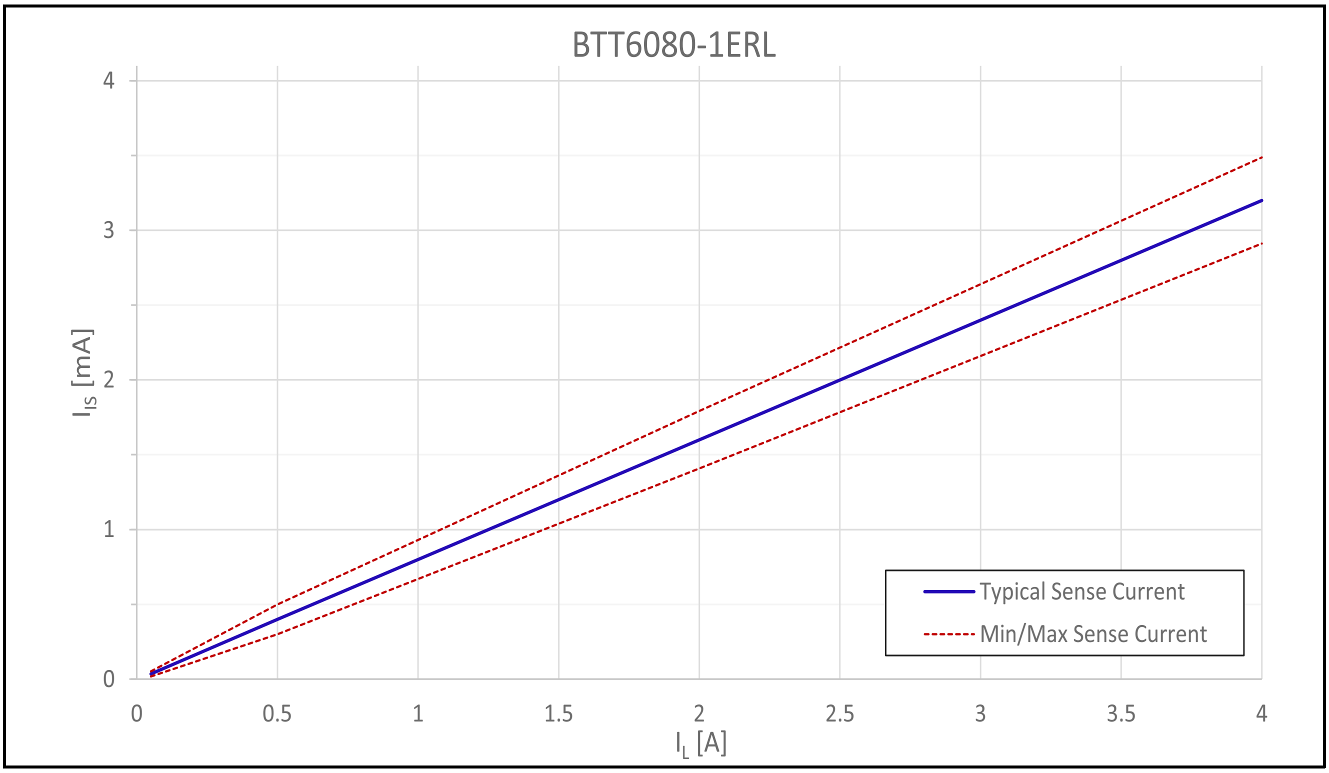


Figure 21 Current Sense for Nominal Load

7.3.1 SENSE Signal Variation as a Function of Temperature and Load Current

In some applications a better accuracy is required around half the nominal current $I_{L(NOM)}$. To achieve this accuracy requirement, a calibration on the application is possible. To avoid multiple calibration points at different load and temperature conditions, the BTT6080-1ERL allows limited derating of the k_{ILIS} value, at a given point (I_{L3}; T_J = +25°C). This derating is described by the parameter Δk_{ILIS}.

Figure 22 shows the behavior of the sense current, assuming one calibration point at nominal load at +25°C. The blue line indicates the typical k_{ILIS} ratio. The red lines indicate the k_{ILIS} accuracy without calibration. The green lines indicate the derating on the parameter across temperature and voltage, assuming one calibration point at nominal temperature and nominal battery voltage.

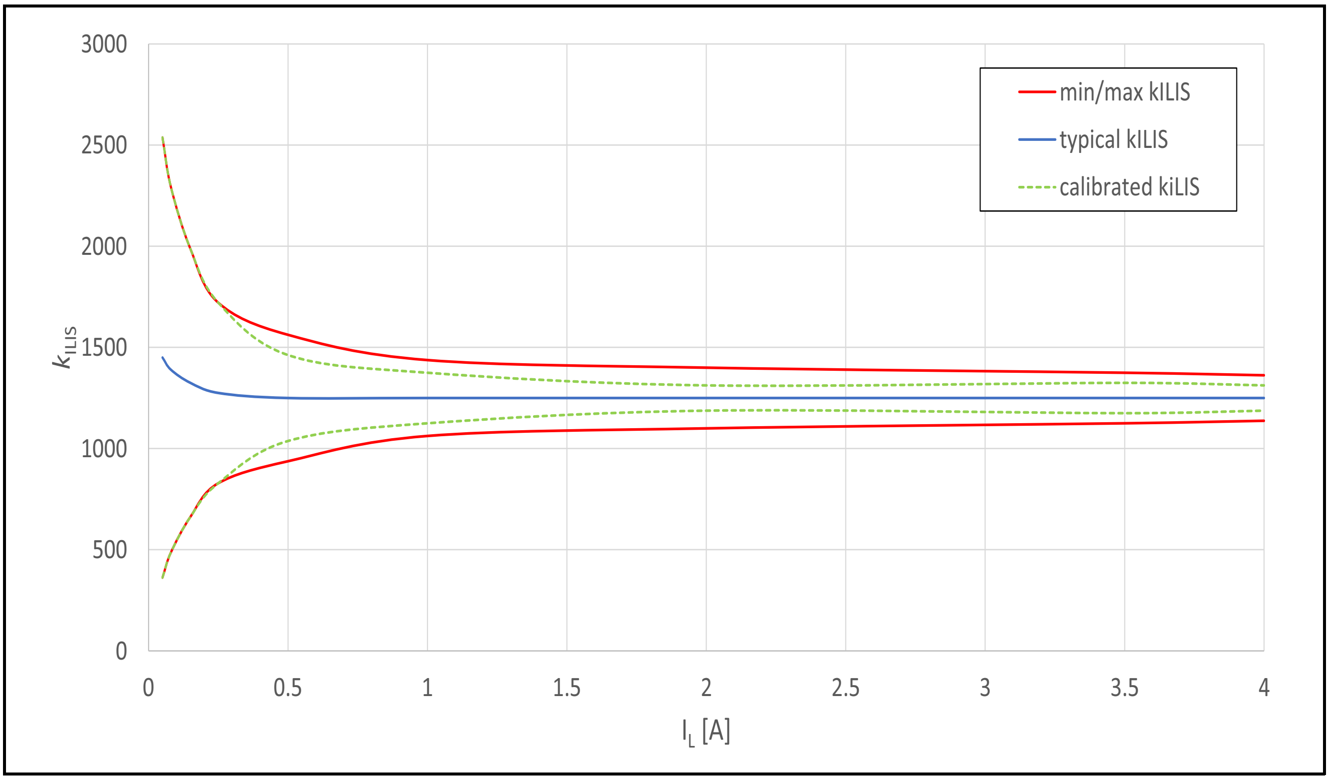


Figure 22 Improved Current Sense Accuracy with One Calibration Point

7.3.2 SENSE Signal Timing

Figure 23 shows the timing during settling and disabling of the sense.

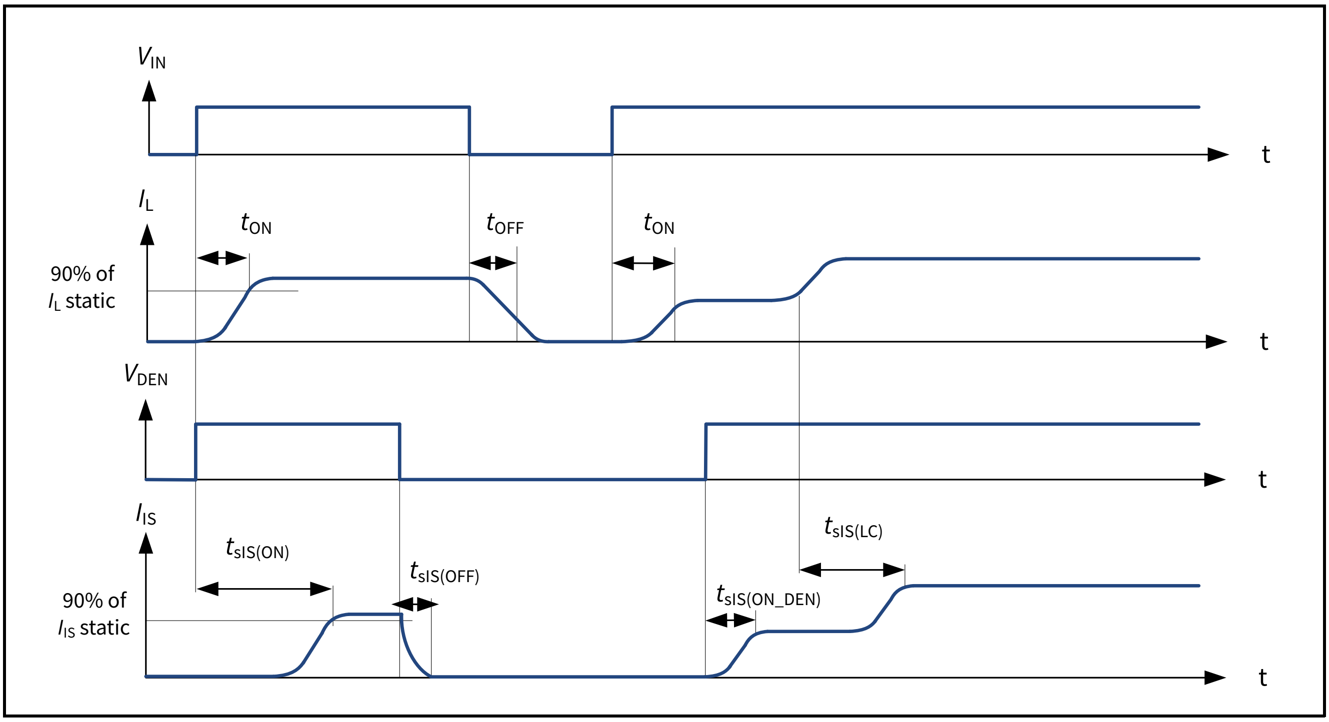


Figure 23 Current Sense Settling / Disabling Timing

7.3.3 SENSE Signal in Open Load

7.3.3.1 Open Load in ON Diagnostic

If the channel is ON, a leakage current can still flow through an open load, for example due to humidity. The parameter $I_{L(OL)}$ gives the threshold of recognition for this leakage current. If the current I_L flowing out the power DMOS is below this value, the device recognizes a failure, if the DEN is selected. In that case, the SENSE current is below $I_{IS(OL)}$. Otherwise, the minimum SENSE current is given above parameter $I_{IS(OL)}$. **Figure 24** shows the SENSE current behavior in this area. The red curve shows a typical product curve. The blue curve shows the ideal current sense ratio.

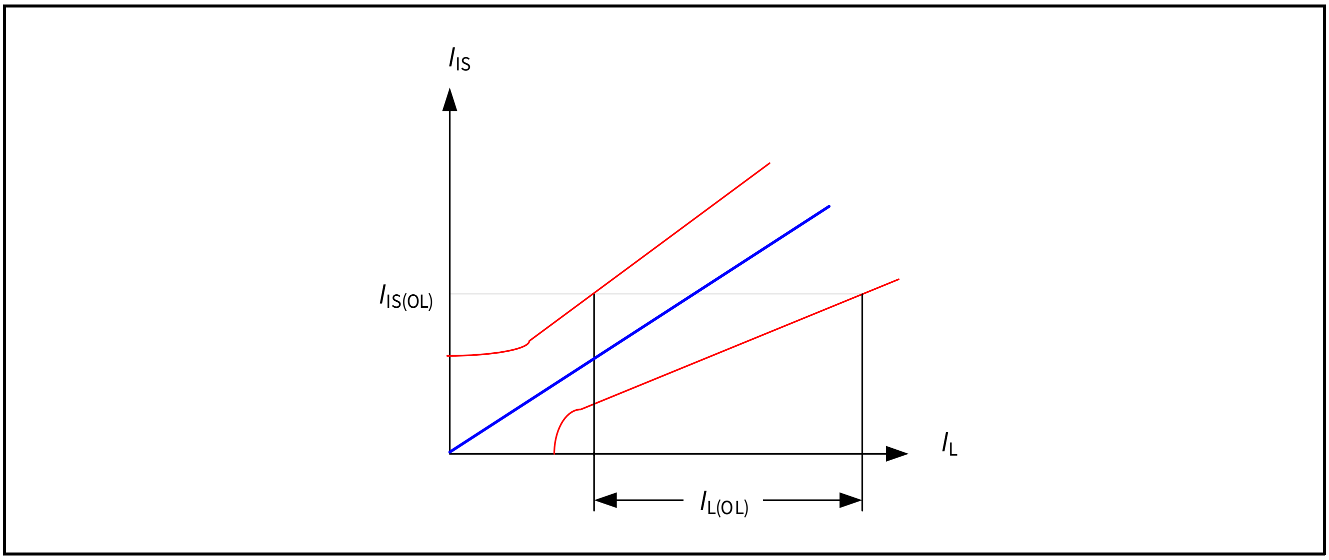


Figure 24 Current Sense Ratio for Low Currents

7.3.3.2 Open Load in OFF Diagnostic

For open load diagnosis in OFF-state, an external output pull-up resistor (R_{OL}) is recommended. For the calculation of pull-up resistor value, the leakage currents and the open load threshold voltage $V_{OL(OFF)}$ have to be taken into account. **Figure 25** gives a sketch of the situation. $I_{leakage}$ defines the leakage current in the complete system, including $I_{L(OFF)}$ (see **Chapter 5.5**) and external leakages in the application. (e.g, due to humidity, corrosion, etc....)

To reduce the stand-by current of the system, an open load resistor switch S_{OL} is recommended. If the channel is OFF, the output is no longer pulled down by the load and V_{OUT} voltage rises to nearly V_S. This is recognized by the device as an open load. The voltage threshold is given by $V_{OL(OFF)}$. In that case, the SENSE signal is switched to the $I_{IS(FAULT)}$.

An additional R_{PD} resistor can be used to pull V_{OUT} to 0 V. Otherwise, the OUT pin is floating. This resistor can be used as well for short circuit to battery detection, see **Chapter 7.3.4**.

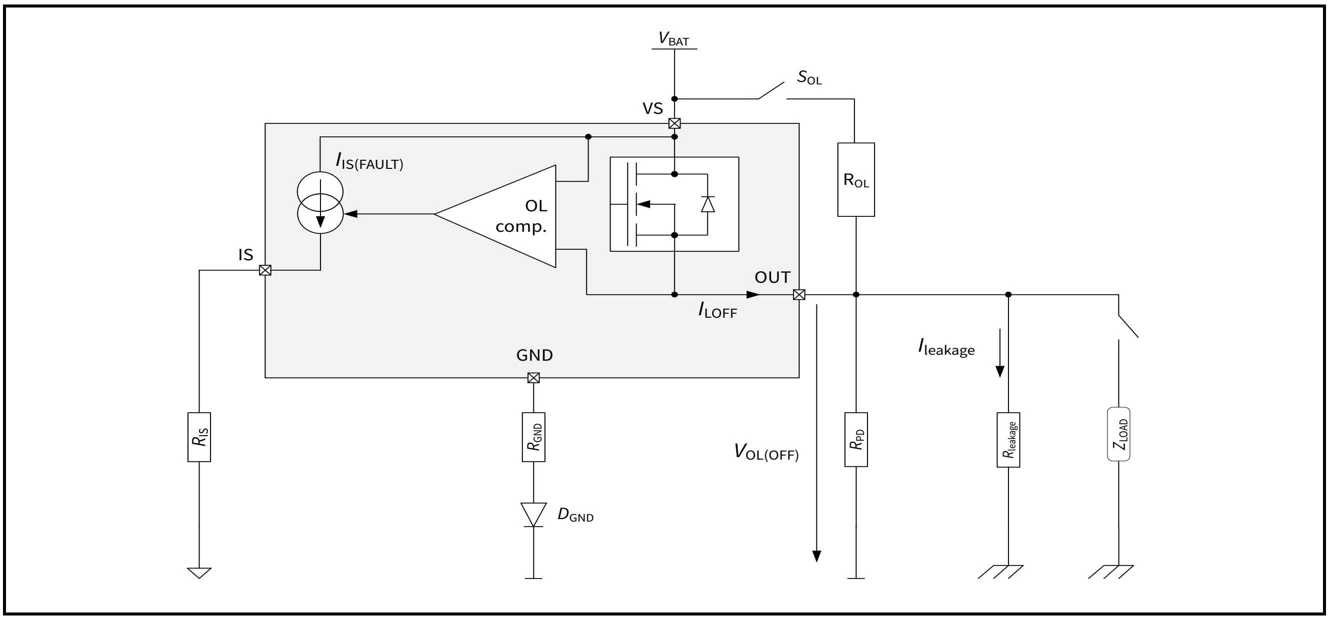


Figure 25 **Open Load Detection in OFF Electrical Equivalent Circuit**

7.3.3.3 Open Load Diagnostic Timing

Figure 26 shows the timing during either Open Load in ON or OFF condition when the DEN pin is HIGH. Please note that a delay $t_{sIS(FAULT\_OL\_OFF)}$ has to be respected after the falling edge of the input, when applying an open load in OFF diagnosis request, otherwise the diagnosis can be wrong.

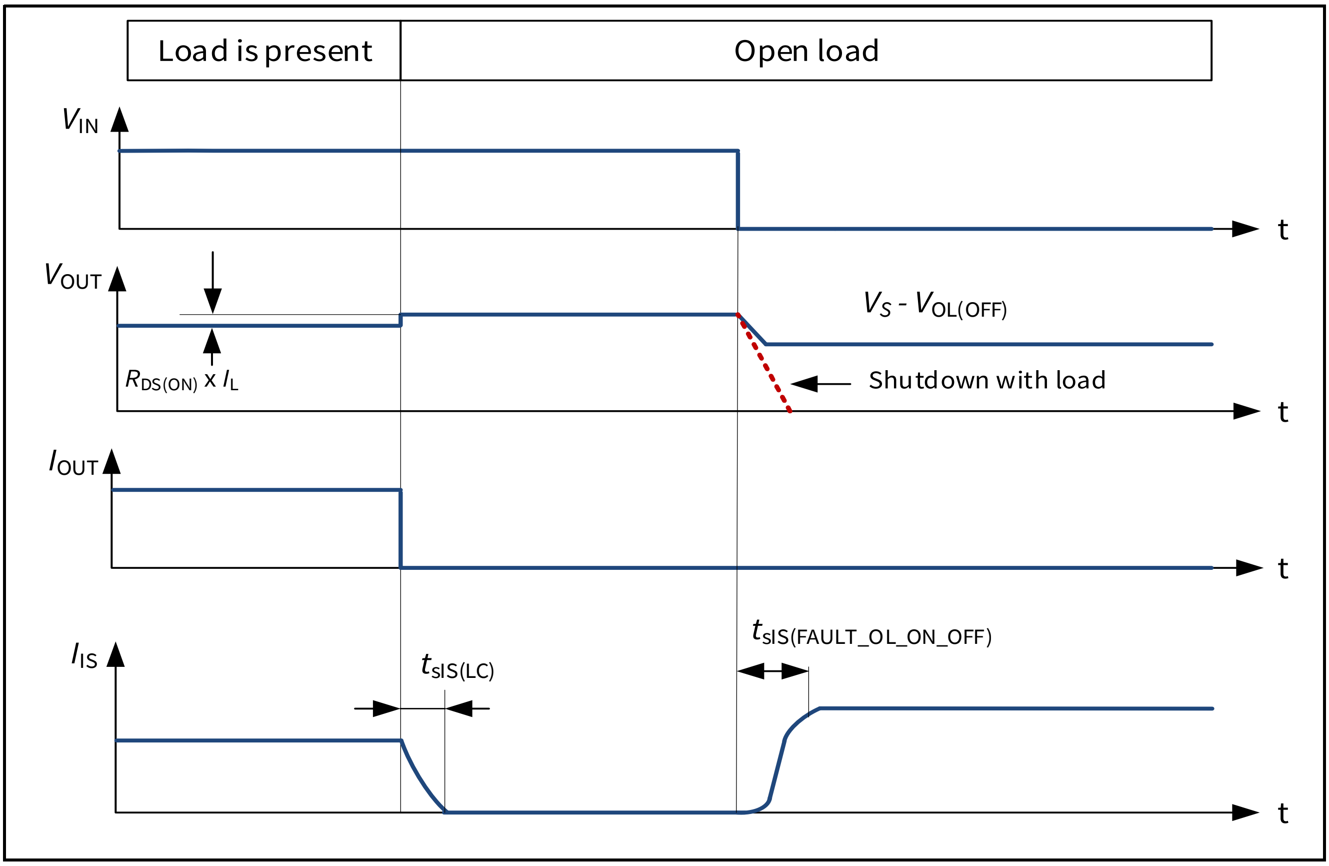


Figure 26 **SENSE Signal in Open Load Timing**

7.3.4 SENSE Signal with OUT in Short Circuit to V_S

In case of a short circuit between the OUTput-pin and the V_S pin, all or portion (depending on the short circuit impedance) of the load current will flow through the short circuit. As a result, a lower current compared to the normal operation will flow through the DMOS of the BTT6080-1ERL, which can be recognized at the SENSE signal. The open load at OFF detection circuitry can also be used to distinguish a short circuit to V_S. In that case, an external resistor to ground R_{SC_VS} is required. **Figure 27** gives a sketch of the situation.

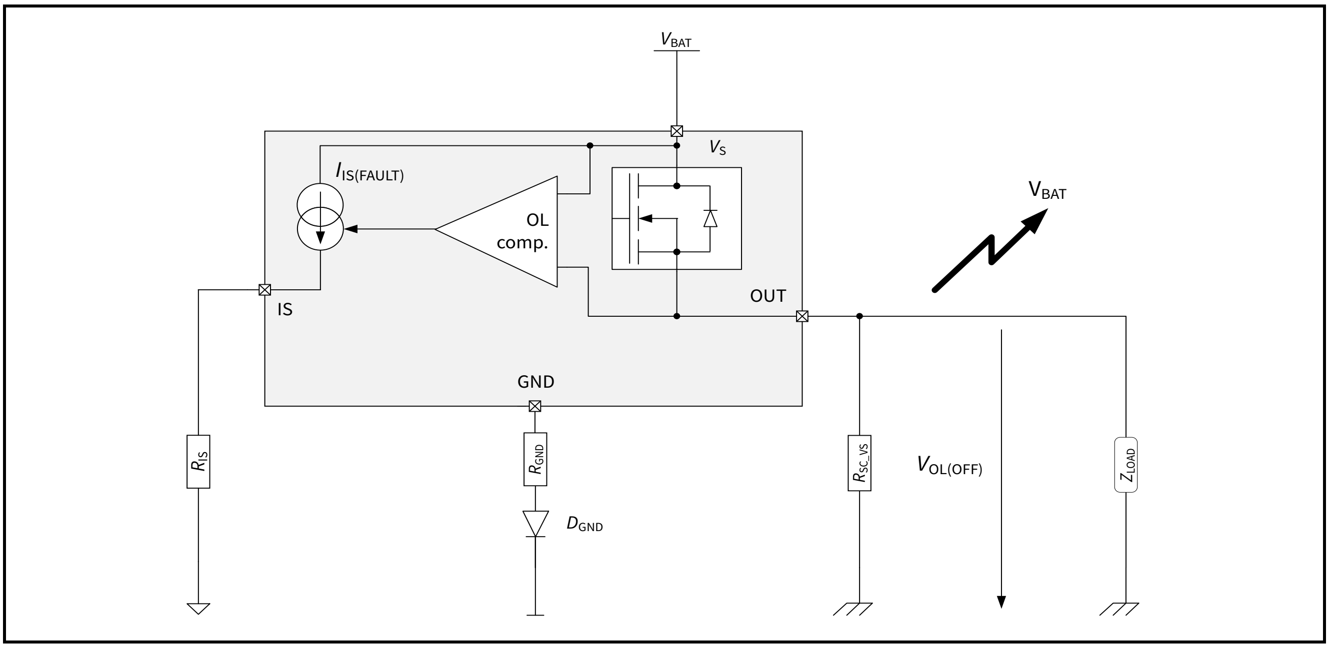


Figure 27 Short Circuit to Battery Detection in OFF Electrical Equivalent Circuit

7.3.5 SENSE Signal in Case of Overload

An overload condition is defined by a current flowing out of the DMOS reaching the current limitation and / or the absolute dynamic temperature swing $T_{J(SW)}$ is reached, and / or the junction temperature reaches the thermal shutdown temperature $T_{J(SC)}$. Please refer to **Chapter 6.5** for details.

If the diagnostic is selected, SENSE signal shows $I_{IS(FAULT)}$ value.

The device has a thermal latch behavior, such that when the overtemperature or the exceed dynamic temperature condition has disappeared, the DMOS is reactivated only when the IN is toggled LOW to HIGH. If the DEN pin is activated the SENSE follows the output stage. If no reset of the latch occurs, the device remains in the latching condition and $I_{S(FAULT)}$ at the IS pin, even though the DMOS is OFF.

7.3.6 SENSE Signal in Case of Inverse Current

In the case of inverse current, the sense signal will indicate open load in OFF state if IN = “low” and indicate open load in ON state if IN = high”.

7.4 Electrical Characteristics Diagnostic Function

Table 9 Electrical Characteristics: Diagnostics

V_S = 8 V to 36 V, T_J = -40°C to +150°C (unless otherwise specified).
Typical values are given at V_S = 28 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Load Condition Threshold for Diagnostic							
Open load detection threshold in OFF state	$V_S - V_{OL(OFF)}$	4	–	6	V	V_{IN} = 0 V V_{DEN} = 4.5 V	P_7.5.1
Open load detection threshold in ON state	$I_{L(OL)}$	3	–	25	mA	$V_{IN} = V_{DEN}$ = 4.5 V $I_{IS(OL)}$ = 5 µA See **Figure 24**	P_7.5.2
Sense Pin							
IS pin leakage current when sense is disabled	$I_{IS\_(DIS)}$	–	–	1	µA	V_{IN} = 4.5 V V_{DEN} = 0 V I_L = 3.5 A	P_7.5.4
Sense signal saturation voltage	$V_S - V_{IS}$ (RANGE)	1	–	3.5	V	V_{IN} = 0 V $V_{OUT} = V_S$ > 10 V V_{DEN} = 4.5 V I_{IS} = 6 mA	P_7.5.6
Sense fault current	$I_{IS(FAULT)\_-40}$	3	24	35	mA	$V_{IS} = V_{IN}$ = 0 V $V_{OUT} = V_S$ > 10 V V_{DEN} = 4.5 V T_J = -40°C See **Figure 20**	P_7.5.7
Sense fault current	$I_{IS(FAULT)\_25}$	4.5	24	35	mA	$V_{IS} = V_{IN}$ = 0 V $V_{OUT} = V_S$ > 10 V V_{DEN} = 4.5 V $T_J \geq$ 25°C See **Figure 20**	P_7.5.33
Sense pin maximum voltage	$V_{IS(AZ)}$	65	70	75	V	I_{IS} = 5 mA See **Figure 20**	P_7.5.3
Current Sense Ratio Signal in the Nominal Area, Stable Load Current Condition							
Current sense ratio I_{L0} = 50 mA	k_{ILIS0}	-75%	1450	+75%		V_{IN} = 4.5 V V_{DEN} = 4.5 V See **Figure 21** T_J = -40 °C; 150 °C	P_7.5.8
Current sense ratio I_{L1} = 0.5 A	k_{ILIS1}	-25%	1250	+25%			P_7.5.9
Current sense ratio I_{L2} = 2.5 A	k_{ILIS2}	-12%	1250	+12%			P_7.5.10
Current sense ratio I_{L3} = 3.5 A	k_{ILIS3}	-10%	1250	+10%			P_7.5.11
k_{ILIS} derating with current and temperature	Δk_{ILIS}	-6	0	+6	%	1) k_{ILIS3} versus k_{ILIS2} See **Figure 22**	P_7.5.17

Table 9 Electrical Characteristics: Diagnostics (cont'd)

V_S = 8 V to 36 V, T_J = -40°C to +150°C (unless otherwise specified).
Typical values are given at V_S = 28 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Diagnostic Timing in Normal Condition							
Current sense settling time to k_{ILIS} function stable after positive input slope on both INput and DEN	$t_{sIS(ON)}$	–	–	350	µs	1) $V_{DEN} = V_{IN}$ = 0 to 4.5 V; V_S =28 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF I_L = 2.5 A See **Figure 23**	P_7.5.18
Current sense settling time with load current stable and transition of the DEN	$t_{sIS(ON\_DEN)}$	–	–	10	µs	V_{IN} = 4.5 V V_{DEN} = 0 to 4.5 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF I_L = 2.5 A See **Figure 23**	P_7.5.19
Current sense settling time to I_{IS} stable after positive input slope on current load	$t_{sIS(LC)}$	–	–	20	µs	1) V_{IN} = 4.5 V V_{DEN} = 4.5 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF $I_L = I_{L2}$= 2.5 A to I_{L3} = 3.5 A; See **Figure 23**	P_7.5.20
Diagnostic Timing in Open Load Condition							
Current sense settling time to I_{IS} stable for open load detection in OFF state	$t_{sIS(FAULT\_OL\_OFF)}$	–	–	100	µs	V_{IN} = 0V V_{DEN} = 0 to 4.5 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF $V_{OUT} = V_S$ = 28 V See **Figure 26**	P_7.5.22
Current sense settling time for open load detection in ON-OFF transition	$t_{sIS(FAULT\_OL\_ON\_OFF)}$	–	200	–	µs	1) V_{IN} = 4.5 to 0 V V_{DEN} = 4.5 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF $V_{OUT} = V_S$ = 28 V See **Figure 26**	P_7.5.23
Diagnostic Timing in Overload Condition							
Current sense settling time to I_{IS} stable for overload detection	$t_{sIS(FAULT)}$	–	–	150	µs	1) $V_{IN} = V_{DEN}$ = 0 to 4.5 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF V_{DS} = 24 V See **Figure 19**	P_7.5.24

Table 9 Electrical Characteristics: Diagnostics (cont'd)

V_S = 8 V to 36 V, T_J = -40°C to +150°C (unless otherwise specified).
Typical values are given at V_S = 28 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current sense over current blanking time	$t_{sIS(OC\_blank)}$	–	350	–	µs	[1] $V_{IN} = V_{DEN}$ = 4.5 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF V_{DS} = 5 V to 0 V See **Figure 19**	P_7.5.32
Diagnostic disable time DEN transition to $I_{IS} < 50\%\ I_L / k_{ILIS}$	$t_{sIS(OFF)}$	–	–	20	µs	V_{IN} = 4.5 V V_{DEN} = 4.5 V to 0 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF $I_L = I_{L3}$ = 3.5 A See **Figure 23**	P_7.5.25

1) Not subject to production test, specified by design

8 Logic Pins

8.1 Input Circuitry

The input circuitry is compatible with 3.3 and 5 V microcontrollers. The concept of the input pin is to react to voltage thresholds. An implemented Schmitt trigger avoids any undefined state if the voltage on the input pin is slowly increasing or decreasing. The output is either OFF or ON but cannot be in a linear or undefined state. The input circuitry is compatible with PWM applications. **Figure 28** shows the electrical equivalent input circuitry. In case the pin is not needed, it must be left opened, or must be connected to device ground (and not module ground) via an input resistor.

The IN and DEN use a comparator with hysteresis. The switching ON / OFF takes place in a defined region, set by the thresholds $V_{IN(L)}$ Max. and $V_{IN(H)}$ Min. The exact value where the ON and OFF take place are unknown and depends on the process, as well as the temperature. To avoid cross talk and parasitic turn ON and OFF, a hysteresis is implemented. This ensures a certain immunity to noise.

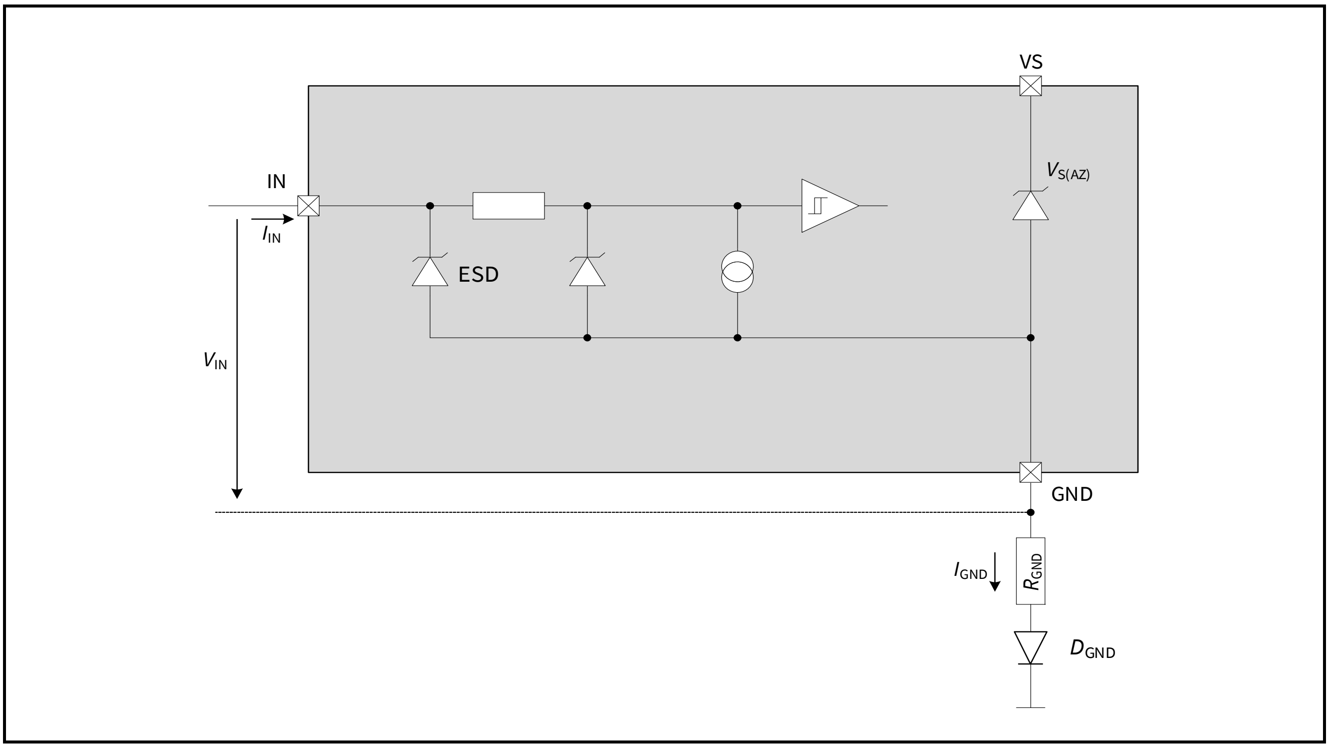


Figure 28 Input Pin Circuitry

8.2 DEN Pin

The DEN pin enables and disables the diagnostic functionality of the device. The pin has the same structure as the INput pin, please refer to **Figure 28**.

8.3 OCT Pin

The device has one analog pin for direct control.
To be able to adjust the overcurrent threshold for the OUT pin, the device offers an OCT pin. The pin needs to be connected to device ground via an external resitor R_{OCT} . The external adjustable current limit allows the flexibility to adjust to overcurrent limitation as defined in the **Table 10**. This improves the reliability of the system by limiting the inrush or overload current. The electrical equivalent of the overcurrent pin circuitry is shown in **Figure 29** below.

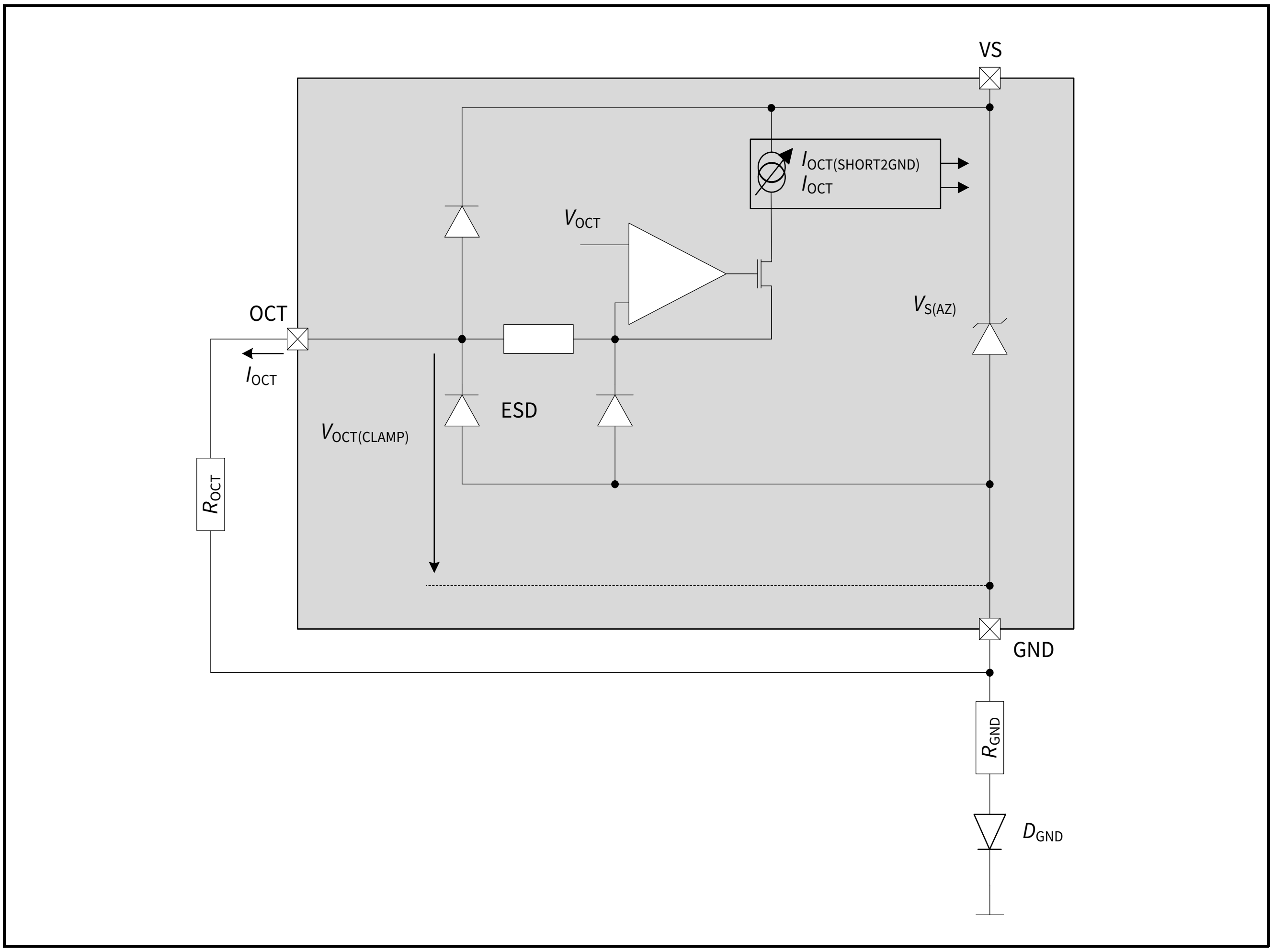


Figure 29 Overcurrent pin circuit

8.4 Electrical Characteristics

Table 10 Electrical Characteristics: Input Pins

V_S = 8 V to 36 V, T_J = -40°C to +150°C (unless otherwise specified).
Typical values are given at V_S = 28 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
INput Pins Characteristics							
Low level input voltage range	$V_{IN(L)}$	-0.3	–	0.8	V		P_8.4.1
High level input voltage range	$V_{IN(H)}$	2	–	6	V		P_8.4.2
Input voltage hysteresis	$V_{IN(HYS)}$	–	250	–	mV	1)	P_8.4.3
Low level input current	$I_{IN(L)}$	1	10	25	µA	V_{IN} = 0.8 V	P_8.4.4
High level input current	$I_{IN(H)}$	2	10	25	µA	V_{IN} = 5.5 V	P_8.4.5
DEN Pin							
Low level input voltage range	$V_{DEN(L)}$	-0.3	–	0.8	V	–	P_8.4.6
High level input voltage range	$V_{DEN(H)}$	2	–	6	V	–	P_8.4.7
Input voltage hysteresis	$V_{DEN(HYS)}$	–	250	–	mV	1)	P_8.4.8
Low level input current	$I_{DEN(L)}$	1	10	25	µA	V_{DEN} = 0.8 V	P_8.4.9
High level input current	$I_{DEN(H)}$	2	10	25	µA	V_{DEN} = 5.5 V	P_8.4.10
OCT Pin							
Analog Input Clamping Voltage of Pin OCT	$V_{OCT(CLAMP)}$	–	V_S	–	V	1) I_{OCT} = 1mA	P_8.4.11
Analog Overcurrent Voltage Threshold	V_{OCT}	0.46	0.51	0.56	V	1) $I_{OCT,MIN} \le I_{OCT} \le I_{OCT,MAX}$ IN = "high"	P_8.4.12
Analog Linear Overcurrent Range	I_{OCT}	6.67	–	97.84	µA	1) IN = "high"	P_8.4.13
OCT short to device ground detection current	$I_{OCT(SHORT2GND)}$	150	–	240	µA	1) DEN = "high" IN = "low"	P_8.4.14

1) Not subject to production test, specified by design

9 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

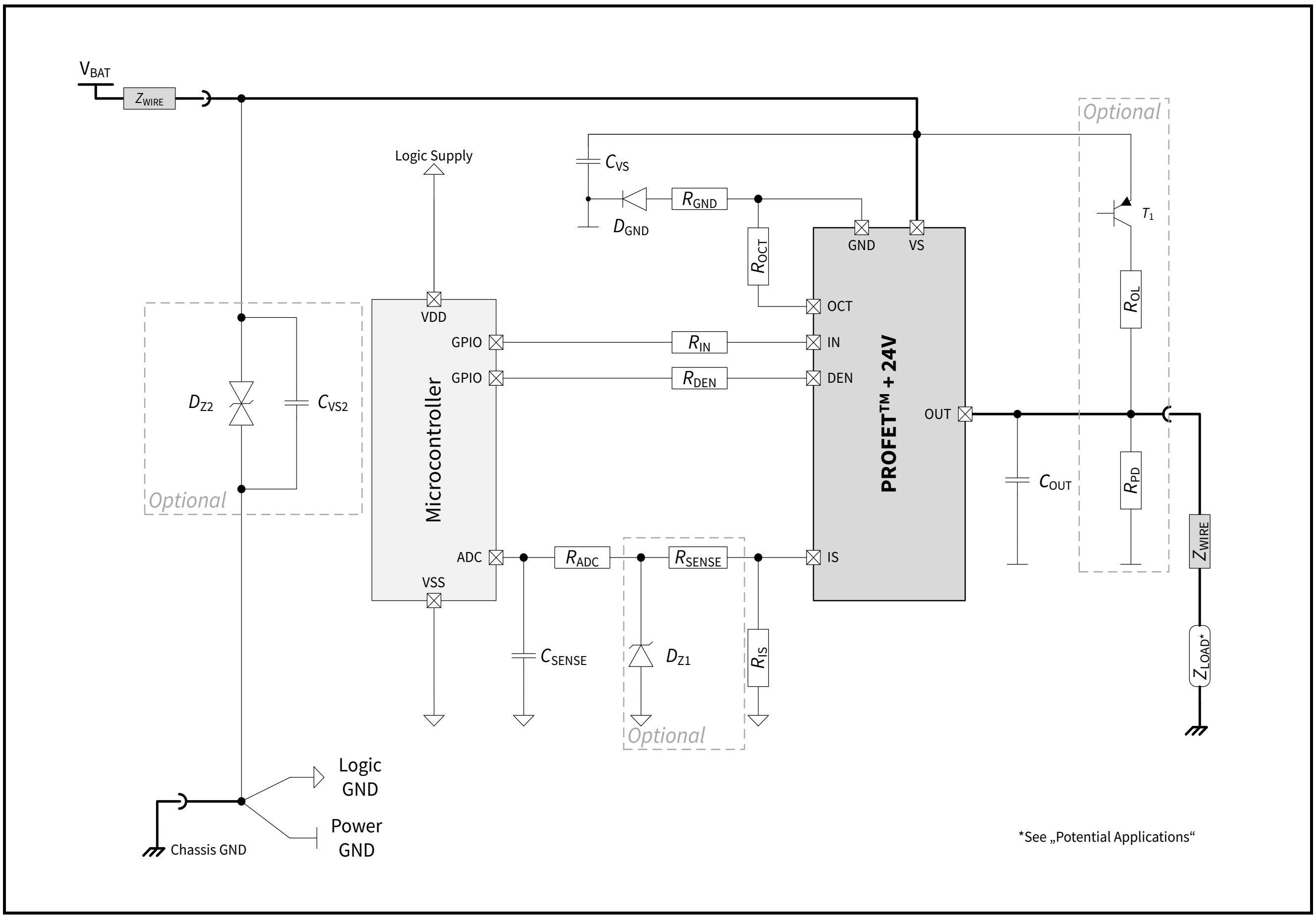


Figure 30 Application Diagram with BTT6080-1ERL

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Table 11 Bill of Material

Reference	Value	Purpose
R_{IN}	10 kΩ	Protection of the microcontroller during overvoltage, reverse polarity. Guarantee BTT6080-1ERL channel is OFF during loss of ground
R_{DEN}	10 kΩ	Protection of the microcontroller during overvoltage, reverse polarity
R_{PD}	47 kΩ	Polarization of the output for short circuit to V_S detection
R_{OL}	1.5 kΩ	Ensures polarization of the BTT6080-1ERL output during open load in OFF diagnostic
R_{IS}	1.2 kΩ	Sense resistor
R_{SENSE}	4.7 kΩ	Overvoltage, reverse polarity, loss of ground. Value to be tuned with micro controller specification

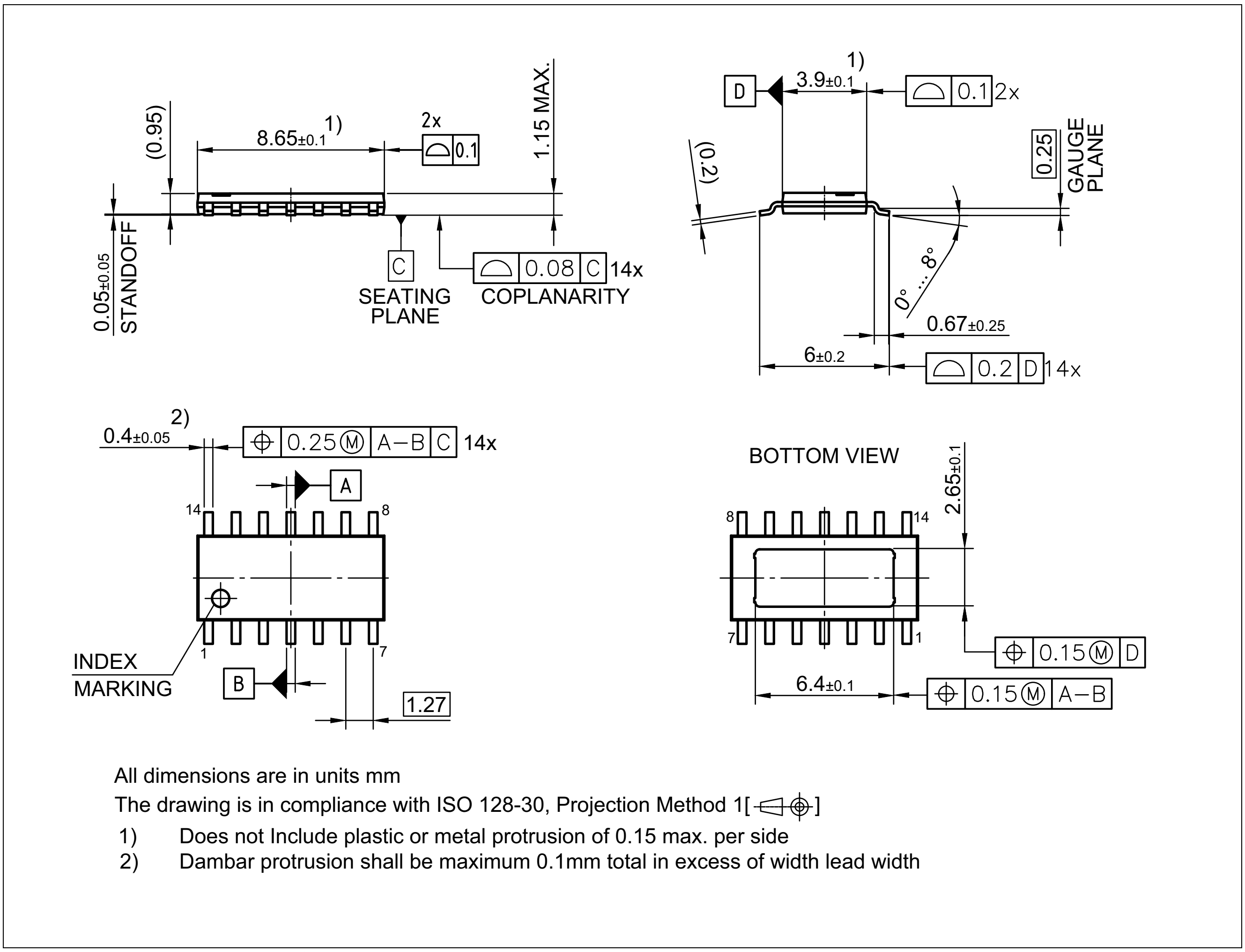
Table 11 **Bill of Material** (cont'd)

Reference	Value	Purpose
R_{OCT}	5.3 kΩ - 75 kΩ	Adjustable overcurrent threshold with different resistors
C_{SENSE}	100 pF	Sense signal filtering
C_{OUT}	10 nF	Protection of the device during ESD and BCI
R_{GND}	27 Ω	Protection of the BTT6080-1ERL during overvoltage
D_{GND}	BAS21	Protection of the BTT6080-1ERL during reverse polarity
D_{Z2}	58 V TVS diode	Protection of the device during overvoltage
C_{VS}	100 nF	Filtering of voltage spikes at the battery line
T1	Dual NPN/PNP	Switch the battery voltage for open load in OFF diagnostic
D_{Z1}	7 V Zener diode	Protection of microcontroller during overvoltage. Value to be tuned according to microcontroller specifications
R_{ADC}	4.7 kΩ	Protection of microcontroller ADC input during overvoltage, reverse polarity, loss of ground. Value to be tuned according to microcontroller specifications
C_{VS2}	–	Filtering/buffer capacitor located at V_{BAT} connector. Value to be tuned according to application requirements

9.1 Further Application Information

- For further information you may visit **www.infineon.com**
- Please contact us for information regarding the pin behavior assessment

10 Package Outlines



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1[ ]

1) Does not Include plastic or metal protrusion of 0.15 max. per side

2) Dambar protrusion shall be maximum 0.1mm total in excess of width lead width

Figure 31 **PG-TDSO-14**1) (Plastic Dual Small Outline Package) (RoHS-Compliant)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Legal Disclaimer for Short-Circuit Capability

Infineon disclaims any warranties and liablilities, whether expressed or implied, for any short-circuit failures below the threshold limit.

Further information on packages

https://www.infineon.com/packages

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1) Dimensions in mm

11 Revision History

Version	Date	Changes
Rev.1.00	2024-10-16	Datasheet release

Table of Contents

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Edition 2024-10-16
Published by
Infineon Technologies AG
81726 Munich, Germany

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Document reference
Z8F68624592

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