OPTIREG™ linear voltage regulator TLT125D0EJ

High-precision voltage tracker

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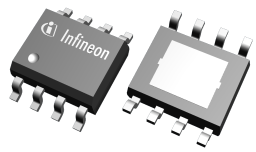
AEC Qualified | RoHS

Features



- AEC-Q100 Grade 1 for extended mission profiles
- 250 mA current capability
- Very high tracking accuracy
- Output voltage adjustable down to 2.0 V
- Stable with ceramic output capacitors
- Very low dropout voltage of typically 250 mV at 250 mA
- Very low current consumption of 0.1 µA in standby mode
- Overvoltage and undervoltage indication at power good output
- Internally controlled soft start
- Wide input voltage range: -16 V ≤ V_{IN} ≤ 45 V
- Wide temperature range: -40°C ≤ T_j ≤ 160°C
- Short circuit protected output (to GND and to battery)
- Reverse polarity protected input
- Overtemperature protection
- Infineon automotive quality
- Green Product (RoHS compliant)

Potential applications

- Truck applications
- CAV applications
- x-EV applications
- Automotive sensor supply
- Protected sensor supply for off-board sensors
- Secondary voltage supply in automotive ECU
- High-precision voltage tracking
- Precision voltage replication
- Power switch for off-board load

Product validation

Qualified for automotive applications with extended lifetime requirements. Product validation according to AEC-Q100.

Description

The OPTIREG™ linear voltage regulator TLT125D0EJ is a monolithic, integrated low-dropout voltage tracking regulator with high accuracy in a small PG-DSO-8 exposed pad package. The TLT125D0EJ is designed to supply off-board systems, for example sensors in powertrain management systems under the severe conditions of automotive applications. The TLT125D0EJ provides protection functions against reverse polarity as well as against short circuit to GND and to battery. The output voltage follows the reference voltage that is applied to the ADJ input with very high accuracy, up to a supply voltage of 40 V and up to an output current of 250 mA. The required minimum reference voltage at ADJ is 2.0 V.

Type	Package	Marking
TLT125D0EJ	PG-DSO-8	T125D0

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1 Block diagram

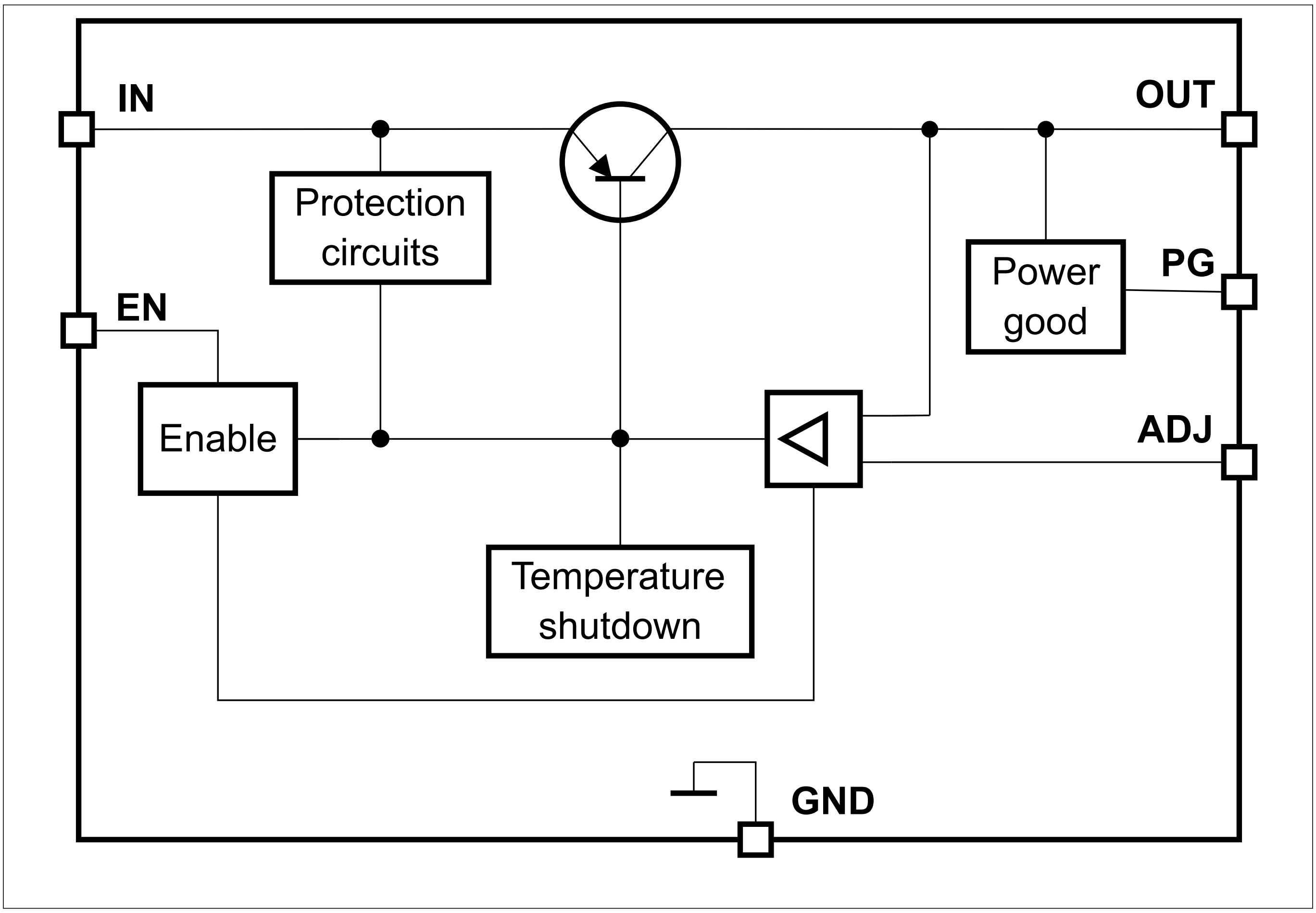


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

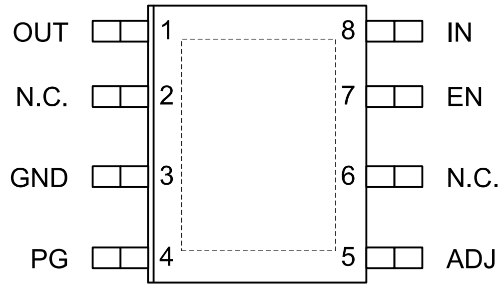


Figure 2 **Pin configuration**

2.2 Pin definitions and functions

Pin	Symbol	Function
1	OUT	Tracker output: 250 mA output current capability. Connect this pin to an output capacitor C_{OUT} to GND close to the IC's terminals, respecting capacitance and *ESR* requirements given in Functional range.
2	N.C.	Not connected
3	GND	Ground
4	PG	Power good output: Connect this pin via a pull-up resistor to a positive voltage rail. A "low" signal indicates a fault condition of the tracker output. This pin is an open drain output.
5	ADJ	Adjust input: Connect this pin to the reference voltage.
6	N.C.	Not connected
7	EN	Enable input: "High" enables the device. "Low" disables the device. If the enable function is not required, then connect this pin to IN.
8	IN	Input: It is recommended to connect this pin to GND using a small ceramic capacitor close to the pins in order to compensate line influence.
Pad	–	Exposed pad: Connect the exposed pad to GND. It is recommended to connect the exposed pad to a heat sink.

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings[1)]

T_j = -40°C to 160°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Input IN							
Voltage	V_{IN}	-16	–	45	V	–	P_3.1.1
Enable EN							
Voltage	V_{EN}	-16	–	45	V	–	P_3.1.2
Adjust ADJ							
Voltage	V_{ADJ}	-16	–	45	V	–	P_3.1.3
Output OUT							
Voltage	V_{OUT}	-5	–	45	V	–	P_3.1.4
Input output voltage difference							
Voltage	V_{IN}-V_{OUT}	-30	–	45	V	–	P_3.1.5
Power good PG							
Voltage	V_{PG}	-0.3	–	7	V	–	P_3.1.6
Temperatures							
Junction temperature	T_j	-40	–	160	°C	–	P_3.1.7
Storage temperature	T_{stg}	-55	–	150	°C	–	P_3.1.8
ESD susceptibility							
ESD susceptibility to GND	$V_{ESD,HBM}$	-4	–	4	kV	[2)] Human Body Model (HBM)	P_3.1.9
ESD susceptibility to GND	$V_{ESD,CDM}$	-1	–	1	kV	[3)] Charged Device Model (CDM)	P_3.1.10
ESD susceptibility to GND	$V_{ESD,CDM}$	-1	–	1	kV	[3)] Charged Device Model (CDM) at corner pins	P_3.1.11

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).
3) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101.

Notes:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.*

2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as outside the normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 2 Functional range

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Input voltage range	V_{IN}	4	–	40	V	–	P_3.2.1
Enable voltage range	V_{IN}	2	–	40	V	–	P_3.2.2
Adjust input voltage range (voltage tracking range)	V_{ADJ}	2	–	14	V	–	P_3.2.3
Capacitance of output capacitor	C_{OUT}	1	–	–	µF	[1) 2)]	P_3.2.4
Equivalent series resistance of output capacitor	$ESR_{C_{OUT}}$	–	–	5	Ω	–[2)]	P_3.2.5
Junction temperature	T_j	-40	–	160	°C	–	P_3.2.6

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.
2) Not subject to production test, specified by design.

Note: *Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.*

3.3 Thermal resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Table 3 Thermal resistance [1)]

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	21	–	K/W	–	P_3.3.1
Junction to pin	R_{thJP}	–	84	–	K/W	–	P_3.3.2
Junction to ambient	R_{thJA}	–	53	–	K/W	[2)] 2s2p board	P_3.3.3
Junction to ambient	R_{thJA}	–	151	–	K/W	[3)] 1s0p board, footprint only	P_3.3.4
Junction to ambient	R_{thJA}	–	77	–	K/W	[3)] 1s0p board, 300 mm^2 heatsink area on PCB	P_3.3.5
Junction to ambient	R_{thJA}	–	66	–	K/W	[3)] 1s0p board, 600 mm^2 heatsink area on PCB	P_3.3.6

1) Not subject to production test, specified by design.
2) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with two inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable, a thermal via array next to the package contacted the first inner copper layer.
3) Specified R_{thJA} value is according to JEDEC JESD51-3 at natural convection on FR4 1s0p board; the product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with one copper layer (1 × 70 µm Cu).

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information visit www.jedec.org.

4 Block description and electrical characteristics

4.1 Functional description tracking regulator

The regulator controls the output voltage V_{OUT} by comparing it to the voltage applied to the ADJ pin and driving a PNP pass transistor accordingly. The stability of the control loop depends on:

- The output capacitor C_{OUT}
- Load current
- Chip temperature
- The poles and zeroes in the frequency response of the circuit consisting of TLT125D0EJ and the load

An input capacitor C_{IN} is strongly recommended for buffering the line influence.

To ensure stable operation, the output capacitor's capacitance and its equivalent series resistance *ESR* must fulfill the requirements in the Functional range. The output capacitor must be sized suitably to buffer load transients.

Connect each capacitor close to the pins.

The internal protection features are designed to protect the device itself as well as the application from destruction in case of catastrophic events. These safeguards contain:

- Output current limitation
- Reverse polarity protection
- Thermal shutdown

Output current limitation

In order to protect the pass element and the package from excessive power dissipation, the device limits the maximum output current at high input voltage.

Reverse polarity protection

The device allows a negative supply voltage. However, in reverse polarity condition several small currents flowing into the device increase the junction temperature. Thermal design must consider this effect,because in reverse polarity condition the overtemperature protection circuit does not operate.

Thermal shutdown

The overtemperature protection circuit is designed to prevent immediate destruction of the device in certain fault conditions (for example a permanent short circuit at output) by switching off the power stage. After the chip cools down, the regulator restarts. If the fault is not removed, then this leads to an oscillatory behavior of the output voltage. A junction temperature above 160 is outside the maximum ratings and reduces the lifetime of the device.

4.2 Electrical characteristics tracking regulator

Table 4 Electrical characteristics tracking regulator

V_{IN} = 13.5 V; V_{ADJ} ≥ 2.0 V; V_{EN} ≥ 2.0 V; T_j = -40°C to 160°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Tracking output							
Output voltage tracking accuracy	ΔV_{OUT}	-7	–	7	mV	$\Delta V_{OUT} = V_{ADJ} - V_{OUT}$; 5.5 V ≤ V_{IN} ≤ 22 V; 0.1 mA ≤ I_{OUT} ≤ 250 mA; 2 V ≤ V_{ADJ} ≤ V_{IN} -0.5 V	P_4.1.1
Output voltage tracking accuracy	ΔV_{OUT}	-7	–	7	mV	$\Delta V_{OUT} = V_{ADJ} - V_{OUT}$; 5.5 V ≤ V_{IN} ≤ 32 V; 0.1 mA ≤ I_{OUT} ≤ 120 mA; 2 V ≤ V_{ADJ} ≤ V_{IN} -0.5 V	P_4.1.2
Load regulation steady state	$\Delta V_{OUT,load}$	-10	-1	–	mV	0.1 mA ≤ I_{OUT} ≤ 250 mA; V_{ADJ} = 5 V	P_4.1.3
Line regulation steady state	$\Delta V_{OUT,line}$	–	1	10	mV	5.5 V ≤ V_{IN} ≤ 32 V; I_{OUT} = 10 mA; V_{ADJ} = 5 V	P_4.1.4
Power supply ripple rejection	*PSRR*	–	80	–	dB	[1] f_{ripple} = 100 Hz; V_{ripple} = 1 Vpp; I_{OUT} = 10 mA; C_{OUT} = 10 µF; ceramic type	P_4.1.5
Output current limitation	$I_{OUT,max}$	251	550	750	mA	$V_{OUT} = V_{ADJ}$ - 0.1 V; V_{ADJ} = 5 V	P_4.1.6
Reverse current	$I_{OUT,rev}$	-10	-1	–	mA	V_{IN} = 0 V; V_{OUT} = 16 V; V_{ADJ} = 5 V	P_4.1.9
Reverse current at negative input voltage	$I_{IN,rev}$	-10	-2	–	mA	V_{IN} = -16 V; V_{OUT} = 0 V; V_{ADJ} = 5 V	P_4.1.10
Dropout voltage	V_{dr}	–	250	500	mV	[2] $V_{dr} = V_{IN} - V_{OUT}$; I_{OUT} = 250 mA; V_{ADJ} = 5 V	P_4.1.11

(table continues...)

Table 4 (continued) Electrical characteristics tracking regulator

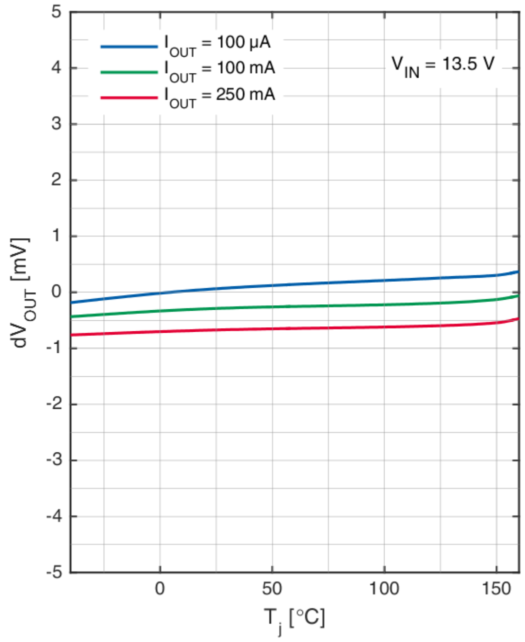
V_{IN} = 13.5 V; V_{ADJ} ≥ 2.0 V; V_{EN} ≥ 2.0 V; T_j = -40°C to 160°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Overtemperature protection							
Overtemperature shutdown threshold	$T_{j,sd}$	–	177	–	°C	T_j increasing due to power dissipation generated by the device	P_4.1.12
Overtemperature shutdown threshold hysteresis	$\Delta T_{j,sdh}$	–	10	–	K	–	P_4.1.13

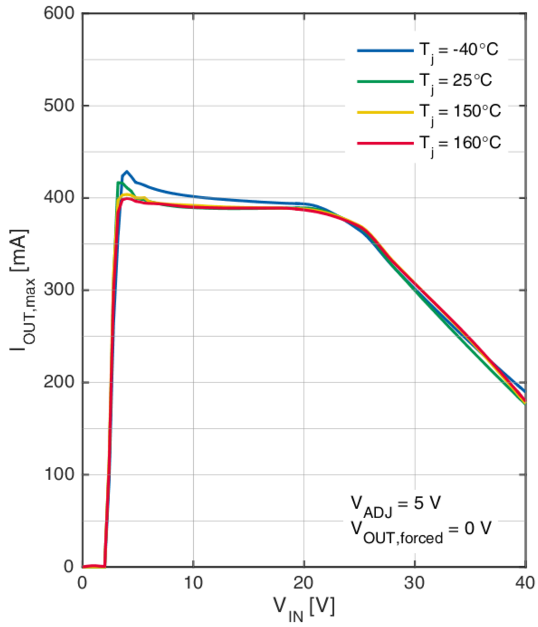
1) Not subject to production test, specified by design.
2) Measured when the output voltage V_{OUT} has dropped 100 mV from the nominal value obtained at V_{IN} = 13.5 V.

4.3 Typical performance characteristics tracking regulator

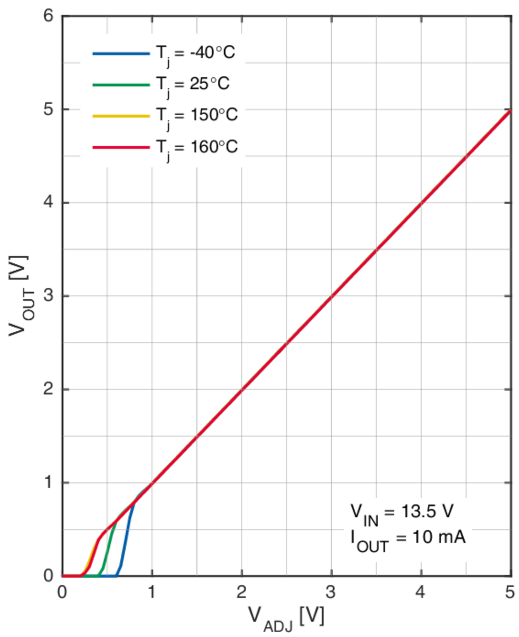
Tracking accuracy ΔV_{OUT} versus junction temperature T_j



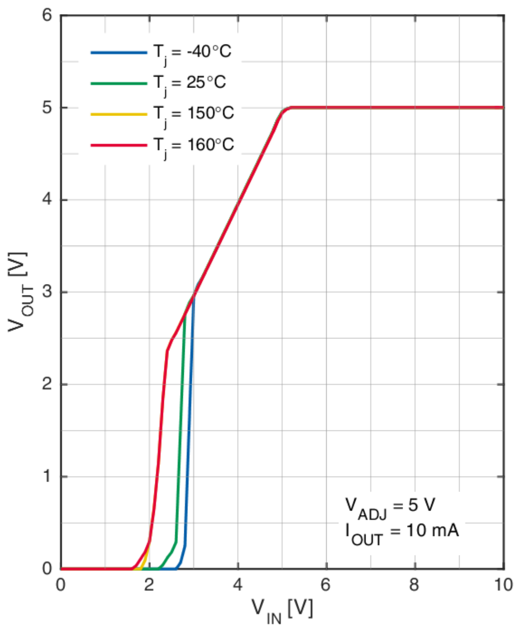
Output current limitation $I_{OUT,max}$ versus input voltage V_{IN}



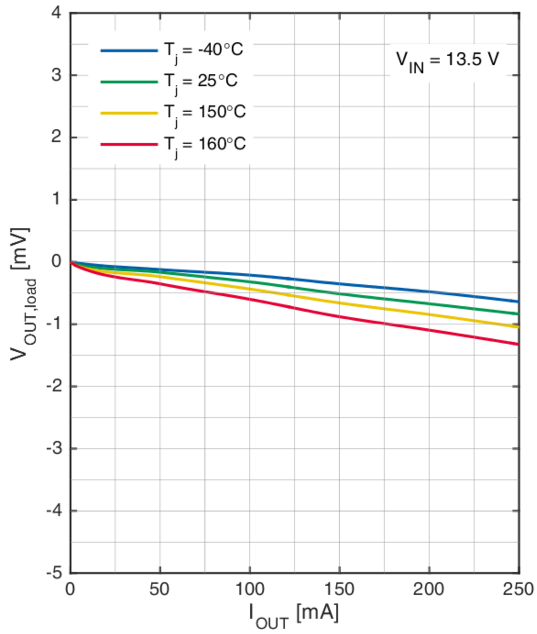
Output voltage V_{OUT} versus adjust voltage V_{ADJ}



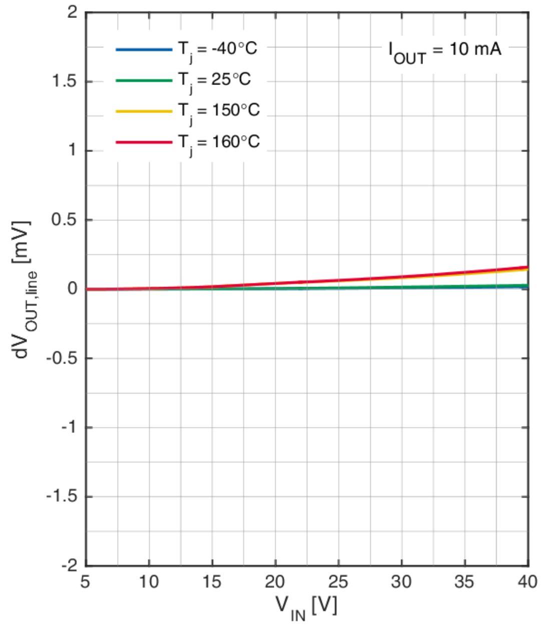
Output voltage V_{OUT} versus input voltage V_{IN}



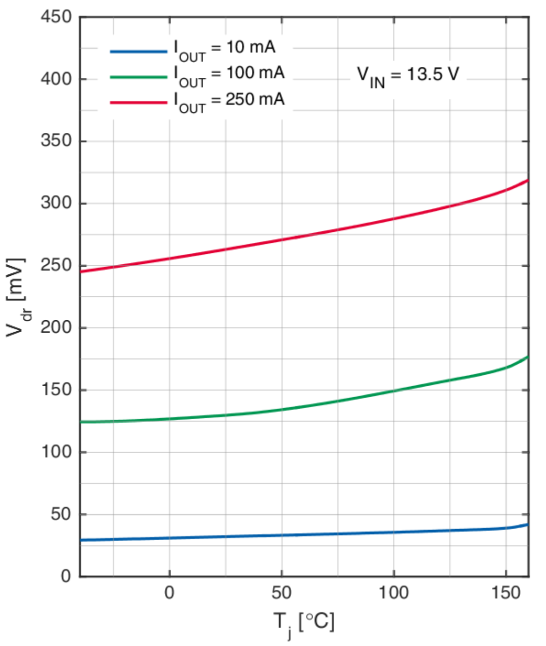
Load regulation $\Delta V_{OUT,load}$ versus output current I_{OUT}



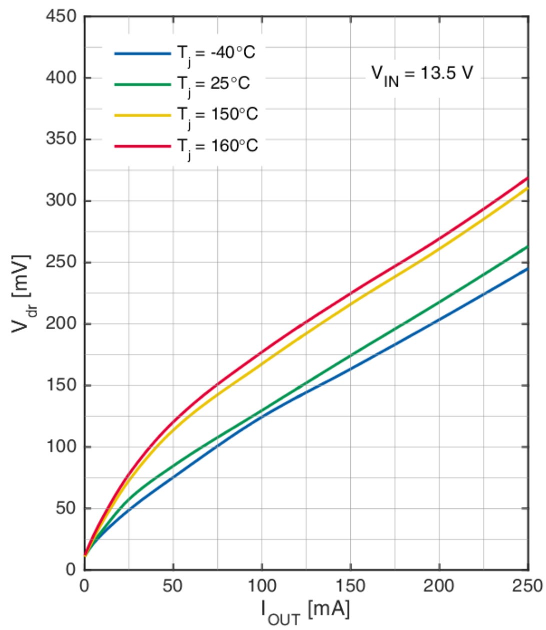
Line regulation $\Delta V_{OUT,line}$ versus input voltage V_{IN}



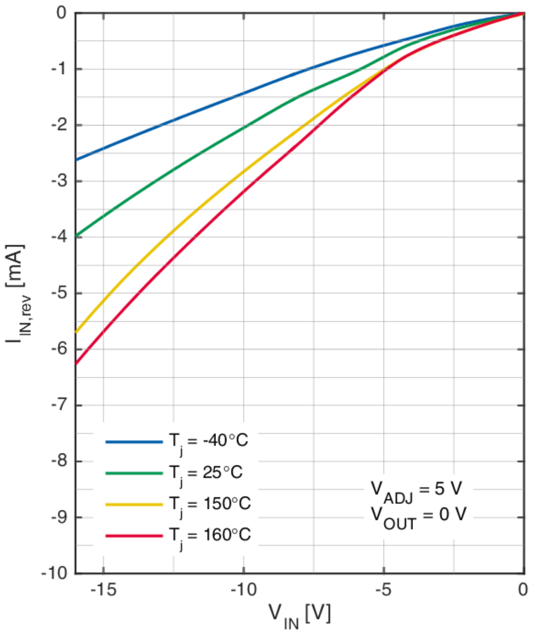
Dropout voltage V_{dr} versus junction temperature T_j



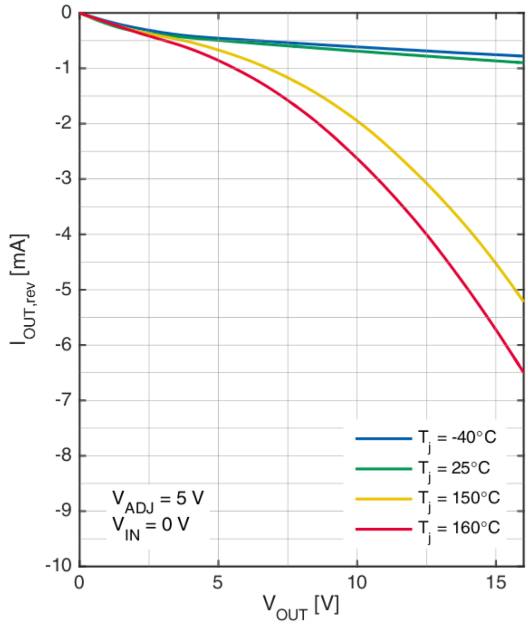
Dropout voltage V_{dr} versus output current I_{OUT}



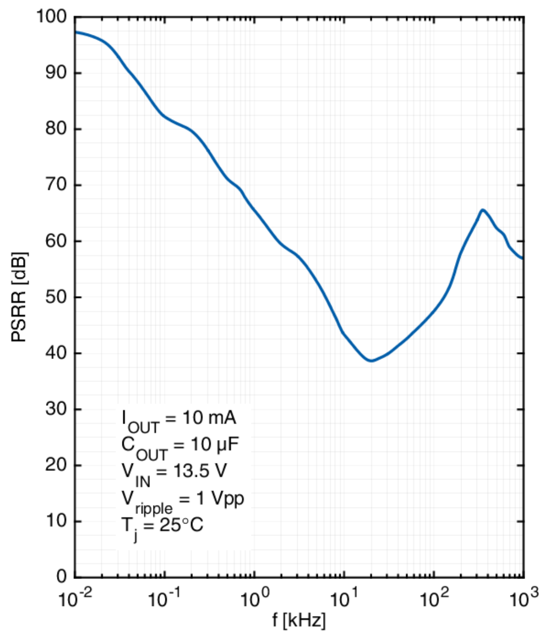
Reverse current $I_{IN,rev}$ versus input voltage V_{IN}



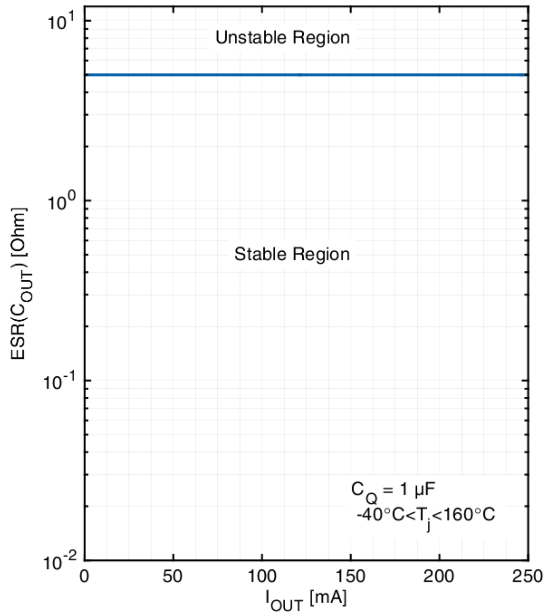
Reverse current $I_{OUT,rev}$ versus output voltage V_{OUT}



Power supply ripple rejection *PSRR* versus ripple frequency f_r



Output capacitor $ESR_{C_{OUT}}$ versus output current I_{OUT}



4.4 Electrical characteristics current consumption

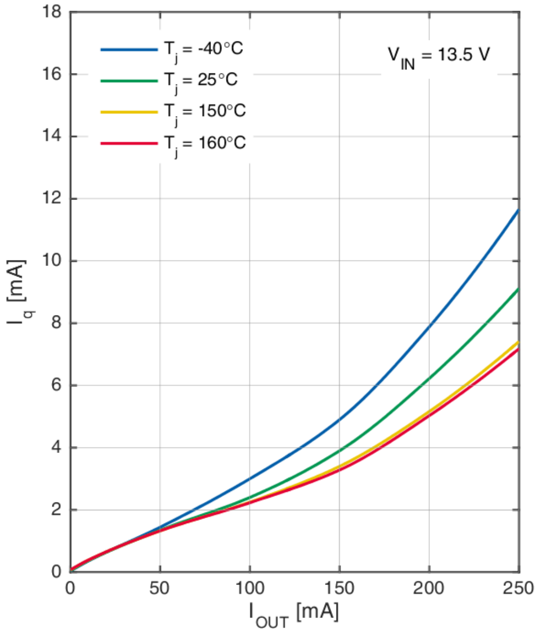
Table 5 Electrical characteristics current consumption

V_{IN} = 13.5 V; $V_{ADJ} \geq 2.0$ V; $V_{EN} \geq 2.0$ V; T_j = -40°C to 160°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

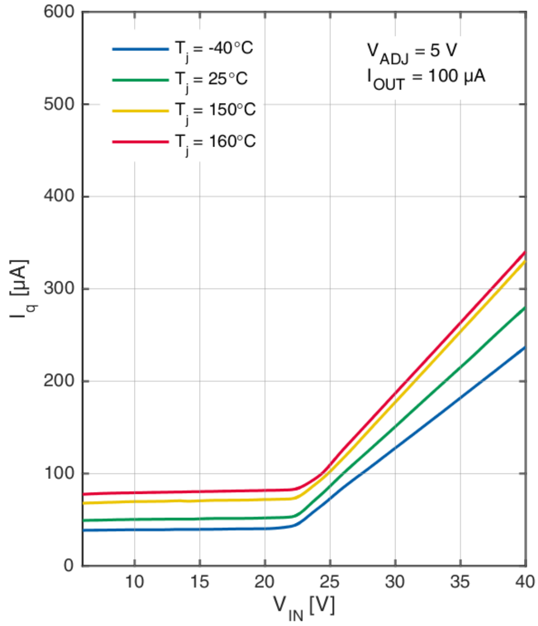
Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Current consumption stand-by state	$I_{q,off}$	–	0.1	7	µA	$I_{q,off} = I_{IN}$; $V_{EN} \leq 0.4$ V; $T_j \leq 125$°C	P_4.3.1
Current consumption	I_q	–	65	110	µA	$I_q = I_{IN} - I_{OUT}$; $I_{OUT} \leq 0.1$ mA; V_{ADJ} = 5 V; $T_j \leq$ 125°C	P_4.3.2
Current consumption	I_q	–	10	25	mA	$I_q = I_{IN} - I_{OUT}$; $I_{OUT} \leq 250$ mA; V_{ADJ} = 5 V	P_4.3.3

4.5 Typical performance characteristics current consumption

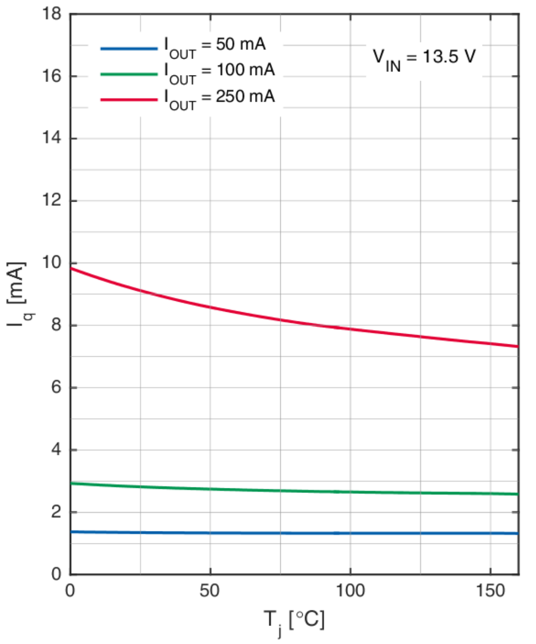
Current consumption I_q versus output current I_{OUT}



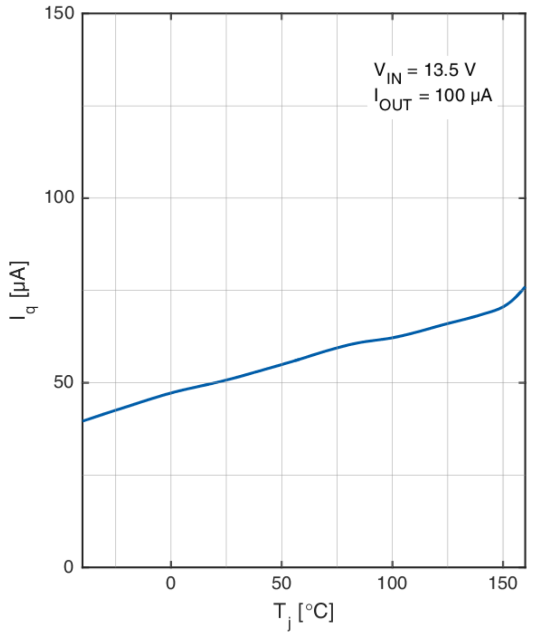
Current consumption I_q versus input voltage V_{IN}



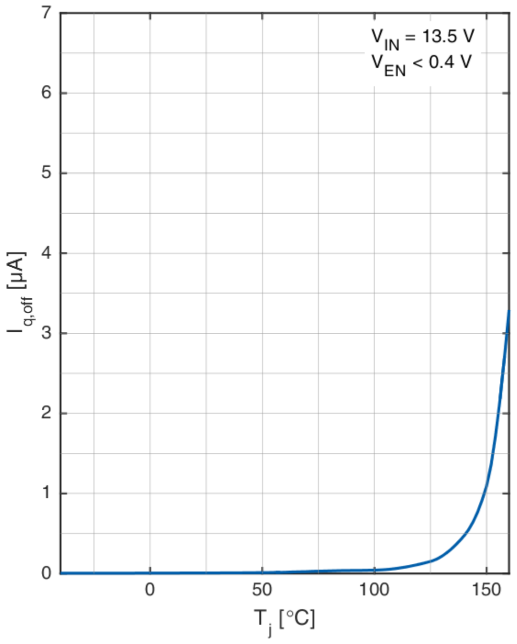
Current consumption I_q versus junction temperature T_j



Current consumption I_q versus junction temperature T_j (I_{OUT} low)



Current consumption in OFF mode $I_{q,off}$ versus junction temperature T_j



4.6 Functional description enable input

On a "low" signal at the enable input EN the device switches to standby mode in order to minimize the quiescent current.

If the EN pin is not connected, then the "low" level from the internal pull-down resistor switches off the regulator.

4.7 Electrical characteristics enable input

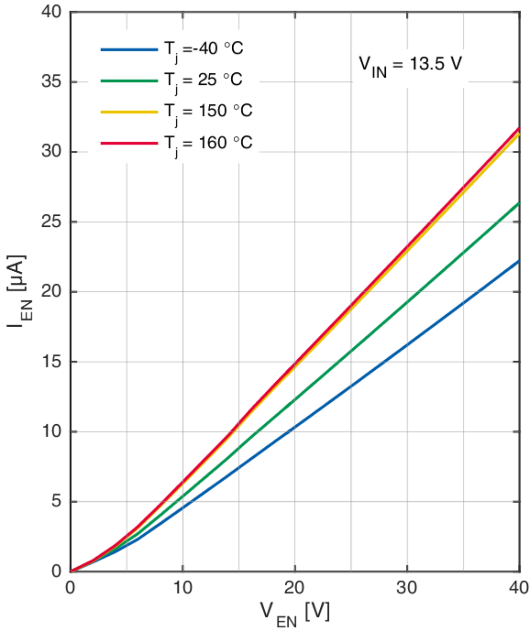
Table 6 Electrical characteristics enable input

V_{IN} = 13.5 V; $V_{ADJ} \geq 2.0$ V; T_j = -40°C to 160°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Enable off voltage range	$V_{EN,off}$	–	–	0.8	V	V_{OUT} = 0 V; $I_{OUT} \leq 5$ µA; $T_j \leq 125$°C	P_4.5.1
Enable on voltage range	$V_{EN,on}$	2	–	–	V	V_{OUT} settled	P_4.5.2
Enable input current	I_{EN}	–	2	4	µA	V_{EN} = 5 V	P_4.5.3

4.8 Typical performance characteristics enable input

Enable input current I_{EN} versus
enable input voltage V_{EN}



4.9 Functional description adjust input

The adjust input must be connected to the reference voltage that the device tracks.

4.10 Electrical characteristics adjust input

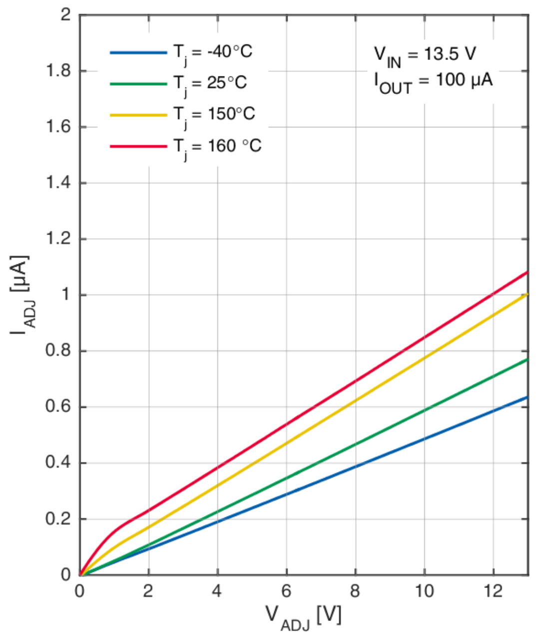
Table 7 Electrical characteristics adjust input

V_{IN} = 13.5 V; V_{ADJ} ≥ 2.0 V; V_{EN} ≥ 2.0 V; T_j = -40°C to 160°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

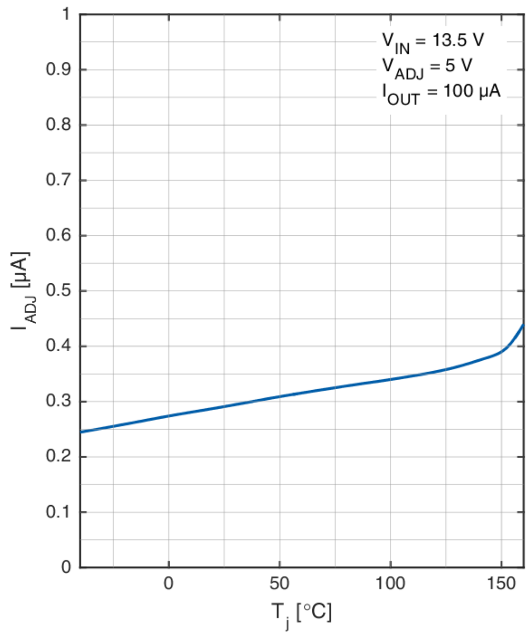
Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Adjust input current	I_{ADJ}	–	0.2	1.5	µA	V_{ADJ} = 5 V	P_4.7.1

4.11 Typical performance characteristics adjust input

Adjust input current I_{ADJ} versus adjust input voltage V_{ADJ}



Adjust input current I_{ADJ} versus junction temperature T_j



4.12 Functional description power good output

The power good output PG indicates an overvoltage or undervoltage condition of the tracker output. For this the device compares the output voltage V_{OUT} to the reference voltage V_{ADJ}. The device indicates variations of the output voltage beyond the power good switching thresholds by a "low" signal at the power good output PG. Transients shorter than the power good reaction time $t_{PG,r}$ do not trigger the power good output.

The power good release delay time $t_{PG,r}$ allows a microcontroller and an oscillator to start up. The power good release delay time is the time period from exceeding the power good switching thresholds until the device switches the power good output from "low" to "high".

The power good output PG is an open drain output that requires a pull-up resistor to a positive voltage rail. The pull-up voltage must maintain the absolute maximum ratings of power good PG, see Absolute maximum ratings.

4.13 Electrical characteristics power good output

Table 8 Electrical characteristics power good output

V_{IN} = 13.5 V; V_{ADJ} ≥ 2.0 V; V_{EN} ≥ 2.0 V; T_j = -40°C to 160°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Power good switching threshold, undervoltage	$V_{OUT,UV}$	V_{ADJ} - 120	V_{ADJ} - 70	V_{ADJ} - 50	mV	V_{OUT} decreasing; $V_{IN} \geq V_{ADJ}$ + 150 mV	P_4.9.1
Power good switching threshold, overvoltage	$V_{OUT,OV}$	V_{ADJ} + 50	V_{ADJ} + 70	V_{ADJ} + 120	mV	V_{OUT} increasing; $V_{IN} \geq V_{ADJ}$ + 150 mV	P_4.9.2
Power good reaction time	$t_{PG,r}$	10	15	30	µs	–	P_4.9.3
Power good release delay time	$t_{PG,rd}$	100	250	650	µs	–	P_4.9.4
Power good output low voltage	$V_{PG,low}$	–	0.2	0.4	V	V_{IN} ≥ 4 V; $I_{PG,ext}$ ≤ 1.8 mA	P_4.9.5
Power good output external input current	$I_{PG,ext}$	–	–	1.8	mA	V_{PG} ≤ 0.4 V	P_4.9.6
Power good output leakage current	$I_{PG,leak}$	–	0	2	µA	$V_{OUT} = V_{ADJ}$; V_{PG} = 5 V	P_4.9.7

5 Application information

Note: The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

5.1 Application diagram

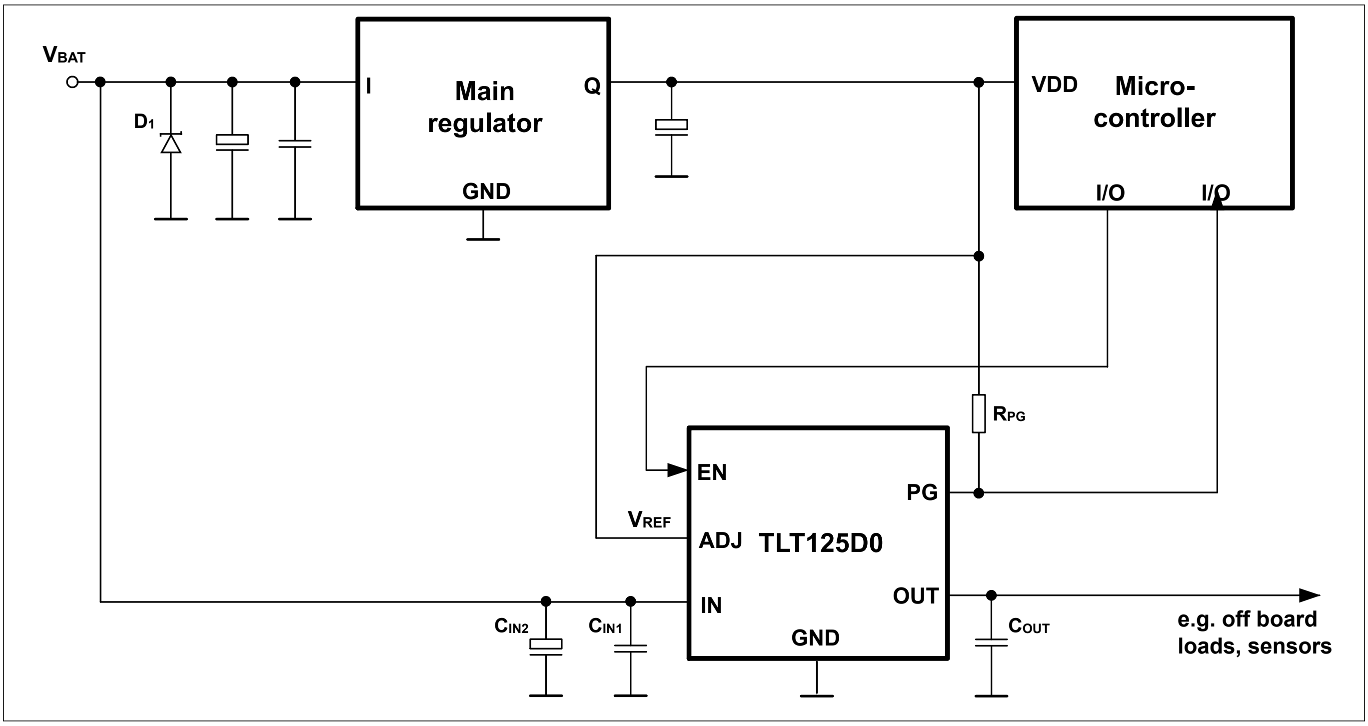


Figure 3 Application diagram

Note: This figure is a simplified example of an application circuit. The function must be verified in the application.

5.2 Selection of external components

5.2.1 Input pin

Figure 3 shows the typical input circuitry for a voltage tracking regulator. The following external components at the input are recommended in case of possible external disturbance:

Ceramic capacitor

A ceramic capacitor C_{IN1} (100 nF to 470 nF) at the input filters high frequency disturbance imposed by the line, such as ISO pulses 3a/b. Place C_{IN1} as close as possible to the input pin of the voltage tracking regulator on the PCB.

Aluminum electrolytic capacitor

An aluminum electrolytic capacitor C_{IN2} (10 µF to 470 µF) at the input smoothens high energy pulses, such as ISO pulse 2a. Place C_{IN2} close to the input pin of the voltage tracking regulator on the PCB.

Overvoltage suppression diode

A suitably sized diode D_1 suppresses high voltage beyond the maximum ratings of the circuit components and protects the device from damage due to overvoltage.

5.2.2 Output pin

An output capacitor C_{OUT} is necessary for the stability of the voltage tracking regulator, see Functional range. The typical performance graph Output capacitor ESRCOUT versusoutput current IOUT shows the stable operation range of the device.

In an automotive environment, ceramic capacitors with X5R or X7R dielectrics are recommended.

Place C_{OUT} on the same side of the PCB as the device and as close as possible to both the OUT pin and GND pin.

In case of rapid transients of the input voltage or of the load current, C_{OUT} must be dimensioned properly to ensure the output stability in the application.

5.2.3 Adjust pin

Figure 3 shows a typical adjust circuitry for a voltage tracking regulator. Typically the adjust pin is connected to a fixed voltage reference that the regulator tracks. In the example of the application diagram ADJ is connected to the supply voltage of a microcontroller. Alternatively, the voltage reference can also be adjusted by a voltage divider.

5.2.4 Power good pin

The power good output is an open drain output, which requires a pull-up resistor to a positive voltage rail. The pull-up voltage must maintain the maximum ratings in Absolute maximum ratings. The example in Figure 3 uses the supply voltage VDD of a microcontroller as pull-up.

To limit the external input current according to the requirement in Functional description power good output), the pull-up resistor must be sized depending on the pull-up voltage.

5.3 Thermal considerations

From the known input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_q$$

Equation 1

with

- P_D: continuous power dissipation
- V_{IN}: input voltage
- V_{OUT}: output voltage
- I_{OUT}: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} can then be calculated:

$$R_{\text{thJA, max}} = \frac{T_{j,\text{max}} - T_a}{P_D}$$

Equation 2

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in Thermal resistance.

Example

Application conditions:
V_{IN} = 13.5 V
V_{OUT} = V_{ADJ} = 5 V
I_{OUT} = 100 mA
T_a = 75°C
Calculation of $R_{thJA,max}$:

$$P_\text{D} = (V_\text{IN} - V_\text{OUT}) \times I_\text{OUT} + V_\text{IN} \times I_\text{q} = (13.5\text{ V} - 5\text{ V}) \times 100\ \text{ mA} + 13.5\text{ V} \times 3.5\text{ mA} = 0.897\text{ W}$$

Equation 3

$$R_{\text{thJA, max}} = \frac{T_{\text{j,max}} - T_\text{a}}{P_\text{D}} = \frac{150°\text{C} - 75°\text{C}}{0.897\text{ W}} = 83.6\text{ K/W}$$

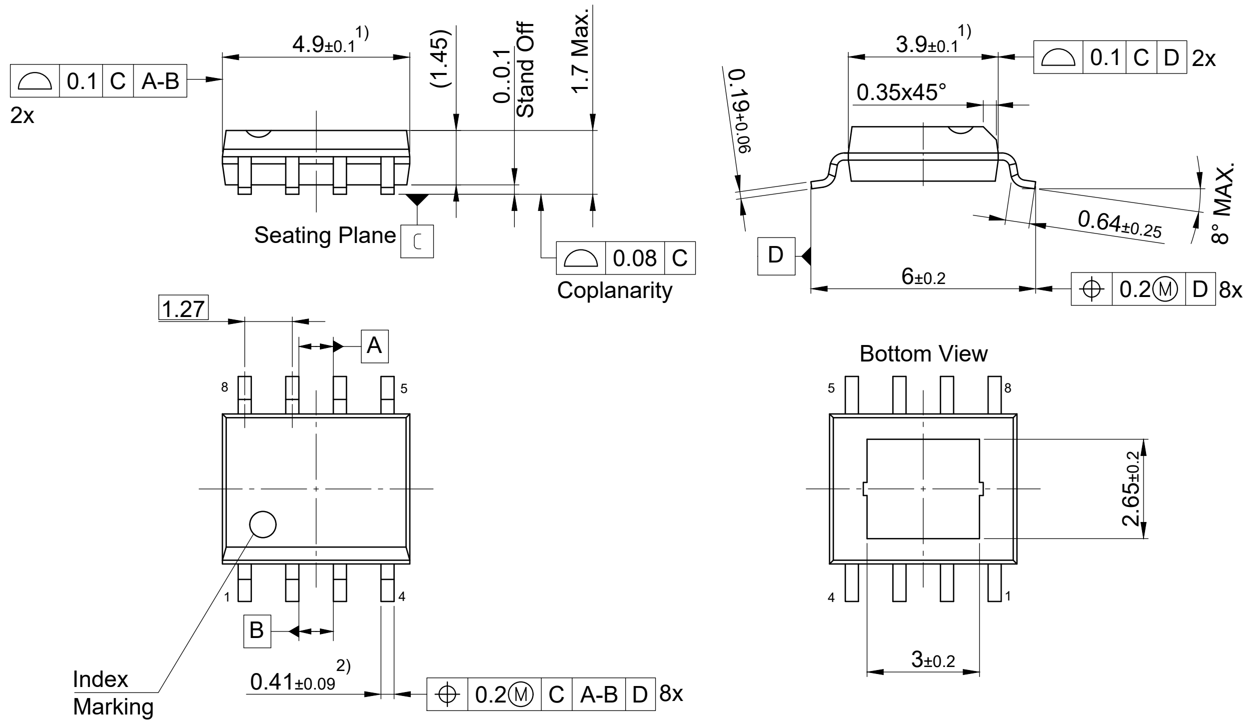
Equation 4

As a result, the PCB design must ensure a thermal resistance R_{thJA} lower than 83.6 K/W. According to Thermal resistance, at least 300 mm^2 heatsink area is required on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

5.4 Further application information

- For further information you may contact http://www.infineon.com/

6 Package information



1) Does not include plastic or metal protrusion of 0.15max. per side

2) Dambar protrusion shall be maximum 0.1mm total in excess of lead width

All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 4 **PG-DSO-8**

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Information on alternative packages

Please visit www.infineon.com/packages.

Revision history

Revision	Date	Changes
1.03	2022-11-10	Datasheet updated • Editorial changes
1.02	2021-06-10	Datasheet updated • Editorial changes
1.01	2021-05-28	Datasheet updated • Editorial changes
1.0	2020-10-23	Datasheet created

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