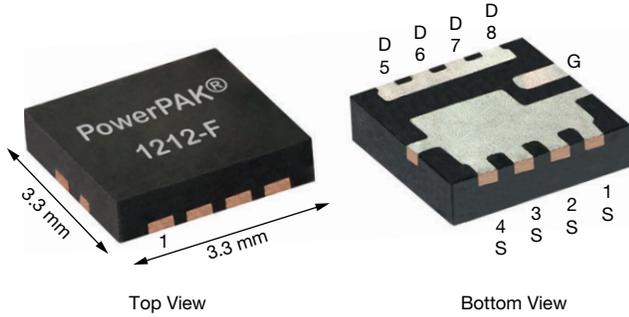


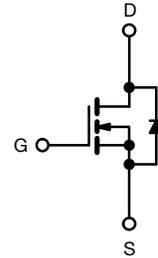
N-Channel 100 V (D-S) MOSFET

PowerPAK® 1212-F

FEATURES

- TrenchFET® Gen IV power MOSFET
- Very low $R_{DS(on)} \times Q_g$ figure-of-merit (FOM)
- Source flip technology, enhance thermal performance
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE
APPLICATIONS

- DC/DC converter
- Synchronous rectification
- Battery management
- Oring and load switch



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	100
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.012
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0145
Q_g typ. (nC)	18
I_D (A)	44 ^a
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 1212-F
Lead (Pb)-free and halogen-free	SiSD4112LDN-T1-UE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	100	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	I_D	44	A
	$T_C = 70$ °C		35.5	
	$T_A = 25$ °C		14 ^{b, c}	
	$T_A = 70$ °C		11 ^{b, c}	
Pulsed drain current ($V_{GS} = 10$ V, $t = 100$ μ s)		I_{DM}	100	
Continuous source-drain diode current	$T_C = 25$ °C	I_S	52	
	$T_A = 25$ °C		4.9 ^{b, c}	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	15	mJ
Single pulse avalanche energy		E_{AS}	11	
Maximum power dissipation	$T_C = 25$ °C	P_D	57	W
	$T_C = 70$ °C		36	
	$T_A = 25$ °C		5.4 ^{b, c}	
	$T_A = 70$ °C		3.5 ^{b, c}	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{d, e}			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SMYBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, f}	$t \leq 10$ s	R_{thJA}	18	23	°C/W
Maximum junction-to-case (source)	Steady state	R_{thJC}	1.7	2.2	

Notes

- Based on $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-F is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 56 °C/W



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	82	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-5.0	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1	-	2.4	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A	-	0.0095	0.012	Ω
		V _{GS} = 4.5 V, I _D = 10 A	-	0.0104	0.0145	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 50 A	-	112	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz	-	2700	-	pF
Output capacitance	C _{oss}		-	170	-	
Reverse transfer capacitance	C _{rss}		-	9	-	
C _{rss} /C _{iss} ratio			-	0.003	0.006	
Total gate charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 15 A	-	40	60	nC
Gate-source charge	Q _{gs}	V _{DS} = 50 V, V _{GS} = 4.5 V, I _D = 15 A	-	18	27	
Gate-drain charge	Q _{gd}		-	8.3	-	
Output charge	Q _{oss}		-	3.8	-	
Gate resistance	R _g	V _{DS} = 50 V, V _{GS} = 0 V f = 1 MHz	0.12	0.6	1.3	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 50 V, R _L = 5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	10	20	ns
Rise time	t _r		-	5	10	
Turn-off delay time	t _{d(off)}		-	25	50	
Fall time	t _f		-	5	10	
Turn-on delay time	t _{d(on)}	V _{DD} = 50 V, R _L = 5 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	22	45	
Rise time	t _r		-	21	45	
Turn-off delay time	t _{d(off)}		-	28	60	
Fall time	t _f		-	5	10	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	52	A
Pulse diode forward current ^a	I _{SM}		-	-	100	
Body diode voltage	V _{SD}	I _S = 10 A	-	0.77	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	40	80	ns
Body diode reverse recovery charge	Q _{rr}		-	61	125	nC
Reverse recovery fall time	t _a		-	34	-	ns
Reverse recovery rise time	t _b		-	6	-	

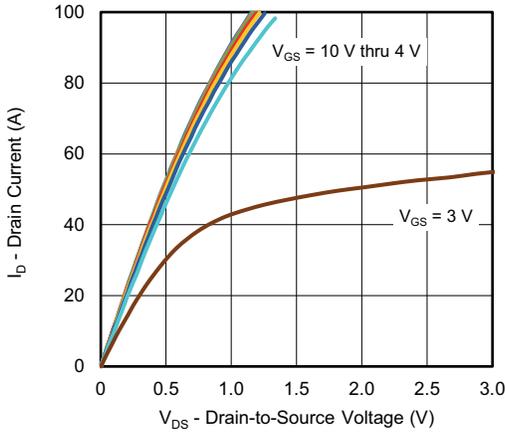
Notes

- a. Pulse test: pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing
- c. Based on characterization, not subject to production testing

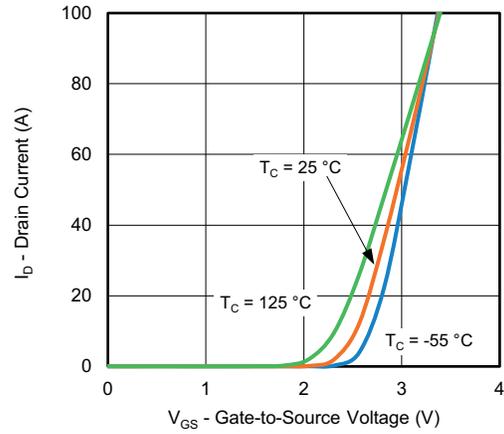
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



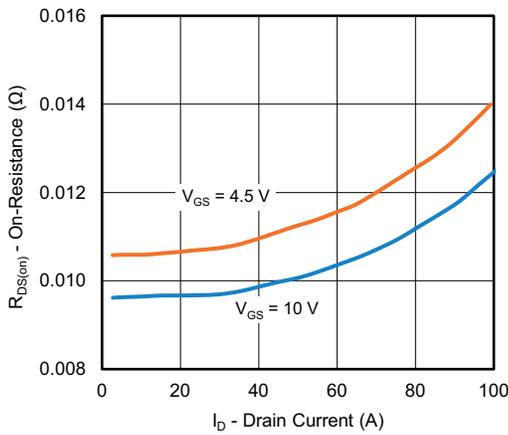
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



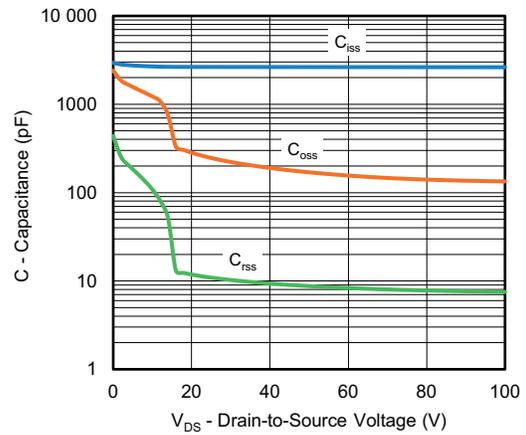
Output Characteristics



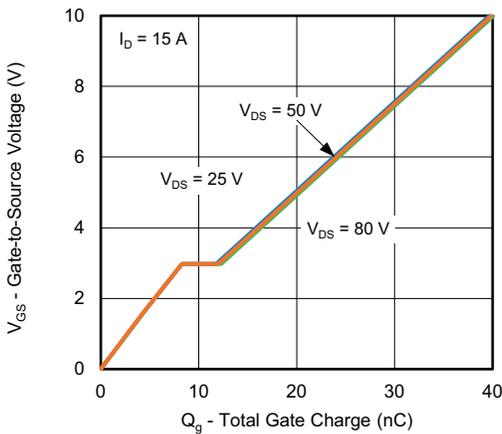
Transfer Characteristics



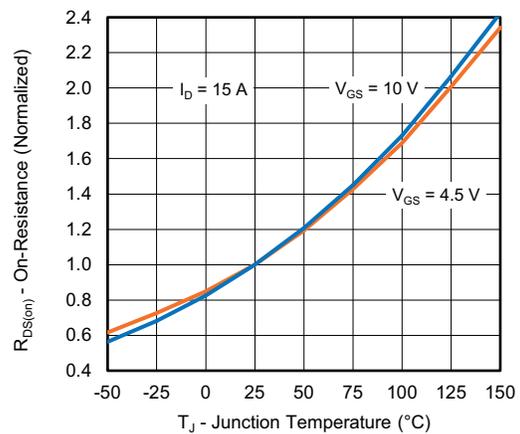
On-Resistance vs. Drain Current



Capacitance



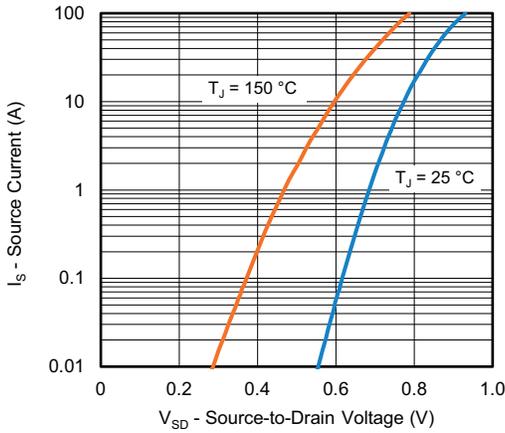
Gate Charge



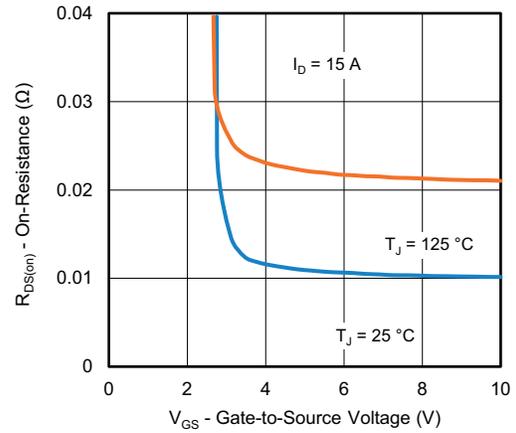
On-Resistance vs. Junction Temperature



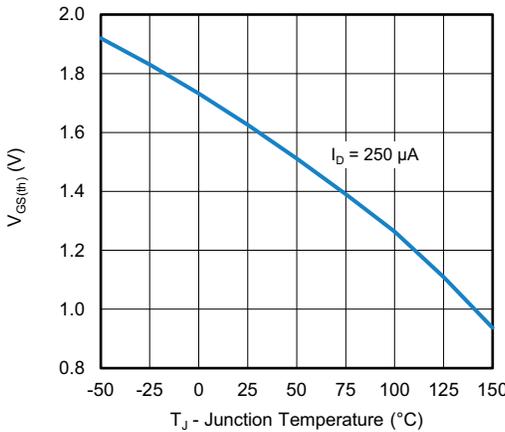
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



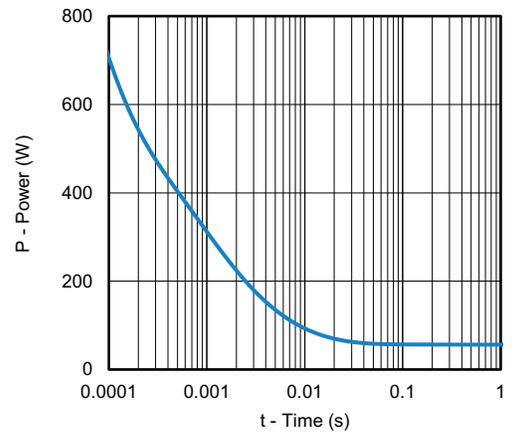
Source-Drain Diode Forward Voltage



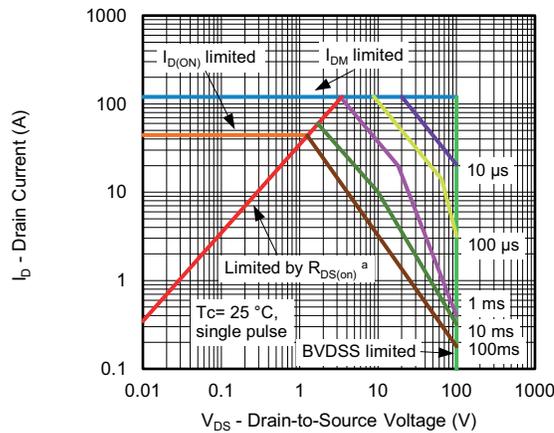
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Case



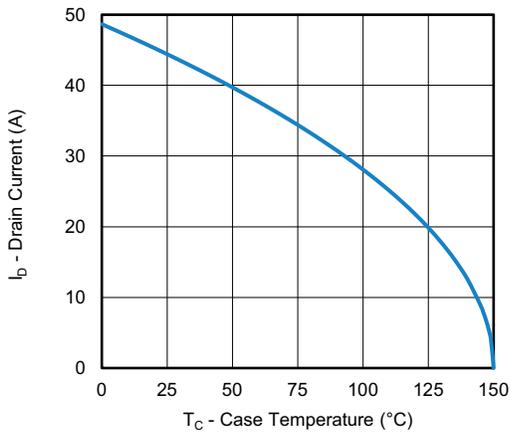
Safe Operating Area

Note

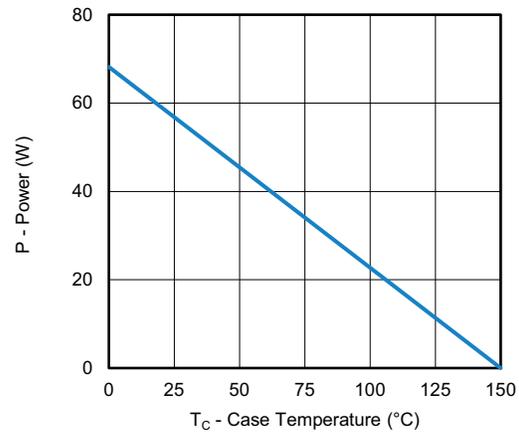
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



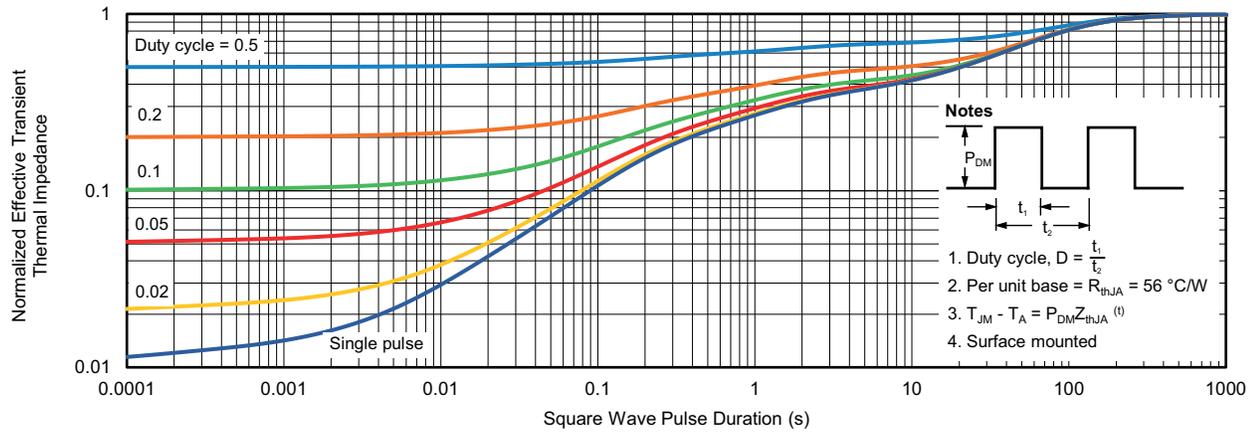
Power, Junction-to-Case

Note

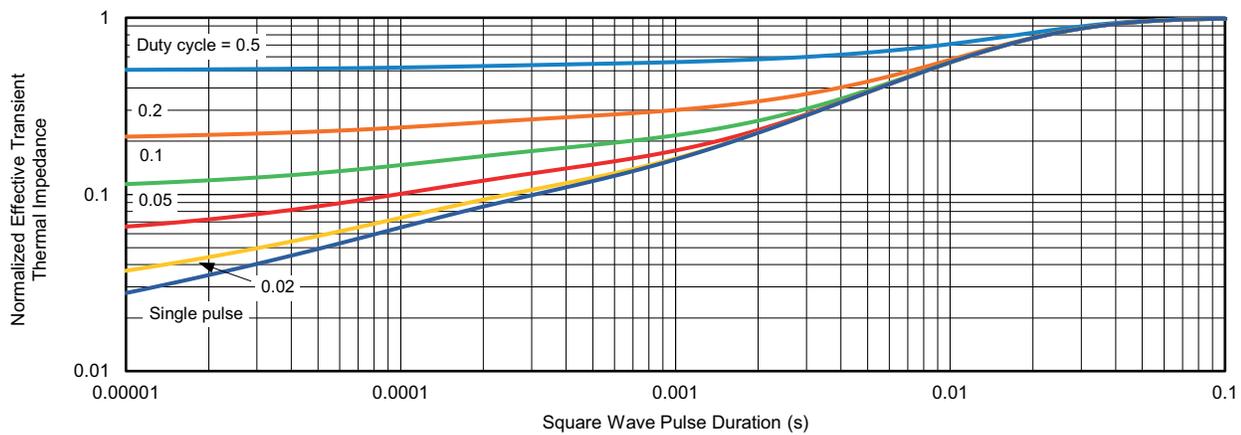
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



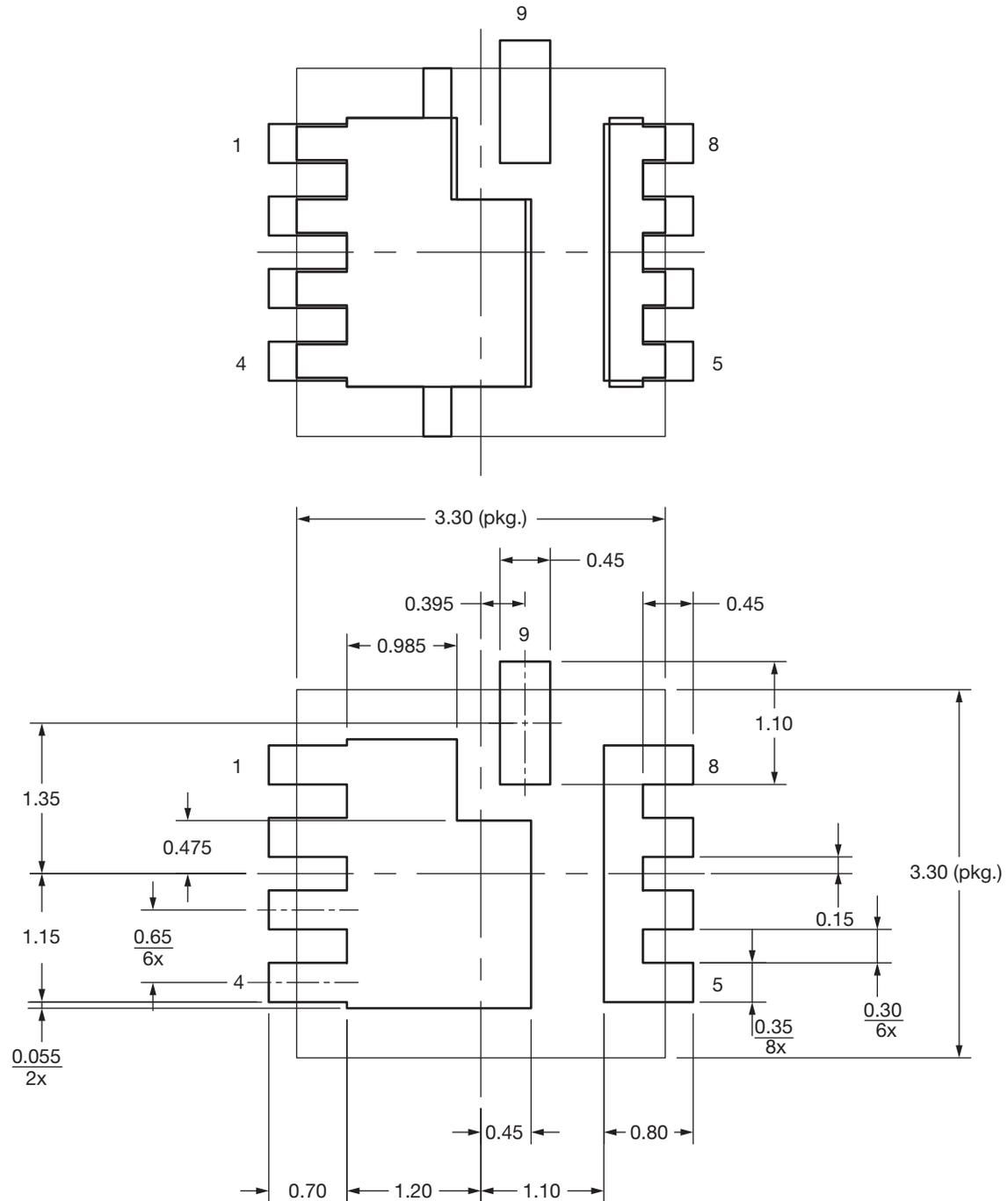
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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Recommended Land Pattern PowerPAK® 1212-F



Note

- Dimensions in mm

ECN: T23-0022-Rev. A, 30-Jan-2023
 DWG: 3017



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