HY16F184
HY16F187
HY16F188
Datasheet

High Precision Mixed-Signal Controller
Embedded 65nV Resolution ADC
32-bit Low Power MCU
64KB Flash ROM

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1. Features

Digital Circuit

- 32-bit MCU 1T Andes Core N801
- C Complier & User Friendly Development Tools
- 2.2V to 3.6V operational voltage.
- -40 to 85℃ operational environment
- Low power operation:
  - Normal Mode: 1.1mA @ CPU_CK=2MHz
  - Idle Mode:5uA @ LSRC=35KHz
  - Sleep Mode: Typ. 2.5uA
- 64K Byte Flash ROM
- 8K Byte SRAM
- 16-bit PWM controller
- I2C/SPI/ UART communication Hardware IP
- RTC Hardware IP
- Low voltage detection/BOR circuit
- Programmable Digital I/O Ports

Analog Circuit

- An ultra low noise 24-bit SD ADC
  - Down to 65nVrms input refer noise
  - Conversion rate up to 10KSPS
  - Input amplification gain up to 128
  - Operation voltage 2.4V to 3.6V
- External High Speed Oscillator Max 16MHz
- External Low Speed Oscillator Mode 32768Hz
- Internal High Speed Oscillator Max 10MHz
- Internal Low Speed Oscillator 35KHz
- Power management
  - Charge Pump regulation
  - Build-in selectable VDDA voltage LDO
  - 1.2V Band gap reference output
- 8-bit resistor ladders can be used as 8-bit DAC
  - Programmable potentiometer
  - Monotonic guarantee
- rail-to-rail operation amplifier
  - CMOS input, 1MHz bandwidth
  - Can use as comparator
- Multi-function Analog Comparator
  - Support touch key

HY16F18 Series Selection Guide:

Part No.	Flash (byte)	SRAM (byte)	24-b ΣΔADC	UART	32-b SPI	I2C	I/O	PWM	8-bit Resistance Ladders	OPAMP	Comp.	Hardware RTC	Temp. Sensor	Change Pump	Package
HY16F184-L048	16K	2K	4-CH	1	1	1	18	2	8-bit	1	1	1	Y	N	LQFP48
HY16F184-N033	16K	2K	4-CH	1	1	1	18	2	8-bit	1	1	1	Y	N	QFN33
HY16F184-T028	16K	2K	4-CH	1	1	1	17	2	8-bit	1	1	1	Y	N	TSSOP28
HY16F187-L048	32K	4K	4-CH	1	1	1	18	2	8-bit	1	1	1	Y	N	LQFP48
HY16F187-N033	32K	4K	4-CH	1	1	1	18	2	8-bit	1	1	1	Y	N	QFN33
HY16F188-L048	64K	8K	4-CH	1	1	1	22	2	8-bit	1	1	1	Y	Y	LQFP48

Note: HY16F184-T028 package does not PT3.7 pin, it cannot do OPO op amp analog output pin function

2. Pin Definition

2.1. HY16F18 Series Pin Introduction

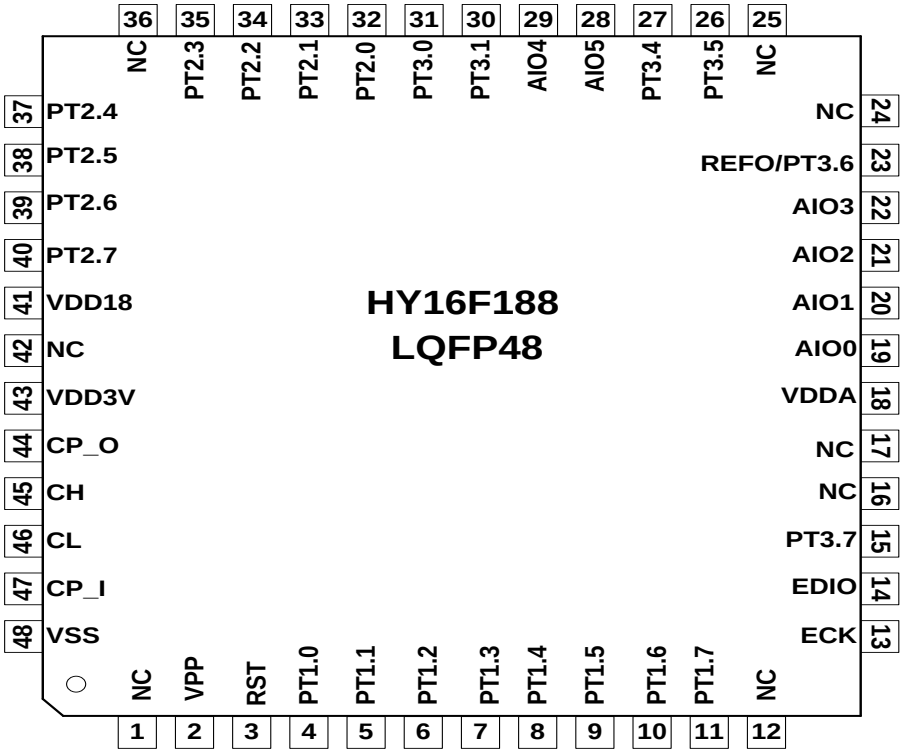


Figure 2-1 HY16F188 LQFP48 Pin Diagram

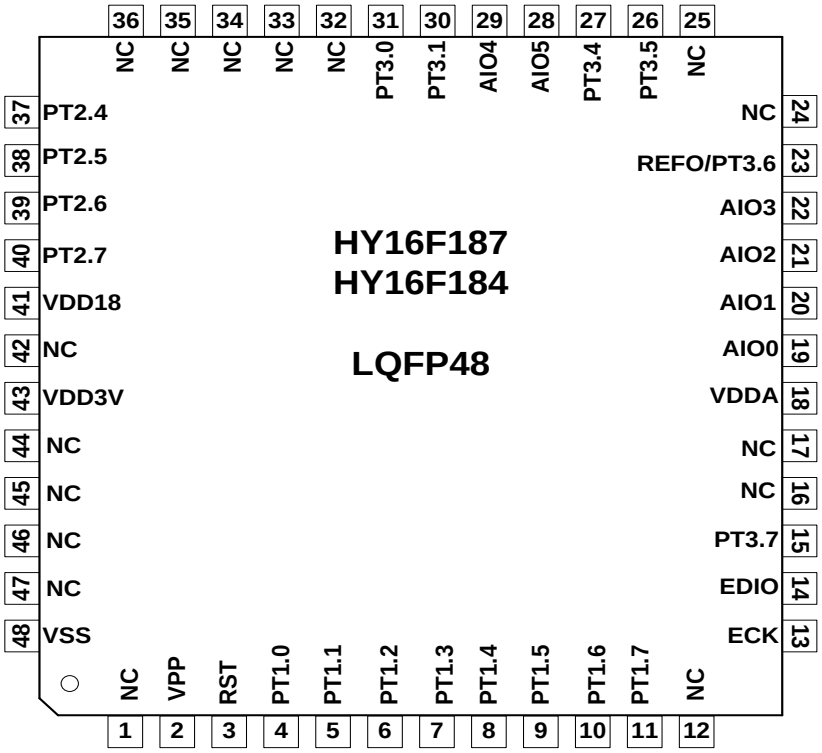


Figure 2-2 HY16F187/184 LQFP48 Pin Diagram

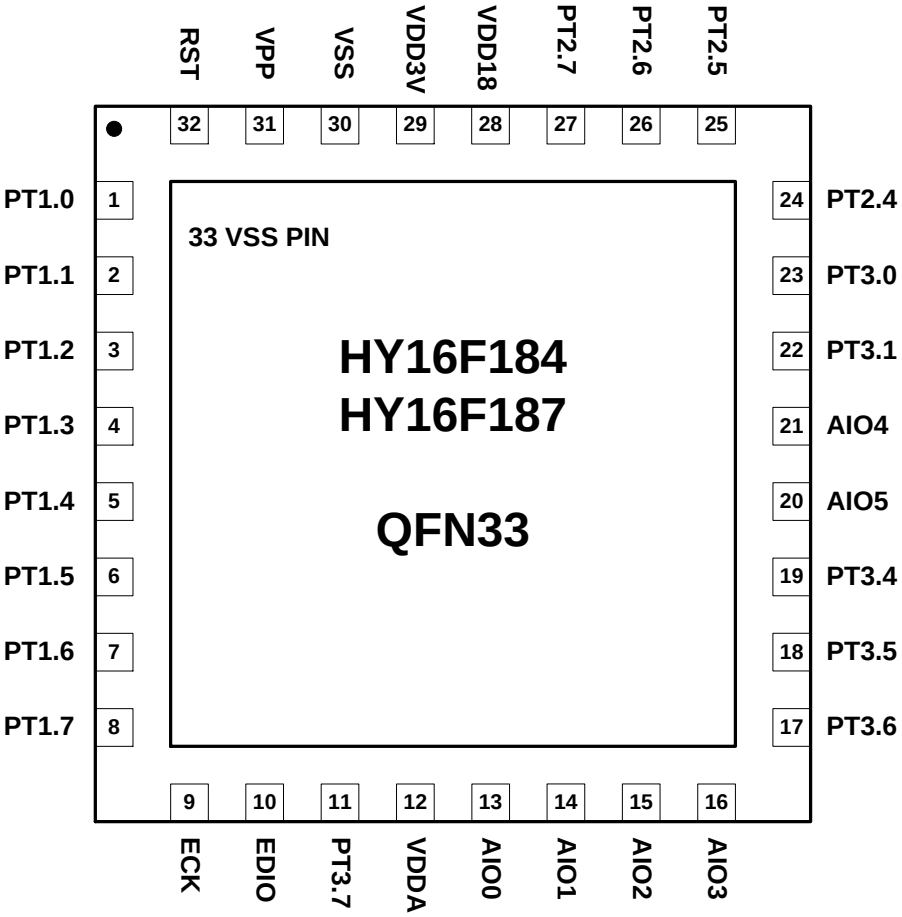


Figure 2-3 HY16F187/184 QFN33 Pin Diagram

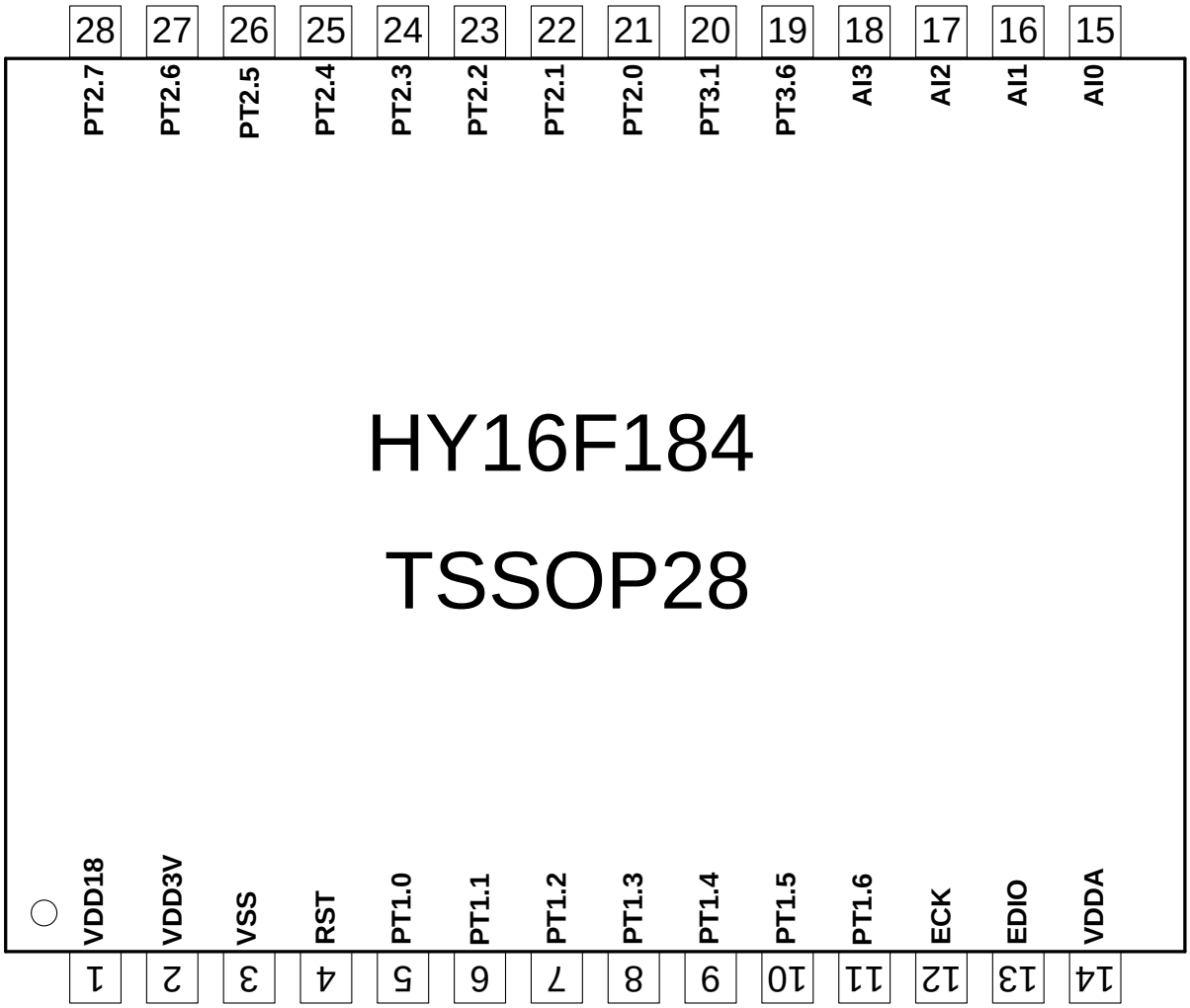


Figure 2-4 HY16F184 TSSOP 28 Pin Diagram

2.2. Pin Name List

2.2.1. HY16F188 LQFP48

PIN	TYPE(1)	NAME	DESCRIPTION
1	NC	NC	Not connect
2	PI	VPP	Reserve (keep floating status)
3	I	RST	Reset IC PIN
4	IO	PT1.0	Digital Input/ Output PIN
	AI	CH1	Comparator Analog Input PIN
	I	INT1.0	Interrupt Source INT1.0
	O	PWM0_1	PWM0_1 Output PIN
	I	CS_1	SPI Communication Interface PIN CS_1
	IO	TX_1	EUART Communication Interface PIN TX_1
	I	TCI1_1	Timer C Capture Module PIN TCI1_1
	IO	SCL_1	I2C Communication Interface PIN SCL_1
5	IO	PT1.1	Digital Input/ Output PIN
	AI	CH2	Comparator Analog Input PIN
	I	INT1.1	Interrupt Source INT1.1
	O	PWM1_1	PWM1_1 Output PIN
	I	CK_1	SPI Communication Interface PIN CK_1
	I	RX_1	EUART Communication Interface PIN RX_1
	I	TCI2_1	Timer C Capture Module PIN TCI2_1
	IO	SDA_1	I2C Communication Interface PIN SDA_1
6	IO	PT1.2	Digital Input/ Output PIN
	AI	CH3	Comparator Analog Input PIN
	I	INT1.2	Interrupt Source INT1.2
	O	PWM0_2	PWM0_2 Output PIN
	I	MISO_1	SPI Communication Interface PIN MISO_1
	IO	TX_2	EUART Communication Interface PIN TX_2
	I	TCI1_2	Timer C Capture Module PIN TCI1_2
	IO	SCL_2	I2C Communication Interface PIN SCL_2
7	IO	PT1.3	Digital Input/ Output PIN
	AI	CL1	Comparator Analog Input PIN
	I	INT1.3	Interrupt Source INT1.3
	O	PWM1_2	PWM1_2 Output PIN
	O	MOSI_1	SPI Communication Interface MOSI_1
	I	RX_2	EUART Communication Interface RX_2
	I	TCI2_2	Timer C Capture Module PIN TC12_2
	IO	SDA_2	I2C Communication Interface PIN SDA_2
8	IO	PT1.4	Digital Input/ Output PIN
	AI	CL2	Comparator Analog Input PIN
	I	INT1.4	Interrupt Source INT1.4
	O	PWM0_3	PWM0_3 Output PIN
	I	CS_2	SPI Communication Interface CS_2
	IO	TX_3	EUART Communication Interface TX_3
	I	TCI1_3	Timer C Capture Module PIN TCI1_3
	IO	SCL_3	I2C Communication Interface PIN SCL_3

PIN	TYPE(1)	NAME	DESCRIPTION
9	IO	PT1.5	Digital Input/ Output PIN
	AI	CL3	Comparator Analog Input PIN
	I	INT1.5	Interrupt Source INT1.5
	O	PWM1_3	PWM1_3 Output PIN
	I	CK_2	SPI Communication Interface PIN CK_2
	I	RX_3	EUART Communication Interface PIN RX_3
	I	TCI2_3	Timer C Capture Module PIN TCI2_3

PIN	TYPE(1)	NAME	DESCRIPTION
	IO	SDA_3	I2C Communication Interface PIN SDA_3
10	IO	PT1.6	Digital Input/output PIN
	AI	CL4	Comparator Analog Input PIN
	I	INT1.6	Interrupt Source INT1.6
	O	PWM0_4	PWM0_4 Output PIN
	I	MISO_2	SPI Communication Interface PIN MISO_2
	IO	TX_4	EUART Communication Interface PIN TX_4
	I	TCI1_4	Timer C Capture Module PIN TCI1_4
	IO	SCL_4	I2C Communication Interface PIN SCL_4
11	IO	PT1.7	Digital Input/ Output PIN
	AO	CMPO1	Comparator Analog Output PIN
	I	INT1.7	Interrupt Source INT1.7
	O	PWM1_4	PWM1_4 Output PIN
	O	MOSI_2	SPI Communication Interface PIN MOSI_2
	I	RX_4	EUART Communication Interface PIN RX_4
	I	TCI2_4	Timer C Capture Module PIN TCI2_4
	IO	SDA_4	I2C Communication Interface PIN SDA_4
12	NC	NC	Not Connect
13	I	ECK	Embedded Debug Module (EDM) Clock Input PIN
14	IO	EDIO	Embedded Debug Module (EDM) Data Input/ Output PIN
15	IO	PT3.7	Digital Input/ Output PIN
	AO	OPO1	RAIL-TO-RAIL OPAMP Output PIN
16	NC	NC	Not Connect
17	NC	NC	Not Connect
18	PIO	VDDA	Analog Power Supply, LDO Output, or Analog Power Input
19	AI	AIO0	Analog Input Signal Port 0
20	AI	AIO1	Analog Input Signal Port 1
21	AI	AIO2	Analog Input Signal Port 2
22	AI	AIO3	Analog Input Signal Port 3
23	IO	PT3.6	Digital Input/ Output PIN
	PIO	REFO	Analog Reference Voltage
24	NC	NC	Not Connect
25	NC	NC	Not Connect
26	IO	PT3.5	Digital Input/ Output PIN
	AI	AIO7	Analog Input Signal Port 7
27	IO	PT3.4	Digital Input/ Output PIN
	AI	AIO6	Analog Input Signal Port 6
28	AI	AIO5	Analog Input Signal Port 5

PIN	TYPE(1)	NAME	DESCRIPTION
29	AI	AIO4	Analog input signal port 4
30	IO	PT3.1	Digital Input/ Output PIN
	DO	OPOD2	RAIL-TO-RAIL OPAMP Output
	AO	DAO	8-bit Resistance Ladders Output pin
31	IO	PT3.0	Digital Input/ Output PIN
	DO	OPOD1	RAIL-TO-RAIL OPAMP Output
32	IO	PT2.0	Digital Input/ Output PIN
	I	INT2.0	Interrupt Source INT 2.0
	O	PWM0_5	PWM0_5 Output PIN
	I	CS_3	SPI Communication Interface PIN CS_3
	IO	TX_5	EUART Communication Interface PIN TX_5
	I	TCI1_5	Timer C Capture Module PIN TCI1_5
	IO	SCL_5	I2C Communication Interface PIN SCL_5

33	IO	PT2.1	Digital Input/ Output PIN
	I	INT2.1	Interrupt Source INT 2.1
	O	PWM1_5	PWM1_5 Output PIN
	I	CK_3	SPI Communication Interface PIN CK_3
	I	RX_5	EUART Communication Interface PIN RX_5
	I	TCI2_5	Timer C Capture Module PIN TCI2_5
	IO	SDA_5	I2C Communication Interface PIN SDA_5
34	IO	PT2.2	Digital Input/output PIN
	I	INT2.2	Interrupt Source INT 2.2
	O	PWM0_6	PWM0_6 Output PIN
	I	MISO_3	SPI Communication Interface PIN MISO_3
	IO	TX_6	EUART Communication Interface PIN TX_6
	I	TCI1_6	Timer C Capture Module PIN TCI1_6
	IO	SCL_6	I2C Communication Interface PIN SCL_6
35	IO	PT2.3	Digital Input/ Output PIN
	I	INT2.3	Interrupt Source INT 2.3
	O	PWM1_6	PWM1_6 Output PIN
	O	MOSI_3	SPI Communication Interface PIN MOSI_3
	I	RX_6	EUART Communication Interface PIN RX_6
	I	TCI2_6	Timer C Capture Module PIN TCI2_6
	IO	SDA_6	I2C Communication Interface PIN SDA_6
36	NC	NC	Not connect
37	IO	PT2.4	Digital Input/ Output PIN
	XI	LS_XIN	LS_XIN
	I	INT2.4	Interrupt Source INT 2.4
	O	PWM0_7	PWM0_7 Output PIN
	I	CS_4	SPI Communication Interface PIN CS_4
	IO	TX_7	EUART Communication Interface PIN TX_7
	I	TCI1_7	Timer C Capture Module PIN TCI1_7
	IO	SCL_7	I2C Communication Interface PIN SCL_7

PIN	TYPE(1)	NAME	DESCRIPTION
38	IO	PT2.5	Digital Input/ Output PIN
	XO	LS_XOUT	LS_XOUT
	I	INT2.5	Interrupt Source INT 2.5
	O	PWM1_7	PWM1_7 Output PIN
	I	CK_4	SPI Communication Interface PIN CK_4
	I	RX_7	EUART Communication Interface PIN RX_7
	I	TCI2_7	Timer C Capture Module PIN TCI2_7
	IO	SDA_7	I2C Communication Interface PIN SDA_7
39	IO	PT2.6	Digital Input/ Output PIN
	XI	HS_XIN	HS_XIN
	I	INT2.6	Interrupt Source INT 2.6
	O	PWM0_8	PWM0_8 Output PIN
	I	MISO_4	SPI Communication Interface PIN MISO_4
	IO	TX_8	EUART Communication Interface PIN TX_7
	I	TCI1_8	Timer C Capture Module PIN TCI1_8
	IO	SCL_8	I2C Communication Interface PIN SCL_8
40	IO	PT2.7	Digital Input/ Output PIN
	XO	HS_XOUT	HS_XOUT
	I	INT2.7	Interrupt Source INT 2.7
	O	PWM1_8	PWM1_8 Output PIN
	O	MOSI_4	SPI Communication Interface PIN MOSI_4
	I	RX_8	EUART Communication Interface PIN RX_8
	I	TCI2_8	Timer C Capture Module PIN TCI2_8
	IO	SDA_8	I2C Communication Interface PIN SDA_8
41	PO	VDD18	Digital Power Supply. LDO Output 1.8V, 1uF Cap to VSS

42	NC	NC	Not connect
43	PI	VDD3V	Power Input For System
44	PO	CP_O	Charge Pump 3V Out
45	PIO	CH	Charge Pump Capacitor High Voltage Plate
46	PIO	CL	Charge Pump Capacitor Low Voltage Plate
47	PI	CP_I	Charge Pump Power Input
48	P	VSS	Power Ground Pad

Table 2-1 HY16F188 LQFP48 Pin Definition and Function description

(1)TYPE Definition：

I = Digital Input

O = Digital Output

OD = Open-drain Output

AI = Analog Input

AO = Analog Output

P = Power Connection

2.2.2. HY16F187/184 LQFP48

PIN	TYPE(1)	NAME	DESCRIPTION
1	NC	NC	Not connect
2	PI	VPP	Reserve (keep floating status)
3	I	RST	Reset IC PIN
4	IO	PT1.0	Digital Input/ Output PIN
	AI	CH1	Comparator Analog Input PIN
	I	INT1.0	Interrupt Source INT1.0
	O	PWM0_1	PWM0_1 Output PIN
	I	CS_1	SPI Communication Interface PIN CS_1
	IO	TX_1	EUART Communication Interface PIN TX_1
	I	TCI1_1	Timer C Capture Module PIN TCI1_1
	IO	SCL_1	I2C Communication Interface PIN SCL_1
5	IO	PT1.1	Digital Input/ Output PIN
	AI	CH2	Comparator Analog Input PIN
	I	INT1.1	Interrupt Source INT1.1
	O	PWM1_1	PWM1_1 Output PIN
	I	CK_1	SPI Communication Interface PIN CK_1
	I	RX_1	EUART Communication Interface PIN RX_1
	I	TCI2_1	Timer C Capture Module PIN TCI2_1
	IO	SDA_1	I2C Communication Interface PIN SDA_1
6	IO	PT1.2	Digital Input/ Output PIN
	AI	CH3	Comparator Analog Input PIN
	I	INT1.2	Interrupt Source INT1.2
	O	PWM0_2	PWM0_2 Output PIN
	I	MISO_1	SPI Communication Interface PIN MISO_1
	IO	TX_2	EUART Communication Interface PIN TX_2
	I	TCI1_2	Timer C Capture Module PIN TCI1_2
	IO	SCL_2	I2C Communication Interface PIN SCL_2
7	IO	PT1.3	Digital Input/ Output PIN
	AI	CL1	Comparator Analog Input PIN
	I	INT1.3	Interrupt Source INT1.3
	O	PWM1_2	PWM1_2 Output PIN
	O	MOSI_1	SPI Communication Interface MOSI_1
	I	RX_2	EUART Communication Interface RX_2
	I	TCI2_2	Timer C Capture Module PIN TC12_2
	IO	SDA_2	I2C Communication Interface PIN SDA_2
8	IO	PT1.4	Digital Input/ Output PIN
	AI	CL2	Comparator Analog Input PIN
	I	INT1.4	Interrupt Source INT1.4
	O	PWM0_3	PWM0_3 Output PIN
	I	CS_2	SPI Communication Interface CS_2
	IO	TX_3	EUART Communication Interface TX_2
	I	TCI1_3	Timer C Capture Module PIN TCI1_3
	IO	SCL_3	I2C Communication Interface PIN SCL_3

PIN	TYPE(1)	NAME	DESCRIPTION
9	IO	PT1.5	Digital Input/ Output PIN
	AI	CL3	Comparator Analog Input PIN
	I	INT1.5	Interrupt Source INT1.5
	O	PWM1_3	PWM1_3 Output PIN
	I	CK_2	SPI Communication Interface PIN CK_2
	I	RX_3	EUART Communication Interface PIN RX_3
	I	TCI2_3	Timer C Capture Module PIN TCI2_3
	IO	SDA_3	I2C Communication Interface PIN SDA_3
10	IO	PT1.6	Digital Input/Output PIN
	AI	CL4	Comparator Analog Input PIN

PIN	TYPE(1)	NAME	DESCRIPTION
	I	INT1.6	Interrupt Source INT1.6
	O	PWM0_4	PWM0_4 Output PIN
	I	MISO_2	SPI Communication Interface PIN MISO_2
	IO	TX_4	EUART Communication Interface PIN TX_4
	I	TCI1_4	Timer C Capture Module PIN TCI1_4
	IO	SCL_4	I2C Communication Interface PIN SCL_4
11	IO	PT1.7	Digital Input/ Output PIN
	AO	CMPO1	Comparator Analog Output PIN
	I	INT1.7	Interrupt Source INT1.7
	O	PWM1_4	PWM1_4 Output PIN
	O	MOSI_2	SPI Communication Interface PIN MOSI_2
	I	RX_4	EUART Communication Interface PIN RX_4
	I	TCI2_4	Timer C Capture Module PIN TCI2_4
	IO	SDA_4	I2C Communication Interface PIN SDA_4
12	NC	NC	Not Connect
13	I	ECK	Embedded Debug Module (EDM) Clock Input PIN
14	IO	EDIO	Embedded Debug Module (EDM) Data Input/ Output PIN
15	IO	PT3.7	Digital Input/ Output PIN
	AO	OPOD1	RAIL-TO-RAIL OPAMP Output PIN
16	NC	NC	Not Connect
17	NC	NC	Not Connect
18	PIO	VDDA	Analog Power Supply, LDO Output, or Analog Power Input
19	AI	AIO0	Analog Input Signal Port 0
20	AI	AIO1	Analog Input Signal Port 1
21	AI	AIO2	Analog Input Signal Port 2
22	AI	AIO3	Analog Input Signal Port 3
23	IO	PT3.6	Digital Input/ Output PIN
	PIO	REFO	Analog Reference Voltage
24	NC	NC	Not Connect
25	NC	NC	Not Connect
26	IO	PT3.5	Digital Input/ Output PIN
	AI	AIO7	Analog Input Signal Port 7
27	IO	PT3.4	Digital Input/ Output PIN
	AI	AIO6	Analog Input Signal Port 6
28	AI	AIO5	Analog Input Signal Port 5

PIN	TYPE(1)	NAME	DESCRIPTION
29	AI	AIO4	Analog input signal port 4
30	IO	PT3.1	Digital Input/ Output PIN
	DO	OPOD2	RAIL-TO-RAIL OPAMP Output
	AO	DAO	8-bit Resistance Ladders Output
31	IO	PT3.0	Digital Input/ Output PIN
	DO	OPOD1	RAIL-TO-RAIL OPAMP Output
32	NC	NC	Not connect
33	NC	NC	Not connect
34	NC	NC	Not connect
35	NC	NC	Not connect
36	NC	NC	Not connect
37	IO	PT2.4	Digital Input/Output PIN
	XI	LS_XIN	LS_XIN
	I	INT2.4	Interrupt Source INT 2.4
	O	PWM0_7	PWM0_7 Output PIN
	I	CS_4	SPI Communication Interface PIN CS_4
	IO	TX_7	EUART Communication Interface PIN TX_7
	I	TCI1_7	Timer C Capture Module PIN TCI1_7
	IO	SCL_7	I2C Communication Interface PIN SCL_7

38	IO	PT2.5	Digital Input/ Output PIN
	XO	LS_XOUT	LS_XOUT
	I	INT2.5	Interrupt Source INT 2.5
	O	PWM1_7	PWM1_7 Output PIN
	I	CK_4	SPI Communication Interface PIN CK_4
	I	RX_7	EUART Communication Interface PIN RX_7
	I	TCI2_7	Timer C Capture Module PIN TCI2_7
	IO	SDA_7	I2C Communication Interface PIN SDA_7
39	IO	PT2.6	Digital Input/Output PIN
	XI	HS_XIN	HS_XIN
	I	INT2.6	Interrupt Source INT 2.6
	O	PWM0_8	PWM0_8 Output PIN
	I	MISO_4	SPI Communication Interface PIN MISO_4
	IO	TX_8	EUART Communication Interface PIN TX_7
	I	TCI1_8	Timer C Capture Module PIN TCI1_8
	IO	SCL_8	I2C Communication Interface PIN SCL_8
40	IO	PT2.7	Digital Input/ Output PIN
	XO	HS_XOUT	HS_XOUT
	I	INT2.7	Interrupt Source INT 2.7
	O	PWM1_8	PWM1_8 Output PIN
	O	MOSI_4	SPI Communication Interface PIN MOSI_4
	I	RX_8	EUART Communication Interface PIN RX_8
	I	TCI2_8	Timer C Capture Module PIN TCI2_8
	IO	SDA_8	I2C Communication Interface PIN SDA_8
41	PO	VDD18	Digital Power Supply. LDO Output 1.8V, 1uF Cap to VSS
42	NC	NC	Not connect
43	PI	VDD3V	Power Input For System
44	NC	NC	Not connect
45	NC	NC	Not connect
46	NC	NC	Not connect
47	NC	NC	Not connect
48	P	VSS	Power Ground Pad

Table 2-2 HY16F187/184 LQFP48 Pin Definition and Function description

2.2.3. HY16F187/184 QFN33

PIN	TYPE(1)	NAME	DESCRIPTION
1	IO	PT1.0	Digital Input/ Output PIN
	AI	CH1	Comparator Analog Input PIN
	I	INT1.0	Interrupt Source INT1.0
	O	PWM0_1	PWM0_1 Output PIN
	I	CS_1	SPI Communication Interface PIN CS_1
	IO	TX_1	EUART Communication Interface PIN TX_1
	I	TCI1_1	Timer C Capture Module PIN TCI1_1
	IO	SCL_1	I2C Communication Interface PIN SCL_1
2	IO	PT1.1	Digital Input/ Output PIN
	AI	CH2	Comparator Analog Input PIN
	I	INT1.1	Interrupt Source INT1.1
	O	PWM1_1	PWM1_1 Output PIN
	I	CK_1	SPI Communication Interface PIN CK_1
	I	RX_1	EUART Communication Interface PIN RX_1
	I	TCI2_1	Timer C Capture Module PIN TCI2_1
	IO	SDA_1	I2C Communication Interface PIN SDA_1
3	IO	PT1.2	Digital Input/ Output PIN
	AI	CH3	Comparator Analog Input PIN
	I	INT1.2	Interrupt Source INT1.2
	O	PWM0_2	PWM0_2 Output PIN
	I	MISO_1	SPI Communication Interface PIN MISO_1
	IO	TX_2	EUART Communication Interface PIN TX_2

PIN	TYPE(1)	NAME	DESCRIPTION
	I	TCI1_2	Timer C Capture Module PIN TCI1_2
	IO	SCL_2	I2C Communication Interface PIN SCL_2
4	IO	PT1.3	Digital Input/ Output PIN
	AI	CL1	Comparator Analog Input PIN
	I	INT1.3	Interrupt Source INT1.3
	O	PWM1_2	PWM1_2 Output PIN
	O	MOSI_1	SPI Communication Interface MOSI_1
	I	RX_2	EUART Communication Interface RX_2
	I	TCI2_2	Timer C Capture Module PIN TC12_2
	IO	SDA_2	I2C Communication Interface PIN SDA_2
5	IO	PT1.4	Digital Input/ Output PIN
	AI	CL2	Comparator Analog Input PIN
	I	INT1.4	Interrupt Source INT1.4
	O	PWM0_3	PWM0_3 Output PIN
	I	CS_2	SPI Communication Interface CS_2
	IO	TX_3	EUART Communication Interface TX_2
	I	TCI1_3	Timer C Capture Module PIN TCI1_3
	IO	SCL_3	I2C Communication Interface PIN SCL_3

PIN	TYPE(1)	NAME	DESCRIPTION
6	IO	PT1.5	Digital Input/ Output PIN
	AI	CL3	Comparator Analog Input PIN
	I	INT1.5	Interrupt Source INT1.5
	O	PWM1_3	PWM1_3 Output PIN
	I	CK_2	SPI Communication Interface PIN CK_2
	I	RX_3	EUART Communication Interface PIN RX_3
	I	TCI2_3	Timer C Capture Module PIN TCI2_3
	IO	SDA_3	I2C Communication Interface PIN SDA_3
7	IO	PT1.6	Digital Input/Output PIN
	AI	CL4	Comparator Analog Input PIN
	I	INT1.6	Interrupt Source INT1.6
	O	PWM0_4	PWM0_4 Output PIN
	I	MISO_2	SPI Communication Interface PIN MISO_2
	IO	TX_4	EUART Communication Interface PIN TX_4
	I	TCI1_4	Timer C Capture Module PIN TCI1_4
	IO	SCL_4	I2C Communication Interface PIN SCL_4
8	IO	PT1.7	Digital Input/ Output PIN
	AO	CMPO1	Comparator Analog Output PIN
	I	INT1.7	Interrupt Source INT1.7
	O	PWM1_4	PWM1_4 Output PIN
	O	MOSI_2	SPI Communication Interface PIN MOSI_2
	I	RX_4	EUART Communication Interface PIN RX_4
	I	TCI2_4	Timer C Capture Module PIN TCI2_4
	IO	SDA_4	I2C Communication Interface PIN SDA_4
9	I	ECK	Embedded Debug Module (EDM) Clock Input PIN
10	IO	EDIO	Embedded Debug Module (EDM) Data Input/ Output PIN
11	IO	PT3.7	Digital Input/ Output PIN
	AO	OPO	RAIL-TO-RAIL OPAMP Output PIN
12	PIO	VDDA	Analog Power Supply, LDO Output, or Analog Power Input
13	AI	AIO0	Analog Input Signal Port 0
14	AI	AIO1	Analog Input Signal Port 1
15	AI	AIO2	Analog Input Signal Port 2
16	AI	AIO3	Analog Input Signal Port 3
17	IO	PT3.6	Digital Input/ Output PIN
	PIO	REFO	Analog Reference Voltage
18	IO	PT3.5	Digital Input/ Output PIN
	AI	AIO7	Analog Input Signal Port 7

PIN	TYPE(1)	NAME	DESCRIPTION
19	IO	PT3.4	Digital Input/ Output PIN
	AI	AIO6	Analog Input Signal Port 6
20	AI	AIO5	Analog Input Signal Port 5

PIN	TYPE(1)	NAME	DESCRIPTION
21	AI	AIO4	Analog input signal port 4
22	IO	PT3.1	Digital Input/ Output PIN
	DO	OPOD2	RAIL-TO-RAIL OPAMP Output
	AO	DAO	8-bit Resistance Ladders Output
23	IO	PT3.0	Digital Input/ Output PIN
	DO	OPOD1	RAIL-TO-RAIL OPAMP Output
24	IO	PT2.4	Digital Input/Output PIN
	XI	LS_XIN	LS_XIN
	I	INT2.4	Interrupt Source INT 2.4
	O	PWM0_7	PWM0_7 Output PIN
	I	CS_4	SPI Communication Interface PIN CS_4
	IO	TX_7	EUART Communication Interface PIN TX_7
	I	TCI1_7	Timer C Capture Module PIN TCI1_7
	IO	SCL_7	I2C Communication Interface PIN SCL_7
25	IO	PT2.5	Digital Input/ Output PIN
	XO	LS_XOUT	LS_XOUT
	I	INT2.5	Interrupt Source INT 2.5
	O	PWM1_7	PWM1_7 Output PIN
	I	CK_4	SPI Communication Interface PIN CK_4
	I	RX_7	EUART Communication Interface PIN RX_7
	I	TCI2_7	Timer C Capture Module PIN TCI2_7
	IO	SDA_7	I2C Communication Interface PIN SDA_7
26	IO	PT2.6	Digital Input/Output PIN
	XI	HS_XIN	HS_XIN
	I	INT2.6	Interrupt Source INT 2.6
	O	PWM0_8	PWM0_8 Output PIN
	I	MISO_4	SPI Communication Interface PIN MISO_4
	IO	TX_8	EUART Communication Interface PIN TX_7
	I	TCI1_8	Timer C Capture Module PIN TCI1_8
	IO	SCL_8	I2C Communication Interface PIN SCL_8
27	IO	PT2.7	Digital Input/ Output PIN
	XO	HS_XOUT	HS_XOUT
	I	INT2.7	Interrupt Source INT 2.7
	O	PWM1_8	PWM1_8 Output PIN
	O	MOSI_4	SPI Communication Interface PIN MOSI_4
	I	RX_8	EUART Communication Interface PIN RX_8
	I	TCI2_8	Timer C Capture Module PIN TCI2_8
	IO	SDA_8	I2C Communication Interface PIN SDA_8
28	PO	VDD18	Digital Power Supply. LDO Output 1.8V, 1uF Cap to VSS
29	PI	VDD3V	Power Input For System
30	P	VSS	Power Ground Pad
31	PI	VPP	Reserve (can't connect to any pin)
32	I	RST	Reset IC PIN
33	P	VSS	Power Ground Pad

Table 2-3 HY16F187/184 QFN33 Pin Definition and Function description

2.2.4. HY16F184 TSSOP28

PIN	TYPE(1)	NAME	DESCRIPTION
1	PO	VDD18	Digital Power Supply. LDO Output 1.8V, 1uF Cap to VSS

PIN	TYPE(1)	NAME	DESCRIPTION
2	PI	VDD3V	Power Input For System
3	P	VSS	Power Ground Pad
4	I	RST	Reset IC PIN
5	IO	PT1.0	Digital Input/ Output PIN
	AI	CH1	Comparator Analog Input PIN
	I	INT1.0	Interrupt Source INT1.0
	O	PWM0_1	PWM0_1 Output PIN
	I	CS_1	SPI Communication Interface PIN CS_1
	IO	TX_1	EUART Communication Interface PIN TX_1
	I	TCI1_1	Timer C Capture Module PIN TCI1_1
	IO	SCL_1	I2C Communication Interface PIN SCL_1
6	IO	PT1.1	Digital Input/ Output PIN
	AI	CH2	Comparator Analog Input PIN
	I	INT1.1	Interrupt Source INT1.1
	O	PWM1_1	PWM1_1 Output PIN
	I	CK_1	SPI Communication Interface PIN CK_1
	I	RX_1	EUART Communication Interface PIN RX_1
	I	TCI2_1	Timer C Capture Module PIN TCI2_1
	IO	SDA_1	I2C Communication Interface PIN SDA_1
7	IO	PT1.2	Digital Input/ Output PIN
	AI	CH3	Comparator Analog Input PIN
	I	INT1.2	Interrupt Source INT1.2
	O	PWM0_2	PWM0_2 Output PIN
	I	MISO_1	SPI Communication Interface PIN MISO_1
	IO	TX_2	EUART Communication Interface PIN TX_2
	I	TCI1_2	Timer C Capture Module PIN TCI1_2
	IO	SCL_2	I2C Communication Interface PIN SCL_2
8	IO	PT1.3	Digital Input/ Output PIN
	AI	CL1	Comparator Analog Input PIN
	I	INT1.3	Interrupt Source INT1.3
	O	PWM1_2	PWM1_2 Output PIN
	O	MOSI_1	SPI Communication Interface MOSI_1
	I	RX_2	EUART Communication Interface RX_2
	I	TCI2_2	Timer C Capture Module PIN TC12_2
	IO	SDA_2	I2C Communication Interface PIN SDA_2
9	IO	PT1.4	Digital Input/ Output PIN
	AI	CL2	Comparator Analog Input PIN
	I	INT1.4	Interrupt Source INT1.4
	O	PWM0_3	PWM0_3 Output PIN
	I	CS_2	SPI Communication Interface CS_2
	IO	TX_3	EUART Communication Interface TX_3
	I	TCI1_3	Timer C Capture Module PIN TCI1_3
	IO	SCL_3	I2C Communication Interface PIN SCL_3

PIN	TYPE(1)	NAME	DESCRIPTION
10	IO	PT1.5	Digital Input/ Output PIN
	AI	CL3	Comparator Analog Input PIN
	I	INT1.5	Interrupt Source INT1.5
	O	PWM1_3	PWM1_3 Output PIN
	I	CK_2	SPI Communication Interface PIN CK_2
	I	RX_3	EUART Communication Interface PIN RX_3
	I	TCI2_3	Timer C Capture Module PIN TCI2_3
	IO	SDA_3	I2C Communication Interface PIN SDA_3
11	IO	PT1.6	Digital Input/output PIN

PIN	TYPE(1)	NAME	DESCRIPTION
	AI	CL4	Comparator Analog Input PIN
	I	INT1.6	Interrupt Source INT1.6
	O	PWM0_4	PWM0_4 Output PIN
	I	MISO_2	SPI Communication Interface PIN MISO_2
	IO	TX_4	EUART Communication Interface PIN TX_4
	I	TCI1_4	Timer C Capture Module PIN TCI1_4
	IO	SCL_4	I2C Communication Interface PIN SCL_4
12	I	ECK	Embedded Debug Module (EDM) Clock Input PIN
13	IO	EDIO	Embedded Debug Module (EDM) Data Input/ Output PIN
14	PIO	VDDA	Analog Power Supply, LDO Output, or Analog Power Input
15	AI	AIO0	Analog Input Signal Port 0
16	AI	AIO1	Analog Input Signal Port 1
17	AI	AIO2	Analog Input Signal Port 2
18	AI	AIO3	Analog Input Signal Port 3
19	IO	PT3.6	Digital Input/ Output PIN
	PIO	REFO	Analog Reference Voltage
20	IO	PT3.1	Digital Input/ Output PIN
	DO	OPOD2	RAIL-TO-RAIL OPAMP Output
	AO	DAO	8-bit Resistance Ladders Output pin
21	IO	PT2.0	Digital Input/ Output PIN
	I	INT2.0	Interrupt Source INT 2.0
	O	PWM0_5	PWM0_5 Output PIN
	I	CS_3	SPI Communication Interface PIN CS_3
	IO	TX_5	EUART Communication Interface PIN TX_5
	I	TCI1_5	Timer C Capture Module PIN TCI1_5
	IO	SCL_5	I2C Communication Interface PIN SCL_5
22	IO	PT2.1	Digital Input/ Output PIN
	I	INT2.1	Interrupt Source INT 2.1
	O	PWM1_5	PWM1_5 Output PIN
	I	CK_3	SPI Communication Interface PIN CK_3
	I	RX_5	EUART Communication Interface PIN RX_5
	I	TCI2_5	Timer C Capture Module PIN TCI2_5
	IO	SDA_5	I2C Communication Interface PIN SDA_5
23	IO	PT2.2	Digital Input/ Output PIN
	I	INT2.2	Interrupt Source INT 2.2
	O	PWM0_6	PWM0_6 Output PIN
	I	MISO_3	SPI Communication Interface PIN MISO_3
	IO	TX_6	EUART Communication Interface PIN TX_6
	I	TCI1_6	Timer C Capture Module PIN TCI1_6
	IO	SCL_6	I2C Communication Interface PIN SCL_6
24	IO	PT2.3	Digital Input/ Output PIN
	I	INT2.3	Interrupt Source INT 2.3
	O	PWM1_6	PWM1_6 Output PIN
	O	MOSI_3	SPI Communication Interface PIN MOSI_3
	I	RX_6	EUART Communication Interface PIN RX_6
	I	TCI2_6	Timer C Capture Module PIN TCI2_6
	IO	SDA_6	I2C Communication Interface PIN SDA_6
25	IO	PT2.4	Digital Input/ Output PIN
	XI	LS_XIN	LS_XIN
	I	INT2.4	Interrupt Source INT 2.4
	O	PWM0_7	PWM0_7 Output PIN
	I	CS_4	SPI Communication Interface PIN CS_4
	IO	TX_7	EUART Communication Interface PIN TX_7
	I	TCI1_7	Timer C Capture Module PIN TCI1_7
	IO	SCL_7	I2C Communication Interface PIN SCL_7
26	IO	PT2.5	Digital Input/ Output PIN

PIN	TYPE(1)	NAME	DESCRIPTION
	XO	LS_XOUT	LS_XOUT
	I	INT2.5	Interrupt Source INT 2.5
	O	PWM1_7	PWM1_7 Output PIN
	I	CK_4	SPI Communication Interface PIN CK_4
	I	RX_7	EUART Communication Interface PIN RX_7
	I	TCI2_7	Timer C Capture Module PIN TCI2_7
	IO	SDA_7	I2C Communication Interface PIN SDA_7
27	IO	PT2.6	Digital Input/ Output PIN
	XI	HS_XIN	HS_XIN
	I	INT2.6	Interrupt Source INT 2.6
	O	PWM0_8	PWM0_8 Output PIN
	I	MISO_4	SPI Communication Interface PIN MISO_4
	IO	TX_8	EUART Communication Interface PIN TX_7
	I	TCI1_8	Timer C Capture Module PIN TCI1_8
	IO	SCL_8	I2C Communication Interface PIN SCL_8
28	IO	PT2.7	Digital Input/ Output PIN
	XO	HS_XOUT	HS_XOUT
	I	INT2.7	Interrupt Source INT 2.7
	O	PWM1_8	PWM1_8 Output PIN
	O	MOSI_4	SPI Communication Interface PIN MOSI_4
	I	RX_8	EUART Communication Interface PIN RX_8
	I	TCI2_8	Timer C Capture Module PIN TCI2_8
	IO	SDA_8	I2C Communication Interface PIN SDA_8

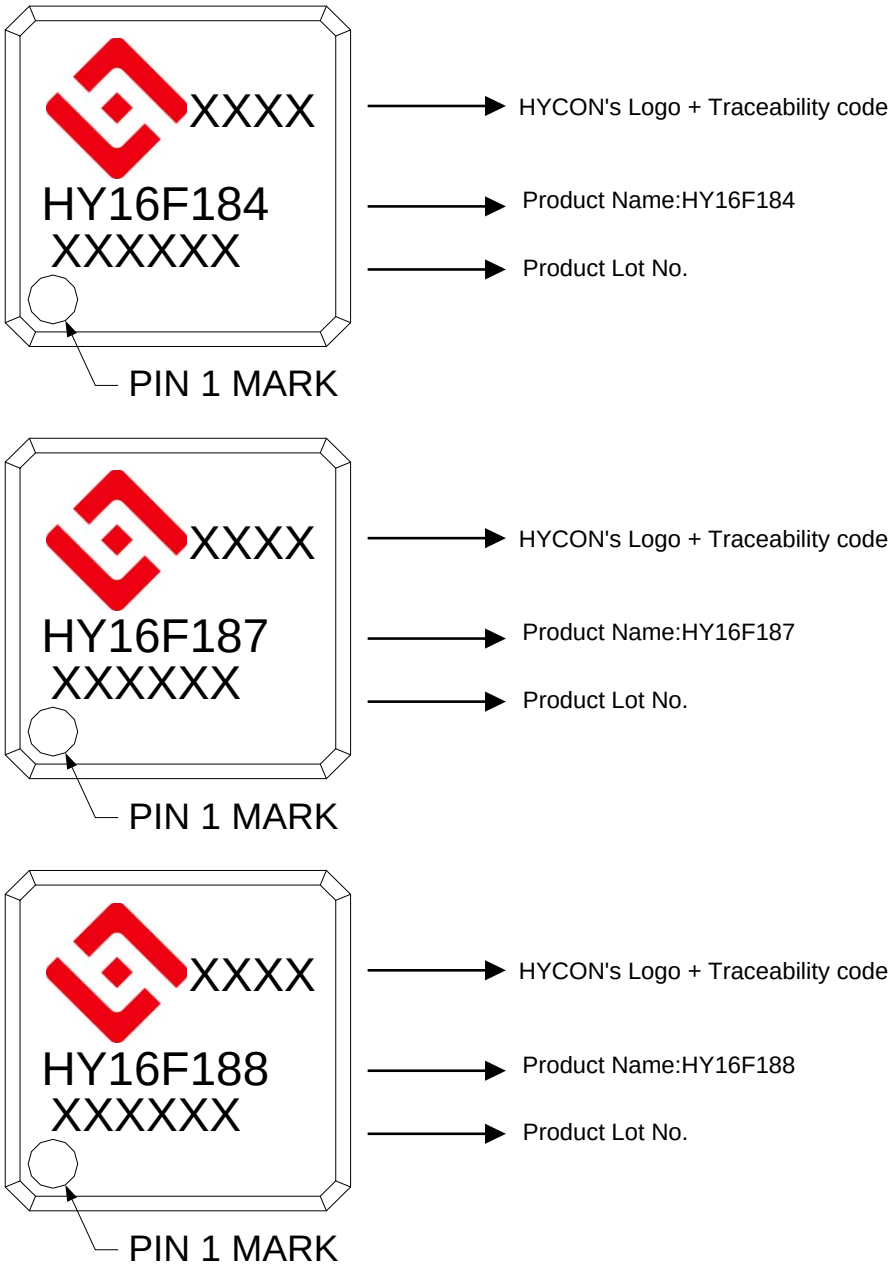
Table 2-4 HY16F184 TSSOP28 Pin Definition and Function description

2.2.5. Function Priority:

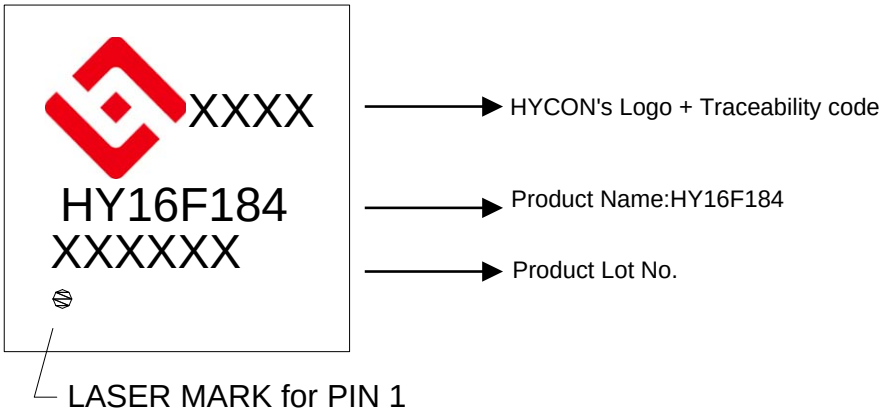
GPIO Port	OSC	Interrupt	Timer C Capture	SPI	IIC	UART	CMP	Analog	Timer B PWM
Priority	0	0	0	1	2	3	4	5	6
PT1.0		INT1.0	TCI1_1	CS_1	SCL_1	TX_1	CH1		PWM0_1
PT1.1		INT1.1	TCI2_1	CK_1	SDA_1	RX_1	CH2		PWM1_1
PT1.2		INT1.2	TCI1_2	MISO_1	SCL_2	TX_2	CH3		PWM0_2
PT1.3		INT1.3	TCI2_2	MOSI_1	SDA_2	RX_2	CL1		PWM1_2
PT1.4		INT1.4	TCI1_3	CS_2	SCL_3	TX_3	CL2		PWM0_3
PT1.5		INT1.5	TCI2_3	CK_2	SDA_3	RX_3	CL3		PWM1_3
PT1.6		INT1.6	TCI1_4	MISO_2	SCL_4	TX_4	CL4		PWM0_4
PT1.7		INT1.7	TCI2_4	MOSI_2	SDA_4	RX_4	CMPO1		PWM1_4
PT2.0		INT2.0	TCI1_5	CS_3	SCL_5	TX_5			PWM0_5
PT2.1		INT2.1	TCI2_5	CK_3	SDA_5	RX_5			PWM1_5
PT2.2		INT2.2	TCI1_6	MISO_3	SCL_6	TX_6			PWM0_6
PT2.3		INT2.3	TCI2_6	MOSI_3	SDA_6	RX_6			PWM1_6
PT2.4	LSXT1	INT2.4	TCI1_7	CS_4	SCL_7	TX_7			PWM0_7
PT2.5	LSXT2	INT2.5	TCI2_7	CK_4	SDA_7	RX_7			PWM1_7
PT2.6	HSXT1	INT2.6	TCI1_8	MISO_4	SCL_8	TX_8			PWM0_8
PT2.7	HSXT2	INT2.7	TCI2_8	MOSI_4	SDA_8	RX_8			PWM1_8
PT3.0							OPOD1		
PT3.1							OPOD2	DAO	
AIO4								AIO4	
AIO5								AIO5	
PT3.4								AIO6	
PT3.5								AIO7	
PT3.6								REFO	
PT3.7								OPO	
AIO0								AIO0	
AIO1								AIO1	
AIO2								AIO2	
AIO3								AIO3	

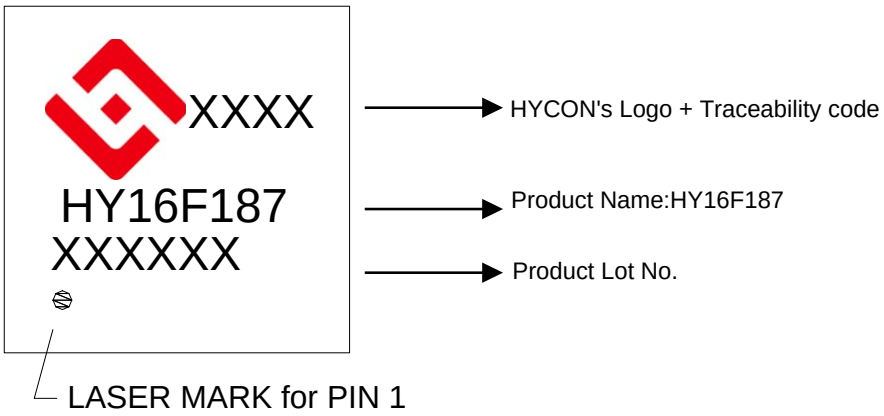
2.3. Package marking information

2.3.1. HY16F184/187/188 LQFP Package marking information

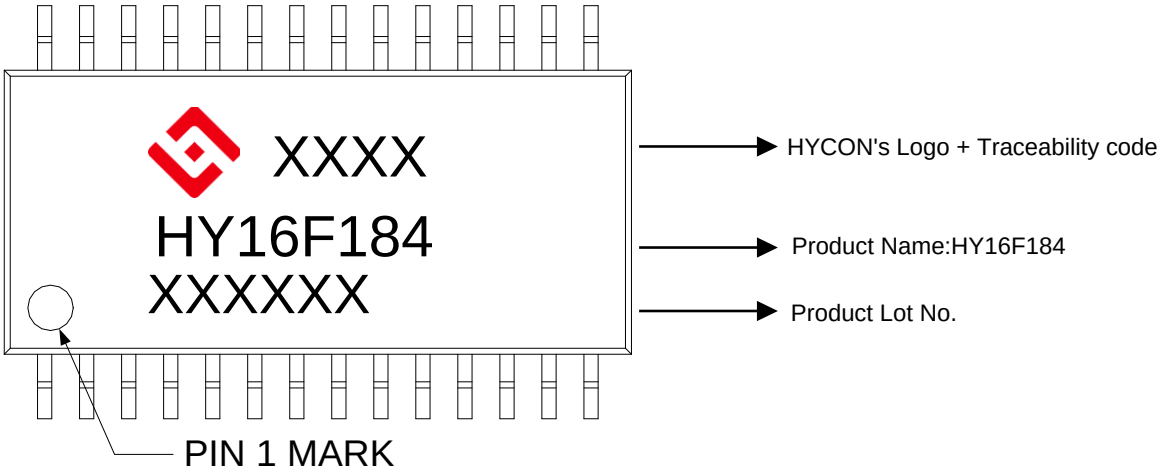


2.3.2. HY16F184 /187QFN Package marking information





2.3.3. HY16F184 TSSOP Package marking information



3. Application Circuit

3.1. Bridge Sensor

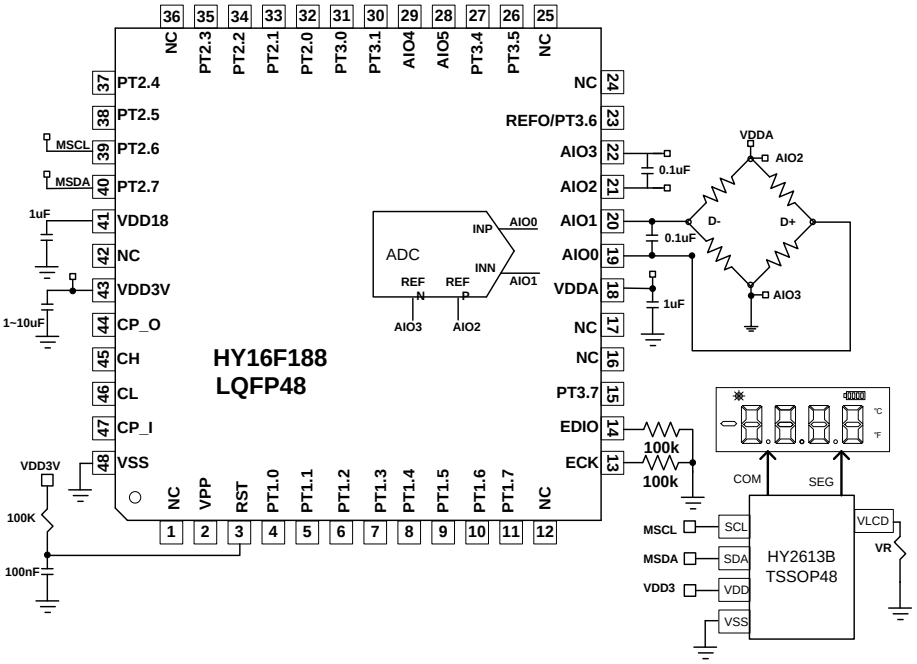


Figure 3-1 Bridge Sensor Circuit

3.2. Blood Pressure Sensor

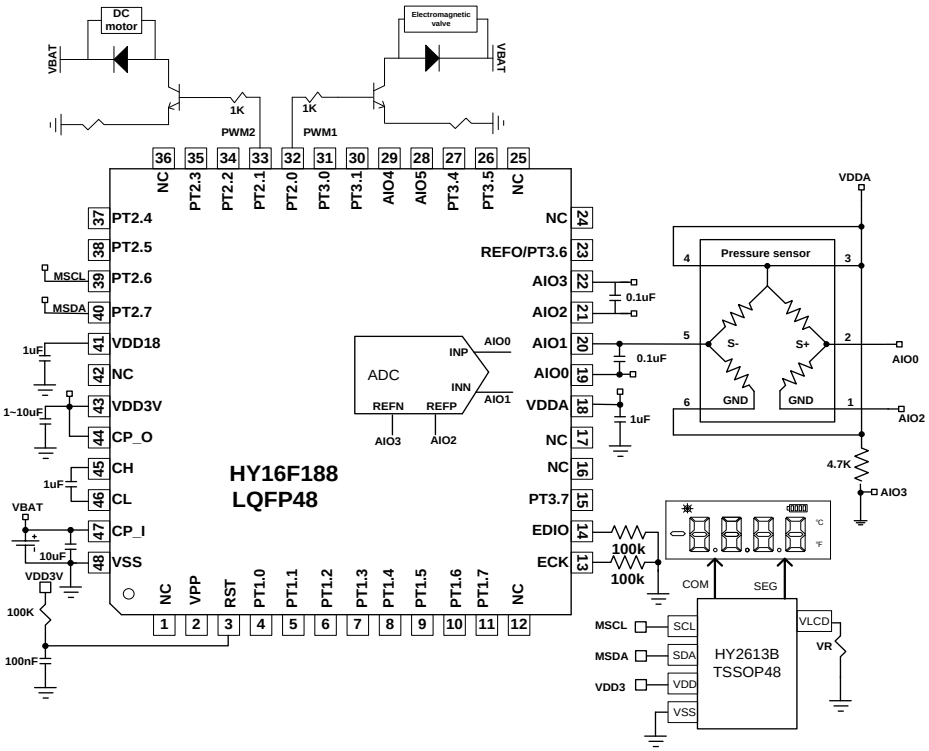


Figure 3-2 Blood Pressure Sensor Circuit

3.3. Electrochemical Sensor

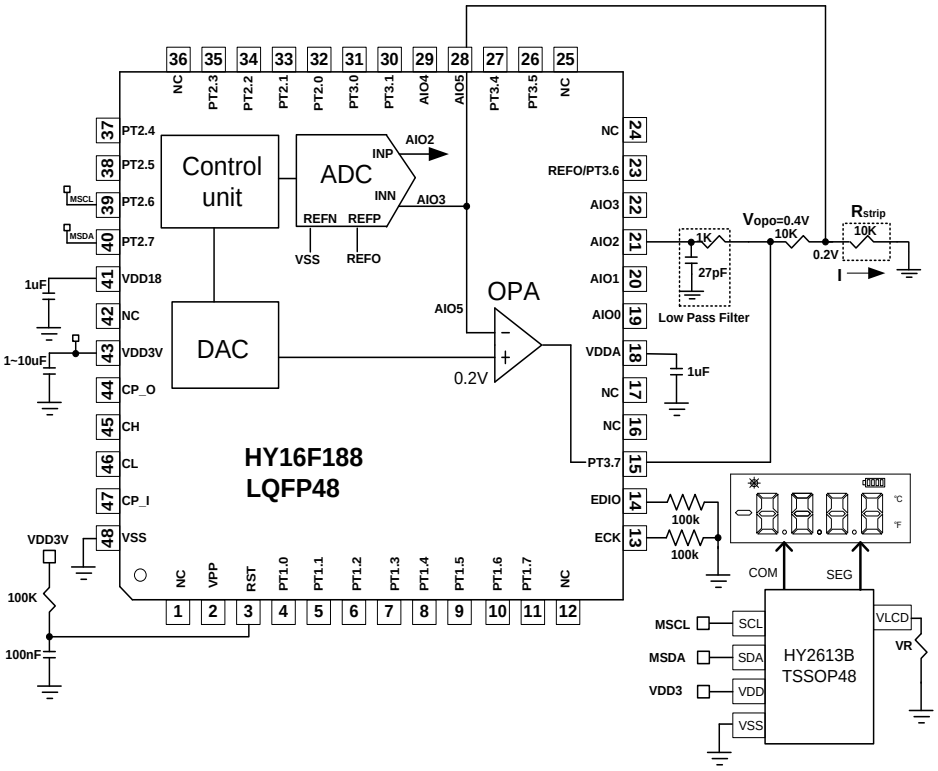


Figure 3-3 Electrochemical Sensor Circuit

3.4. Touch Key Sensor

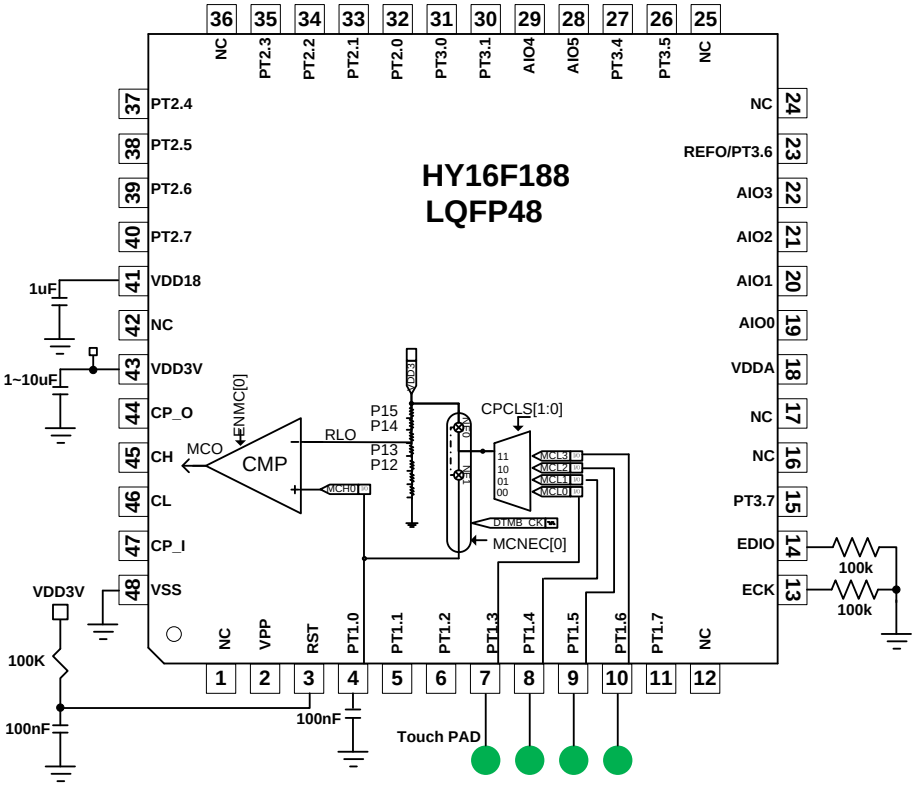


Figure 3-4 Touch Key Sensor Circuit

4. Function Outline

4.1. Internal Block Diagram

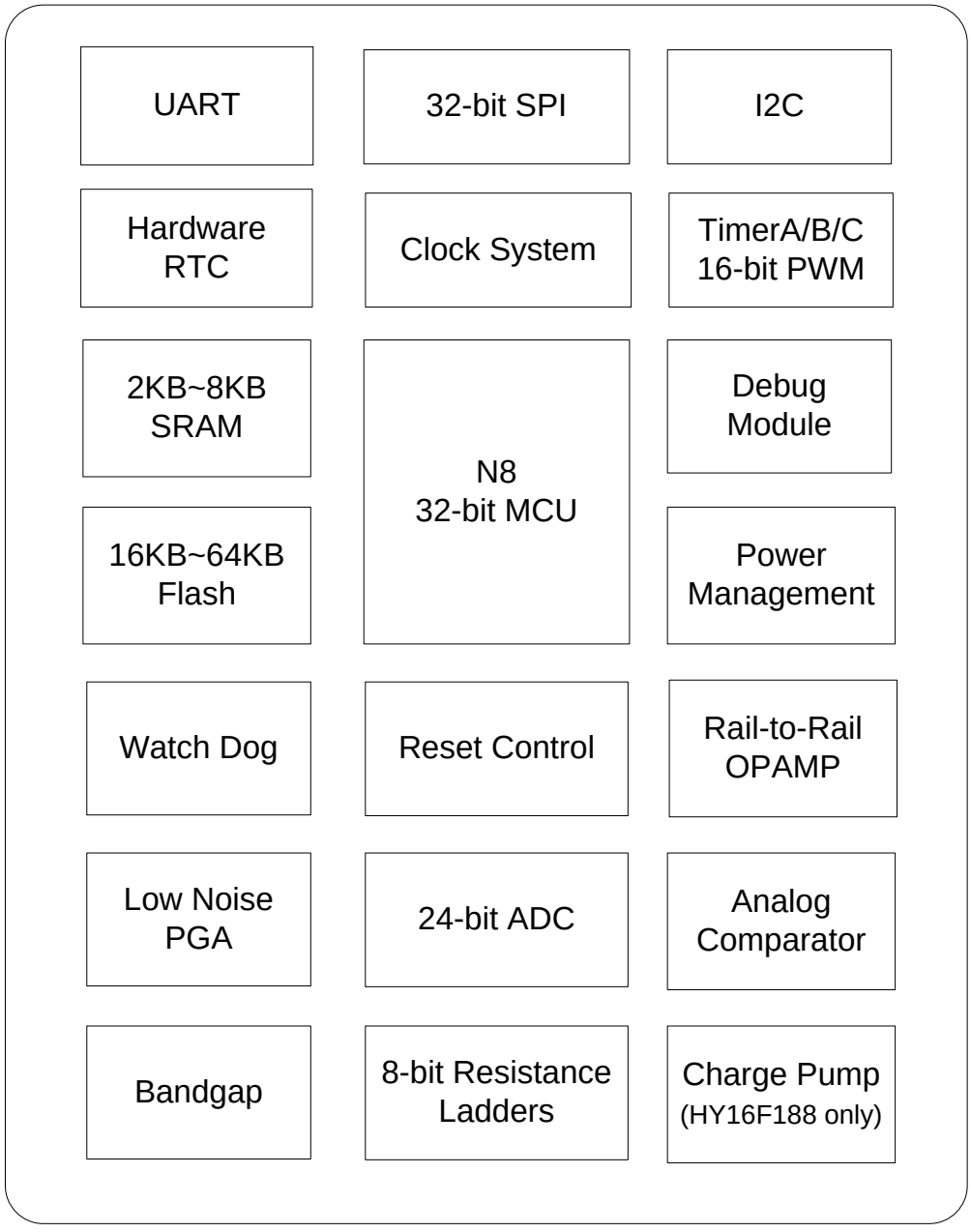


Figure 4-1 Internal Block Diagram

4.2. Building Block Diagram

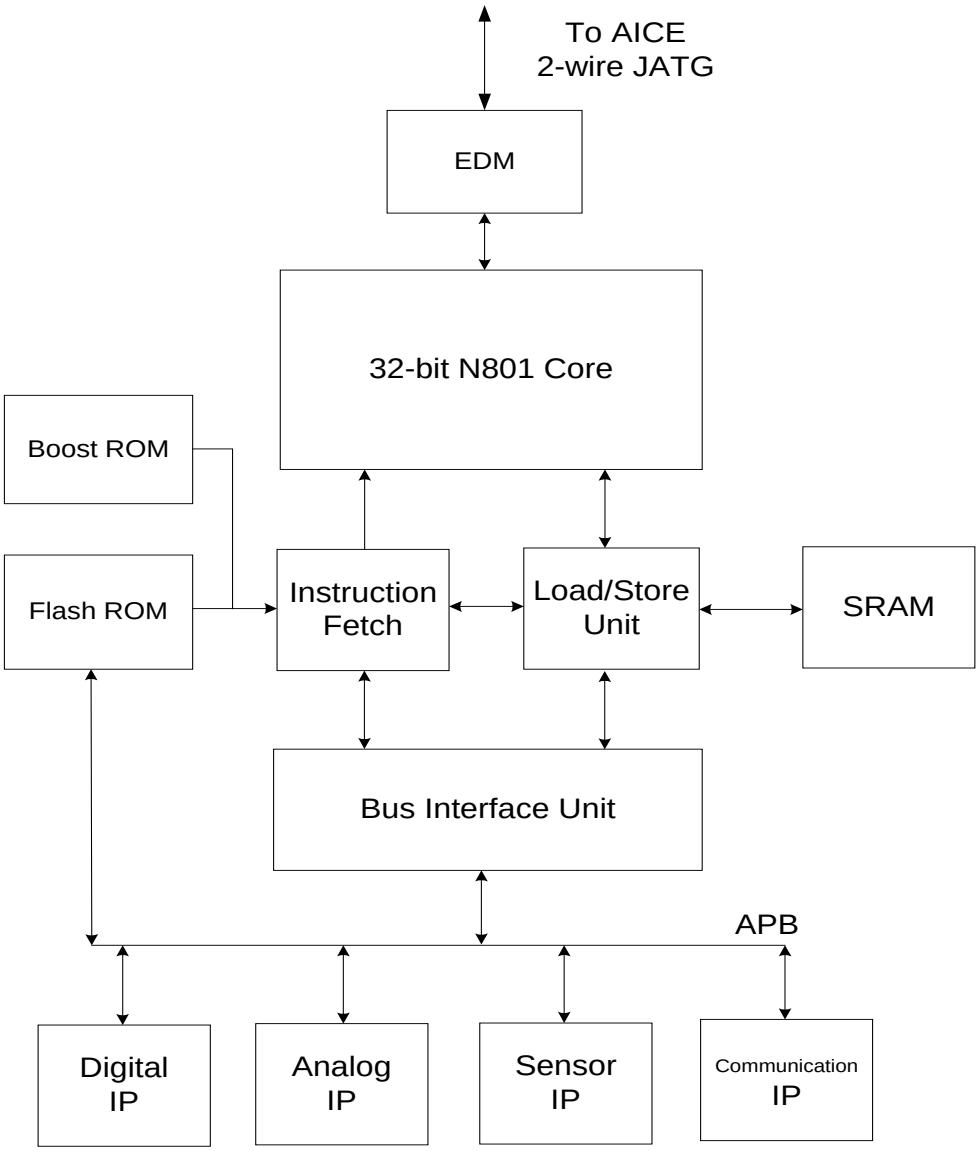
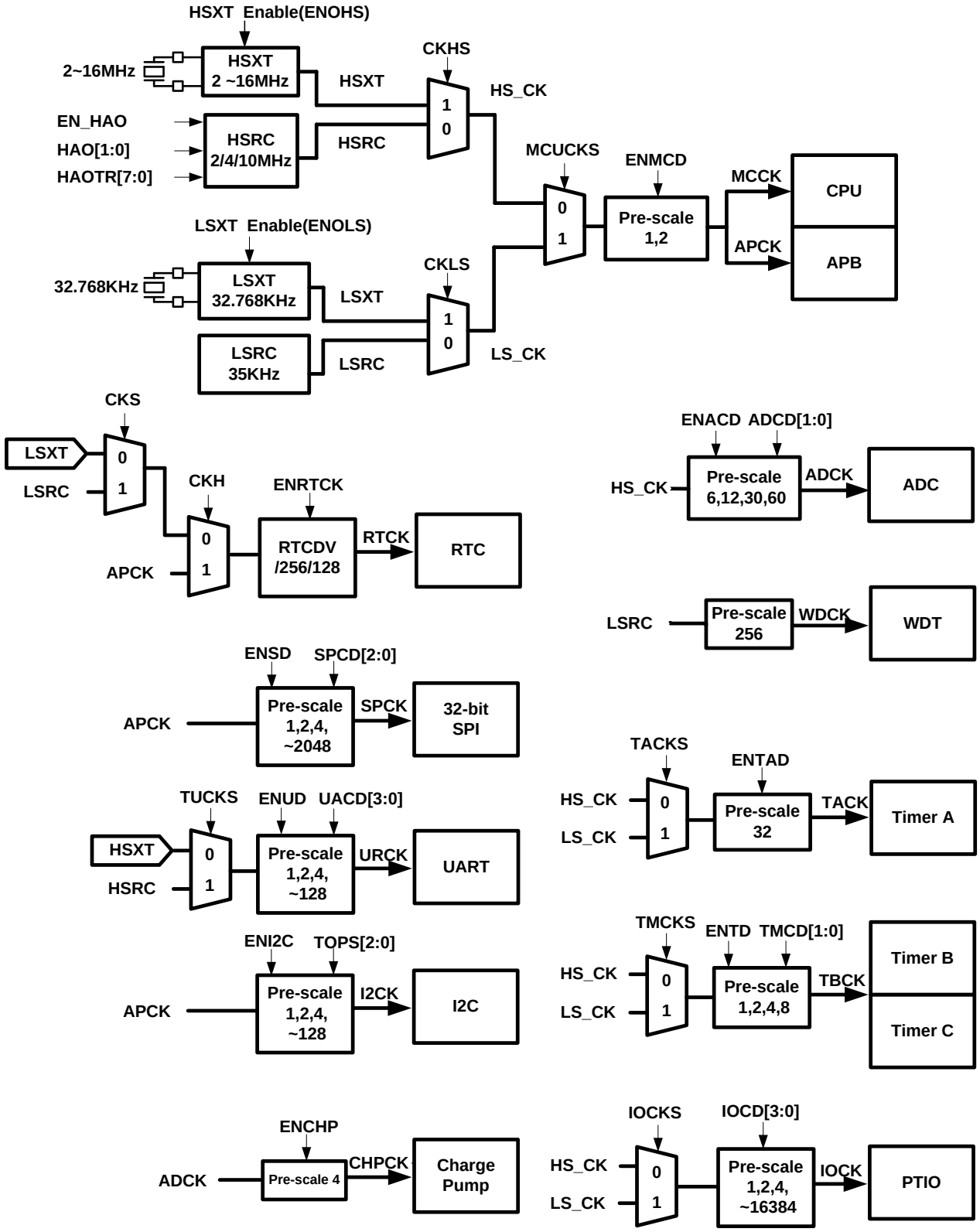


Figure 4-2 Build Block Diagram

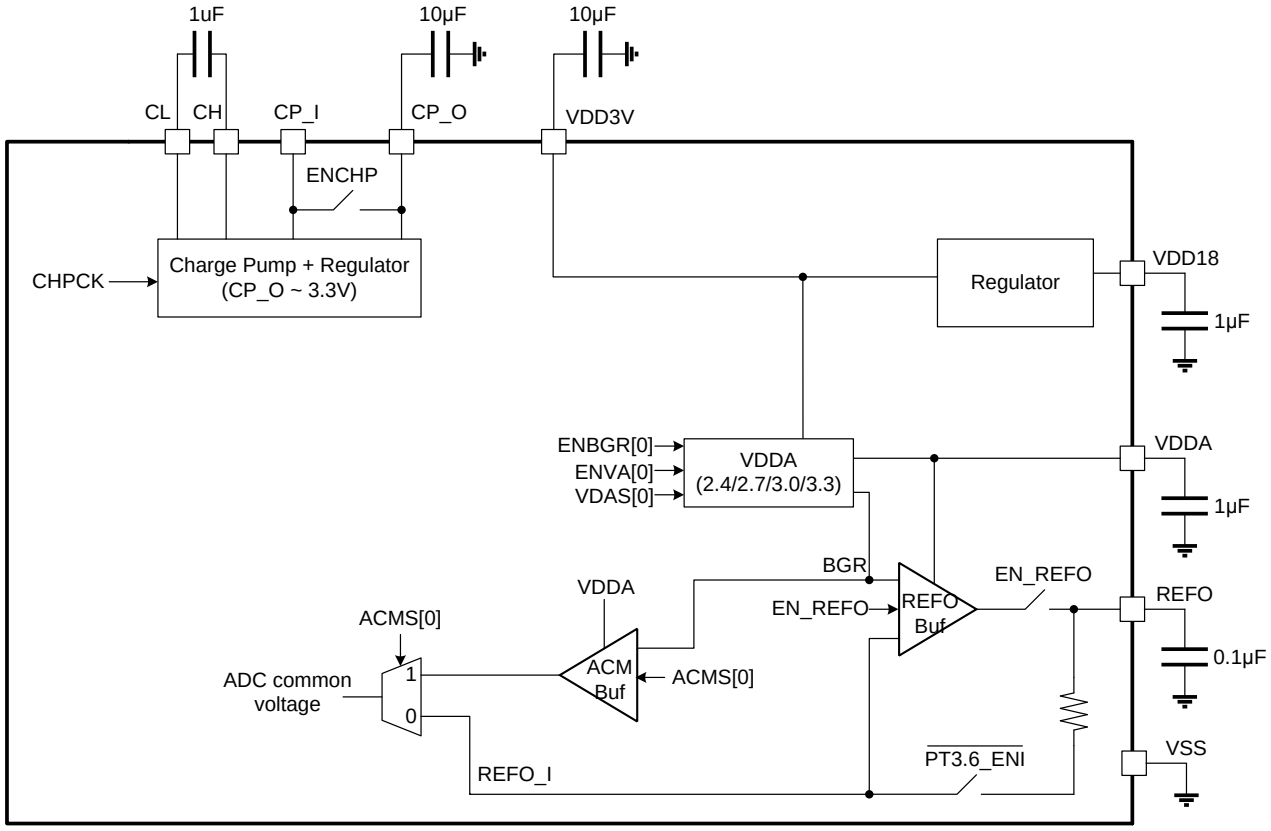
4.3. Supporting Document

NO	File Name	Description
1	UG-HY16F188	HY16F188 User's Manual
2	APD-HY16IDE001	HY16F18 Series IDE Software Manual
3	APD-HY16IDE002	HY16F18 Series IDE Hardware Manual
4	APD-HY16IDE004	HY16F18 C Peripheral Driver Library
5	APD-HY16IDE006	HY16F Series Writer Kit Manual
6	APD-HY16F003	HY16F18 IP User Manual

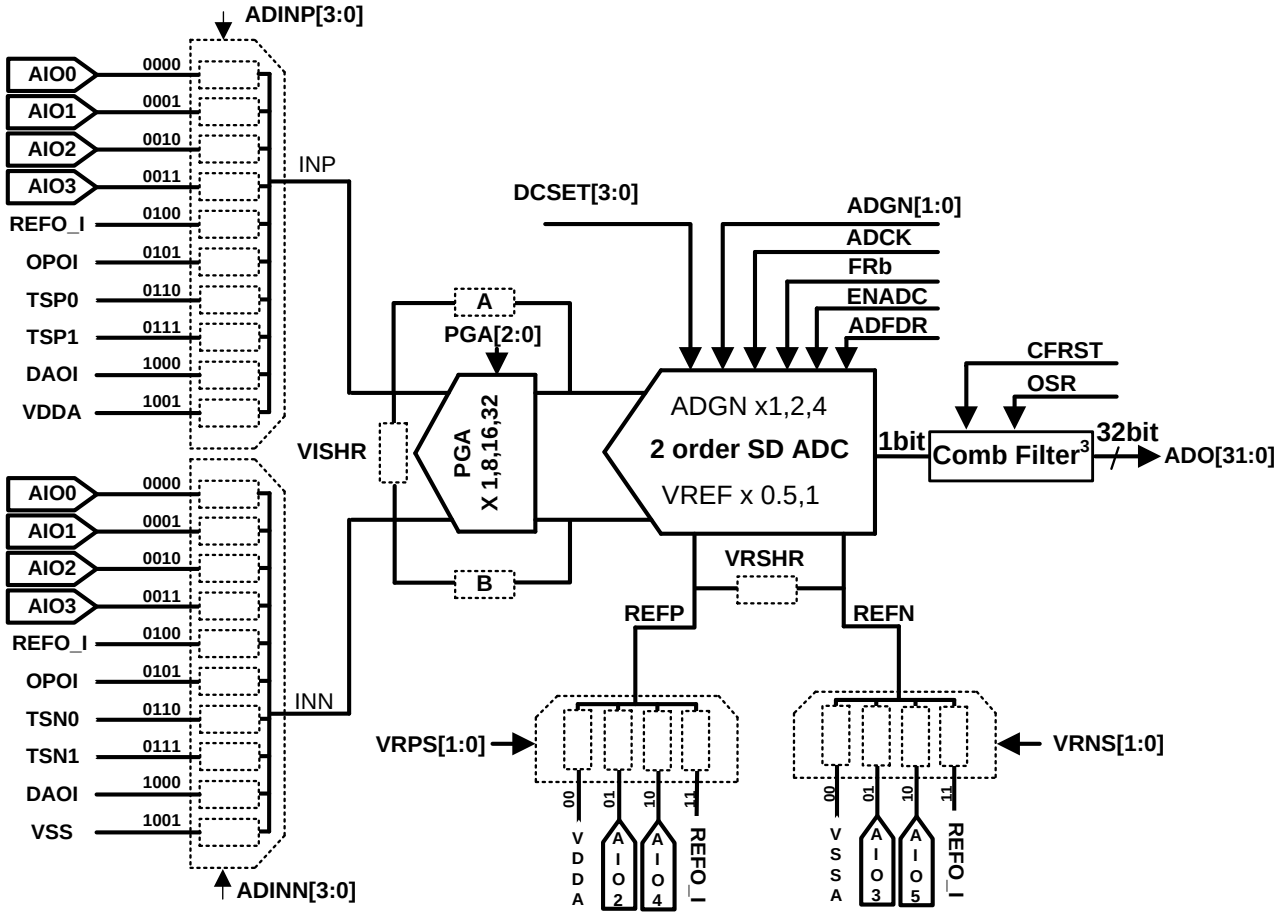
4.4. Clock System Network



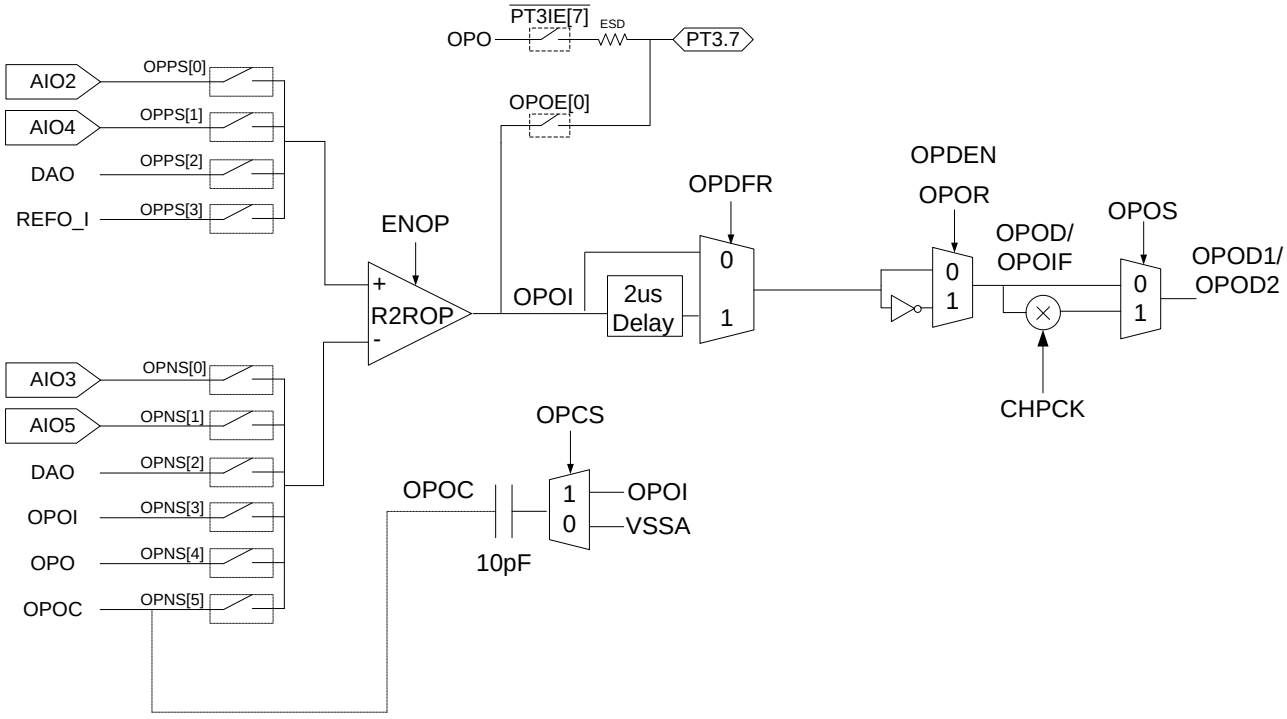
4.5. Power System Network



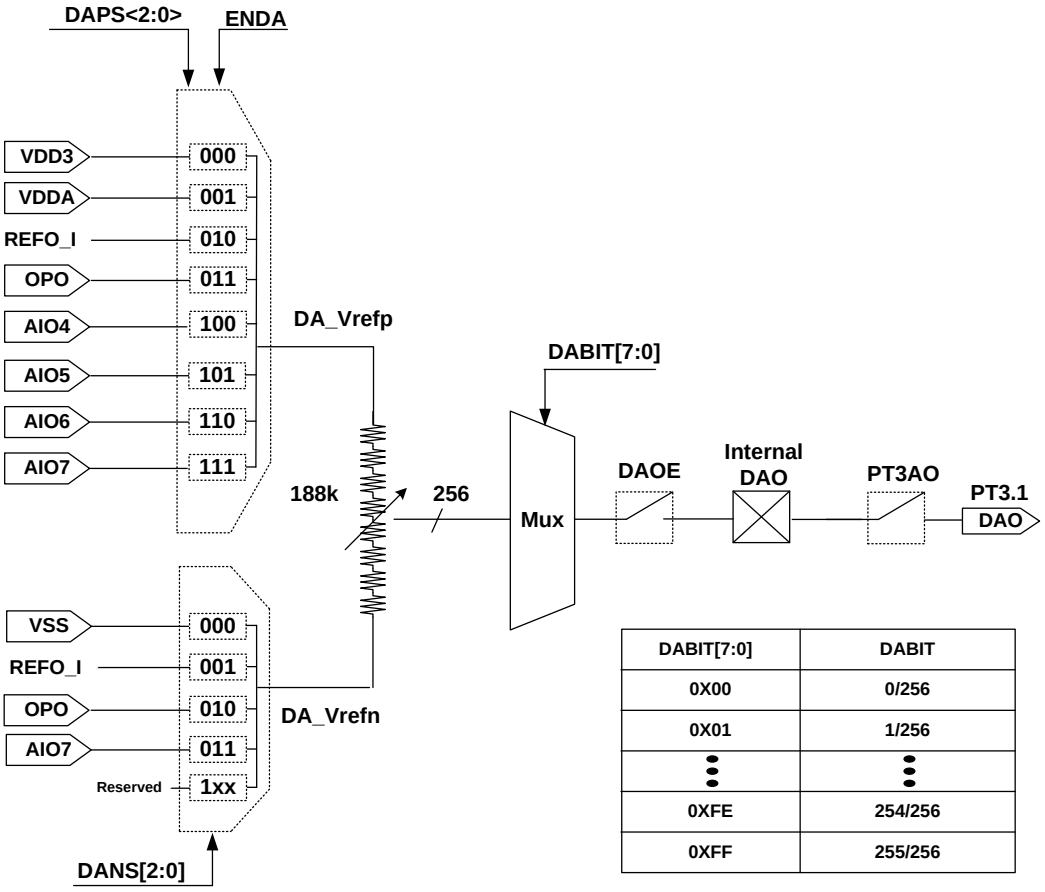
4.6. 24-bit Σ △ ADC Network



4.7. Rail to Rail OPAMP Network



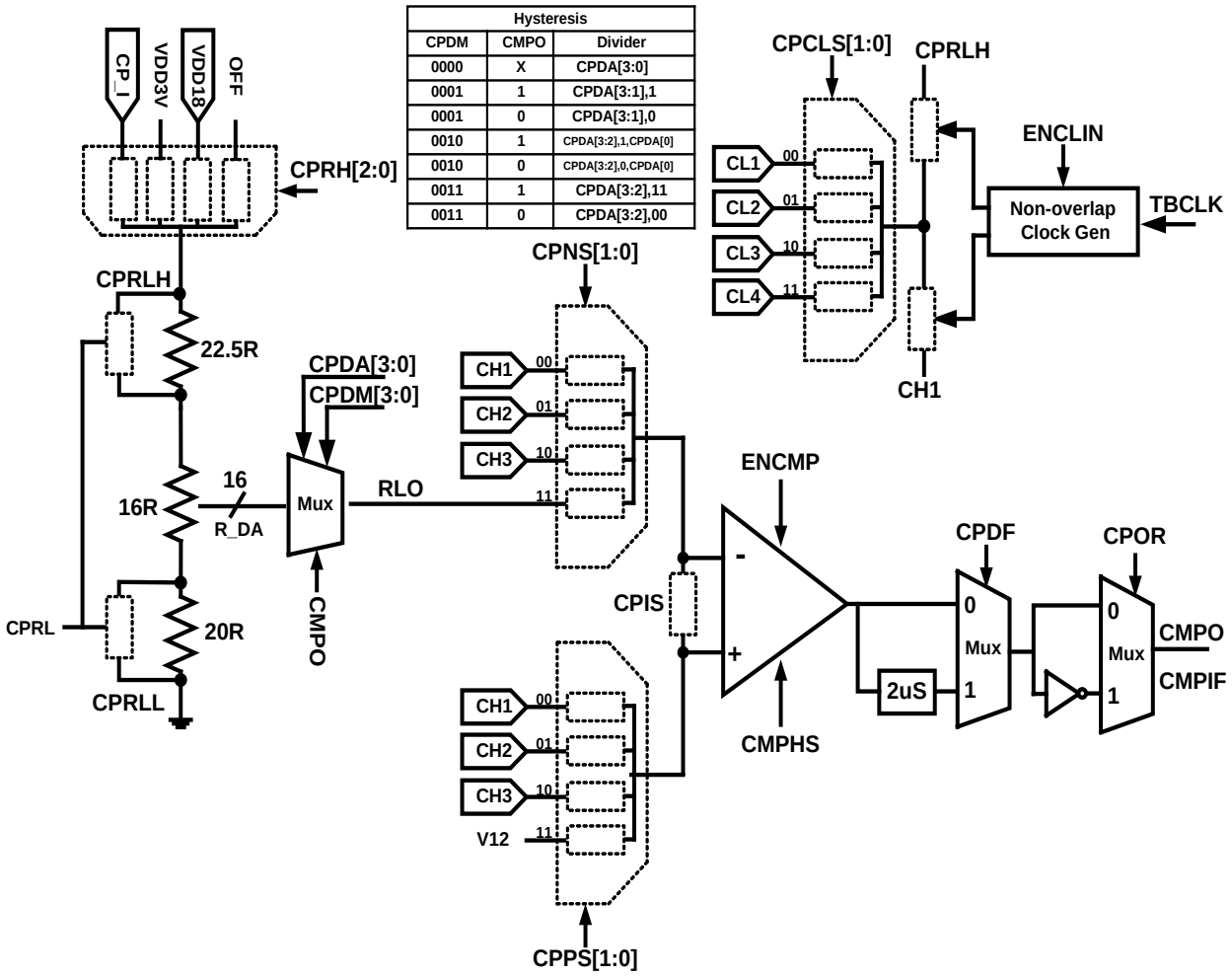
4.8. 8-bit Resistance Ladders Network



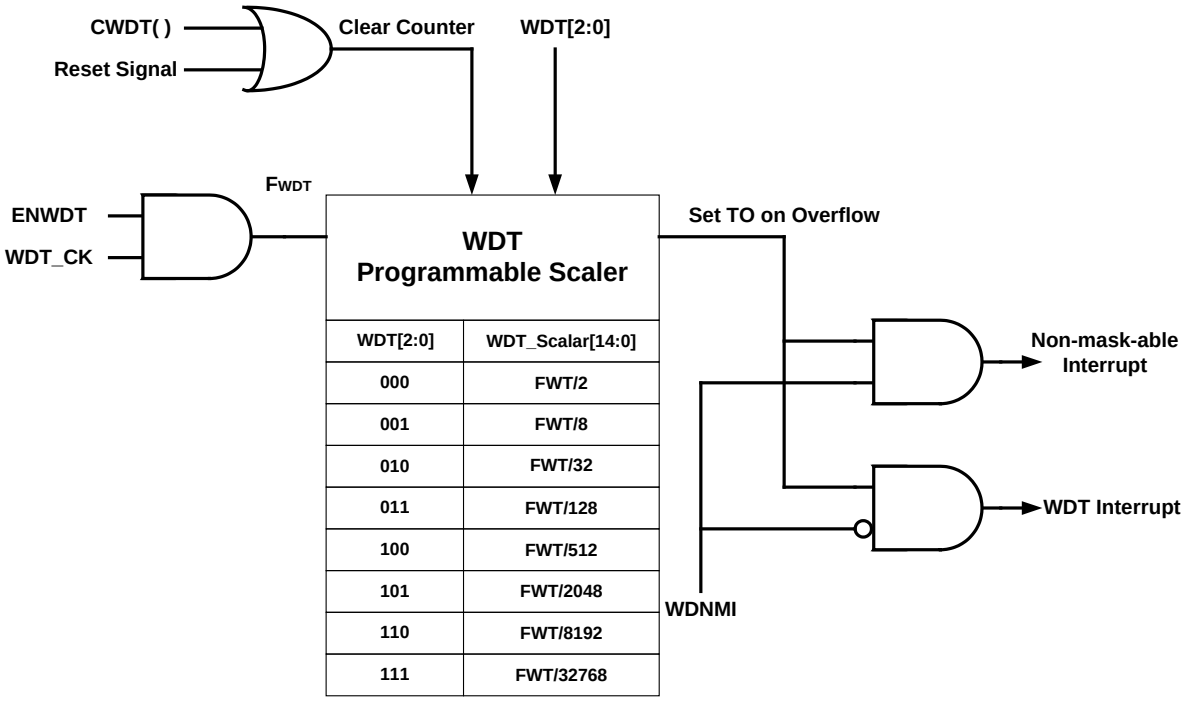
DABIT[7:0]	DABIT
0X00	0/256
0X01	1/256
⋮	⋮
0XFE	254/256
0XFF	255/256

4.9. Analog Comparator Network

Hysteresis		
CPDM	CMPO	Divider
0000	X	CPDA[3:0]
0001	1	CPDA[3:1],1
0001	0	CPDA[3:1],0
0010	1	CPDA[3:2],1,CPDA[0]
0010	0	CPDA[3:2],0,CPDA[0]
0011	1	CPDA[3:2],11
0011	0	CPDA[3:2],00

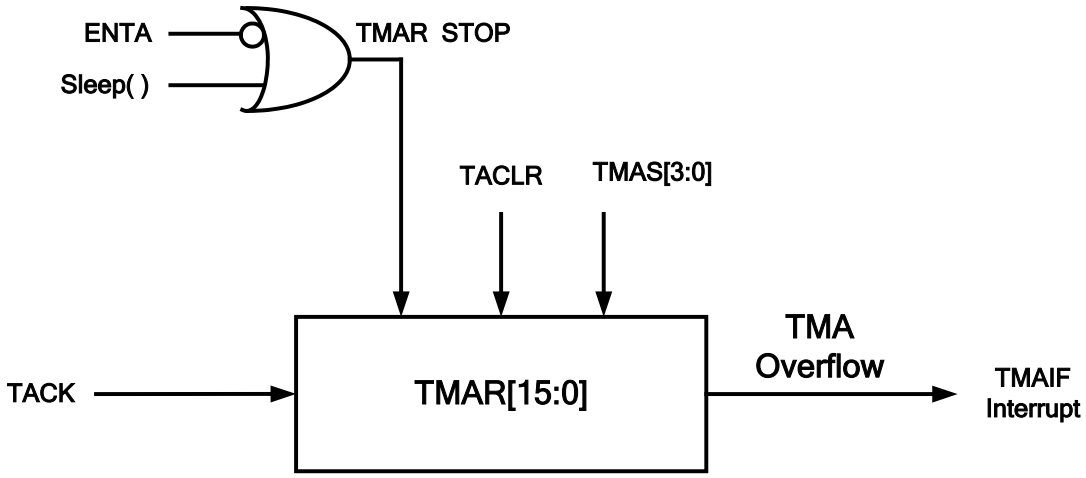


4.10. Watch Dog Timer Network



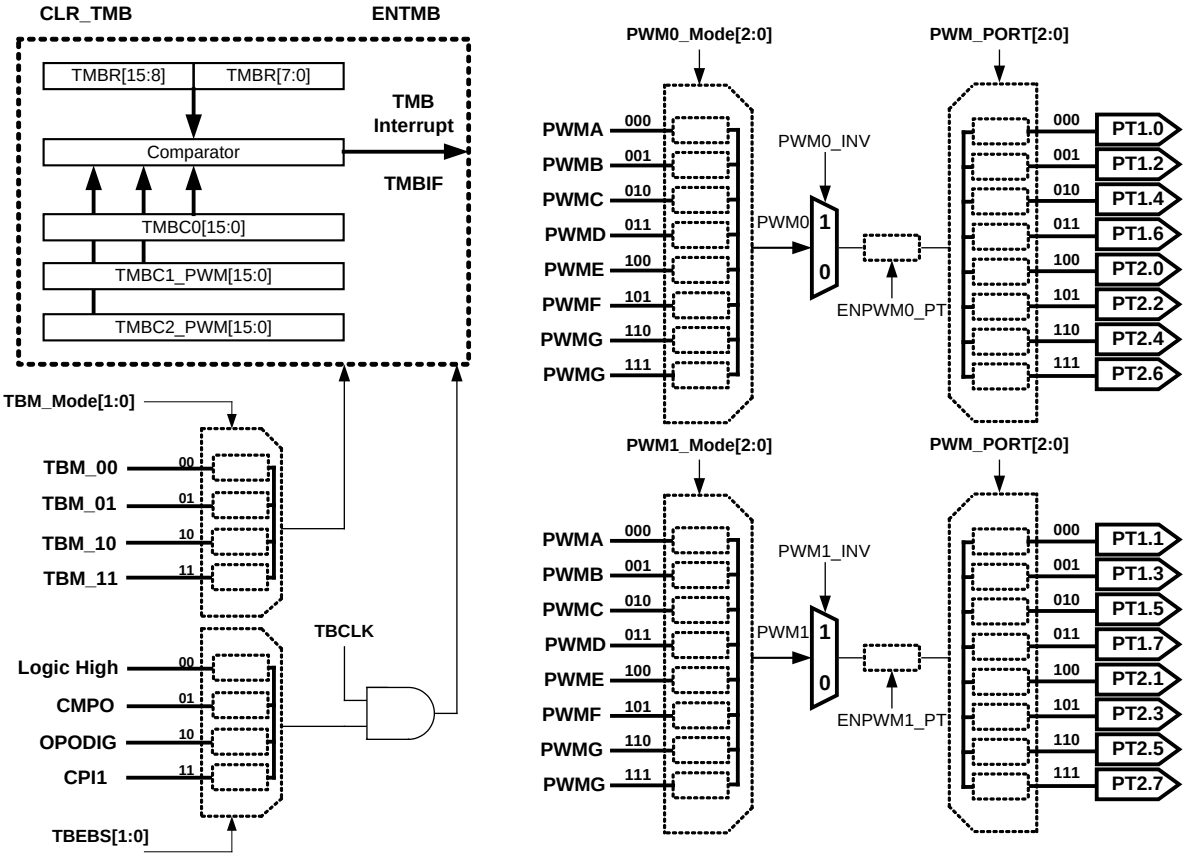
WDT[2:0]	WDT_Scalar[14:0]
000	FWT/2
001	FWT/8
010	FWT/32
011	FWT/128
100	FWT/512
101	FWT/2048
110	FWT/8192
111	FWT/32768

4.11. Timer A Network

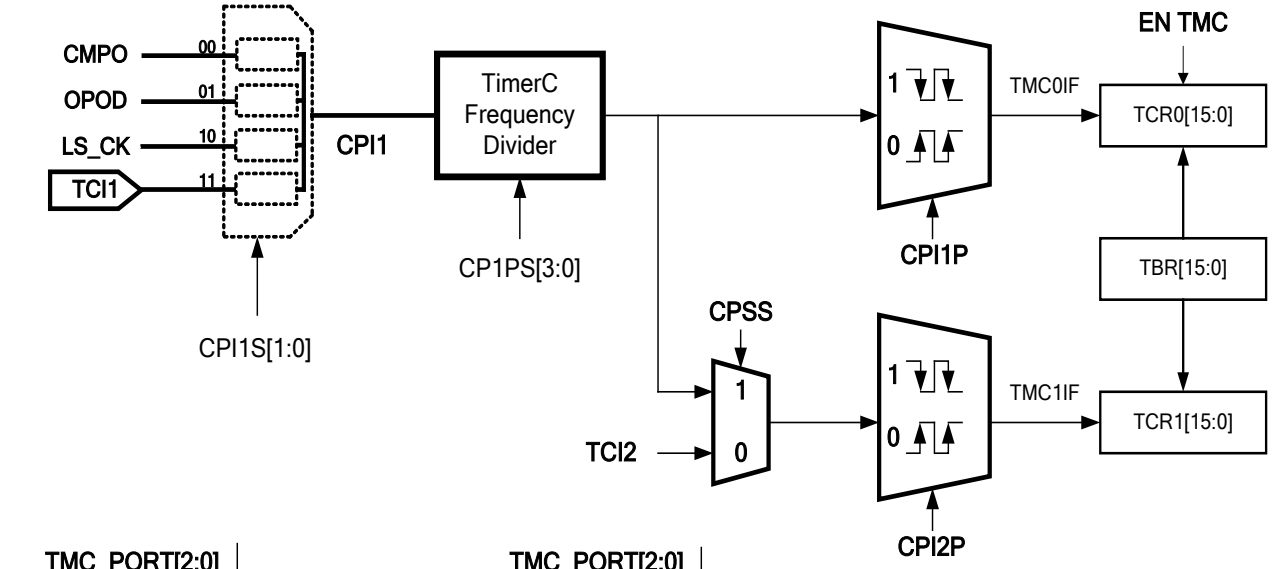


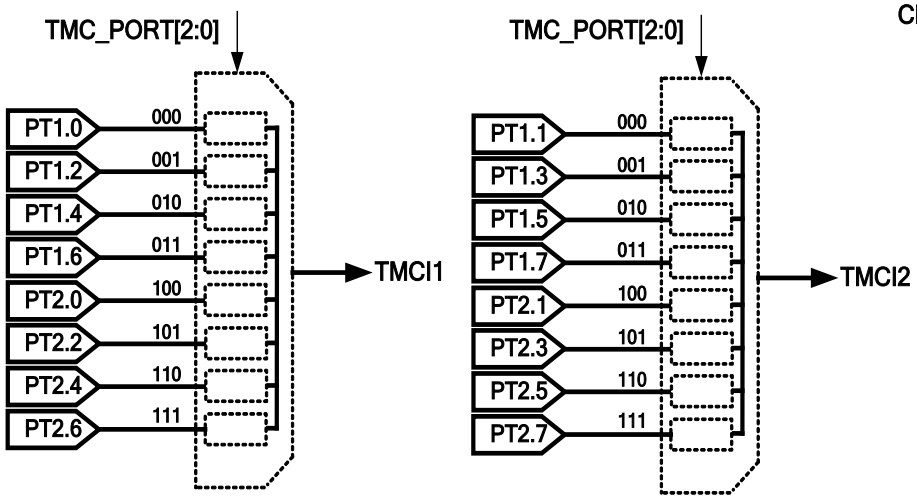
TMAS[3:0]	TMAR[15:0]
0000	TACK/2
0001	TACK/4
:	:
1110	TACK/32768
1111	TACK/65536

4.12. Timer B Network



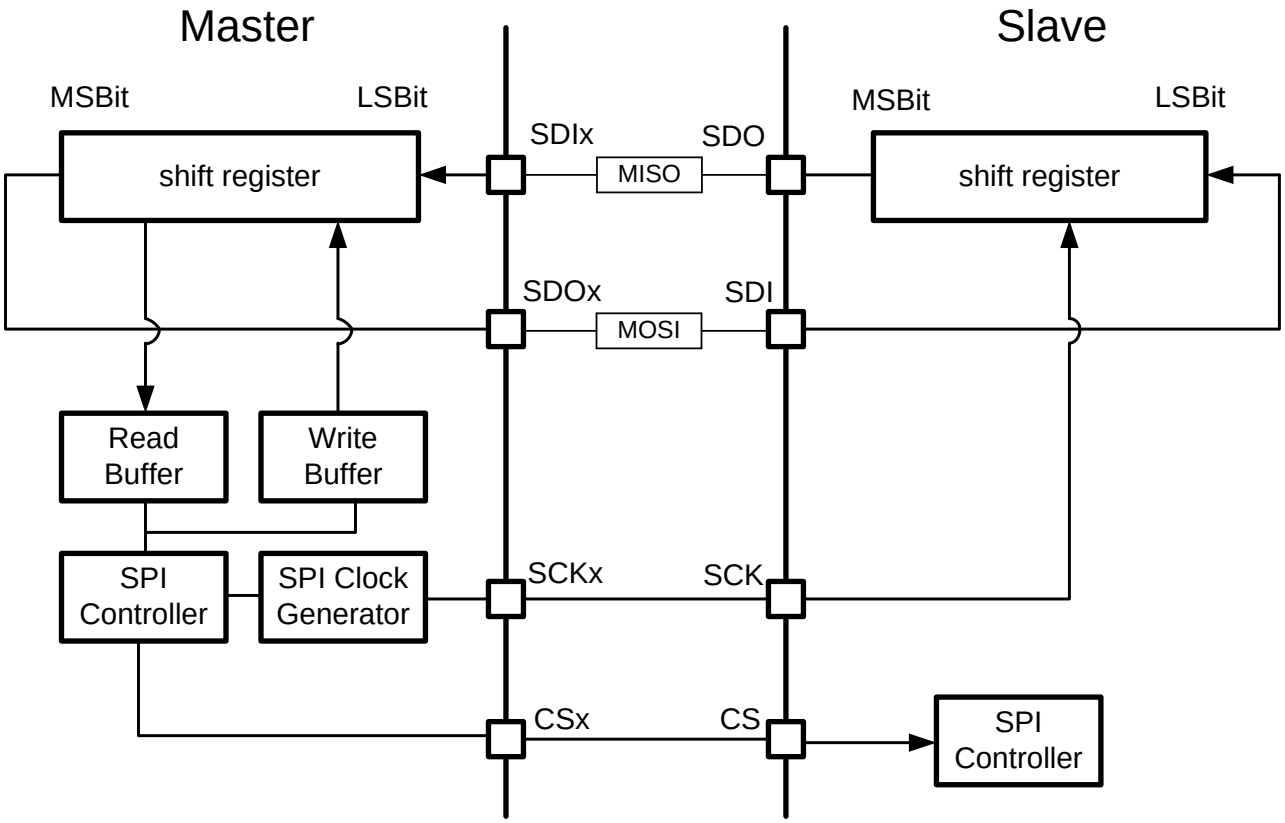
4.13. Timer C Network





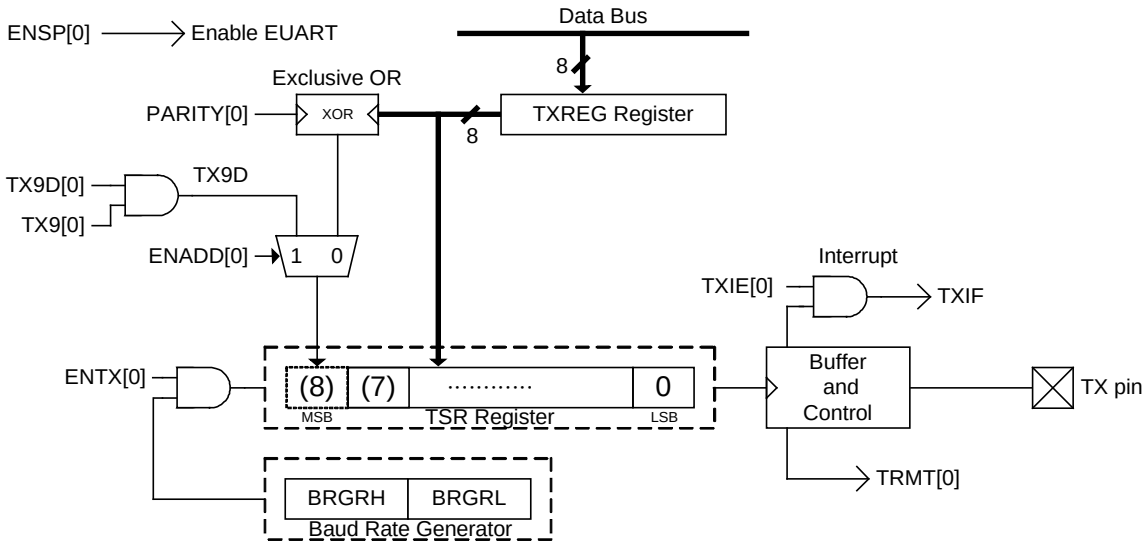
CP1PS[3:0]	CPI1 Divider
0000	CPI1÷1
0001	CPI1÷2
▪ ▪	▪ ▪
1110	CPI1÷16384
1111	CPI1÷32768

4.14. 32-bit SPI Diagram

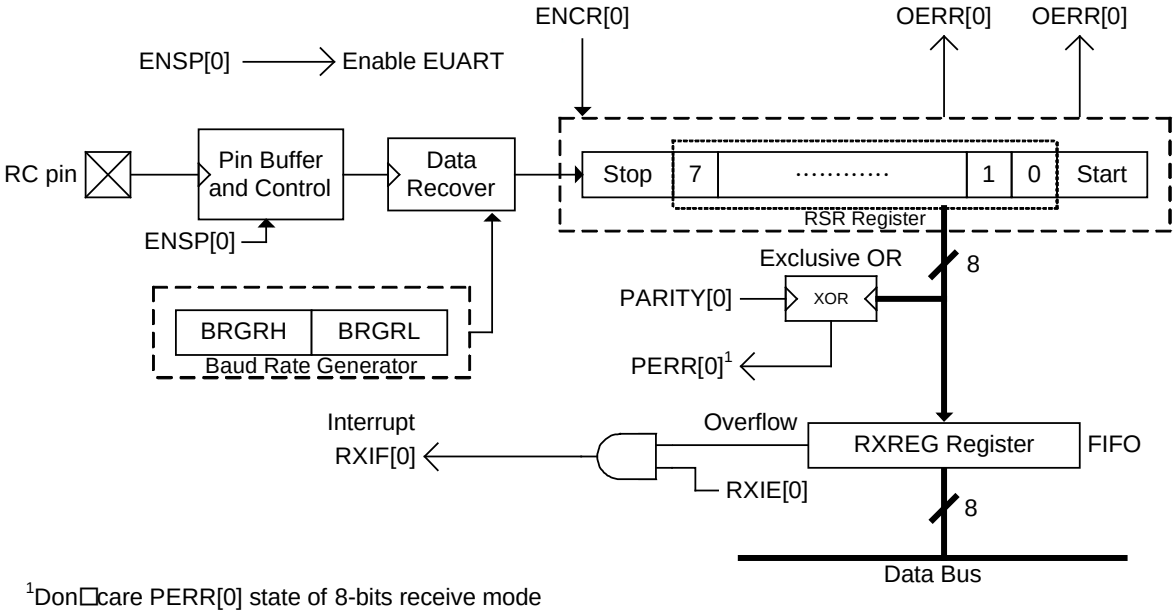


4.15. UART Block Diagram

EUART TRANSMIT BLOCK DIAGRAM

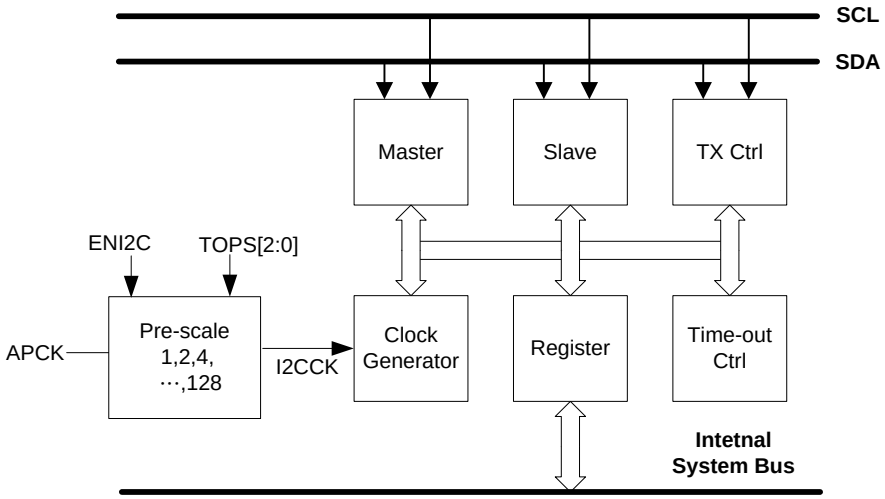


EUART 8-BITs RECEIVE BLOCK DIAGRAM

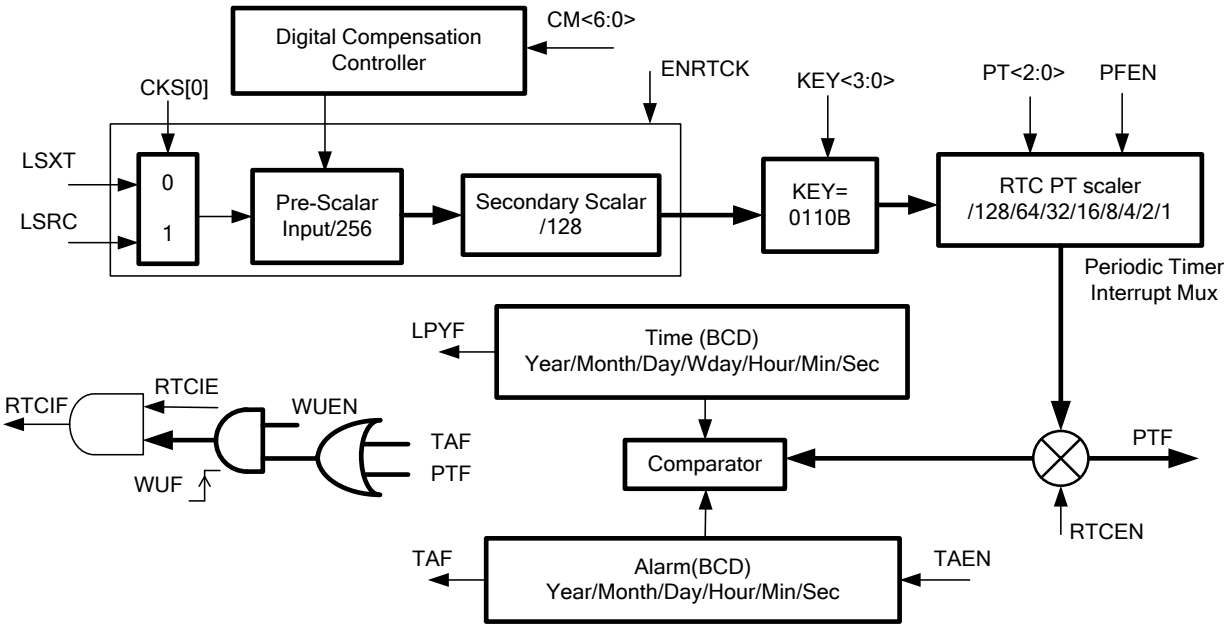


[1]Don□care PERR[0] state of 8-bits receive mode

4.16. I2C Block Diagram



4.17. Hardware RTC Block Diagram



5. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Parameter	Sym.	Min.	Max.	Unit
Voltage applied at VDD3V to VSS		-0.2	4.0	V
Voltage applied to Pin	Vin	-0.2	VDD3V+0.3	V
Diode current @ device terminal		-2	2	mA
Storage Temperature	TST	−55	150	°C
Operating Temperature	TA	−40	85	°C
Soldering Temperature(10s)			260	°C
Maximum output current sink by any PORT1 to PORT3 I/O PIN			10	mA

5.1. Recommended Operating Conditions

VDD3V=2.2V ~ 3.6V.T_A=25℃,Unless otherwise noted.

Parameter	Sym.	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VDD3V	Digital Application	2.2		3.6	V
		Digital Analog Application	2.4		3.6	V
Supply Current	I_Sleep	Sleep Mode ,VDD18 LDO OFF		2.5		uA
		Sleep Mode ,VDD18 LDO ON		3.5		
	I_Idle	LSRC=35KHz+IDLE Mode		5		uA
	Free Run_2MHz	HSRC=2MHz@CPU_CK:2MHz		1.1		mA
	Free Run_4MHz	HSRC=4MHz@CPU_CK:4MHz		2.1		mA
	Free Run_10MHz	HSRC=10MHz@CPU_CK:10MHz		3.3		mA
Power–Up Delay	$t_{PU,DLY}$	Wake up from deep sleep		64		ms

5.2. Clock System

Parameter	Sym.	Test Conditions	Min.	Typ.	Max.	Unit
HSXT	High Speed Crystal Operating Voltage Range	2MHz~4MHz (OHS_HS=0b)	2.2		3.6	V
		4MHz~16MHz (OHS_HS=1b)	2.2		3.6	V
I_{XHS}	High Speed Crystal Current	HSXT = 16MHz		100		uA
LSXT	Low Speed Crystal Frequency	VDD3V = 2.2V~3.6V		32.768		KHz
I_{XLS}	Low Speed Crystal Current			2		uA
F_{HAO}	Internal High Speed Oscillator Frequency	F_{HAO} = 2MHz F_{HAO} = 2MHz After Trim Note1	-10% -2%	2 2	+10% +2%	MHz
		F_{HAO} = 4MHz F_{HAO} = 4MHz After Trim Note1	-10% -2%	4 4	+10% +2%	MHz
		F_{HAO}= 10MHz F_{HAO} = 10MHz After Trim Note1	-10% -2%	10 10	+10% +2%	MHz
V_{HAO}	Voltage Coefficient	VDD3V = 2.2V ~3.6V	-0.2		+0.2	%
T_{HAO}	Temperature Coefficient	-40~85	-1.5		+1.5	%
I_{HAO}	Internal High Speed Oscillator Current	F_{HAO} = 2MHz		20		uA
D_{HAO}	Duty OF Internal High Speed Oscillator		40		60	%
WT_{HAO}	Wake Up Time	F_{HAO} = 2MHz		30		us
F_{LPO}	Internal Low Speed Oscillator Frequency	VDD3V= 3.0V	-20%	35	+20%	KHz
V_{LPO}	Voltage Coefficient	VDD3V= 2.2V ~3.6V	-2.5		+2.5	%
T_{LPO}	Temperature Coefficient	-40~85	-2.5		+2.5	%
I_{LPO}	Internal Low Speed Oscillator Current			0.35	0.7	uA
D_{LPO}	Duty OF Internal Low Speed Oscillator		40		60	%

Note1

After Trim: According to the factory calibration parameters of HAO to calibrate HAO, and need to corresponding to the selected HAO frequency. Configure the register 0x40304[7:0]. Please refer to the chapter 6.1.2 “UG-HY16F188_EN” to know how to use that in detail.

5.3. Power Management System

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Coarse Band Gap Reference						
	Operation Voltage		2.2		3.6	V
	Output Voltage	VDD3V=3.0V	1.05	1.2	1.35	V
Band Gap Performance						
	Operation Voltage	VDDA	2.4		3.6	V
	Output Voltage	VDDA =2.4V	1.15	1.2	1.25	V
	Temperature Coefficient			50		ppm/°C
	Startup Time			40		us
VDDA LDO						
	Output Voltage Error		-5		5	%
	Capacitor Loading		22		10,00	nF
	Settling Time	Capacitor Loading = 100nF 99% OF VDDA		50		us
	Operation Current	Bias + Band Gap + VDDA LDO		35	50	uA
	Dropout Voltage	I=10mA		0.2		V
	Voltage Coefficient	VDD3V= 2.5 ~ 3.6V		0.1		%/V
	Select VDDA Output Voltage	VDAS=00		2.4		V
		VDAS=01		2.7		V
		VDAS=10		3.0		V
		VDAS=11		3.3		V
	Temperature Coefficient	Using BRG VDDA=3.0V		100		ppm/°C
VDD18 LDO						
	Output Voltage		1.7	1.8	1.9	V
	Capacitor Loading			10,00		nF
	Maxim Current	VDD3V= 2.2 ~ 3.6V	10			mA
	Voltage Coefficient	VDD3V= 2.2 ~ 3.6V		1		%/V
	Temperature Coefficient			100		ppm/°C
	Load Regulation	Load = 0.1~10mA		0.1		V/A
	Dropout Voltage	Load = 10mA		0.2		V
REFO Buffer						
	Capacitor Loading		22	100	1000	nF
	Operation Current			15		uA
	Input Resistance	Push Pull R		5	20	Ω
	Output Current	1% Change Voltage	0.25	1		mA
	Temperature Coefficient	Using BRG VDDA=3.0V		80		ppm/°C
	Offset Voltage	REFO = 1.2V		±3	±12	mV
	Voltage coefficient	DC		0.1		%/V

5.4. Reset Management System

Reset Management System = (Brownout/External RST Pin/Low Voltage Detect)

Typical values are at TA=25℃ and VDD3V= 3.0V. Unless otherwise noted.

Sym.	Parameter Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, $t_{d\text{-}LVR}$	2			us
	VDD3V Start Voltage to accepted reset internally (L→H),V_{LVR}	1.8	1.95	2.1	V
	Ta=-40℃~85℃	-0.50		+50	mV
	Hysteresis, $V_{HYS\text{-}LVR}$		30		mV
POR	Operation Slew Rate			0.1	V/us
	Start Voltage to Accepted Reset	0.6			V

5.5. GPIO Port

Typical values are at T_A=25℃ and VDD3V = 3.3V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
PT 1.0 ~ 3.7 GPIO Port						
R_{PU}	Internal pull high resistor		65	85	105	kΩ
V_{IH}	Input high voltage		0.7*VDD3V			V
V_{IL}	Input low voltage				0.3*VDD3V	V
I_{OH}	Source current			10		mA
I_{OL}	Sink current			10		mA

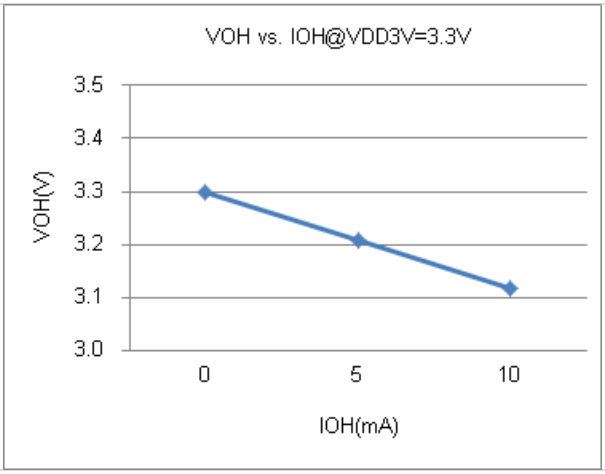


Figure5.5-1 VOH vs. IOH

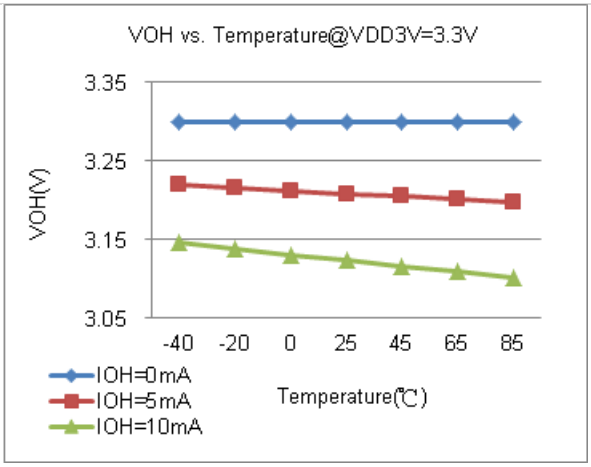


Figure5.5-2 VOH vs. Temperature

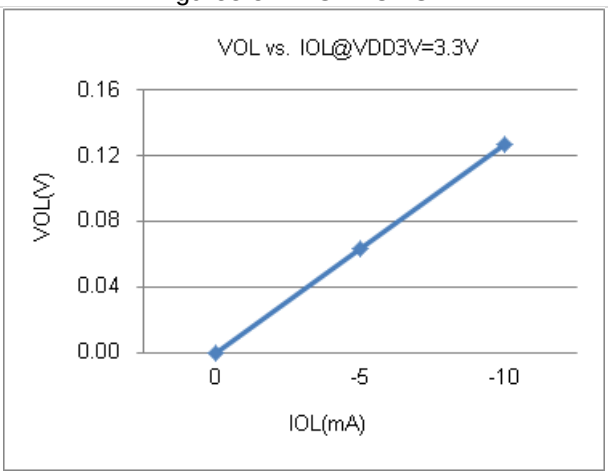


Figure5.5-3 VOL vs. IOL

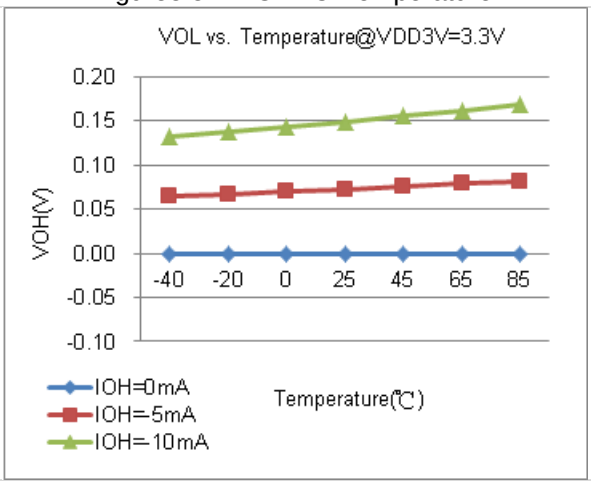


Figure5.5-4 VOL vs. Temperature

5.6. ΣΔADC ENOB and RMS Noise

Typical values are at TA=25℃ and VDD3V = 3.3V, VDDA=2.4V unless otherwise noted.

HY16F188 provides important input noise specification that aims at ΣΔADC. Table 7.5-1 and Table 7.5-2 lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short, voltage reference: 1.2V and 1024 records were sampled.

ENOB(RMS) with OSR/GAIN at A/D Clock=333Khz, VDDA=2.4V, VREF=1.2V														
Max. Vin(mV) =0.9*VREF (1)	OSR					32	64	128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					10417	5208	2604	1302	651	326	163	81	41	20	10
	Gain	=	PGA	×	ADGN											
±1080	1	=	1	×	1	12.5	15.0	16.6	17.3	17.7	18.1	18.7	19.2	19.6	20.3	20.7
±540	2	=	1	×	2	12.4	14.4	16.3	16.9	17.0	17.4	17.9	19.1	19.3	20.0	20.4
±270	4	=	1	×	4	12.2	14.6	16.1	16.6	16.9	17.2	17.9	18.8	19.4	19.8	20.3
±33.75	32	=	8	×	4	12.2	13.7	15.1	15.6	16.1	16.5	17.0	17.7	18.1	18.6	19.1
±16.875	64	=	16	×	4	12.1	13.8	14.6	15.2	15.6	16.2	16.7	17.2	17.6	18.1	18.5
±8.4375	128	=	32	×	4	12.0	13.3	14.1	14.7	15.1	15.6	16.1	16.6	17.1	17.6	18.1
(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).																

Table 5.6-1ΣΔADC ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=333Khz, VDDA=2.4V, VREF=1.2V															
Max. Vin(mV) =0.9*VREF	OSR					32	64	128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					10417	5208	2604	1302	651	326	163	81	41	20	10
	Gain	=	PGA	×	ADGN											
±1080	1	=	1	×	1	426.3	71.0	23.3	14.56	10.92	8.29	5.72	3.98	2.95	1.89	1.410
±540	2	=	1	×	2	216.6	54.1	14.5	9.93	9.37	7.17	4.77	2.19	1.89	1.12	0.838
±270	4	=	1	×	4	129.5	23.5	8.5	6.04	4.85	4.02	2.46	1.29	0.89	0.65	0.455
±33.75	32	=	8	×	4	15.8	5.5	2.1	1.53	1.07	0.78	0.56	0.36	0.27	0.18	0.135
±16.875	64	=	16	×	4	8.5	2.6	1.5	0.99	0.75	0.51	0.36	0.26	0.19	0.13	0.098
±8.4375	128	=	32	×	4	4.6	1.9	1.1	0.71	0.52	0.37	0.27	0.19	0.14	0.10	0.068

Table 5.6 -2ΣΔADC RMS Table

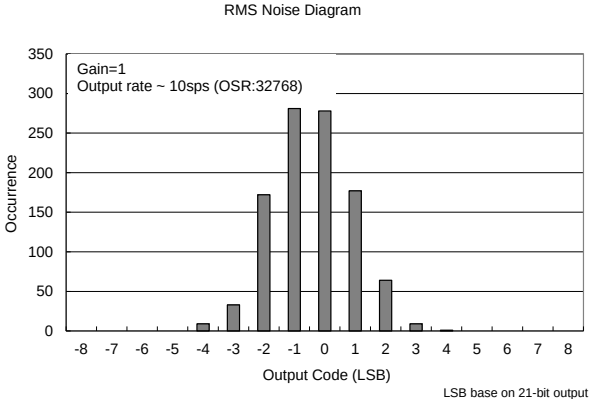


Figure5.6-1(a) RMS Noise Diagram

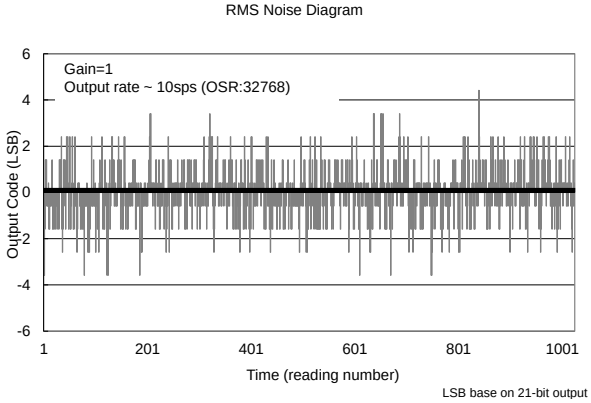


Figure5.6-1(b) Output Code Diagram

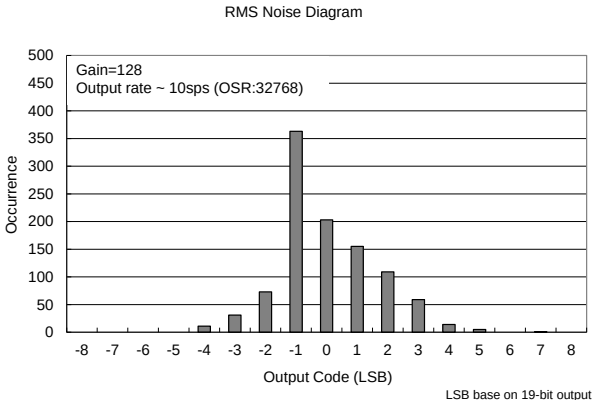


Figure5.6-2(a) RMS Noise Diagram

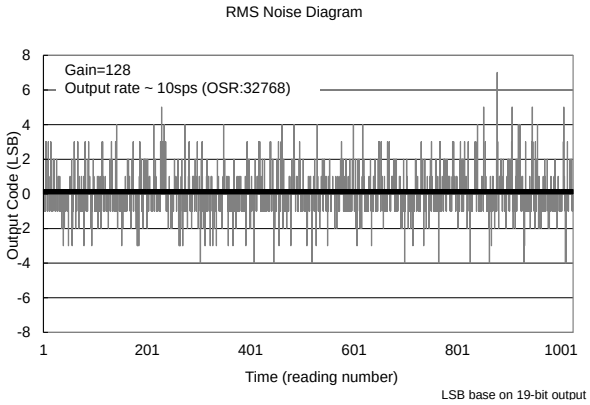


Figure5.6-2(b) Output Code Diagram

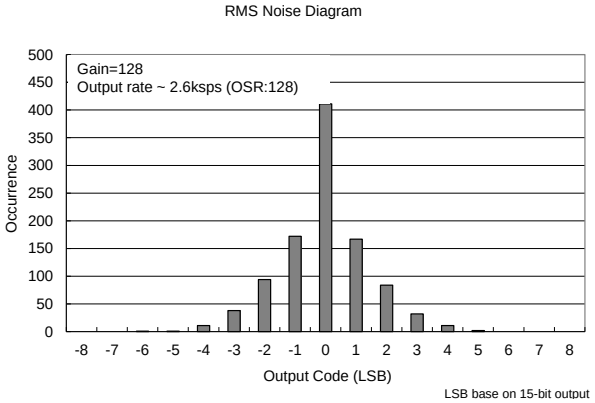


Figure5.6-3(a) RMS Noise Diagram

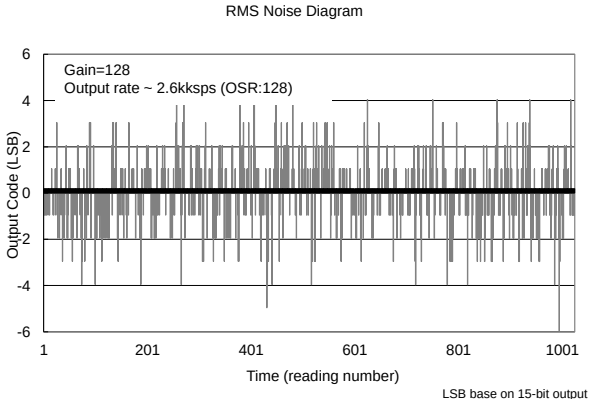


Figure5.6-3(b) Output Code Diagram

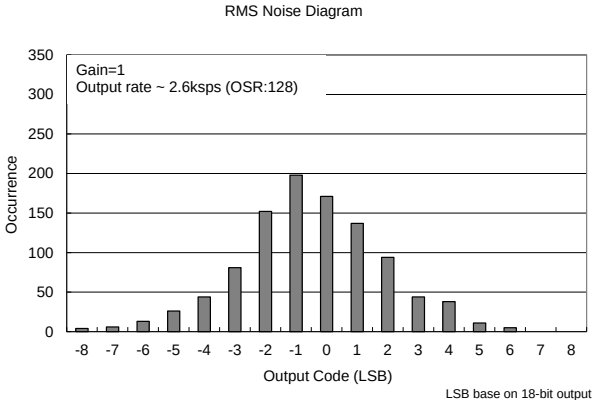


Figure5.6-4(a) RMS Noise Diagram

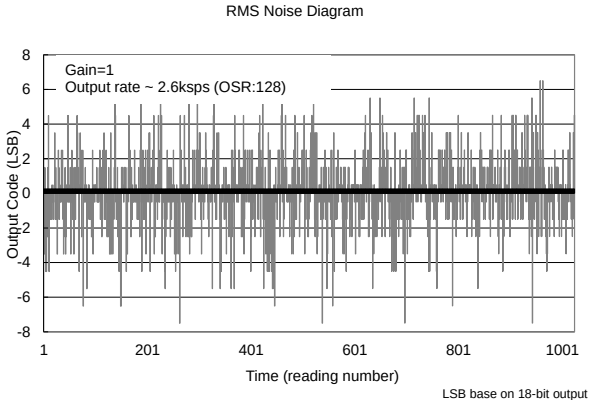


Figure5.6-4(b) Output Code Diagram

5.7. ADC Management System

All specifications at T_A=-40℃ to +85℃,

VDDA=REFP=3.0V, REFN=VSS, and Gain=128. Unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Analog Inputs							
	Full-scale input voltage (VINP - VINN)	Considering ADC performance matches ADC ENOB table. REFP=VDDA, REFN=VSS VREF be set to 1/2 only		±0.5*VREF/Gain			V
		Considering ADC performance matches ADC ENOB table. REFP=REFO_I REFN=VSS VREF be set to 1 only		±VREF/Gain			
	Common-mode input range	Gain = 1, @25℃		VSS-0.2V		VDDA	V
Analog Inputs							
	Full-scale input voltage (VINP - AINN)			±0.5*VREF/Gain			V
	Common-mode input range	Gain = 1, @25℃		VSS-0.2V		VDDA	V
System Performance							
	Resolution	No missing codes			24		Bits
	Data rate	ADC Clock			ADC Clock /OSR		SPS
	Digital filter settling time	Full setting			3		Data
	Integral nonlinearity (INL)	Differential input End-point fit,OSR=32768			15		PPM
	ADC Gain drift	40℃ to +85℃,			5		ppm/℃
	Normal-mode rejection	f_{IN}=60Hz ±1Hz, Output rate = 10 SPS	Internal OSC		70		dB
			External OSC		80		dB
	Common-mode rejection	ΔVDDA = 0.1V @ DC			80		dB
	Input-referred noise	Output rate= 10 SPS			65		nV, rms
	Power-supply rejection	ΔVDDA = 0.1V @ DC			80		dB
Voltage Reference Input							
	Voltage reference input	VREF = REFP - REFN				VDDA	V
	Positive Reference Input	REFP, @25℃		VDDA/2		VDDA	V
	Negative Reference Input	REFN, @25℃		VSS		VDDA/2	V
ADC Modulator Current							
ADC	ADC Modulator	VDD3V=3.3V,VDDA=2.4V			150		uA
PGA	ADC PGA	VDD3V=3.3V,VDDA=2.4V			625		uA

5.8. Internal Temperature Sensor

Typical values are at TA=25℃ and VDD3V = 3.0V, VDDA=2.4V unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC_S	Sensor Temperature Drift			178		uV/℃
KT	Absolute Temperature Scale 0°K			-285		℃
TC_{ERR}	One Point Calibrate Error Temperature	Calibration at 25℃，-40℃~85℃		±2		℃

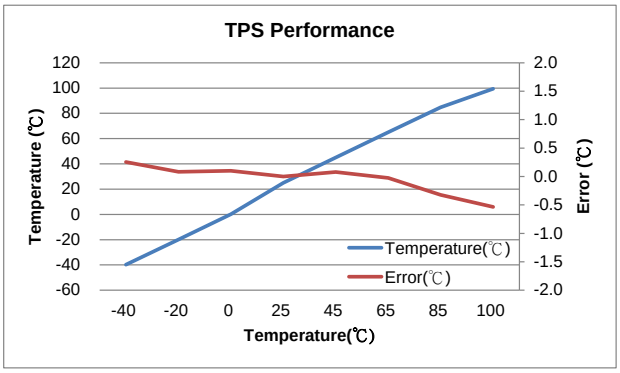


Figure5.8-1 TPS Performance

5.9. 8-bit Resistance Ladders Management System

Typical values are at TA=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Resolution	Monotonic		8		Bit
	Power Supply		2.4		VDD3V	V
V_{OUT}	8-bit Resistance Ladders Output Range		VR-		VR+	V
V_{REFP}	Positive Reference Voltage Range	$V_{REFP} > V_{REFN}$	0		VDD3V	V
V_{REFN}	Negative Reference Voltage Range		0		VDD3V	V
R_{ON}	8-bit Resistance Ladders output switch(PT3AO switch resistance)	VDD3V = 3.0V 0.5V < DAO < VDD3V-0.5V			200	Ω
		VDD3V = 3.0V 0.5V > DAO, DAO > VDD3V-0.5V		10		Ω
R_{RSW}	Reference Voltage Switch(DA_Vrefp switch resistance, DA_Vrefn switch resistance)	DA_V_{refp} = 2.2V, DA_V_{refn} = 0V, VDDA = 2.4V		15	30	Ω
R_{LADDER}	One LSB Resistance Ladder		621	730	840	Ω
INL	Integral Linearity Error	VR+ = 2.4V VR-= 0V		±0.5	±1	LSB
DNL	Differential Linearity Error	VR+ = 2.4V VR-= 0V		±0.5	±1	LSB
E_{OS}	Offset Error	VR+ = 2.4V VR-= 0V			1	LSB

5.10. OPAMP Management System

Typical values are at TA=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA	Power Supply		2.4		3.6	V
V_{OUT}	Output Range		0		VDDA	V
V_{IN}	Input Common Range		0		VDDA	V
I_{OPA}	OPA current			120		uA
I_{OPA_LOAD}	Output Current Loading (Push OR Pull)	VDDA = 3.0V, 0.3V < Output Voltage < VDDA-0.3V			1	mA
		VDDA = 2.2V, 0.3V < Output Voltage < VDDA-0.3V			0.5	mA
C_{LOAD}	Max Output Capacitor Load				1000	pF
SR	Slew Rate	Loading R=10K, C=100pF, 0.3 -> VDDA-0.3V		0.6		V/us
UGB	Unit Gain Bandwidth	Loading C=100pF, -3dB		1000		KHz
V_{OS}	Offset Error	Vin = 1.2V	-5		+5	mV
DFD	Digital Filter Delay	VDDA=3.0V		2		us
C_{SA}	Sample Capacitor			10		pF

5.11. CMP Management System

Typical values are at TA=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{MC}	Operation Supply Current	ENCMP[0]=1, CMPHS[0]=1		10		uA
	Low Power Mode	ENCMP[0]=1, CMPHS[0]=0		1		
V_{IC}	Common-mode Input Voltage		0		VDD3V-1	V
V_{OS}	Offset Voltage		-5		5	mV
V_{hys}	Input Hysteresis		0	0.7	1.5	mV
V_{REF}	Reference Voltage	CPPS[1:0]=11	1	1.2	1.4	V
	Temperature Drift	CPPS[1:0]=11		80		ppm/℃
I_R	Multi-node Resistor Current	CPRLS[0]=0		10		uA
		CPRLS[0]=1		30		

5.12. Flash DC Electrical Characteristics

Typical values are at TA=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
N_{ENDUR}	Endurance		20000			cycles[*1]
T_{RET}	Data Retention	T_A=25℃	10			year
T_{RAT}	Read Access Time				85	ns
T_{PWT}	Page Write Time				3	ms
I_{FRC}	Read Current	10MHz		1.63		mA
I_{FWC}	Write Current			1		mA
I_{FEC}	Erase Current			1		mA

Notes:

1. Number of Write/Erase cycles.
2. Guaranteed by design, not test in production.

6. Ordering Information

6.1. HY16F18 Series Device Number Selection

Device No.[1]	Package Type	Pins	Package Drawing		Code[2]	Shipment Packing Type	Unit Q'ty	Material Composition	MSL[3]
HY16F188-D000	Die	-	D	000	-	-	200	Green[4]	-
HY16F188-L048	LQFP	48	L	048	-	Tray	250	Green[4]	MSL-3
HY16F187-L048	LQFP	48	L	048	-	Tray	250	Green[4]	MSL-3
HY16F184-L048	LQFP	48	L	048	-	Tray	250	Green[4]	MSL-3
HY16F187-N033	QFN	33	N	033	-	Tray	490	Green[4]	MSL-3
HY16F184-N033	QFN	33	N	033	-	Tray	490	Green[4]	MSL-3
HY16F184-T028	TSSOP	28	T	028	000	Tube	50	Green[4]	MSL-3
HY16F184-T028	TSSOP	28	T	028	000	Tape & Reel	4000	Green[4]	MSL-3

[1] Device No.: Model No. – Package Type Description

HY16F188-L048

IC part Number

IC PKG Type

EX：You request in LQFP 48package.

The device No. will be HY16F188-L048.

And please clearly indicate the shipment packing type when placing orders.

[3] MSL:

The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

[4] Green (RoHS & no Cl/Br):

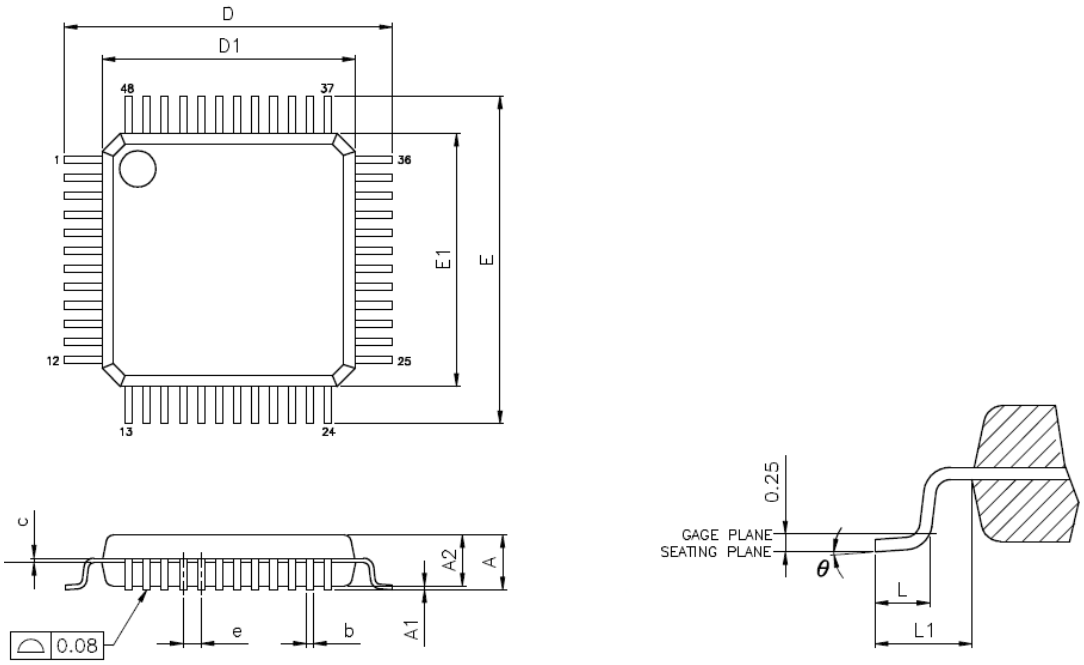
HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br/Cl<0.1%).

7. Package Information

7.1. LQFP48 PKG Diagram

Package Outline Drawing--- LQFP 7X7 48L

Unit: mm



SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note:

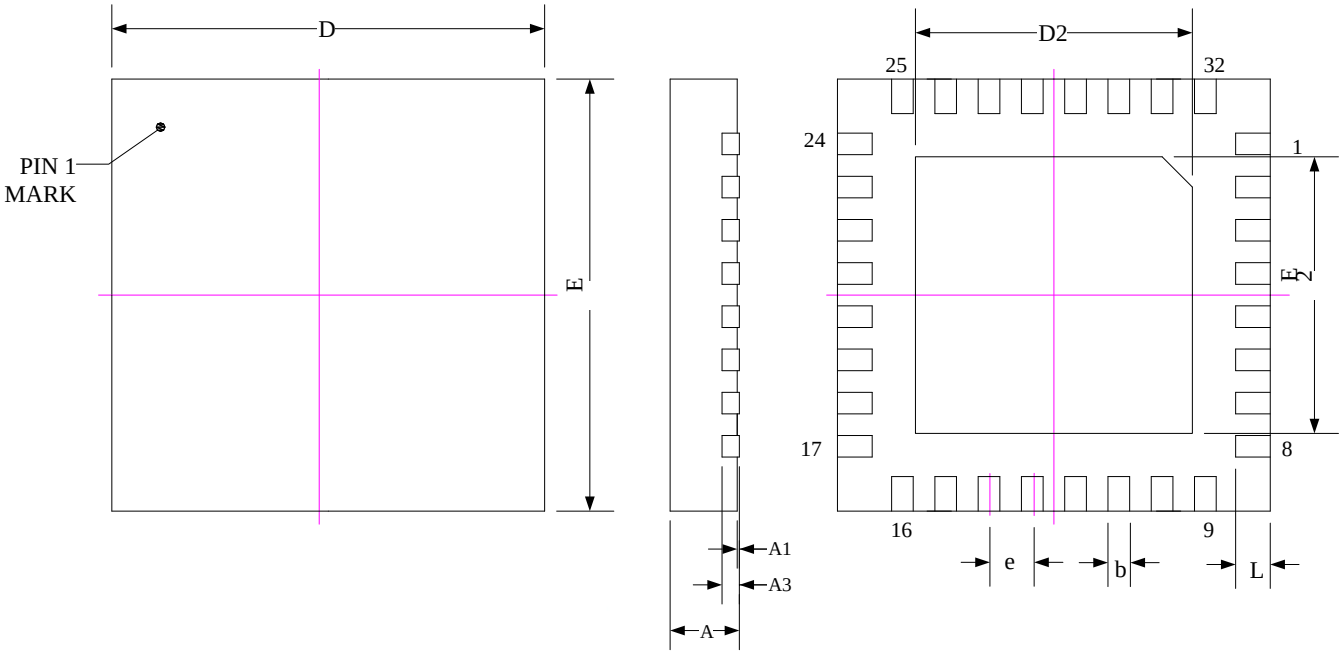
(1)All dimensions refer to JEDEC OUTLINE MS-026.

(2)Do not include Mold Flash or Protrusions.

7.2. QFN33 PKG Diagram

Package Outline Drawing--- QFN 5X5 33 Unit: mm

PIN33=VSS

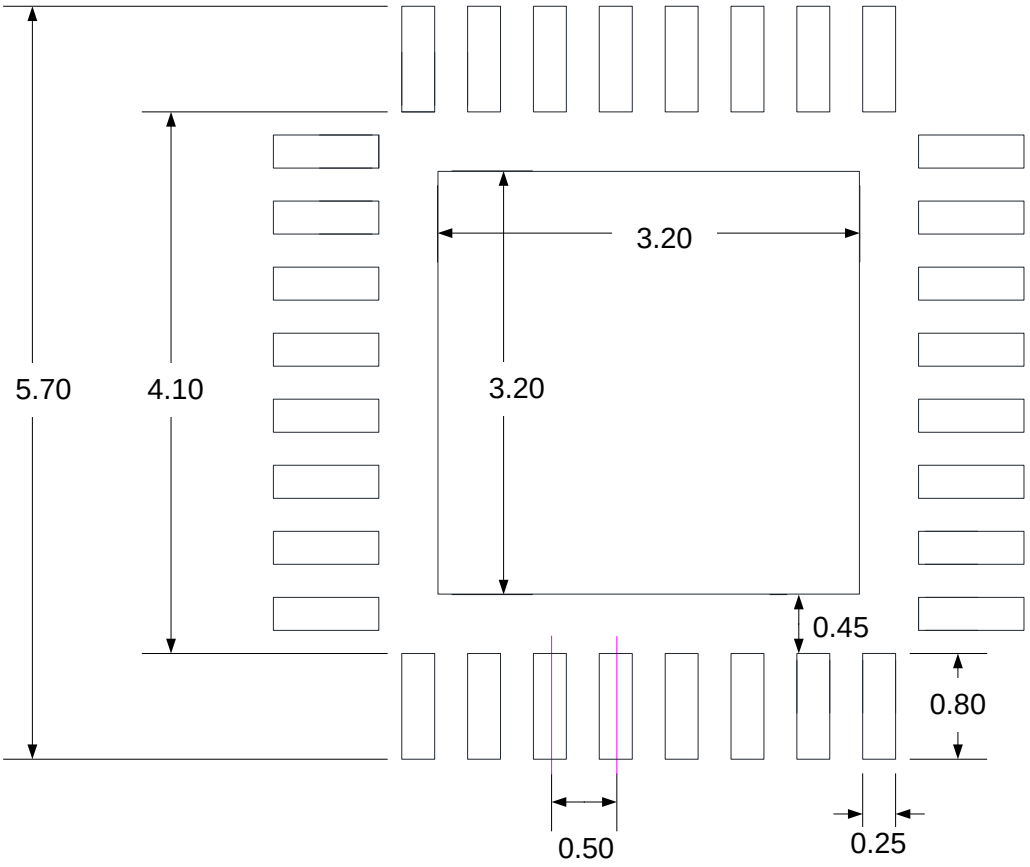


SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
D2	3.10	3.20	3.30
E2	3.10	3.20	3.30
L	0.35	0.40	0.45
e		0.50 BSC	

Note: All dimensions refer to JEDEC OUTLINE MO-220.

7.3. Land Pattern Design Recommendations

Unit: mm



Note:

Publication IPC-7351 is recommended for alternate designs

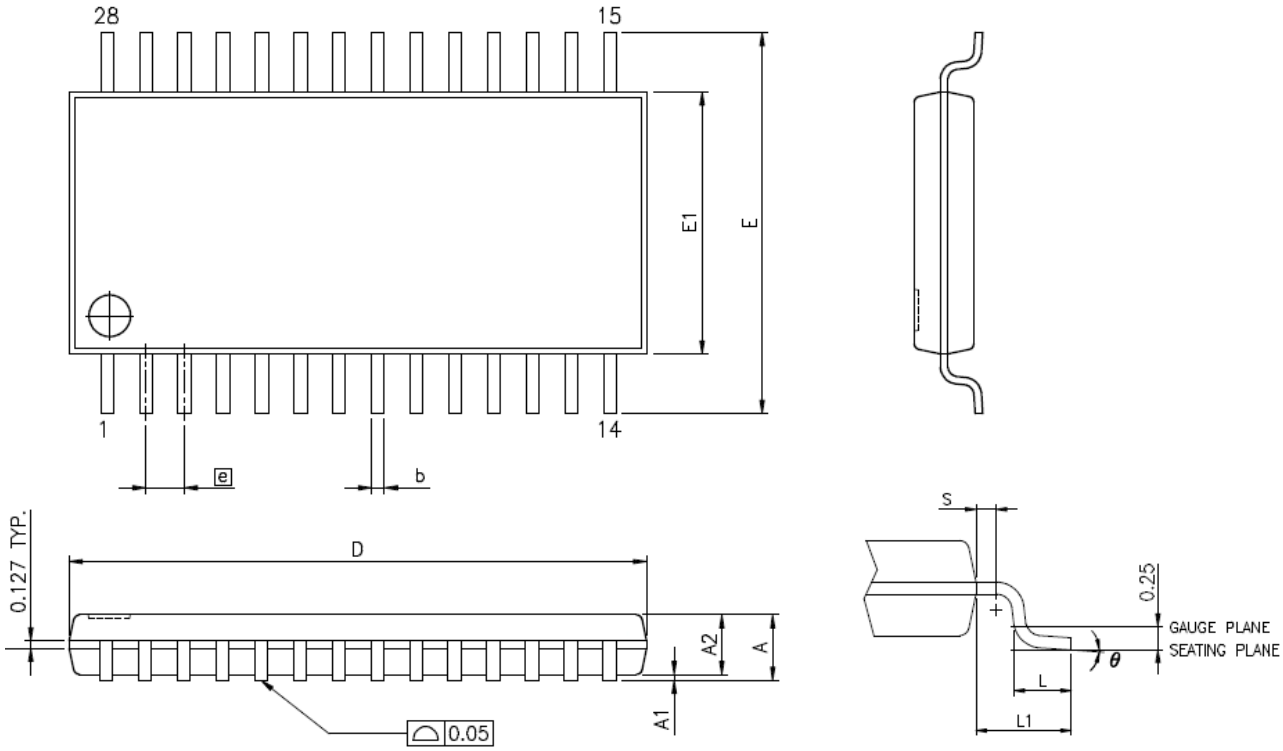
Unit : mm

http://www.hycontek.com/wp-content/uploads/QFN_DFN_PCB.pdf

7.4. TSSOP28 PKG Diagram

Package Outline Drawing--- TSSOP 28

Unit: mm



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

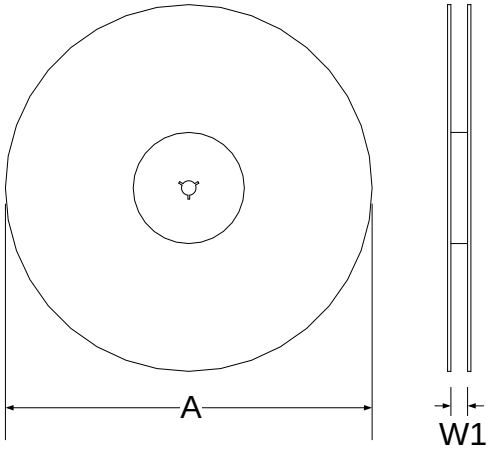
Note:

1. All dimensions refer to JEDEC OUTLINE MO-153.
2. Do not include Mold Flash or Protrusions

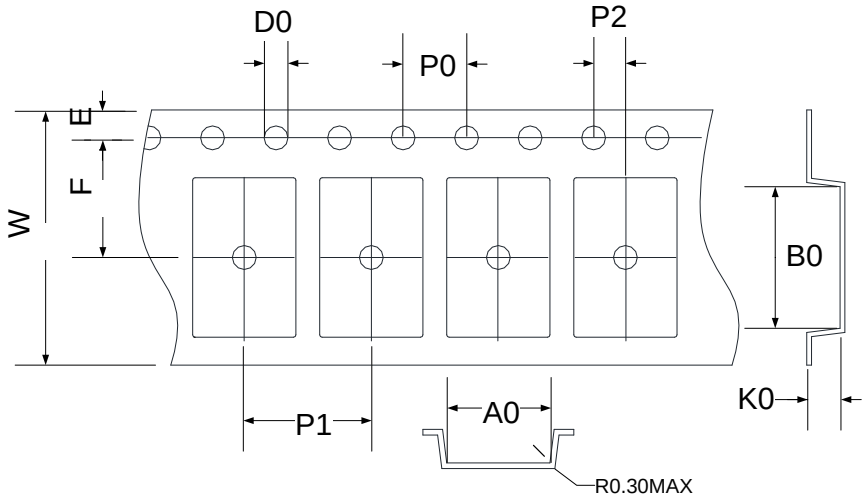
7.5. Tape & Reel Information---TSSOP28(173mil)

Unit : mm

1. Reel Dimensions



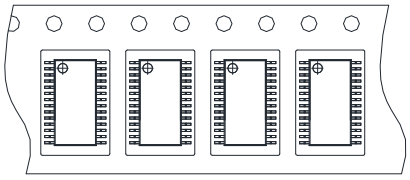
2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	16.5	6.80	10.20	1.60	4.00	8.00	2.00	1.75	7.50	1.50	16.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

3. Pin1 direction



8. Revisions

Major differences are stated thereinafter:

Version	Page	Summary of Changes	Date
V01	ALL	First edition	2013/05/20
V05	ALL	(1)Added HY16F184/187 Pin out (2)In Ordering Information added HY16F184/187 description. (3)In Package Information added LQFP48 and QFN33 description.	2013/09/16
V06	ALL	(1) Name change: VDD3 to VDD3V. VDD to VDD18.	2013/12/20
V07	ALL	(1)Remove PT4.0 sign (2)Original Description of OPO be revised to analog OPO (3)Digital OPO1 and OPO2 are revised to be OPOD1 and OPOD2 Digital Output (3)Revise Electronic Characteristic	2014/05/05
V08	ALL	“DAC “ be revised to be as “8-bit Resistance Ladders”	2015/06/09
	ALL	HSXT External High Speed Oscillator revised as 16MHz	
	CH4.5	REFOI is revised as REFO_I	
	CH4.6	ADC Network input OPO is Revised to be OPOI, REFO is revised to be REFO_I	
	CH4.7	OPAMP Network OPNS[3]is revised as OPOI, OPNS[4]is revised as OPO, R2ROPoutput description revise, REFO is revised as REFO_I	
	CH4.8	8-bit Resistance Ladders Network input pin’s REFO is revised as REFO_I	
	CH7.3	Capacitor Loading of REFO Buffer the unit is revised from pF to nF, and add Min value 22nF	
V09	ALL	Added Description HY16F184 SSOP28 Package Information & IC Package Pin Plots & Shipping Info	2016/10/14
	ALL	Added a chapter to the section on the package Information	
	ALL	Added QFN33 Land pattern information	
	ALL	1. Description ADC conversion speed up to 350KSPS amended to 10Ksps. 2. The original description 64Kb Flash ROM / 8Kb SRAM amended to 64KB Flash ROM / 8KB SRAM 3. Built-in low-speed LSRC oscillator frequency as low as 35KHz	
	ALL	Corrected Charge Pump clock system network description, modified LSRC frequency is 35kHz	
	CH4.8	The original description of DABIT is 1/256, the	

		correction is described as the first order from 0/256, and so on.	
	CH5.2	Remove Section 5.2, HY16F18 Series Selection Guide, and HY16F18 Series Selection Guide to Section CH1 Supplement for Description.	
	CH7.2	1. Add HAO 2M / 4M / 8M Before Trim and After Trim center frequency value 2. Correct the LSRC center frequency to 35KHz, the error value is +/- 20%	
	CH7.5	ADC ENOB Table When Gain = 4x, Vin = 135mV is corrected to 270mV	
	CH7.6	Corrected table description of ADC Management system	
V10	CH7.2	Add HAO (after trim) description	2016/05/24
V11	CH7.8(P56)	Modify the RLADDER value and increase the upper and lower limits.	2017/02/13
	CH7.10(P57)	Add VREF (Reference Voltage) upper and lower limits	
	CH7.3(P51)	Modify REFO Operation Current Typ. = 20uA	
	CH7.1(P48)	Modify Sleep power consumption with symbols and test conditions	
	CH7.2	Modify electrical characteristics symbol (HAO & LPO)	
	CH4.14 CH5 CH5.3 CH4.5	Modify SPI Diagram Electrical Characteristics Move to Chapter 5 VDD18 LDO (Capacitor Loading) The maximum value is changed to 1uF Modify Power system Diagram	
V12	ALL CH5.5 CH5.9	1. Remove the PT3.2 and PT3.3 multiplexing pin functions, and retain the AIO4 and AIO5 analog functions. 2. Added GPIO Electrical Characteristics Chapter 5.5 3. Modify 5.9 sections R_{ON} Test Conditions description and 8-bit Resistance Ladder Network Diagram. 4. ADC network diagram (ADCLK renamed ADCK).	2017/11/07