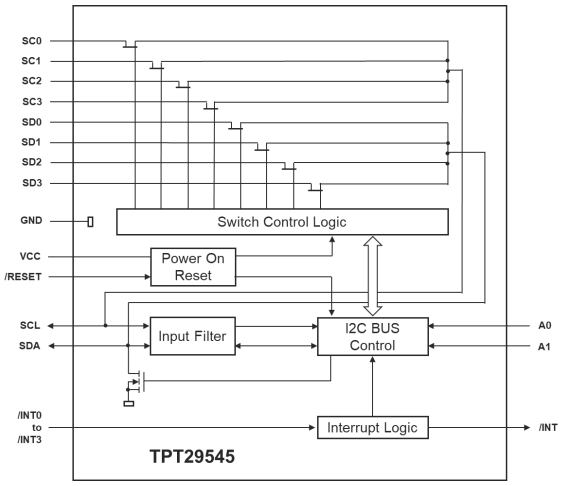
Features

- Bidirectional Translator of 1:4 I²C Switch
- Four Active-Low Interrupt Inputs
- Active-Low Interrupt Output and Active-Low Reset Input
- Two Address Terminals, Allowing up to Four Devices on the I²C Bus
- Operating Power-Supply Voltage Range of 2.3 to 5.5V
- Allow Voltage-Level Translation among 2.5V, 3.3V, and 5V Buses
- Support Standard Mode and Fast Mode I²C Devices，0 to 400 kHz Clock Frequency
- Low RON Switches
- Latch-Up Performance Exceeds 200 mA per JESD 78
- ESD Protection Exceeds JESD 22
  - ±4000V Human-Body Model
  - ±1500V Charged-Device Model

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products with I²C Slave Address Conflicts (e.g. Multiple, Identical Temp Sensors)

Typical Application Circuit



Description

The TPT29545 is a 1:4 bidirectional translating I²C switch. The SCL/SDA upstream pair fans out to four downstream channels. Any single SCn/SDn channel or combination of channels can be selected, determined by the programmable control register. Four interrupt inputs ($\overline{INT0}$ – $\overline{INT3}$), which are designed as one for each of the downstream pairs. One interrupt ($\overline{INT}$) output acts as an AND of the four interrupt inputs.

If one of the downstream I²C buses is stuck in a low state, then an active-low reset ($\overline{RESET}$) input helps the TPT29545 to recover. Pulling $\overline{RESET}$ low resets the I²C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the VCC terminal can be used to limit the maximum high voltage, which will be passed by the TPT29545. This allows the use of different bus voltages on each pair, so that 2.5V, or 3.3V parts can communicate with 5V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5 V tolerant.

TPT29545 is available in the TSSOP20 package, and is characterized from –40°C to +85°C.

Table of Contents

Revision History

Date	Revision	Notes
2020/03/04	Rev. Pre. 0	Initial Version
2021/06/29	Rev. Pre. 1	Preliminary version; added typical electrical data
2021/06/30	Rev. Pre. 2	Updated tape and reel information
2021/07/16	Rev. Pre. 3	Updated electrical data
2021/08/27	Rev. Pre. 4	Updated ordering information
2022/08/05	Rev A.0	Release version

Pin Configuration and Functions

TPT29545
TSSOP20 Package
Top View

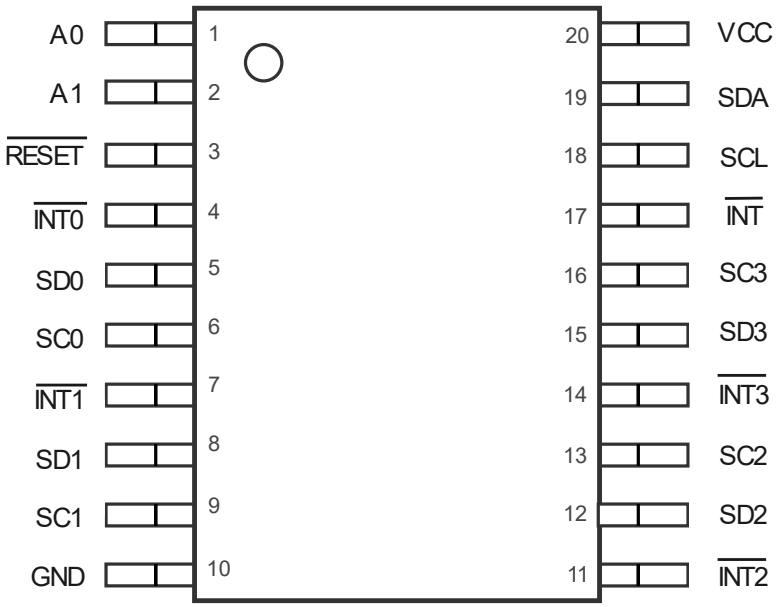


Table 1. Pin Functions: TPT29545

Pin	Name	I/O	Description
1	A0	Input	Address input 0. Connect directly to V_{CC} or ground.
2	A1	Input	Address input 1. Connect directly to V_{CC} or ground.
3	$\overline{RESET}$	Input	Active-low reset input. Connect to V_{CC} or V_{DPUM}(1) through a pull-up resistor if not used.
4	$\overline{INT0}$	Input	Active-low interrupt input 0. Connect to V_{DPU0}(1) through a pull-up resistor.
5	SD0	I/O	Serial data 0. Connect to the power of slave channel 0 through a pull-up resistor
6	SC0	I/O	Serial clock 0. Connect to the power of slave channel 0 through a pull-up resistor
7	$\overline{INT1}$	Input	Active-low interrupt input 1. Connect to V_{DPU1}(1) through a pull-up resistor.
8	SD1	I/O	Serial data 1. Connect to the power of slave channel 1 through a pull-up resistor
9	SC1	I/O	Serial clock 1. Connect to the power of slave channel 1 through a pull-up resistor
10	GND	GND	Ground

11	$\overline{INT2}$	Input	Active-low interrupt input 2. Connect to V_{DPU2}(1) through a pull-up resistor.
12	SD2	I/O	Serial data 2. Connect to the power of slave channel 0 through a pull-up resistor
13	SC2	I/O	Serial clock 2. Connect to the power of slave channel 0 through a pull-up resistor
14	$\overline{INT3}$	Input	Active-low interrupt input 3. Connect to V_{DPU3}(1) through a pull-up resistor.
15	SD3	I/O	Serial data 3. Connect to the power of slave channel 0 through a pull-up resistor
16	SC3	I/O	Serial clock 3. Connect to the power of slave channel 0 through a pull-up resistor
17	$\overline{INT}$	Output	Active-low interrupt output. Connect to V_{DPUM}(1) through a pull-up resistor.
18	SCL	I/O	Clock bus. Connect to V_{CC} through a pull-up resistor
19	SDA	I/O	Data bus. Connect to V_{CC} through a pull-up resistor
20	VCC	Supply	Supply power

Specifications

Absolute Maximum Ratings(1)

Parameters		Condition	Min	Max	Unit
V_{CC}	Supply Voltage		–0.5	7	V
V_I	Input Voltage		–0.5	7	V
I_{IK}	Input Clamp Current	$V_I < 0$		±20	mA
I_{OK}	Output Clamp Current	$V_O < 0$		±25	mA
I_{CC}	Continuous Current through GND			±100	mA
T_J	Maximum Junction Temperature			125	°C
T_A	Operating Temperature Range		–45	85	°C
Tstg	Storage Temperature		–60	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Recommended Operating Conditions

Parameters		Condition	Min	Max	Unit
V_{CC}	Supply Voltage		2.3	5.5	V
V_{IH}	High-level Input Voltage	SCL, SDA	0.7 × V_{CC}	5.5	V
		A1,A0, /RESET, /INTx	0.7 × V_{CC}	5.5	V
V_{IL}	Low-level Input Voltage	SCL, SDA	–0.5	0.3 × V_{CC}	mA
		A1,A0, /RESET, /INTx	–0.5	0.3 × V_{CC}	mA
T_A	Operating Temperature Range		-40	85	°C

ESD Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±1.5	kV

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP20	120	50	°C/W

Electrical Characteristics – DC Parameters

All test condition is VCC = 2.3V~3.6V, TA = -40 ~ +85°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply						
IDD	Supply Current in Operating Mode	VCC= 3.6 V; no load; V_I = VCC or GND; f_{SCL} = 100 kHz	-	2.4	20	uA
		VCC= 3.6 V; no load; V_I = VCC or GND; f_{SCL} = 400 kHz	-	6.5	30	uA
Istb	Standby Current	VCC = 3.6 V; no load; VI = VCC or GND	-	0.9	3.0	uA
V_{POR}	Power-on Reset Voltage, VCC rising	no load; VI = VCC or GND	-	1.2	1.45	V
	Power-on Reset Voltage, VCC falling		0.8	1.2		V
Input SCLx; Input/output SDAx						
VIL	Low-level Input Voltage	VCC=2.3V			0.3VCC	V
VIH	High-level Input Voltage	VCC=2.3V	0.7VCC			V
IOL	Low-level Output Current	VCC=2.3V, VOL = 0.4 V	3	10		mA
	Low-level Output Current, INT	VCC=2.3V, VOL = 0.6 V	6	13		mA
IL	Leakage Current	VCC=2.3V, VI = VCC or GND	-1	0.1	1	uA
C_i	Input Capacitance (1)	VI = GND		15		pF
Select Inputs A0,A1, /RESET						
VIL	Low-level Input Voltage	VCC=2.3V			0.3VCC	V
VIH	High-level Input Voltage	VCC=2.3V	0.7VCC			V
ILI	Input Leakage Current	VCC=2.3V, pin at VCC or GND	-1	0.1	1	uA
C_i	Input Capacitance (1)	VI = GND		3		pF
Pass Gate						
Ron	ON-state Resistance	VCC = 3.0 V to 3.6 V; VO = 0.4 V; IO = 15 mA	2	4.8	25	Ω
		VCC = 2.3 V to 2.7 V; VO = 0.4 V; IO = 10 mA	4	6.5	30	Ω
Vo(sw)	Switch Output Voltage (1)	Vi(sw) = VCC = 3.3 V; Io(sw) = -100 uA	-	2.1	-	V
		Vi(sw) = VCC = 3.0 V to 3.6 V; Io(sw) = -100 uA	1.6		2.8	V

(1) Parameters are provided by lab bench test and design simulation

Electrical Characteristics – DC Parameters (Continued)

All test condition is VCC = 2.3V~3.6V, TA = -40 ~ +85°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
		Vi(sw) = VCC = 2.5 V; Io(sw) = -100 uA	-	1.5	-	V
		Vi(sw) = VCC = 2.3 V to 2.7 V; Io(sw) = -100 uA	1.0		2.0	V
IL	Leakage Current	VI = VCC or GND	-1	0.1	1	uA
Cio	Input/output Capacitance(1)	VI = GND		3		pF
Output, /INT						
I_{OL}	Low-level Output Current	V_{OL} = 0.4 V	3			mA
I_{OH}	High-level Output Current				10	uA

(2) Parameters are provided by lab bench test and design simulation

Electrical Characteristics – DC Parameters (Continued)

All test condition is VCC = 4.5V~5.5V, TA = -40 ~ +85°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply						
IDD	Supply Current in Operating Mode	VCC= 5.5 V; no load; VI = VCC or GND; f_{SCL} = 100 kHz	-	5	20	uA
		VCC= 5.5 V; no load; VI = VCC or GND; f_{SCL} = 400 kHz		14	30	uA
Istb	Standby Current	VCC = 5.5 V; no load; VI = VCC or GND	-	1.8	3.0	uA
V_{POR}	Power-on Reset Voltage, VCC rising	no load; VI = VCC or GND	-	1.25	1.45	V
	Power-on Reset Voltage, VCC falling		0.8	1.2		V
Input SCL; Input/output SDA						
V_{IL}	Low-level Input Voltage (1)	VCC=5.5V			0.3VCC	V
V_{IH}	High-level Input Voltage	VCC=5.5V	0.7VCC			V
I_{OL}	Low-level Output Current	VCC=5.5V, VOL = 0.4 V	3	22		mA
	Low-level Output Current, INT	VCC=5.5V, VOL = 0.6 V	6	32		mA
I_L	Leakage Current	VI = VCC or GND	-1	0.1	1	uA
C_i	Input Capacitance (1)	VI = GND		15		pF

(1) Parameters are provided by lab bench test and design simulation

Electrical Characteristics – DC Parameters (Continued)

All test condition is VCC = 4.5V~5.5V, TA = -40 ~ +85°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Select inputs A0 to A2, /RESET, /INTx						
V_{IL}	Low-level Input Voltage	VCC=5.5V			0.3VCC	V
V_{IH}	High-level Input Voltage	VCC=5.5V	0.7VCC			V
I_{LI}	Input Leakage Current	pin at VCC or GND	-1	0.1	1	uA
C_i	Input Capacitance (1)	VI = GND		3		pF
Pass gate						
R_{on}	ON-state Resistance	VCC = 4.5 V to 5.5 V; VO = 0.4 V; IO = 15 mA	1	3.3	20	Ω
Vo(sw)	Switch Output Voltage (1)	Vi(sw) = VCC = 5.0 V; Io(sw) = -100 uA	-	3.55	-	V
		Vi(sw) = VCC = 4.5 V to 5.5 V; Io(sw) = -100 uA	2.6		4.5	V
I_L	Leakage Current	VI = VCC or GND	-1	0.1	1	uA
C_{io}	Input/output Capacitance (1)	VI = GND		3		pF
Output, /INT						
I_{OL}	Low-level Output Current	V_{OL} = 0.4 V	3			mA
I_{OH}	High-level Output Current				10	uA

(1) Parameters are provided by lab bench test and design simulation

Electrical Characteristics – AC Parameters

I²C Interface Timing Requirements

Over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Condition	Min	Max	Unit
I²C BUS—Fast Mode					
fscl	I²C Clock Frequency		0	400	kHz
tsch	I²C Clock High Time		0.6		μs
tscl	I²C Clock Low Time		1.3		μs
tsp	I²C Spike Time			50	ns
tsds	I²C Serial Data Setup Time		100		ns
tsdh	I²C Serial Data Hold Time		0		ns
ticr	I²C Input Rise Time		20	300	ns
ticf	I²C Input Fall Time		20+0.1Cb	300	ns
tocf	I²C Output Fall Time(1)	10-pF to 400-pF bus	20+0.1Cb	300	ns
tbuf	I²C bus free time between stop and start		1.3		μs
tsts	I²C start or repeated start condition setup		0.6		μs
tsth	I²C start or repeated start condition hold		0.6		μs
tsps	I²C Stop Condition Setup		0.6		μs
tvd(data)	Valid Data Time	SCL low to SDA output valid		0.9	μs
tvd(ack)	Valid Data Time of ACK Condition	ACK signal from SCL low to SDA (out) low		0.9	μs
tSP	pulse width of spikes that must be suppressed by the input filter			50	ns
t_{PD}	Propagation Delay (1)	from SDA to SDx, or SCL to SCx		0.3	ns
C_b	I²C Bus Capacitive Load			400	pF

(1) The propagation delay is calculated from the 20 typical Ron and the 15 pF load capacitance.

Switching Characteristics

Over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted)

Parameter		Condition	Min	Max	Unit
Tvd; DAT	Data Valid Time	HIGH to LOW		1	μs
		LOW to HIGH		0.55	μs
Tvd; DAT	Data Valid Time Acknowledge Time			1	ns
/RESET					
$t_{w(rst)L}$	Low-level Reset Time		4		ns
t_{rst}	Reset Time	SDA clear		500	ns
$t_{REC;STA}$	Recovery Time to START Condition		0		ns

(1) Parameters are provided by lab bench test and design simulation.

Parameter Measurement Waveforms

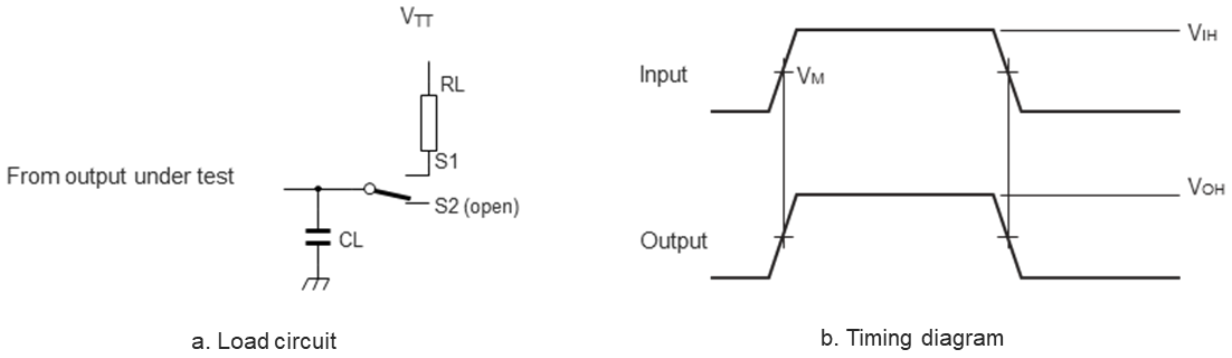


Figure 1. Load Circuit for Outputs

Detailed Description

Overview

The TPT29545 is a 1:4 bidirectional translating I²C switch. The SCL/SDA upstream pair fans out to four downstream channels. Any single SCn/SDn channel or combination of channels can be selected, determined by the programmable control register. Four interrupt inputs ($\overline{INT0}$–$\overline{INT3}$), which are designed as one for each of the downstream pairs. One interrupt ($\overline{INT}$) output acts as an AND of the four interrupt inputs.

If one of the downstream I²C buses is stuck in a low state, then an active-low reset ($\overline{RESET}$) input helps the TPT29545 to recover. Pulling $\overline{RESET}$ low resets the I²C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

Functional Block Diagram

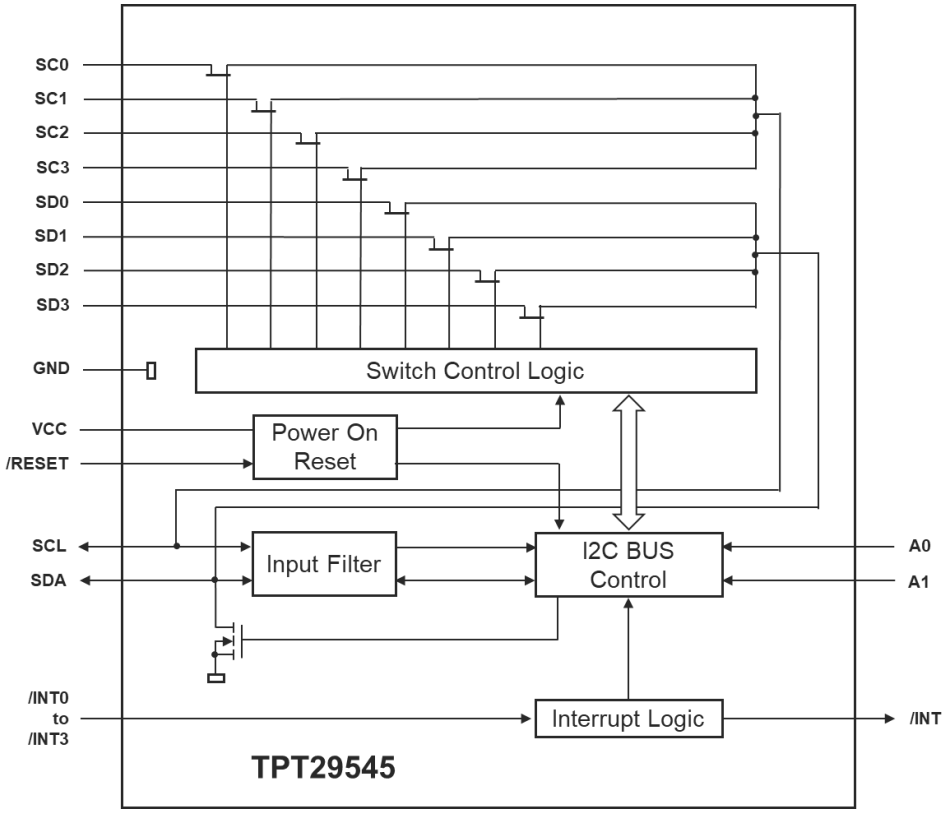


Figure 2. Functional Block Diagram

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

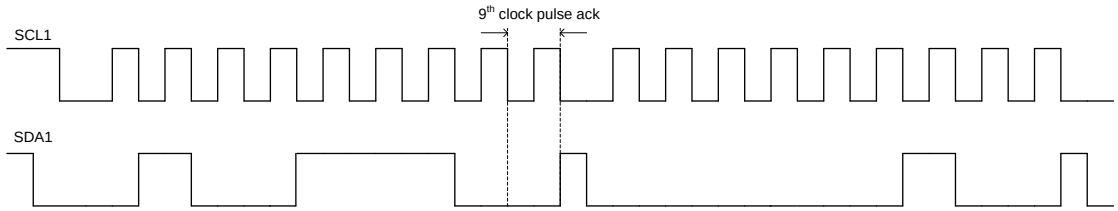


Figure 3. I²C BUS（2.3V~5.5V) Waveform

Device Address

Following a START condition, the bus master must output the address of the slave when it is accessing. To conserve power, no internal pull-up resistor is incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW. The address of the TPT29545 is shown below.

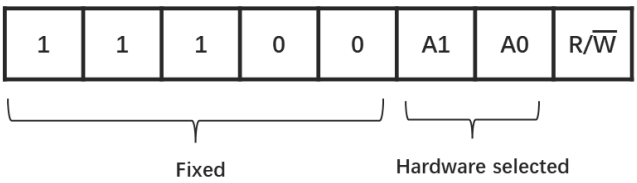


Figure 4. Slave Device Address

Control Register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the TPT29545, which will be stored in the control register. If multiple bytes are received by the TPT29545, it will save the last byte received. This register can be written and read via the I²C -bus.

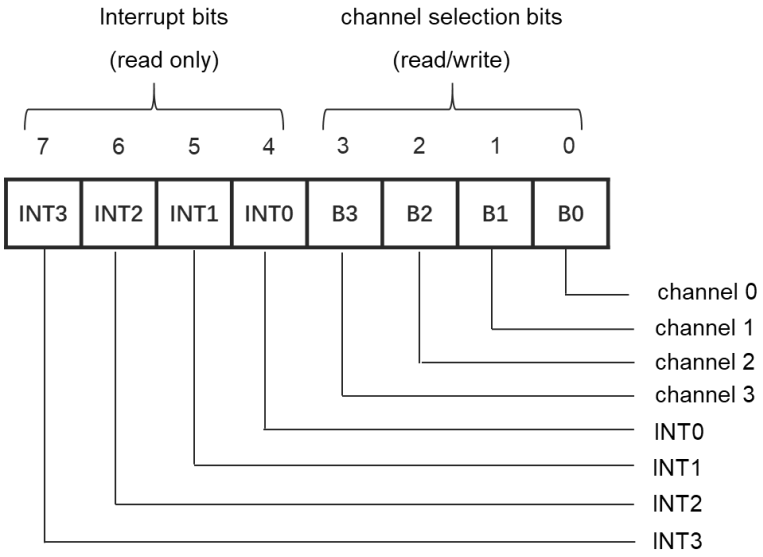


Figure 5. Control Register

Control Register Definition

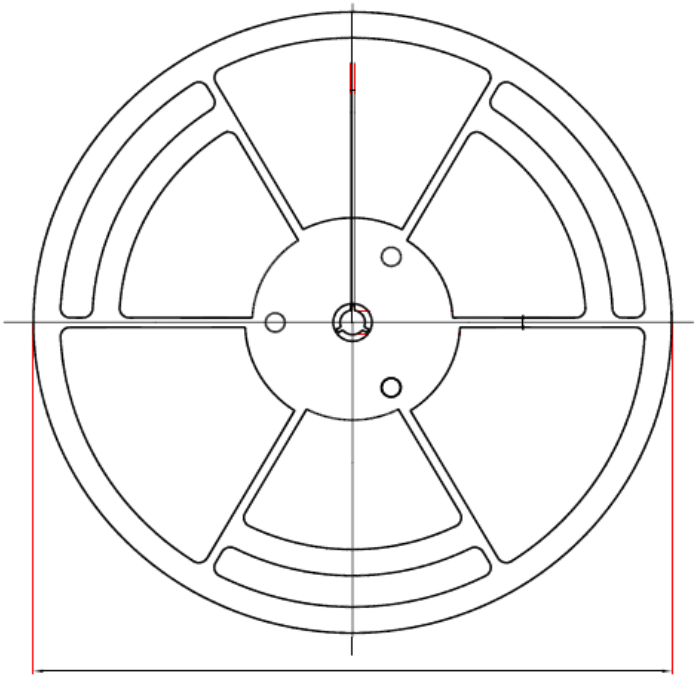
One or several SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the TPT29545. The 4 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a STOP condition has been placed on the I²C-bus. This ensures that all SCx/SDx lines are in a HIGH state when the channel is made active so that no false conditions are generated at the time of connection.

Control register: Write—channel selection; Read—channel status

B7	B6	B5	B4	B3	B2	B1	B0	Command
x	x	x	x	x	x	x	0	Channel 0 disable
x	x	x	x	x	x	x	1	Channel 0 enable
x	x	x	x	x	x	0	x	Channel 1 disable
x	x	x	x	x	x	1	x	Channel 1 enable
x	x	x	x	x	0	x	x	Channel 2 disable
x	x	x	x	x	1	x	x	Channel 2 enable
x	x	x	x	0	x	x	x	Channel 3 disable
x	x	x	x	1	x	x	x	Channel 3 enable
0	0	0	0	0	0	0	0	no channel selected; power-up/reset default state

Remark: Multiple channels can be enabled at the same time. Example: B3 = 0, B2 = 1, B1 = 1, B0 = 0, means that channel 0 and channel 3 are disabled and channel 1 and channel 2 are enabled. Care should be taken not to exceed the maximum bus capacitance.

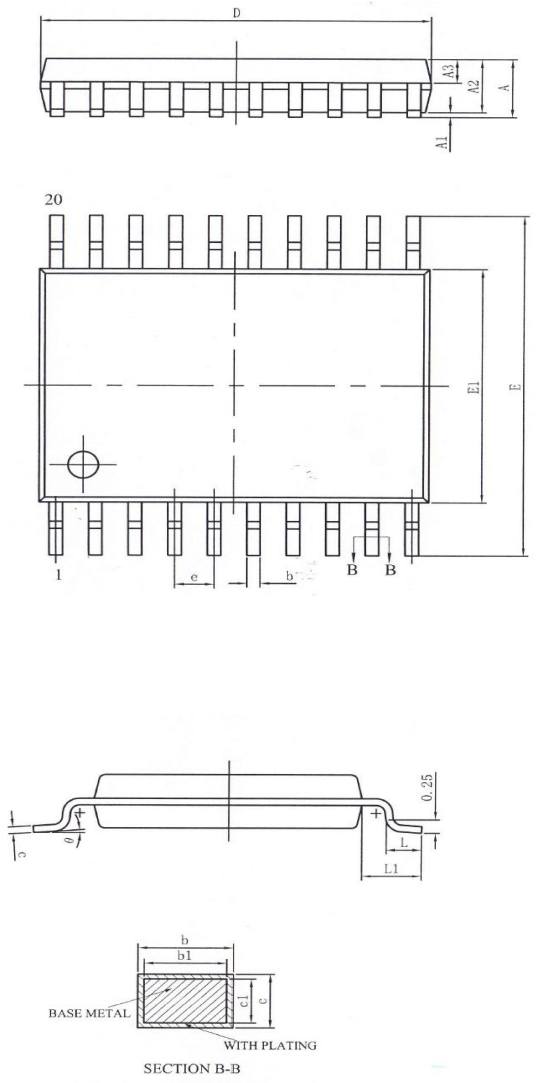
Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT29545-TS4R	TSSOP20	330	22.4	6.8	6.9	1.5	8.0	16.0	Q1

Package Outline Dimensions

TSSOP20



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0. 80	1. 00	1. 05
A3	0. 39	0. 44	0. 49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0. 45	0. 60	0. 75
L1	1.00BSC		
θ	0	—	8°

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29545-TS4R	-40 to 85°C	20-Pin TSSOP	29545	MSL3	3,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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