

Features

- Bidirectional Translator of I²C Applications and SMBus Compatible
- Support Fast-mode Plus, up to 1-Mbps Data Rate
- High-Impedance SCL1, SDA1, SCL2, and SDA2 Pins for EN = LOW
- 1-V Pre-Charge on All SDA and SCL Lines Prevents Corruption during Live Board Insertion
- Operating Power Supply Range from 2.3 V to 5.5 V
- Low I_{CC}Chip Shutdown Current: 0.3 μA (typ)
- Powered-Off High-Impedance I²C Pins
- Built-in ΔV/Δt Rise Time Accelerator
- ACK Error Protection to Avoid Direction Switching Error
- ESD Protection:
 - 7-kV Human-Body Model
 - 1.5-kV Charged-Device Model

Applications

- Servers/Storages
- Enterprise Switching
- Telecom Switching Equipment and Base Stations
- Industrial Automation Equipment

Description

The TPT29511B device is a dual bidirectional I²C and SMBus hot-swap buffer with an enable (EN) input, and works from 2.3 V to 5.5 V V_{CC}, which supports IO cards live insertion and removal from the backplane. The control circuit prevents the backplane-side I²C lines (in) from the other card-side I²C lines (out) until a stop command or bus idle condition occurs on the backplane without bus contention on the card. When the connection is made, the TPT29511B provides bidirectional buffering, keeping the backplane and card capacitances isolated.

The TPT29511B rise time accelerator circuitry allows the use of weaker DC pull-up currents while also meeting rise time requirements ($\Delta V/\Delta t > 0.6 \text{ V}/\mu\text{s}$).

The TPT29511B incorporates a digital enable input pin, which enables the device when asserted high and forces the device into a low current mode when asserted low, and an open-drain ready output pin, which indicates that the backplane and card sides are connected (high) or not (low).

TPT29511B is available in the MSOP8 package, and is characterized from -40°C to +125°C.

Functional Block Diagram

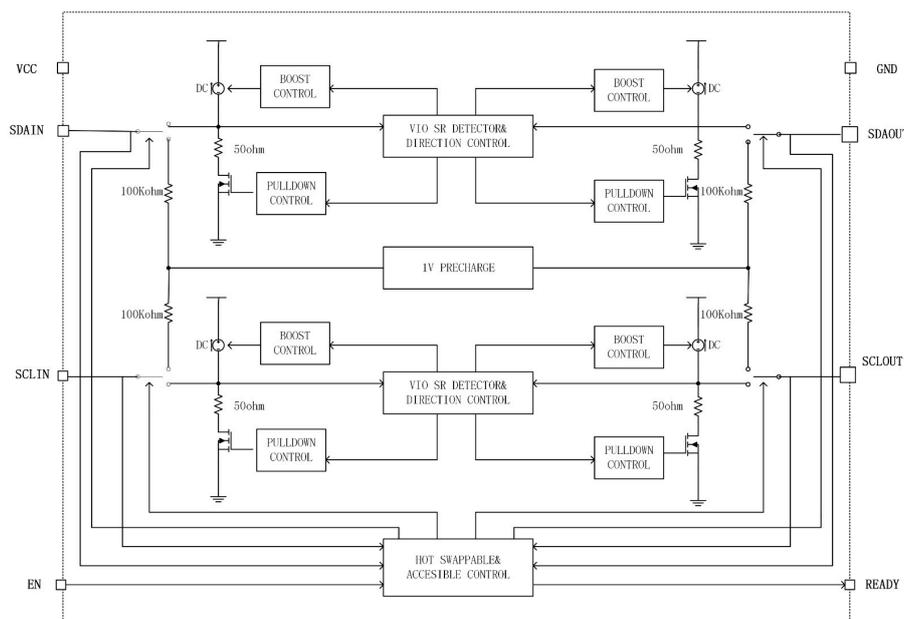


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Revision History

Date	Revision	Notes
2024-03-22	Rev.A.0	Released version

Pin Configuration and Functions

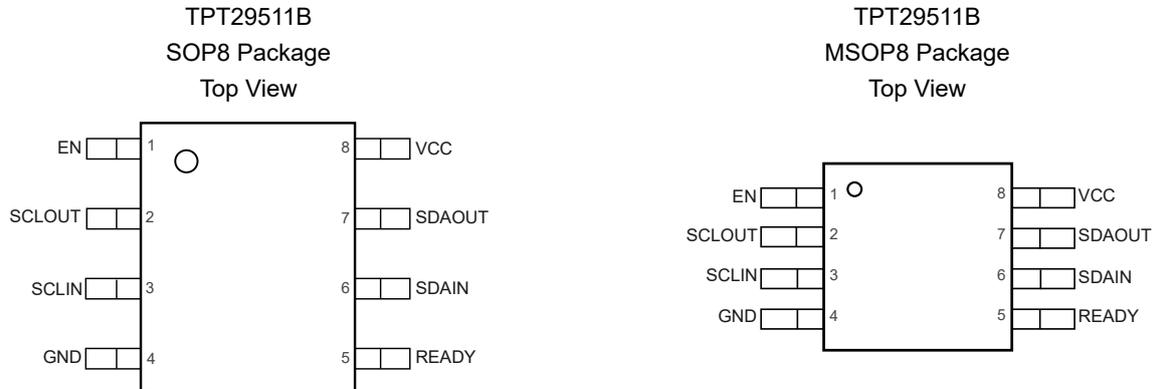


Table 1. Pin Functions: TPT29511B

Pin		I/O	Description
No.	Name		
1	EN	I	Active-high chip enable pin. If EN is low, the device is in a low current mode.
2	SCLOUT	I/O	Serial clock output to and from the SCL bus on the card
3	SCLIN	I/O	Serial clock input to and from the SCL bus on the backplane
4	GND	-	Ground.
5	READY	O	Open-drain output which pulls LOW when SDAIN and SCLIN are disconnected from SDAOUT and SCLOUT, and goes HIGH when the two sides are connected
6	SDAIN	I/O	Serial data input to and from the SDA bus on the backplane
7	SDAOUT	I/O	Serial data output to and from the SDA bus on the card
8	VCC	-	Power supply

Specifications

Absolute Maximum Ratings ⁽¹⁾

Parameter		Min	Max	Unit
V _{CC}	Power Supply	-0.5	+7	V
IO PIN	SDAIN, SCLIN, SDAOUT, SCLOUT, EN, READY	-0.5	+7	V
I _{IK}	Input Clamp Current		-50	mA
I _{OK}	Output Clamp Current		-50	mA
I _O	Continuous Output Current		±50	mA
I _{CC}	Continuous Current through VCC or GND		±100	mA
T _J	Maximum Junction Temperature		150	°C
T _{STG}	Storage Temperature Range	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) This data was taken with the JEDEC low effective thermal conductivity test board.

(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 ⁽²⁾	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter			Min	Max	Unit
V _{CC}	Supply Voltage		2.3	5.5	V
V _I	Input Voltage Range	EN input	0	5.5	V
V _{IO}	Input/output Voltage Range	SDAIN, SCLIN, SDAOUT, SCLOUT	0	5.5	V
V _O	Output Voltage Range	READY	0	5.5	V
T _A	Ambient Temperature		-40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP8	150	44	°C/W

Electrical Characteristics

All test conditions: $V_{CC} = 3.3\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply						
I_{CC}	Supply Current	$V_{CC} = 5.5\text{ V}$ SDAIN, SCLIN = 0 V SDAOUT, SCLOUT = 10k R_{PU}		4	6	mA
I_{SD}	Supply Current in Shutdown Mode through the V_{CC} Pin	EN = 0 V, SDAIN, SCLIN, SDAOUT, SCLOUT = 0 V or V_{CC} , READY pin = Hi-Z EN pulled low after bus connection event (disable pre-charge)		0.3	4	μA
$UVLO^{(1)}$	Under Voltage Lockout (rising)	EN = V_{CC}		2.15		V
	Under Voltage Lockout (falling)	READY = 10 k Ω to V_{CC}		2		
DC Electrical Characteristics						
V_{PRE}	Pre-charge Voltage	SDA, SCL = Hi-Z	0.8	1	1.2	V
I_{PU}	RTA pull-up Current ⁽¹⁾	Position transition on SDA, SCL $V_{SDA/SCL} > 0.8\text{ V}$, Slew rate = 1.25 V/ μs . $V_{CC} = 3.3\text{ V}$		5		mA
I_{LI}	Input Pin Leakage	SDA/SCL pins = V_{CC} , or 0 V, EN = 0 V	-1		1	μA
V_{OS}	Input-output Offset Voltage (SCLIN to SCLOUT, SCLOUT to SCLIN and SDAIN to SDAOUT, SDAOUT to SDAIN)	R_{PU} for SDA/SCL = 10 k Ω	50	105	175	mV
I_{I_RDY}	Ready Pin Leakage	EN = V_{CC} , READY = V_{CC} , Bus connected	-2		2	μA
V_{IH}	High-level Input Voltage		$0.7 \times V_{CC}$		V_{CC}	V
V_{IL}	Low-level Input Voltage	EN	0		$0.3 \times V_{CC}$	V
V_{OL_IO}	Low-level Output Voltage	SDAIN, SCLIN, SDAOUT, SCLOUT, $I_{OL} = 3\text{ mA}$, $V_{IN} = 0\text{ V}$		0.25	0.4	V
V_{OL_READY}	Low-level Output Voltage	Power on, READY = L, $I_{OL} = 3\text{ mA}$			0.4	V
		Power off, $R_{PU} = 10\text{ k}\Omega$ to 3.3 V		0.6	0.7	V
$C_{IN(EN)}$	EN input Capacitance ⁽¹⁾	$V_{EN} = 0\text{ V}$ or V_{CC} , $f = 400\text{ kHz}$		3		pF
$C_{IO(READY)}$	READY Output Capacitance ⁽¹⁾	$V_{READY} = 0\text{ V}$ or V_{CC} , $f = 400\text{ kHz}$		3		pF
$C_{IO(SDA/SCL)}$	SDA/SCL Pin Capacitance ⁽¹⁾	$V_{PIN} = 0\text{ V}$ or V_{CC} , $f = 400\text{ kHz}$		5		pF

(1) Test data based on bench test and design simulation; NOT test in production.

AC Electrical Characteristics

All test conditions: $V_{CC} = 3.3\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit	
Start-up Switching						
t_{EN}	Time from V_{POR} to Digital being Ready	V_{CC} transition from 0 V to V_{CC} , Time from V_{POR} to earliest stop bit recognized	50	105	200	μs
t_{IDLE}	Bus Idle Time to READY Active	SDA, SCL = 10 k Ω to V_{CC} EN = V_{CC} Measured at $0.5 \times V_{CC}$	50	100	200	μs
$t_{DISABLE}$	Time from EN High to Low to READY Low	SDA, SCL = 10 k Ω to V_{CC} READY = 10 k Ω to V_{CC} Measured at $0.5 \times V_{CC}$		25	200	ns
t_{STOP}	SDAIN to READY Delay after Stop Condition	SDA, SCL = 10 k Ω to V_{CC} READY = 10 k Ω to V_{CC} Measured at $0.5 \times V_{CC}$		1.2	2	μs
t_{READY}	SCLOUT/SDAOUT to READY	SDA, SCL = 10 k Ω to V_{CC} READY = 10 k Ω to V_{CC} Measured at $0.5 \times V_{CC}$		1.2	2	μs
t_{PLH}	Low to High Propagation Delay (1)	R_{PU} for SDA/SCL = 10 k Ω $C_L = 100\text{ pF}$ per pin Measured at $0.5 \times V_{CC}$		4.5	– (1)	ns
t_{PHL}	High to Low Propagation Delay	R_{PU} for SDA/SCL = 10 k Ω $C_L = 100\text{ pF}$ per pin Measured at $0.5 \times V_{CC}$		66	150	ns

(1) t_{PLH} typ data based on bench test and design simulation, the max value depends on the input source and cannot test in the FT.

AC Electrical Characteristics (continued)

All test conditions: $V_{CC} = 3.3\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted. ⁽¹⁾

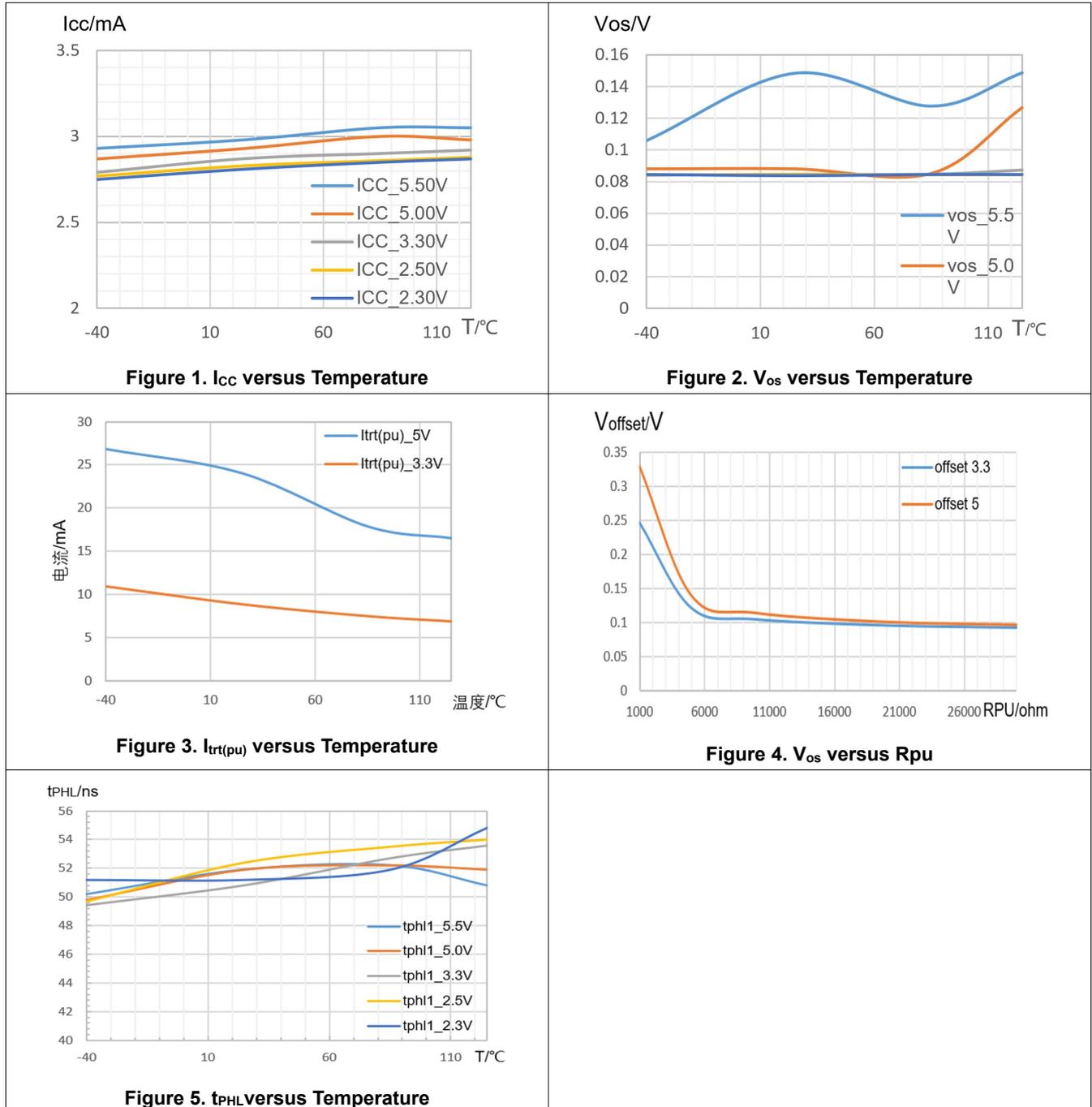
Parameter	Conditions	Min	Typ	Max	Unit
Timing characteristics (only reference to I²C 400 kHz) ⁽¹⁾					
f_{SCL_MAX}	Maximum SCL Clock Frequency ⁽¹⁾	400			kHz
t_{BUF}	Bus Free Time between a STOP and START Condition	1.3			μs
$t_{HD;STA}$	Hold Time for a Repeated START Condition	0.6			μs
$t_{SU;STA}$	Set-up Time for a Repeated START Condition	0.6			μs
$t_{SU;STO}$	Set-up Time for a STOP Condition	0.6			μs
$t_{HD;DAT}$	Data Hold Time	0			ns
$t_{SU;DAT}$	Data set-up Time	100			ns
t_{LOW}	LOW Period of the SCL Clock	1.3			μs
t_{HIGH}	HIGH Period of the SCL Clock	0.6			μs
t_F	Fall Time of both SDA and SCL Signals ⁽²⁾	5+ 0.1*Cb		300	ns
t_R	Rise Time of both SDA and SCL Signals ⁽²⁾	20 +0.1*Cb		300	ns

(1) All timing characteristics should reference to I²C standard @400 kHz, all parameters in table are NOT test in production.

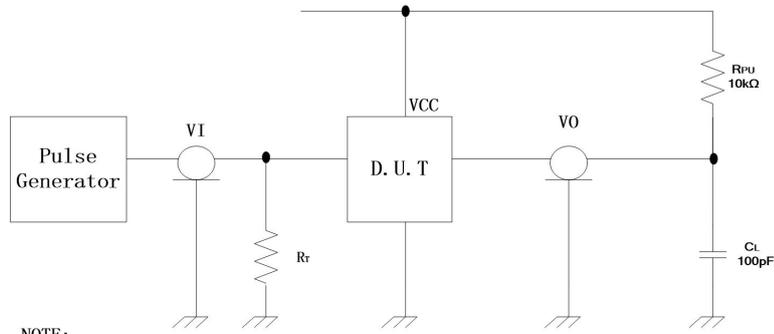
(2) t_F is 6 ns on bench test, and Cb is total capacitance of one bus line in pF.

Typical Performance Characteristics

All test conditions: $V_{IN} = 5V$, $V_A = +25^\circ C$, unless otherwise noted.



Test Circuitry



NOTE:
 R_{pu} is pull up resistor, C_l is load capacitance (includes jig and probe capacitance).
 R_r is terminations resistance (equal to the output impedance Z_o of the pulse generators.)

Figure 6. Test Circuitry of TPT29511B

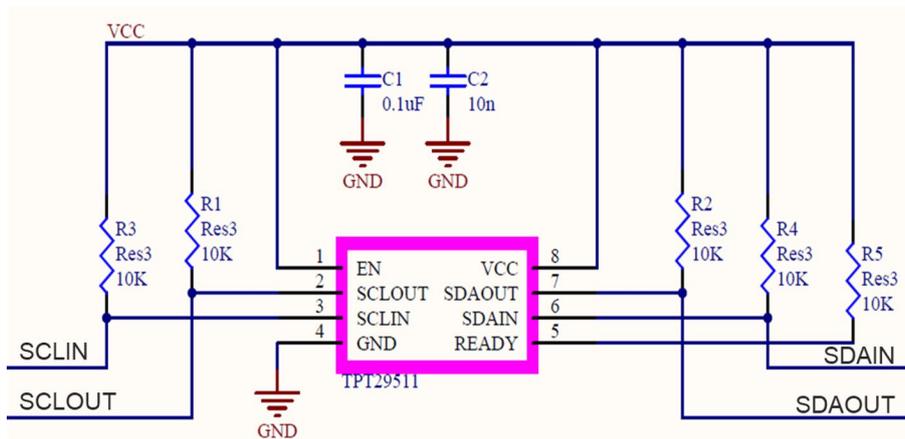


Figure 7. Reference Circuitry of TPT29511B

Test Timing Diagrams

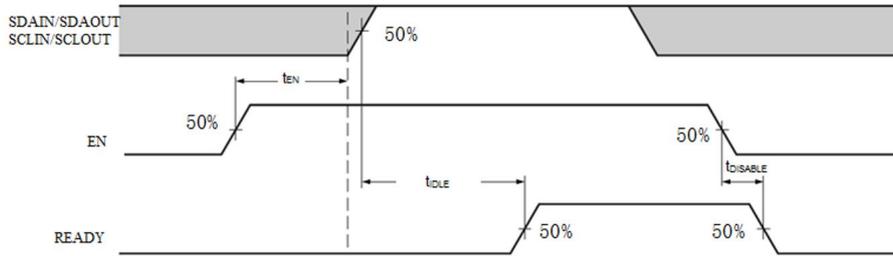
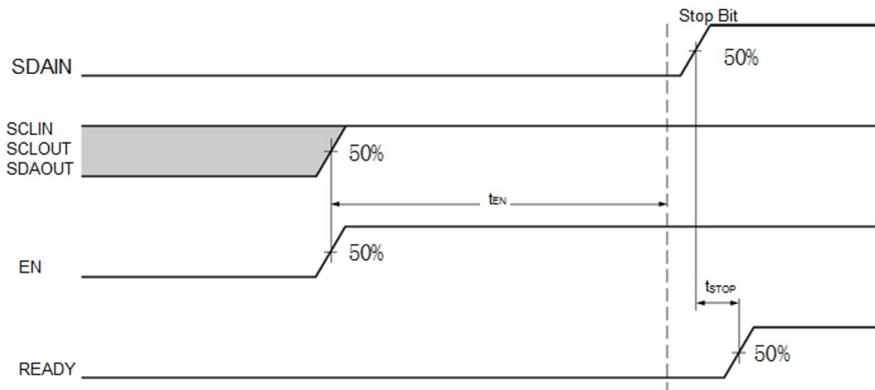
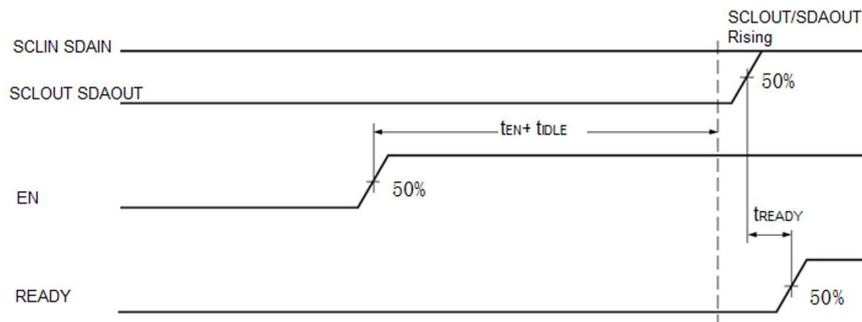


Figure 8. Timing for t_{EN} , t_{IDLE} , $t_{DISABLE}$



t_{STOP} is only available after t_{EN} delay.

Figure 9. Timing for t_{STOP}



t_{READY} is only available after $t_{EN}+t_{IDLE}$ delay.

Figure 10. Timing for t_{READY}

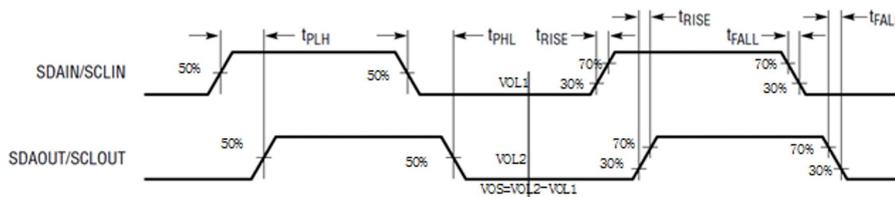


Figure 11. Timing for t_{PHL} , t_{PLH} , t_R , t_F , V_{OS}

Detailed Description

Overview

The TPT29511B device is a dual bidirectional I²C and SMBus Hot-swap buffer with an enable (EN) input, and works from 2.3 V to 5.5 V V_{CC}, which supports IO cards live insertion and removal from the backplane. The control circuit prevents the backplane-side I²C lines (in) from the other card-side I²C lines (out) until a stop command or bus idle condition occurs on the backplane without bus contention on the card. When the connection is made, the TPT29511B provides bidirectional buffering, keeping the backplane and card capacitances isolated.

The TPT29511B rise time accelerator circuitry allows the use of weaker DC pull-up currents while also meeting rise time requirements ($\Delta V/\Delta t > 0.6$ V/us).

The TPT29511B incorporates a digital enable input pin, which enables the device when asserted high and forces the device into a low current mode when asserted low, and an open-drain ready output pin, which indicates that the backplane and card sides are connected (high) or not (low).

Functional Block Diagram

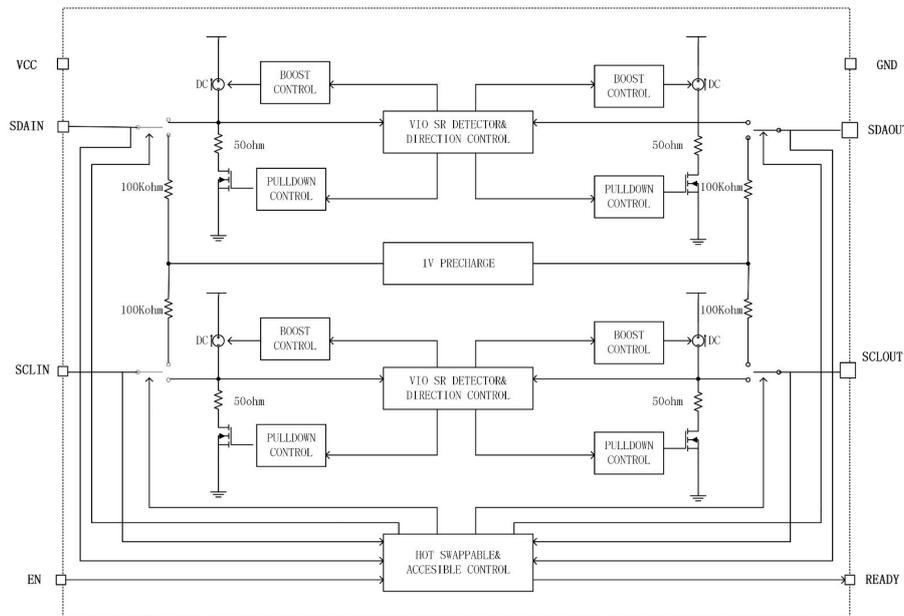


Figure 12. Functional Block Diagram

Feature Description

Enable (EN)

The device is in an active mode as pin EN is at high-voltage level. If EN is low, the device is in a low current mode.

Under-Voltage Lockout (UVLO)

The device uses an under-voltage lockout circuit to keep the device in shutdown mode until the supply voltage is higher than the UVLO threshold.

Over-Voltage Protection (OVP)

The device uses an over-voltage protection circuit to prevent the device from damage when the supply voltage is higher than the OVP threshold.

READY

The output pin will go HIGH to indicate that SDAIN and SCLIN are connected from SDAOUT and SCLOUT. And pull LOW when two sides are disconnected. The pin is driven by an open-drain pull-down capable of sinking 6 mA while holding 0.4 V on the pin. A 10-k Ω resistor is suggested connecting to VCC to provide the pull-up status.

Rise Time Accelerators

During positive bus transitions a 5-mA current source is switched on to quickly slew the SDA and SCL lines HIGH once the input level of 0.8 V for the TPT29511B is exceeded. The rising edge rate should be at least 0.6 V/ μ s to guarantee the accelerators turned on. The built-in $\Delta V/\Delta t$ rise time accelerators on all SDA and SCL lines requires the bus pull-up voltage and supply voltage (VCC) to be the same. If $\Delta V/\Delta t$ rise time accelerator < 0.2 V/ μ s, the time accelerators will stop to avoid the ack error.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPT29511B device is a dual bidirectional I²C and SMBus Hot-swap buffer, which supports IO cards live insertion and removal from backplane, such as the application in Servers/Storages and Enterprise Switching.

Typical Application

The following figures show the typical application schematics.

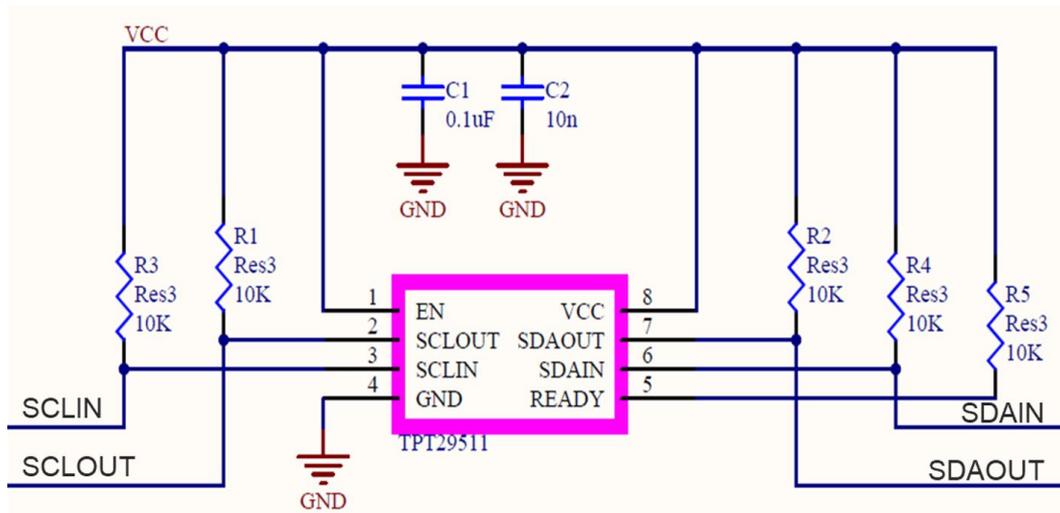


Figure 13. Reference Circuitry of TPT29511B

Layout

Layout Example

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they will have to turn corners. Figure 14 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

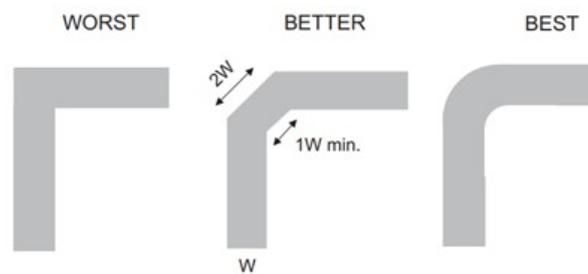
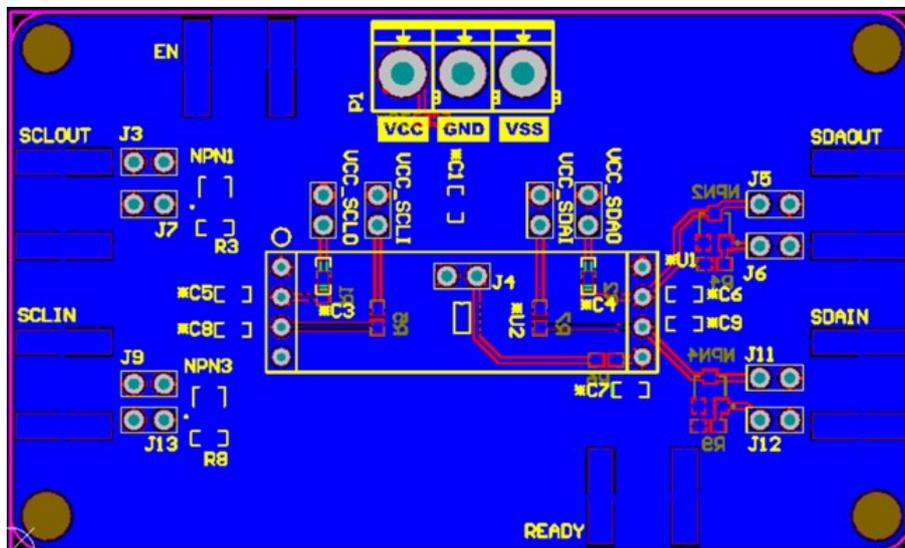
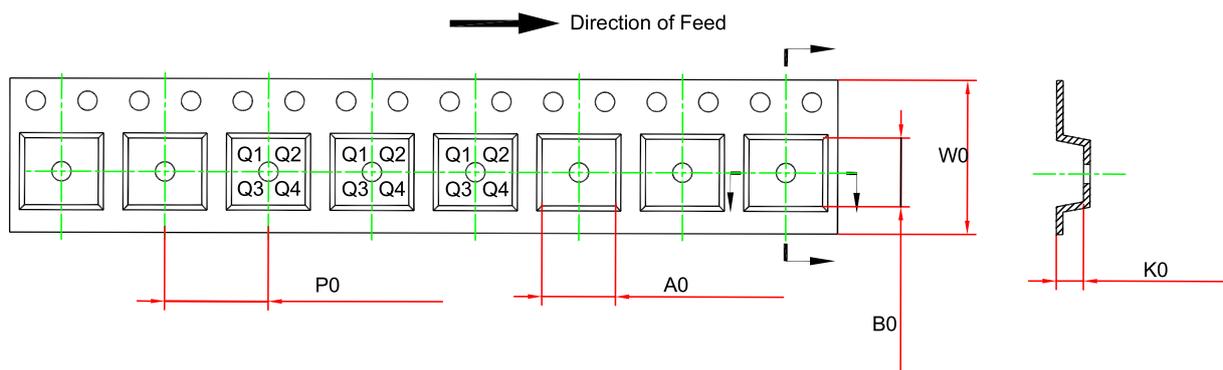
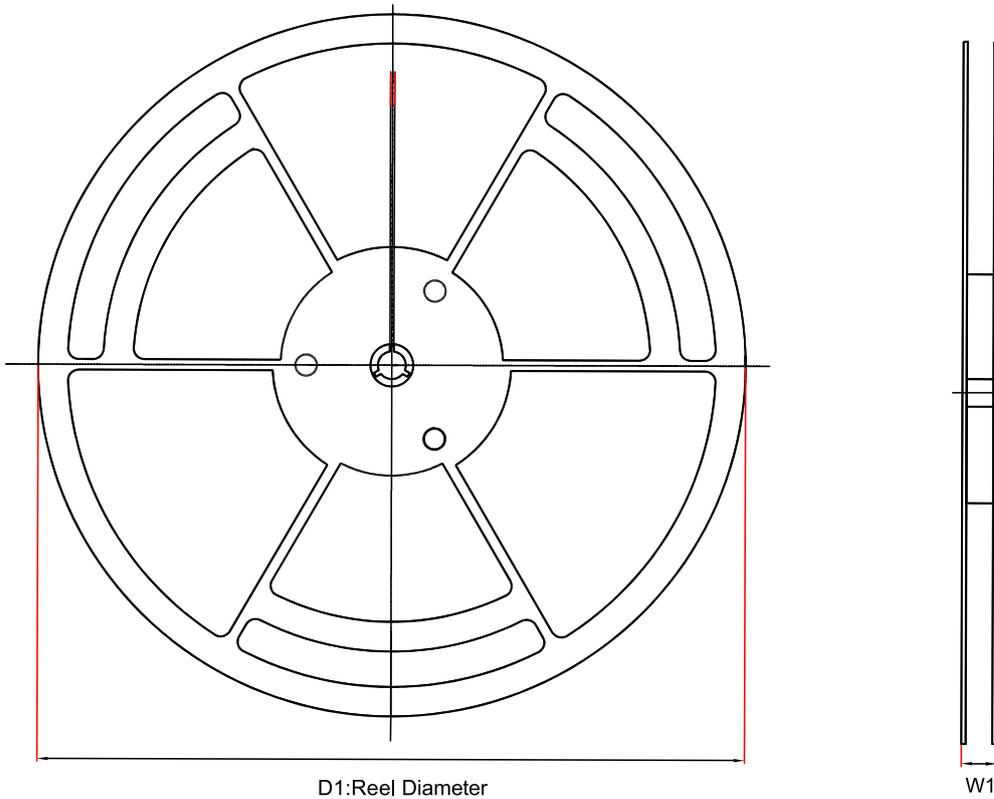


Figure 14. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.



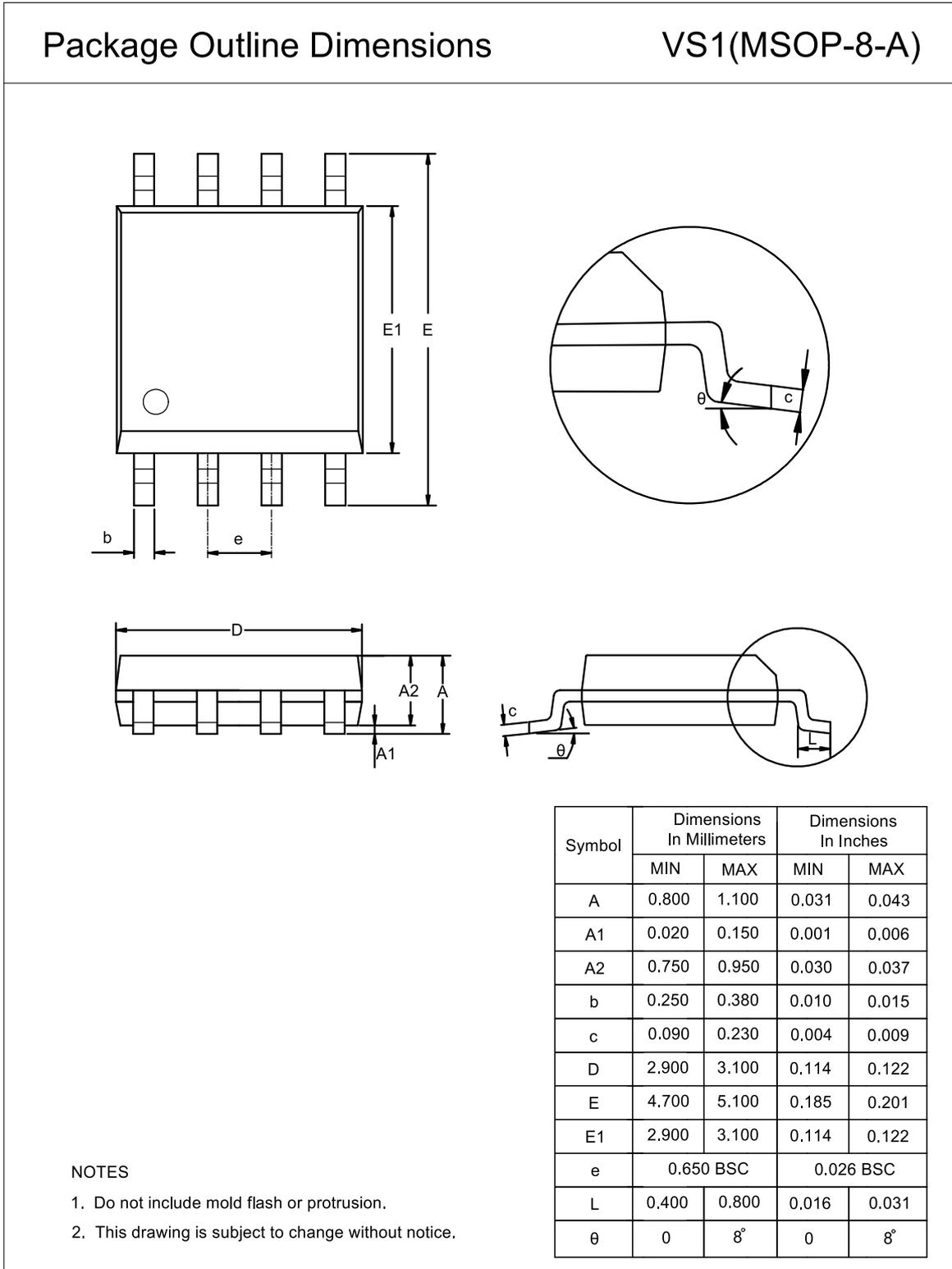
Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT29511B-VS1R	MSOP8	330.0	17.6	5.4	3.3	1.3	8.0	12.0	Q1

Package Outline Dimensions

MSOP8



Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29511B-VS1R	-40 to 125°C	MSOP8	9511B	MSL3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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