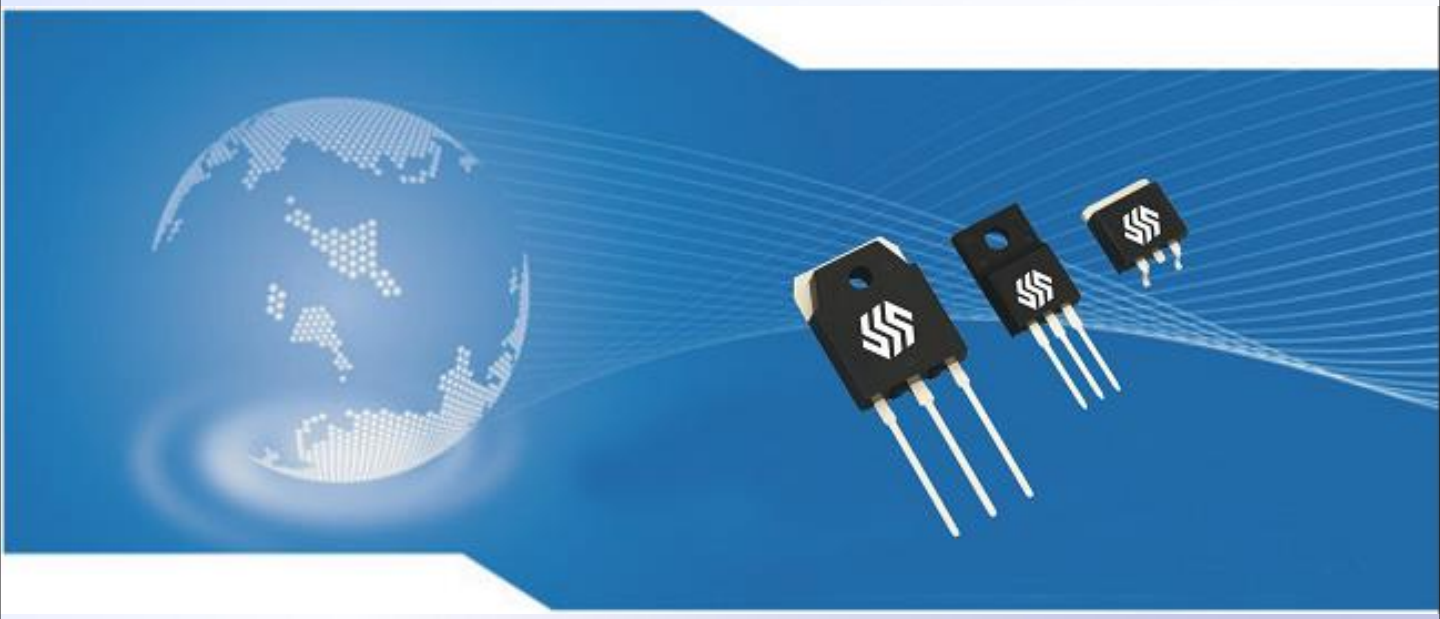
SUPER-SEMI



SUPER-MOSFET

Super Junction Metal Oxide Semiconductor Field Effect Transistor

650V Super Junction Power MOSFET Gen-Ⅱ
SS*65R600S2

Rev. 1.2
Jun. 2022

www.supersemi.com.cn

SSF65R600S2/SSP65R600S2/SSB65R600S2
650V N-Channel Super-Junction MOSFET Gen-Ⅱ

Description

SJ-FET is new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.
This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy.
SJ-FET is suitable for various AC/DC power conversion in switching mode operation for higher efficiency.

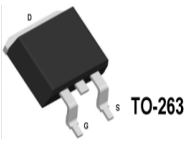
Features

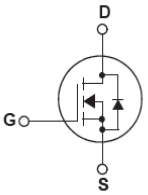
- Multi-Epi process SJ-FET
- 700V @TJ = 150 ℃
- Typ. RDS(on) = 0.54Ω
- Ultra Low Gate Charge (typ. Qg = 11.8nC)
- 100% avalanche tested

SSF65R600S2

SSP65R600S2

SSB65R600S2





Absolute Maximum Ratings

Symbol	Parameter	SSP_B65R600S2	SSF65R600S2	Unit
V_{DSS}	Drain-Source Voltage	650		V
I_D	Drain Current -Continuous (TC = 25℃) -Continuous (TC = 100℃)	8* 5*		A
I_{DM}	Drain Current - Pulsed (Note 1)	32		A
V_{GSS}	Gate-Source voltage	±30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	240		mJ
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max)	4		A
dv/dt	Peak Diode Recovery dv/dt (Note 3)	15		V/ns
dVds/dt	Drain Source voltage slope (Vds=480V)	50		V/ns
P_D	Power Dissipation (TC = 25℃)	80	30	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		℃
T_L	Maximum Lead Temperature for Soldering Purpose, 1/16” from Case for 10 Seconds	260		℃

* Drain current limited by maximum junction temperature. Maximum duty cycle D=0.75.

Thermal Characteristics

Symbol	Parameter	SSP_B65R600S2	SSF65R600S2	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.55	4.2	℃/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	-	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	80	℃/W

Electrical Characteristics TC = 25℃ unless otherwise noted

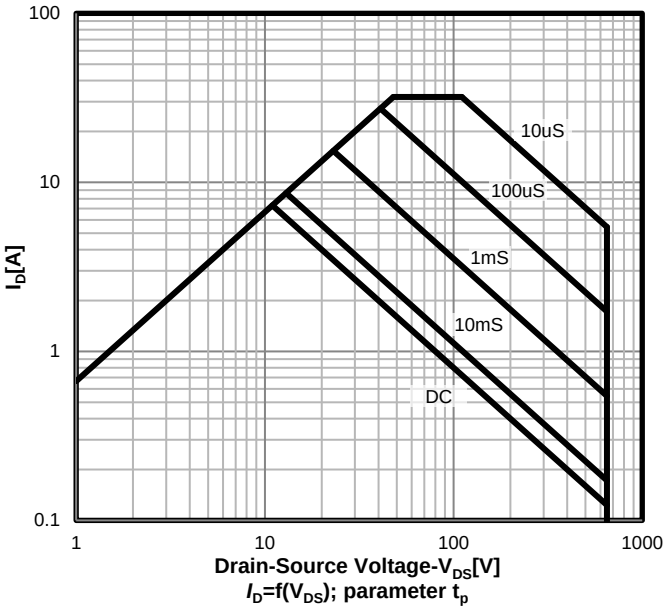
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA, T_J = 25℃	650	-	-	V
		V_{GS} = 0V, I_D = 250μA, T_J = 150℃	700	-	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25℃	-	0.6	-	V/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650V, V_{GS} = 0V -T_J = 125℃	-	-	1 100	μA μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30V, V_{DS} = 0V	-	-	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30V, V_{DS} = 0V	-	-	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0	3.0	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10V, I_D = 4A	-	0.54	0.6	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1.0MHz	-	480	-	pF
C_{oss}	Output Capacitance		-	36	-	pF
C_{rss}	Reverse Transfer Capacitance		-	2.3	-	pF
Q_g	Total Gate Charge	V_{DS} = 400V, I_D = 4A, V_{GS} = 10V (Note 4)	-	11.8	-	nC
Q_{gs}	Gate-Source Charge		-	2.4	-	nC
Q_{gd}	Gate-Drain Charge		-	4.7	-	nC
$V_{plateau}$	Gate plateau voltage		-	4.8	-	V
Rg	Gate resistance	f=1 MHz, open drain	-	26	-	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 400V, I_D = 8A, R_G = 25Ω, V_{GS} = 10V (Note 4)	-	17	-	ns
t_r	Turn-On Rise Time		-	26	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	53	-	ns
t_f	Turn-Off Fall Time		-	38	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		-	-	8	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		-	-	32	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0V, I_S = 8A	-	0.9	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, V_{DS} = 400V, I_S = 4A, dI_F/dt =100A/μs	-	240	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.5	-	μC
Irrm	Peak Reverse Recovery Current		-	13.5	-	A

NOTES:

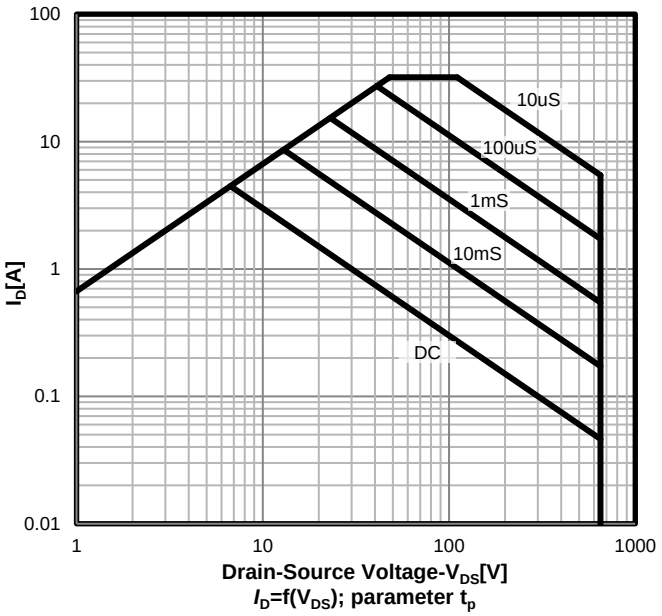
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. ID=I_{AS}, VDD=50V, L=30mH, Starting TJ=25 ℃
3. I_{SD}≤ID, di/dt ≤ 200A/us, V_{DD} ≤ BV_{DSS}, Starting TJ = 25 ℃
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

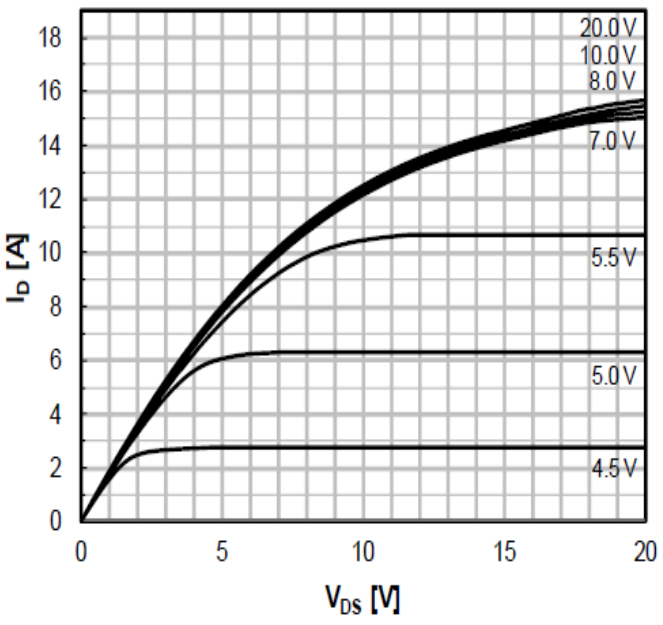
Safe operating area TC=25 ℃
TO-220,TO-263



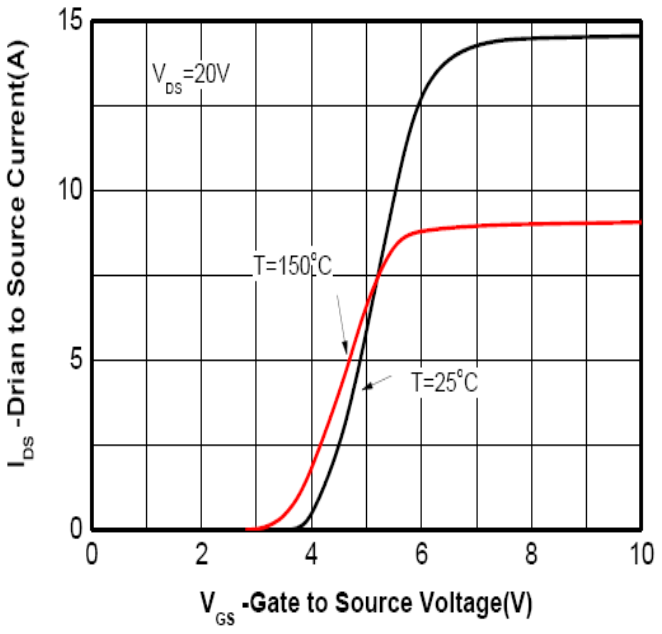
Safe operating area TC=25 ℃
TO-220FullPAK



Typ. output characteristics T_j=25 ℃

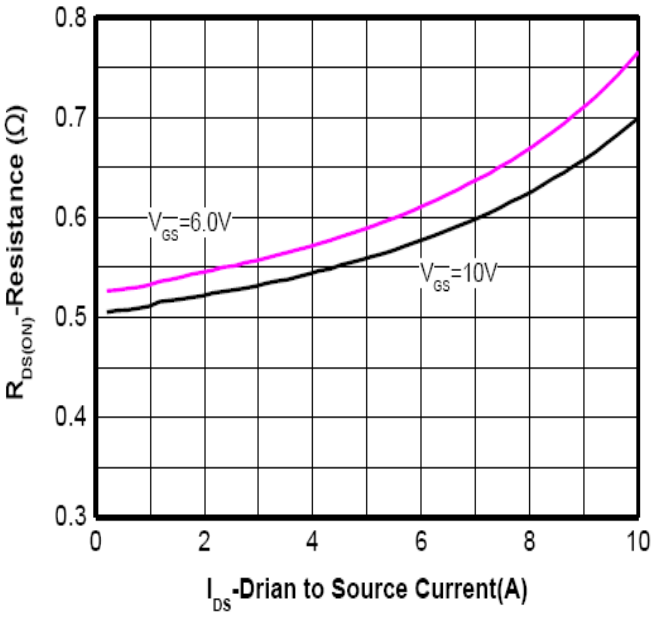


Typ. transfer characteristics

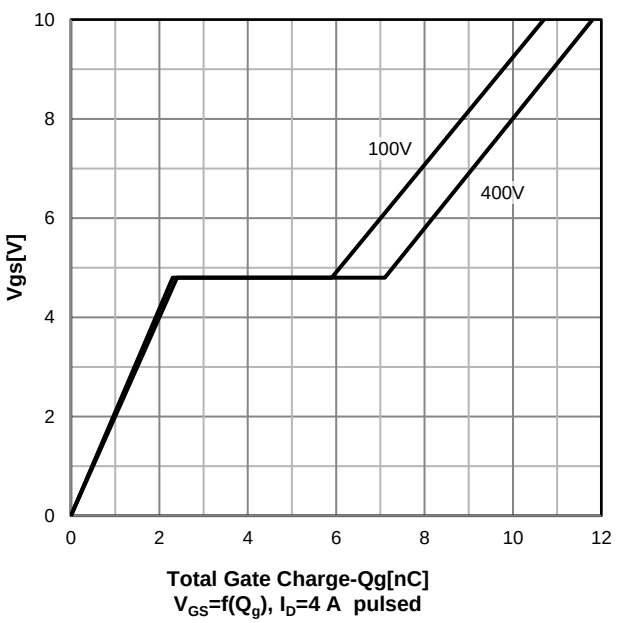


Typical Performance Characteristics

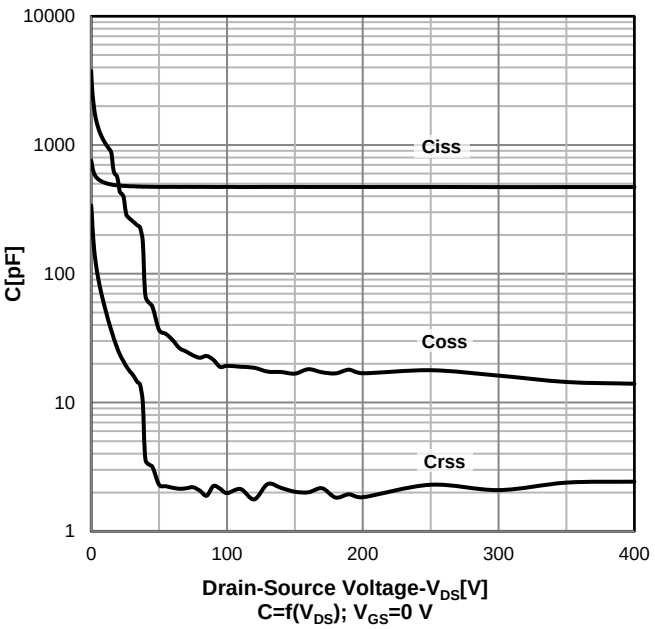
Typ. drain-source on-state resistance



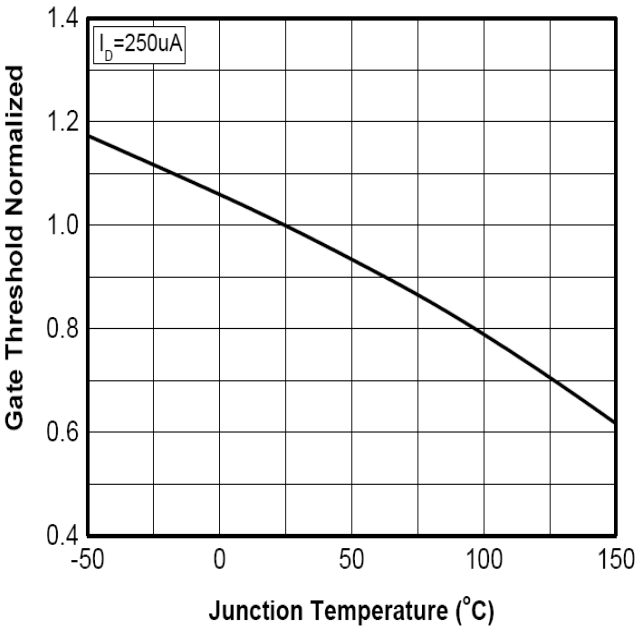
Typ. gate charge characteristics



Typ. capacitances

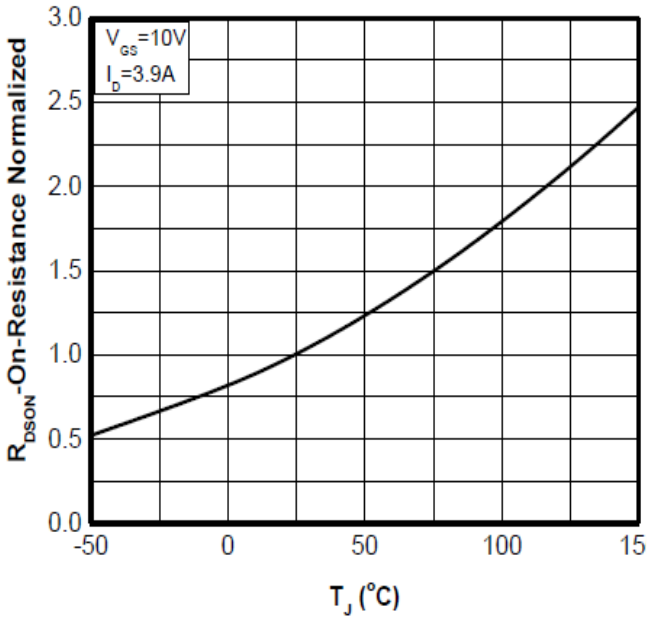


Normalized $V_{GS(th)}$ characteristics

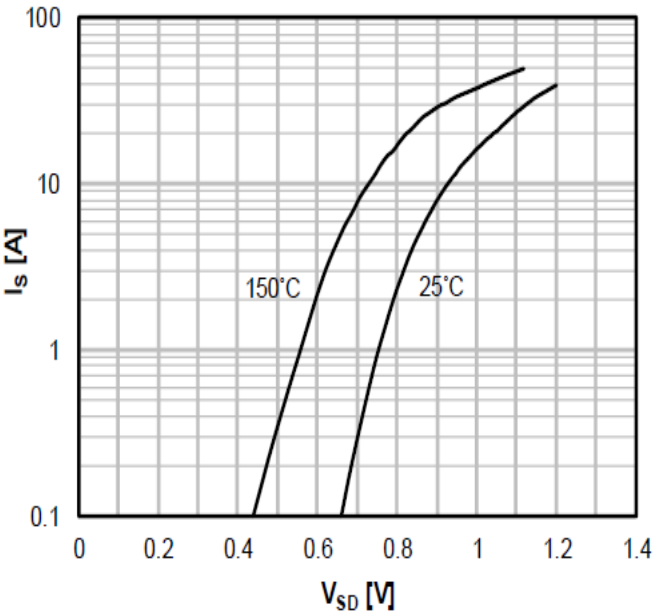


Typical Performance Characteristics

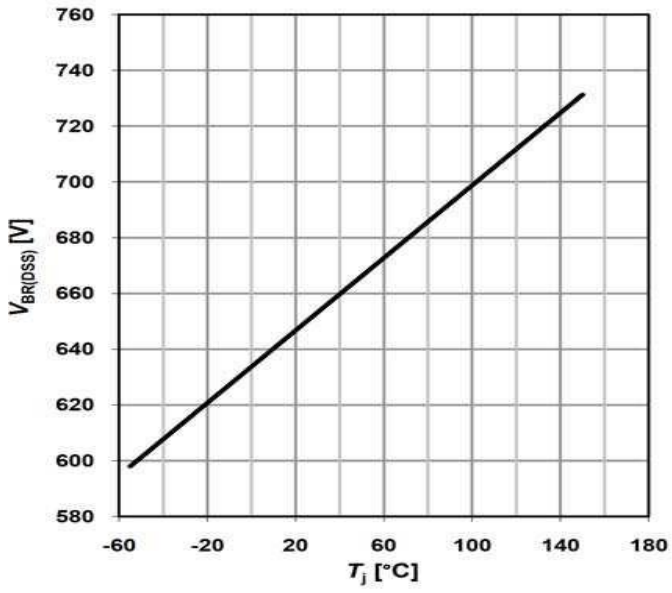
Normalized on-resistance vs temperature



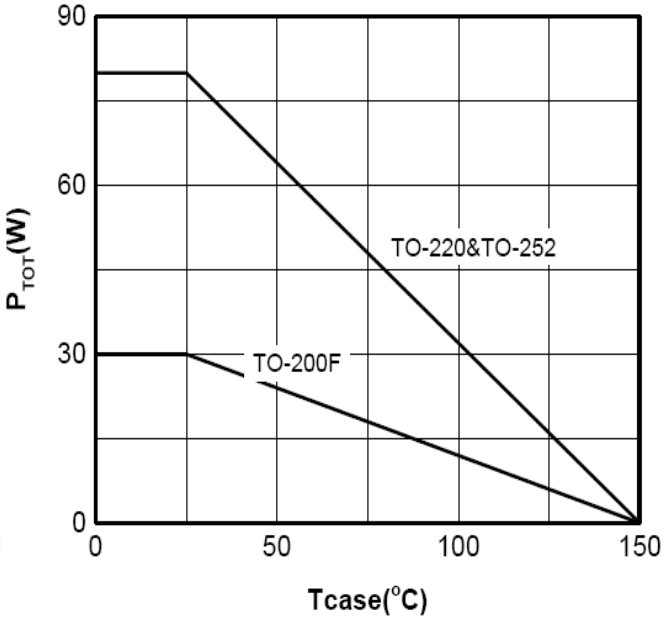
Forward characteristics of reverse diode



Drain-source breakdown voltage

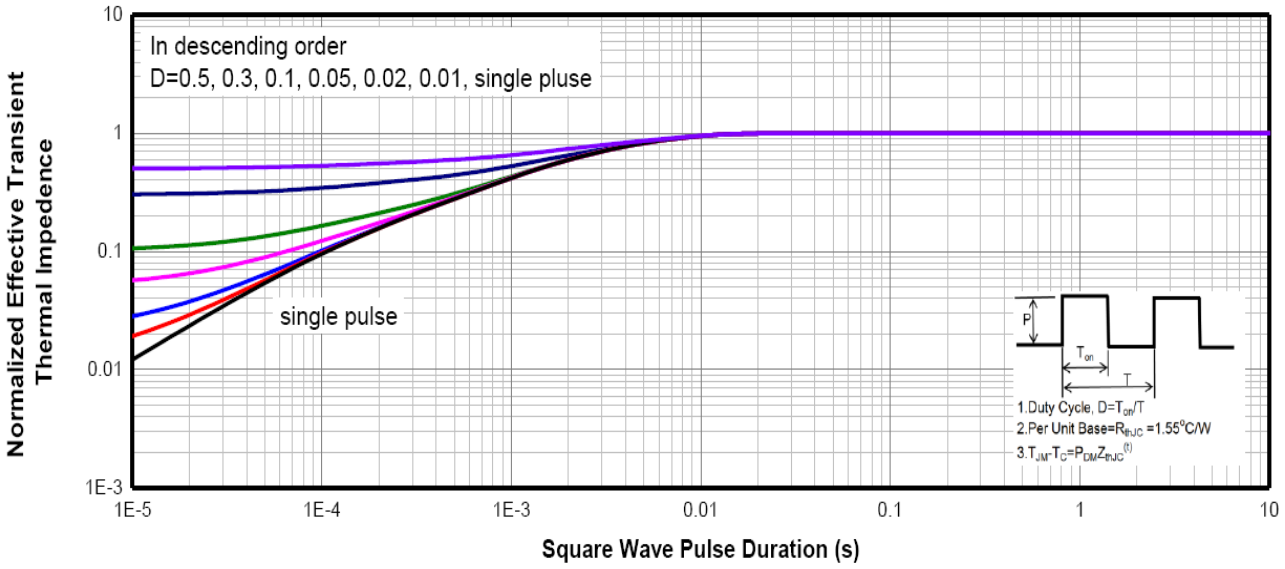


Power dissipation

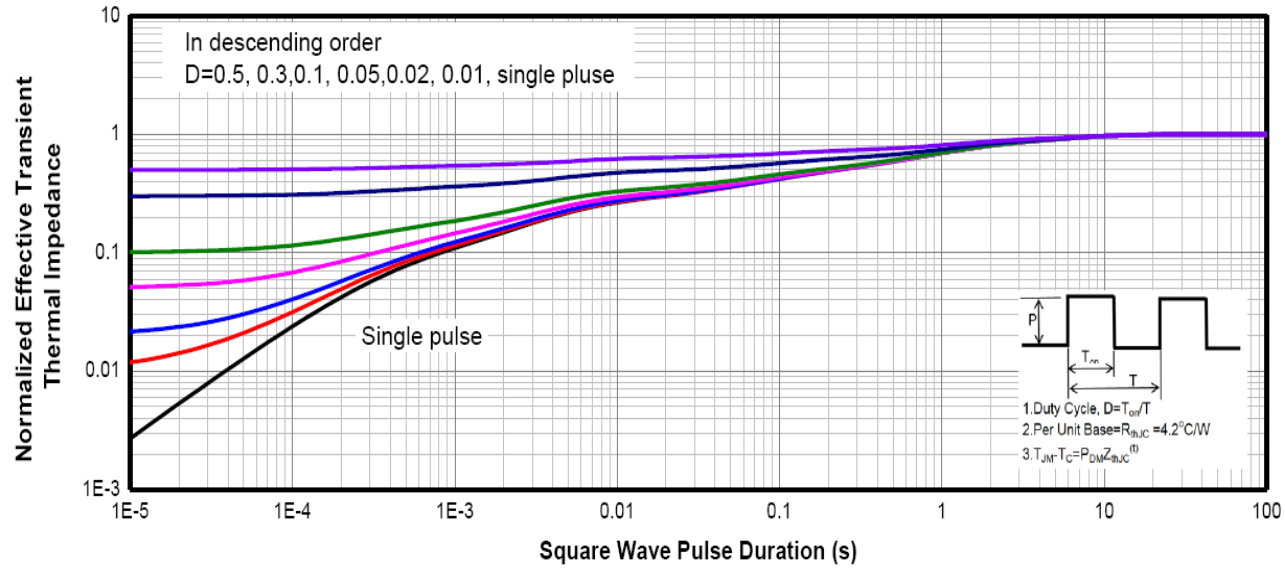


Typical Performance Characteristics

Max. transient thermal impedance
TO-220,TO-263

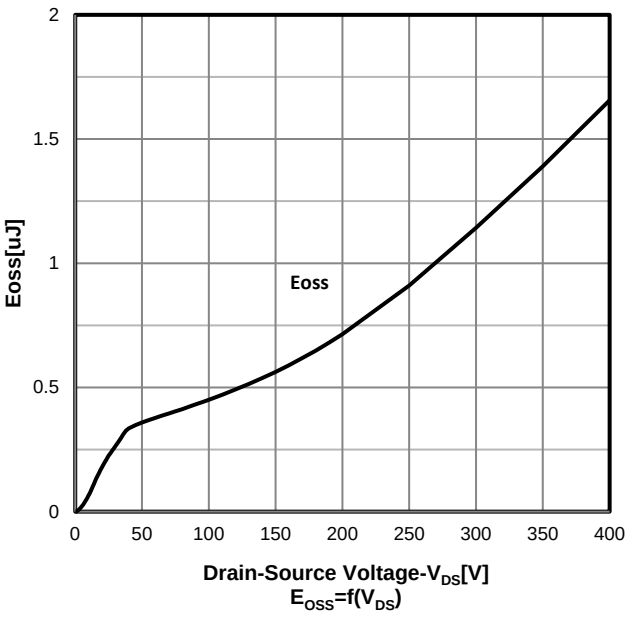


Max. transient thermal impedance
TO-220FullPAK



Typical Performance Characteristics

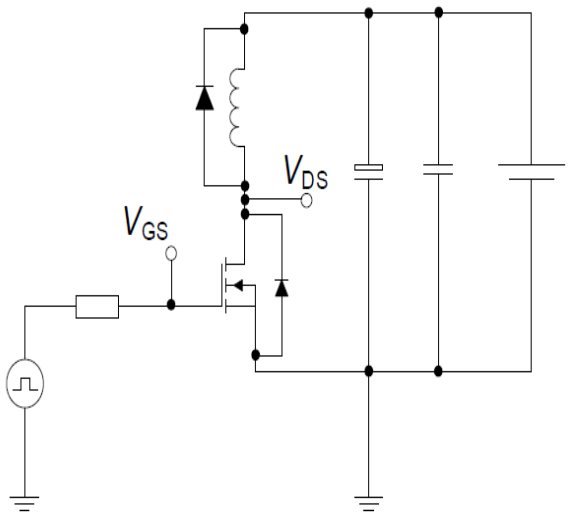
Coss stored energy



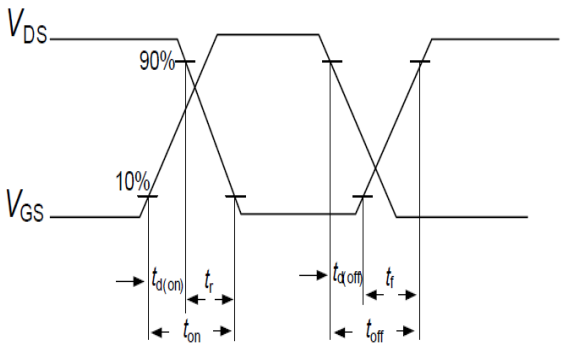
Test circuits

Switching times test circuit and waveform for inductive load

Switching times test circuit for inductive load

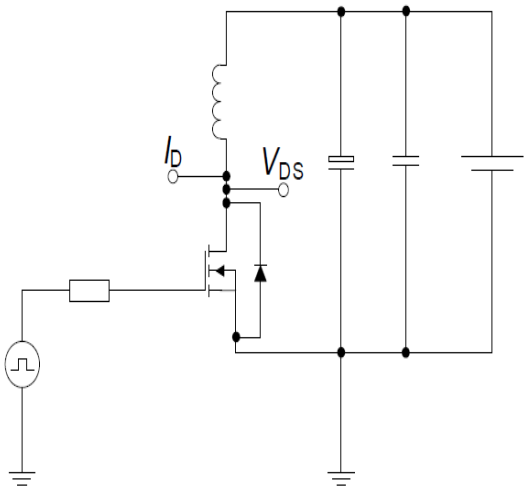


Switching time waveform

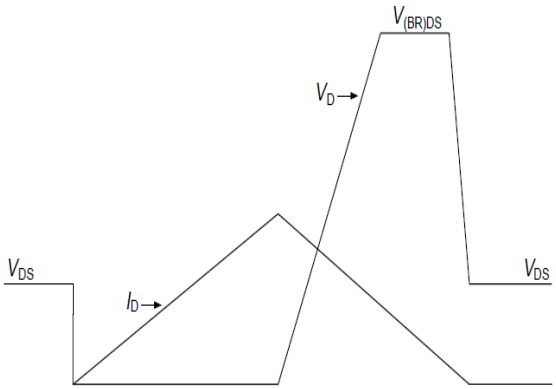


Unclamped inductive load test circuit and waveform

Unclamped inductive load test circuit



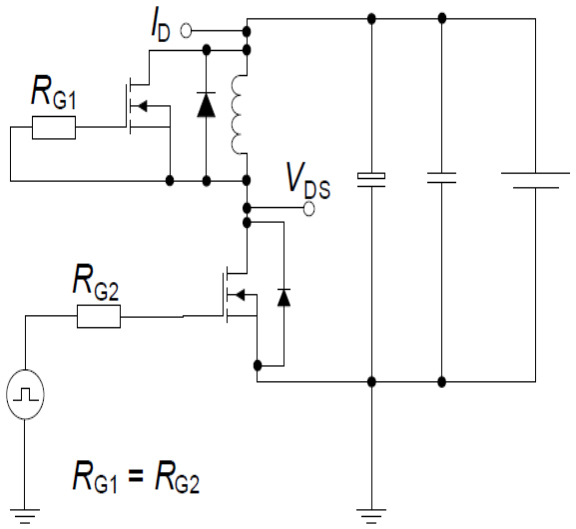
Unclamped inductive waveform



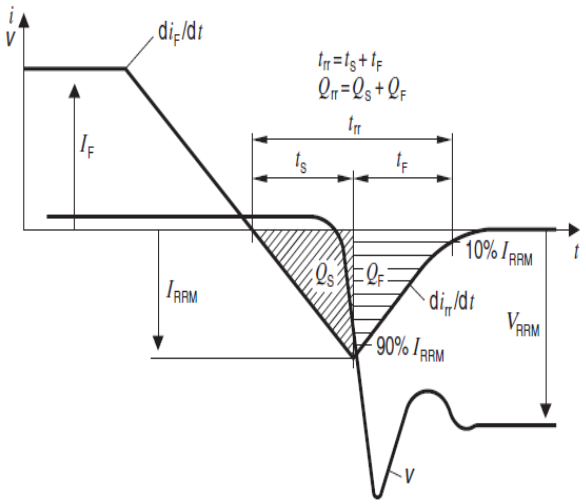
Test circuits

Test circuit and waveform for diode characteristics

Test circuit for diode characteristics

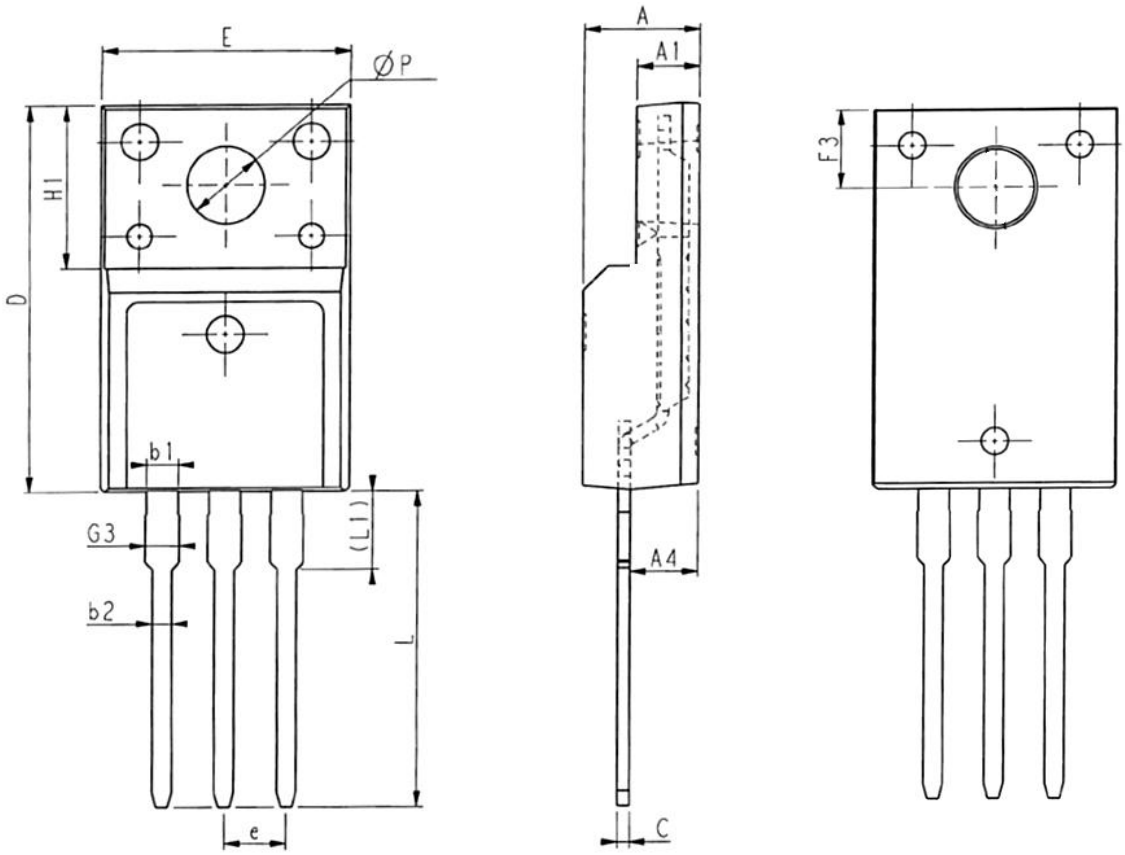


Diode recovery waveform



Package Outline

TO-220 Full PAK

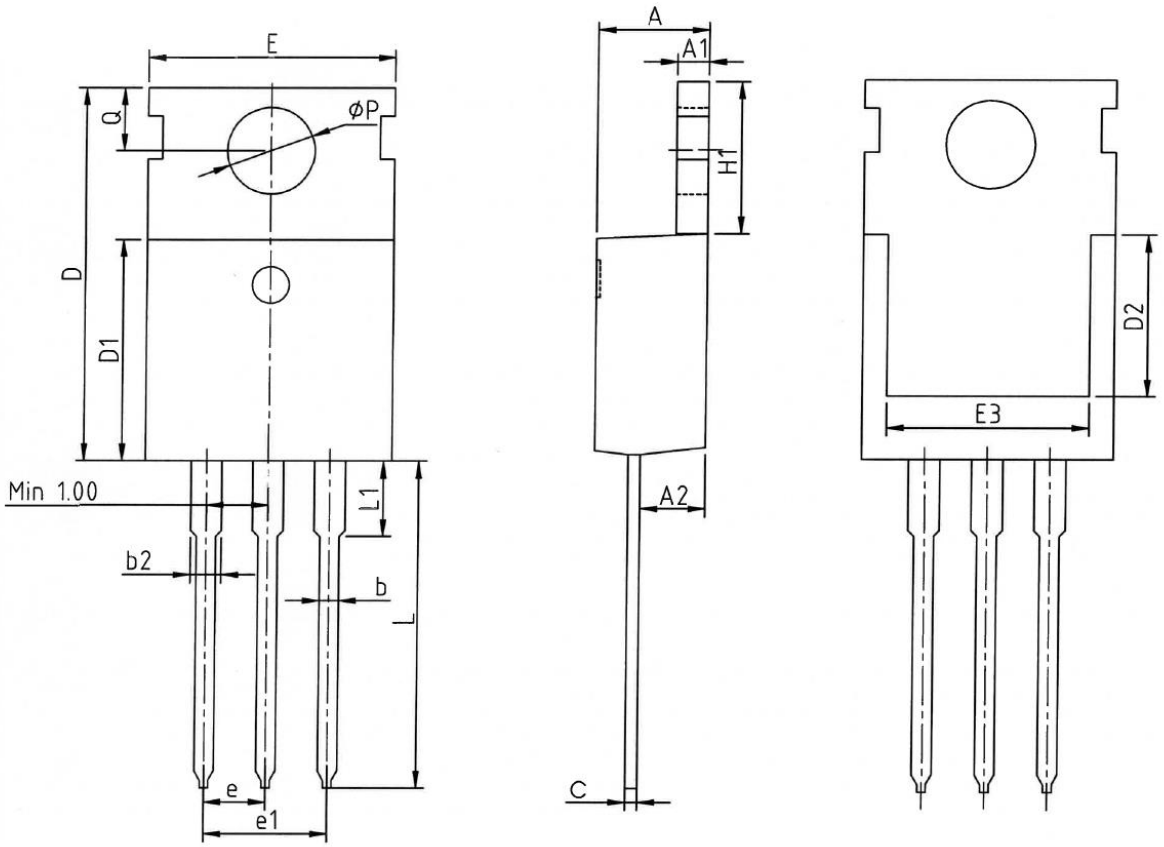


COMMON DIMENSIONS

SYMBOL	UNIT(mm)		
	MIN	NOM	MAX
E	9.86	10.16	10.36
A	4.50	4.70	4.90
A1	2.34	2.54	2.84
A4	2.56	2.76	2.96
C	0.35	0.50	0.65
D	15.50	15.87	16.25
H1	6.70REF		
e	2.54BSC		
L	12.60	12.98	13.35
L1	3.03	3.23	3.43
ΦP	3.00	3.20	3.40
F3	3.10	3.30	3.50
G3	1.20	1.35	1.60
b1	1.18	1.28	1.43
b2	0.70	0.80	0.95

Package Outline

TO-220

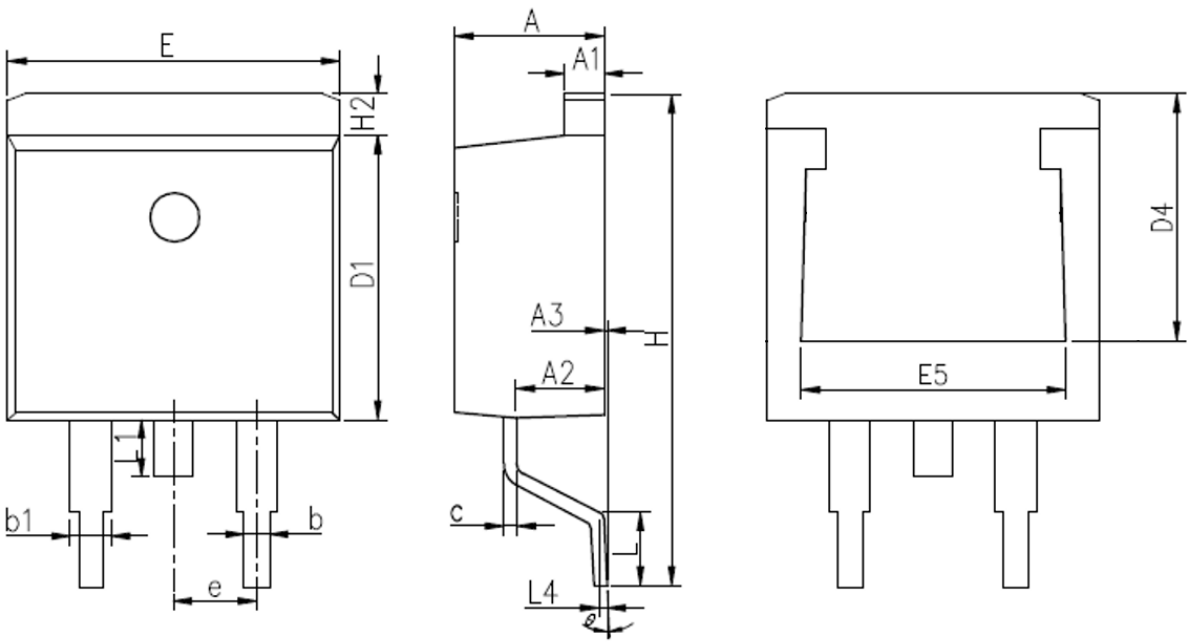


COMMON DIMENIONS

SYMBOL	MIN	NOM	MAX
A	4.37	4.57	4.70
A1	1.25	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	0.95
b2	1.17	1.27	1.47
c	0.45	0.50	0.60
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	6.30	7.10
E	9.70	10.00	10.30
E3	7.00	7.80	8.60
e		2.54 BSC	
e1		5.08 BSC	
H1	6.25	6.50	6.85
L	12.75	13.50	13.80
L1	-	3.10	3.40
ΦP	3.40	3.60	3.80
Q	2.60	2.80	3.00

Package Outline

TO-263



COMMON DIMENSIONS

SYMBOL	MM		
	MIN	NOM	MAX
A	4.37	4.57	4.77
A1	1.22	1.27	1.42
A2	2.49	2.69	2.89
A3	0.00	0.13	0.25
b	0.70	0.81	0.96
b1	1.17	1.27	1.47
c	0.30	0.38	0.53
D1	8.50	8.70	8.90
D4	6.60	-	-
E	9.86	10.16	10.36
E5	7.06	-	-
e		2.54 BSC	
H	14.70	15.10	15.50
H2	1.07	1.27	1.47
L	2.00	2.30	2.60
L1	1.40	1.55	1.70
L4		0.25 BSC	
θ	0°	5°	9°

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