Description

The P8803 provides a 4-channel low side driver with overcurrent protection. It has built-in diodes to clamp turnoff transients generated by inductive loads and can be used to drive unipolar stepper motors, DC motors, relays, solenoids, or other loads. In the SOIC (DW) package, the P8803 can supply up to 1.5-A (one channel on) or 800-mA (all channels on) continuous output current per channel, at 25°C. In the HTSSOP (PWP) package, it can supply up to 2-A (one channel on) or 1-A (four channels on) continuous output current per channel, at 25°C with proper PCB heat sinking.

The device is controlled through a simple parallel interface.

Internal shutdown functions are provided for over current protection, short circuit protection,Under voltage lockout and over temperature and faults are indicated by a fault output pin.

The P8803 is available in a 20-pin thermally-enhanced SOIC package and a 16-pin HTSSOP package (Eco-friendly: RoHS & no Sb/Br).

Features

- 4-Channel Protected Low-Side Driver
  - Four NMOS FETs With Overcurrent Protection
  - Integrated Inductive Clamp Diodes

  Parallel Interface
- DW Package: 1.5-A (Single Channel On) / 800-mA (Four Channels On) Maximum Drive Current per Channel (at 25°C)
- PWP Package: 2-A (Single Channel On) / 1-A (Four Channels On) Maximum Drive Current per Channel (at 25°C, With Proper PCB Heatsinking)
- 5-V to 60-V Operating Supply Voltage Range
- Thermally Enhanced Surface Mount Package

Applications

- Relay Drivers
- Unipolar Stepper Motor Drivers
- Solenoid Drivers
- General Low-Side Switch Applications

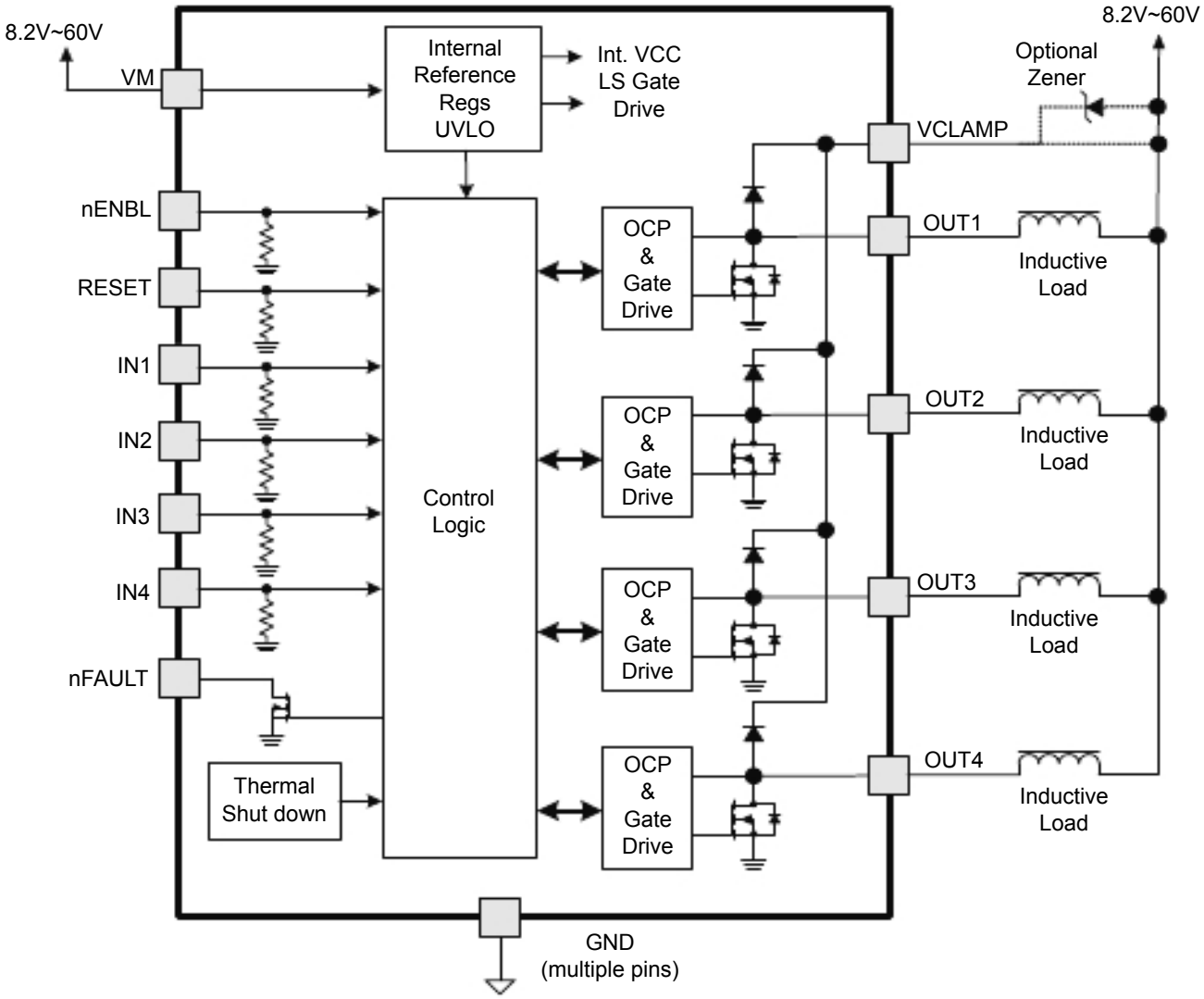
ORDERING INFORMATION (1)

PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
(SOIC) - DW	Reel of 2000	P8803DWR	P8803
	Tube of 25	P8803DW	P8803
(HTSSOP) - PWP	Reel of 2000	P8803PWPR	P8803
	Tube of 90	P8803PWP	P8803

Note:

1. For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the prisemi web site at www.prisemi.com.
2. Package drawings, thermal data, and symbolization are available at www.prisemi.com.

DEVICE INFORMATION
Functional Block Diagram



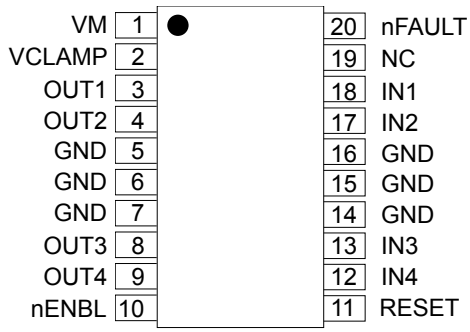
Terminal Functions

NAME	PIN (SOIC)	PIN (HTSSOP)	I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND					
GND	5,6,7, 14,15,16	5,12, PPAD	-	Device ground	All pins must be connected to GND.
VM	1	1	-	Device power supply	Connect to motor supply (5 V - 60 V).
CONTROL					
nENBL	10	8	I	Enable input	Active low enables outputs – internal pulldown
RESET	11	9	I	Reset input	Active high resets internal logic and OCP – internal pulldown
IN1	18	14	I	Channel 1 input	IN1 = 1 drives OUT1 low – internal pulldown
IN2	17	13	I	Channel 2input	IN2 = 1 drives OUT2 low – internal pulldown
IN3	13	11	I	Channel 3 input	IN3 = 1 drives OUT3 low – internal pulldown
IN4	12	10	I	Channel 4 input	IN4 = 1 drives OUT4 low – internal pulldown
STATUS					
nFAULT	20	16	OD	Fault	Logic low when in fault condition (overtemp, overcurrent)
OUTPUT					
OUT1	3	3	O	Output 1	Connect to load 1
OUT2	4	4	O	Output 2	Connect to load 2
OUT3	8	6	O	Output 3	Connect to load 3
OUT4	9	7	O	Output 4	Connect to load 4
VCLAMP	2	2	-	Output clamp voltage	Connect to VM supply, or zener diode to VM supply

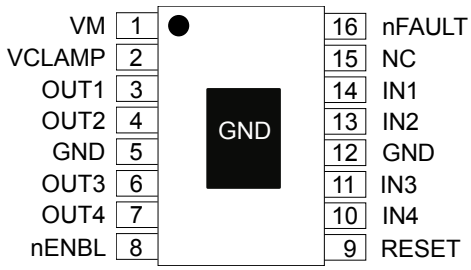
Note:

1. Directions: I = input, O = output, OD = open-drain output.

DW (WIDE SOIC) PACKAGE
(TOP VIEW)



PWP (HTSSOP) PACKAGE
(TOP VIEW)



Absolute maximum rating

over operating free-air temperature range (unless otherwise noted) (1) (2)

		VALUE	UNIT
VM	Power supply voltage range	–0.3 to 65	V
VOUTx	Output voltage range	–0.3 to 65	V
VCLAMP	Clamp voltage range	–0.3 to 65	V
nFAULT	Output current	20	mA
	Peak clamp diode current	2	A
	DC or RMS clamp diode current	1	A
	Digital input pin voltage range	–0.5 to 7	V
nFAULT	Digital output pin voltage range	–0.5 to 7	V
	Peak motor drive output current, t < 1 μS	Internally limited	A
	Continuous total power dissipation	See Dissipation Ratings table	
T_J	Operating virtual junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature range	–60 to 150	°C

Note:

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to network ground terminal.

Thermal Information

THERMAL METRIC		P8803		UNITS
		DW (SOIC) 20 PINS	PWP (HTSSOP) 16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.7	39.6	°C /W
$R_{\Theta jc(top)}$	Junction-to-case (top) thermal resistance	32.9	24.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	35.4	20.3	
ψ_{JT}	Junction-to-top characterization parameter	8.2	0.7	
ψ_{JB}	Junction-to-board characterization parameter	34.9	20.1	
$R_{\Theta jc(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	2.3	

Recommended operating con ditions

		MIN	NOM	MAX	UNIT
VM	Power supply voltage range	5		60	V
VCLAMP	Output clamp voltage range(1)	0		60	V
IOUT	Continuous output current, single channel on, TA = 25°C, SOIC package(2)			1.5	V
	Continuous output current, four channels on, TA = 25°C, SOIC package(2)			0.8	V
	Continuous output current, single channel on, TA = 25°C, HTSSOP package(2)			1.5	V
	Continuous output current, four channels on, TA = 25°C, HTSSOP package(2)			0.8	V

Note:

1. VCLAMP is used only to supply the clamp diodes. It is not a power supply input.
2. Power dissipation and thermal limits must be observed.

Elec trical charac teristics

TA = 25°C, over recommended operating conditions (unless otherwise noted).

Parameter		TEST CONDITIONS	Min.	Typ.	Max.	Units
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V		1	1.5	mA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising			5	V
LOGIC-LEVEL INPUTS (SCHMITT TRIGGER INPUTS WITH HYSTERESIS)						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2			V
V_{HYS}	Input hysteresis			0.45		V
I_{IL}	Input low current	VIN = 0	-20		20	uA
I_{IH}	Input high current	VIN = 3.3 V			50	uA
R_{PD}	Pulldown resistance			450		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	uA

Parameter		TEST CONDITIONS	Min.	Typ.	Max.	Units
LOW-SIDE FETS						
$R_{DS(ON)}$	FET on resistance	V_M = 24 V, I_O = 700 mA, T_J = 25°C		0.5		Ω
		V_M = 24 V, I_O = 700 mA, T_J = 85°C		0.75	0.8	
I_{OFF}	Off-state leakage current		-50		50	uA
HIGH-SIDE DIODES						
V_F	Diode forward voltage	V_M = 24 V, I_O = 700 mA, T_J = 25°C		1.2		V
I_{OFF}	Off-state leakage current	V_M = 24 V, T_J = 25°C	-50		50	uA
OUTPUTS						
t_R	Rise time	VM = 24 V, IO = 700 mA, Resistive load	50		300	nS
t_F	Fall time	VM = 24 V, IO = 700 mA, Resistive load	50		300	nS
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		2.3	3	3.8	A
t_{OCP}	Overcurrent protection deglitch time			8		uS
t_{RETRY}	Overcurrent protection retry time			3		mS
t_{TSD}	Thermal shutdown temperature	Die temperature(1)	150	160	180	°C

Note:

1. Not production tested.

Timing requirements

over operating free-air temperature range (unless otherwise noted) (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{OE(ENABLE)}$	Enable time, nENBL to output low		200	nS
2	$t_{PD(L-H)}$	Propogation delay time, INx to OUTx, low to high		200	nS
3	$t_{PD(H-L)}$	Propogation delay time, INx to OUTx, high to low		200	nS
-	t_{RESET}	RESET pulse width	20		uS

Note:

1. Not production tested.

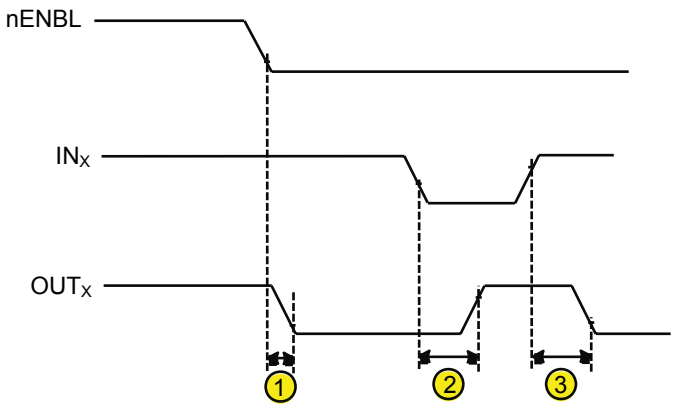


Figure 1. P8803 Timing Requirements

Functional description

Output Drivers

The P8803 contains four protected low-side drivers. Each output has an integrated clamp diode connected to a common pin, VCLAMP.

VCLAMP can be connected to the main power supply voltage, VM. It can also be connected to a zener or TVS diode to VM, allowing the switch voltage to exceed the main supply voltage VM. This connection can be beneficial when driving loads that require very fast current decay, such as unipolar stepper motors.

In all cases, the voltage on the outputs must not be allowed to exceed the maximum output voltage specification.

Parallel Interface Operation

The P8803 is controlled with a simple parallel interface. Logically, the interface is shown in Figure 2.

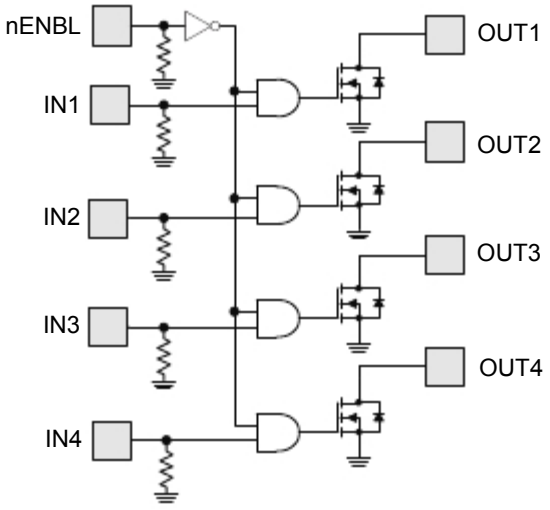


Figure 2. Parallel Interface Operation

nENBL and RESET Operation

The nENBL pin enables or disables the output drivers. nENBL must be low to enable the outputs. Note that nENBL has an internal pulldown.

The RESET pin, when driven active high, resets internal logic. Note that RESET has an internal pulldown. An internal power-up reset is also provided, so it is not required to drive RESET at power-up.

Protection Circuits

The P8803 is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the tOCP deglitch time (approximately 8 μs), the driver will be.

disabled and the nFAULT pin will be driven low. The driver will remain disabled for the tRETRY retry time (approximately 3 ms), then the fault will be automatically cleared. The fault will be cleared immediately if either RESET pin is activated or VM is removed and re-applied.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low.

Once the die temperature has fallen to a safe level, operation will automatically resume.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

THERMAL INFORMATION

Thermal Protection

The P8803 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the P8803 is dominated by the power dissipated in the output FET resistance, or RDS(ON). Average power dissipation of each FET when running a static load can be roughly estimated by.

Equation 1:

$$P = R_{DS(ON)} \cdot (I_{OUT})^2$$

where P is the power dissipation of one FET, RDS(ON) is the resistance of each FET, and IOUT is equal to the average current drawn by the load. Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also need to be taken into consideration. When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that RDS(ON) increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

Heatsinking

The P8803DW package uses a standard SOIC outline, but has the center pins internally fused to the die pad in order to more efficiently remove heat from the device. The two center leads on each side of the package should be connected together to as large a copper area on the PCB as is possible to remove heat from the device. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

In general, the more copper area that can be provided, the more power can be dissipated.

The P8803PWP package uses an HTSSOP package with an exposed PowerPAD™. The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

IMPORTANT NOTICE

and Prisemi® are registered trademarks of **Prisemi Electronics Co., Ltd (**Prisemi**)** ,Prisemi reserves the right to make changes without further notice to any products herein. Prisemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Prisemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in Prisemi data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. Prisemi does not convey any license under its patent rights nor the rights of others. The products listed in this document are designed to be used with ordinary electronic equipment or devices, Should you intend to use these products with equipment or devices which require an extremely high level of reliability and the malfunction of with would directly endanger human life (such as medical instruments, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

Website: http://www.prisemi.com

For additional information, please contact your local Sales Representative.