700V N-ch Planar MOSFET

Lead Free Package and Finish

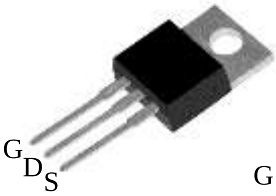
BV_{DSS}	$R_{DS(ON),typ.}$	I_D
700V	0.80Ω	10A

General Features

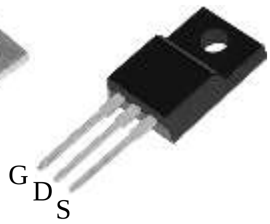
- RoHS Compliant
- $R_{DS(ON),typ.}$=0.80 Ω@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

Applications

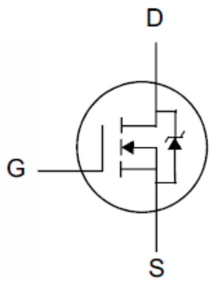
- Adaptor
- Charger
- SMPS Standby Power



TO-220



TO-220F



Package No to Scale

Ordering Information

Part Number	Package	Brand
PSP10N70	TO-220	
PSA10N70	TO-220F	

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	PSP10N70	PSA10N70	Unit
V_{DSS}	Drain-to-Source Voltage	700		V
V_{GSS}	Gate-to-Source Voltage	±30		
I_D	Continuous Drain Current	10		A
I_{DM}	Pulsed Drain Current at V_{GS}=10V	40		
E_{AS}	Single Pulse Avalanche Energy	500		mJ
dv/dt	Peak Diode Recovery dv/dt	5.5		V/ns
P_D	Power Dissipation	218	51	W
	Derating Factor above 25℃	1.75	0.4	W/℃
T_L	Soldering Temperature Distance of 1.6mm from case for 10 seconds	300		℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 150		

Caution: Stresses greater than those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	PSP10N70	PSA10N70	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.57	2.45	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	100	

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Electrical Characteristics

OFF Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	700	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	uA	V_{DS}=700V, V_{GS}=0V
		--	--	125		V_{DS}=560V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+30V, V_{DS}=0V
		--	--	-100		V_{GS}=-30V, V_{DS}=0V

ON Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	0.80	0.90	Ω	V_{GS}=10V, I_D=5A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250uA
gfs	Forward Transconductance	--	10	--	S	VDS=15V,ID=5A

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	1540	--	pF	V_{GS}=0V, V_{DS}=25V, f=1.0MH$_Z$
C_{rss}	Reverse Transfer Capacitance	--	16	--		
C_{oss}	Output Capacitance	--	150	--		
Q_g	Total Gate Charge	--	40	--	nC	V_{DD}=350V, I_D=10A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	7	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	17	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	14	--	ns	V_{DD}=350V, I_D=10A, V_{GS}=10V Rg=9.1 Ω
t_{rise}	Rise Time	--	23	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	48	--		
t_{fall}	Fall Time	--	32	--		

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Source-Drain Body Diode Characteristics

T_J=25℃ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current[2]	--	--	10	A	Integral pn-diode in MOSFET
I_{SM}	Pulsed Source Current[2]	--	--	40		
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_S=10A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	289	--	ns	V_{GS}=0V I_F=10A, di/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	1.9	--	uC	

Note:

[1] T_J=+25℃ to +150℃
[2] Pulse width≤380μs; duty cycle≤2%.

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Typical Characteristics

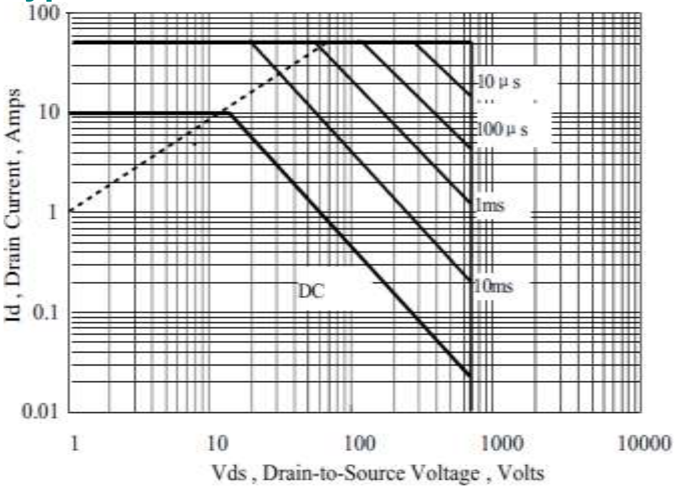

Figure 1 Maximun Forward Bias Safe Operating Area

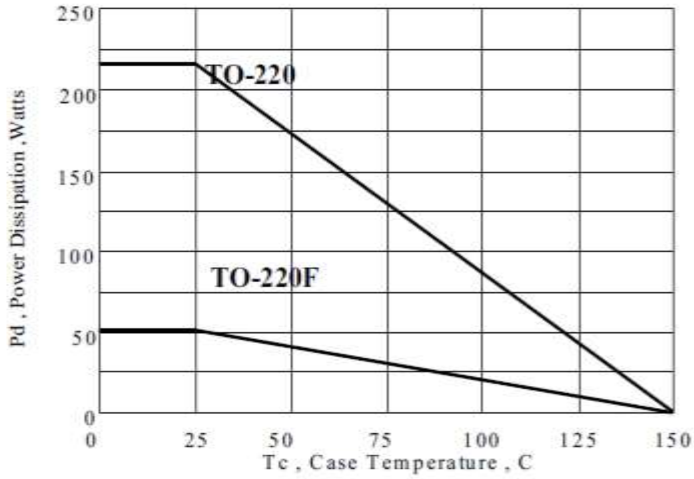

Figure 2 Maximun Power Dissipation vs Case Temperature

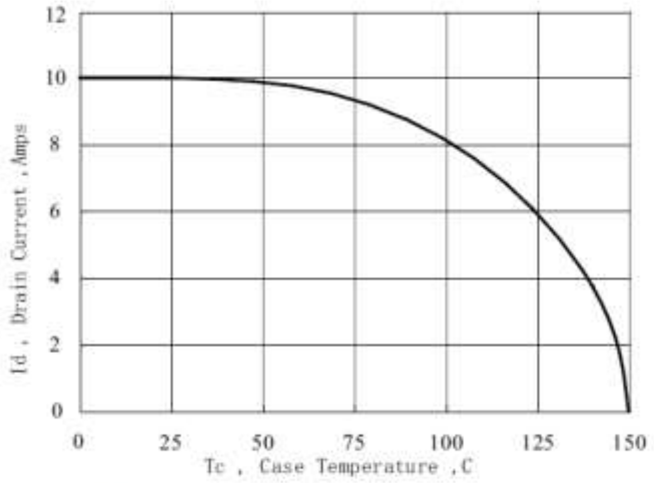

Figure 3 Maximum Continuous Drain Current vs Case Temperature

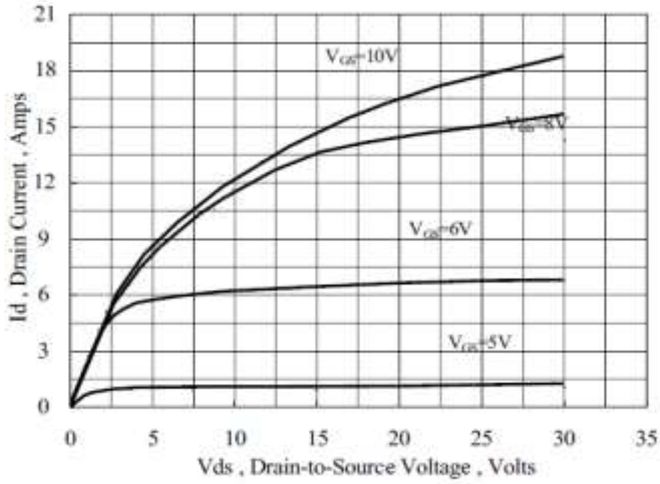

Figure 4 Typical Output Characteristics

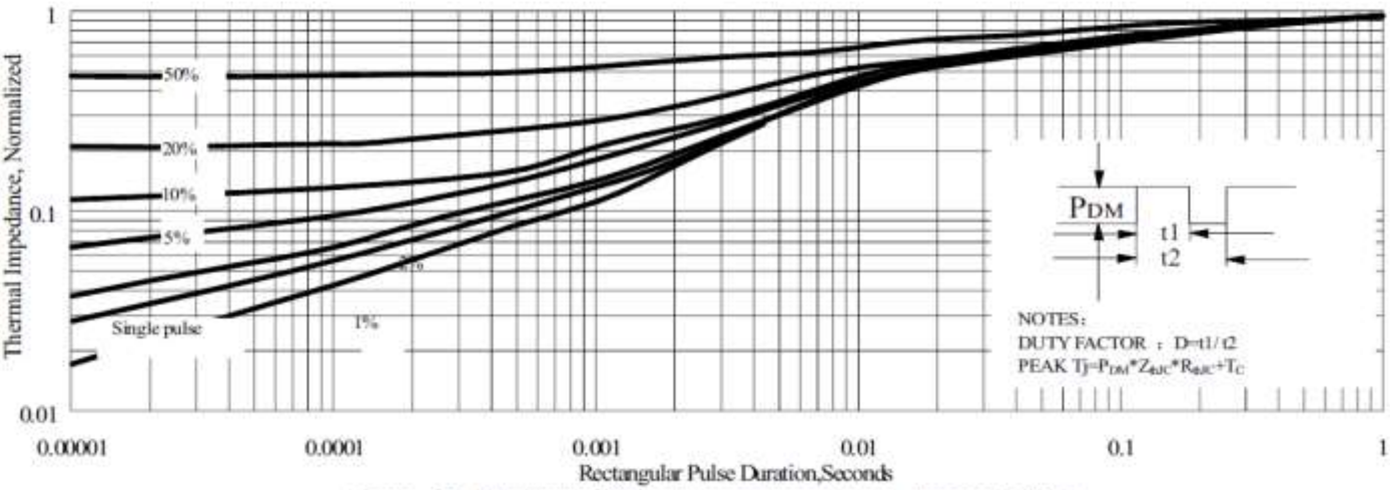

Figure 5 Maximum Effective Thermal Impendance , Junction to Case

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Typical Characteristics(Cont.)

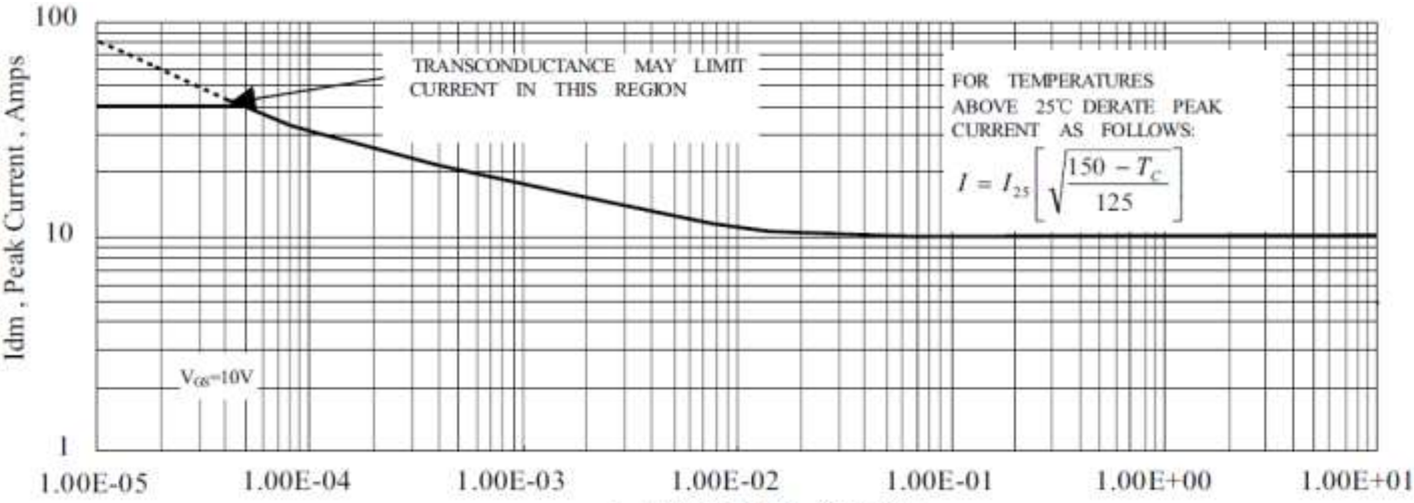

Figure 6 Maximun Peak Current Capability

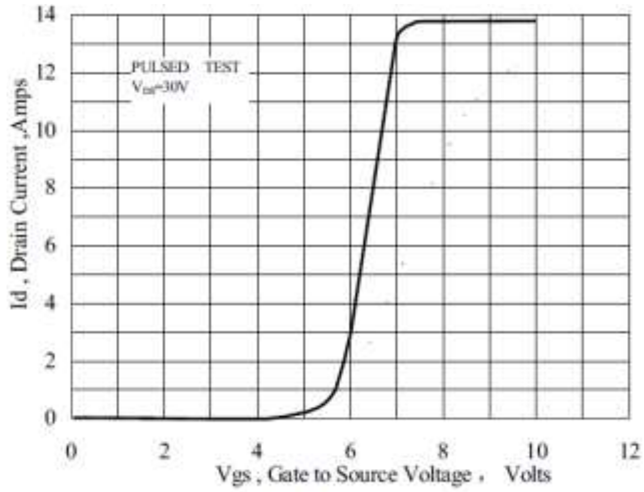

Figure 7 Typical Transfer Characteristics

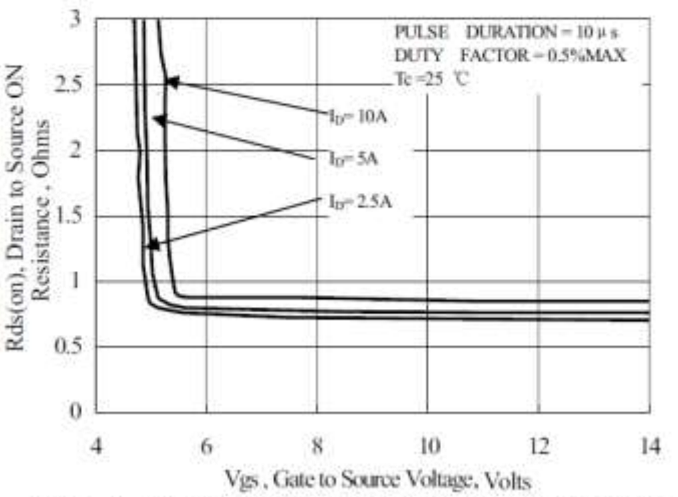

Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage

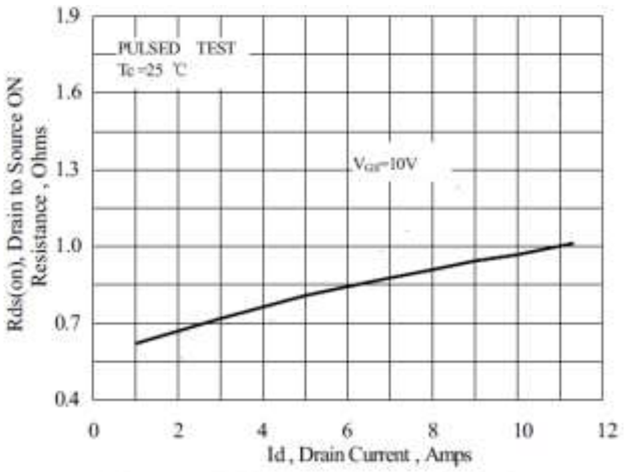

Figure 9 Typical Drain to Source ON Resistance vs Drain Current

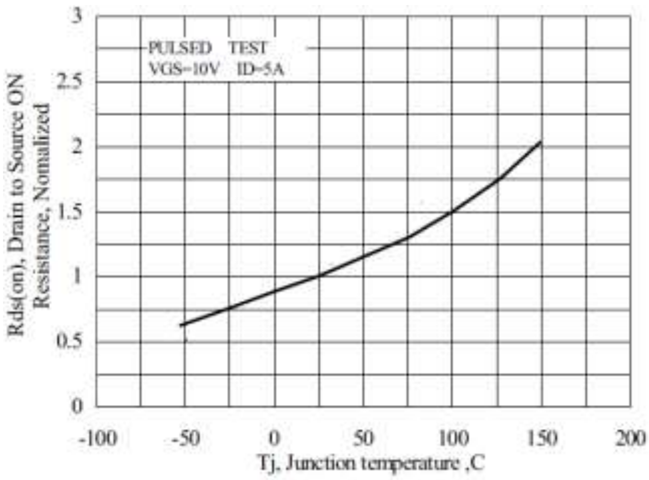

Figure 10 Typical Drian to Source on Resistance vs Junction Temperature

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Typical Characteristics(Cont.)

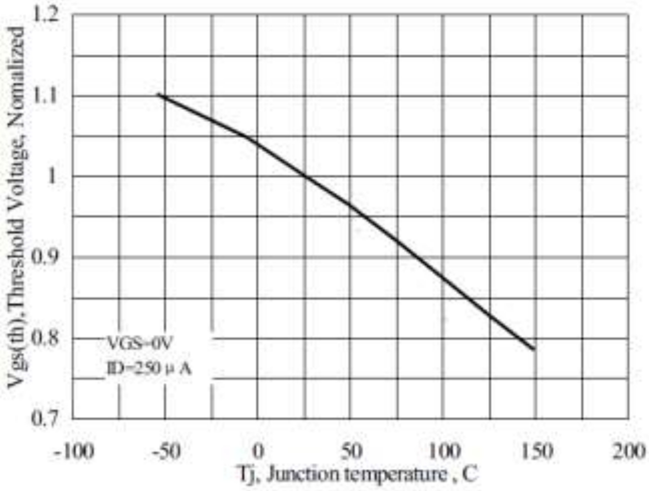

Figure 11 Typical Theshold Voltage vs Junction Temperature

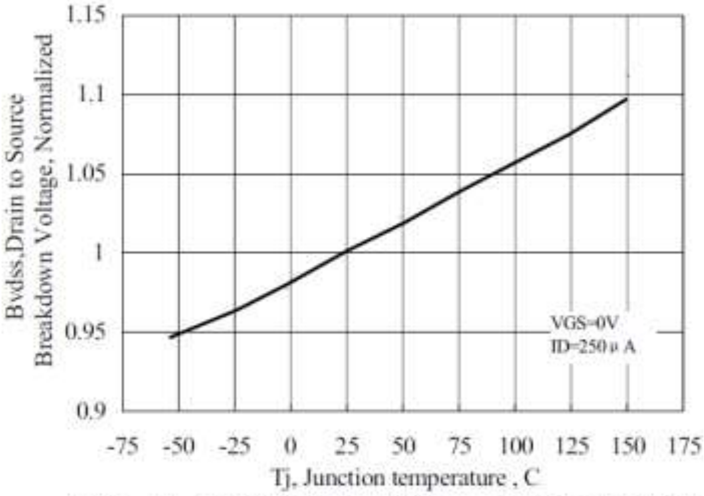

Figure 12 Typical Breakdown Voltage vs Junction Temperature

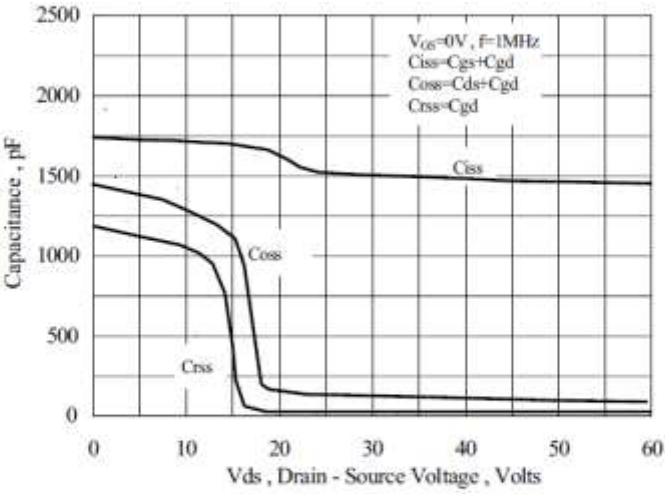

Figure 13 Typical Capacitance vs Drain to Source Voltage

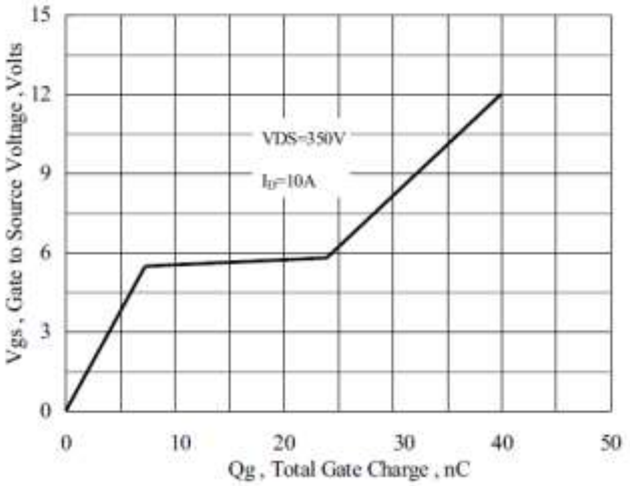

Figure 14 Typical Gate Charge vs Gate to Source Voltage

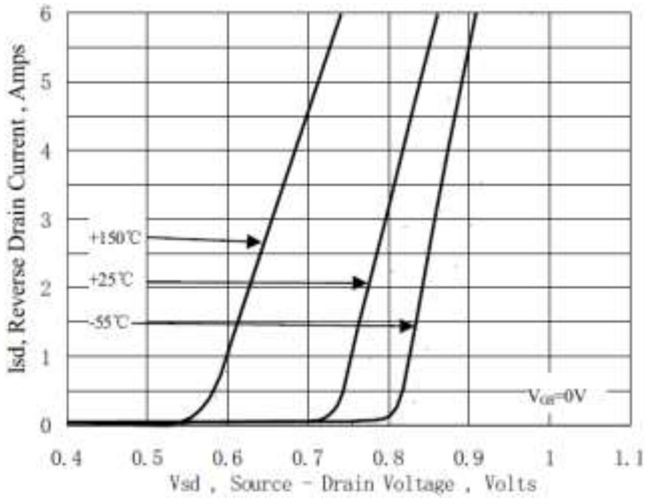

Figure 15 Typical Body Diode Transfer Characteristics

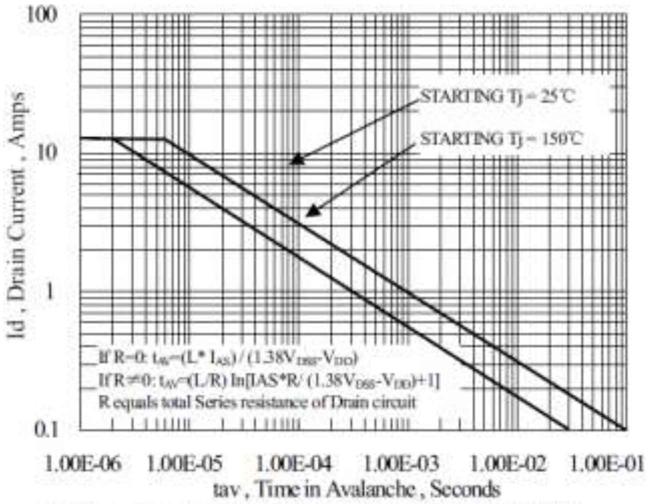

Figure 16 Unclamped Inductive Switching Capability

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Test Circuits and Waveforms

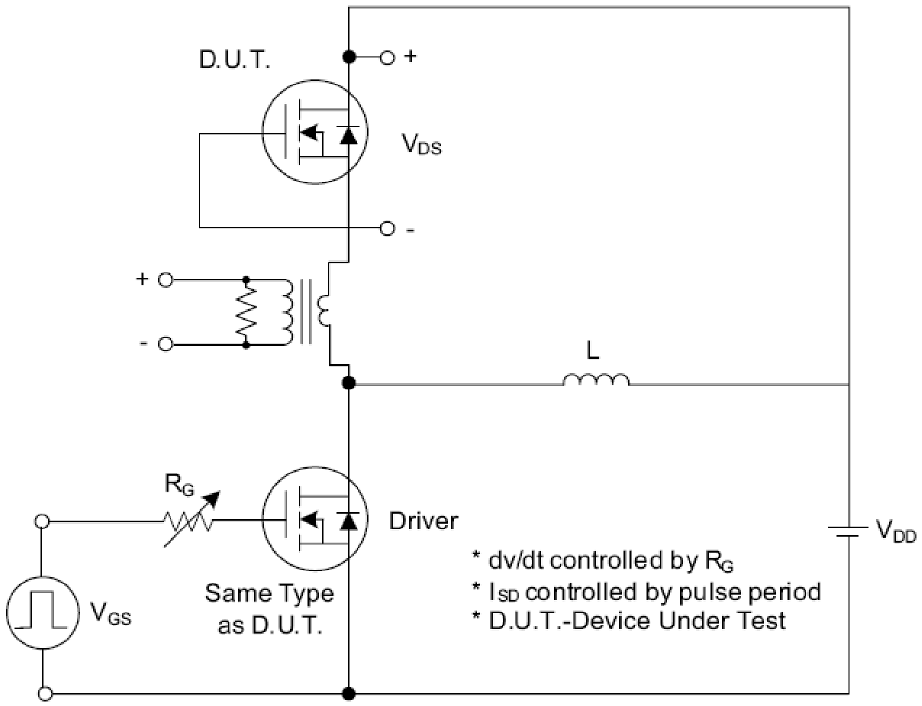

Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

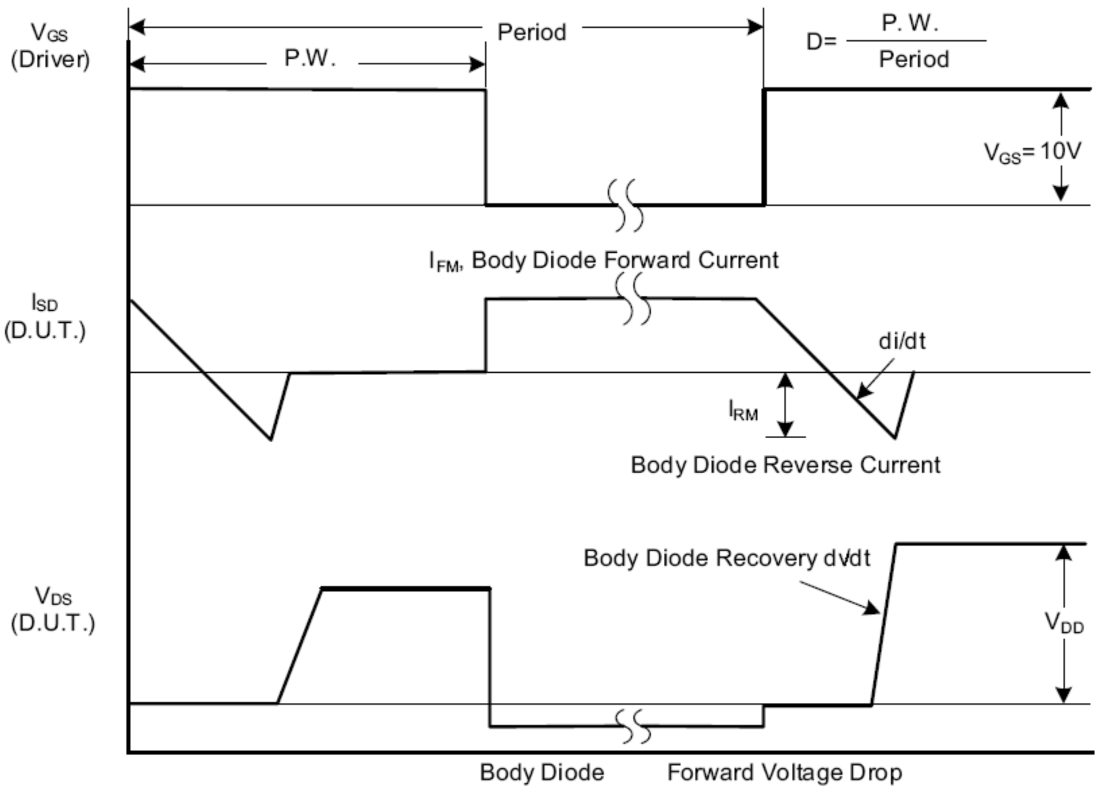

Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

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Test Circuits and Waveforms (Cont.)

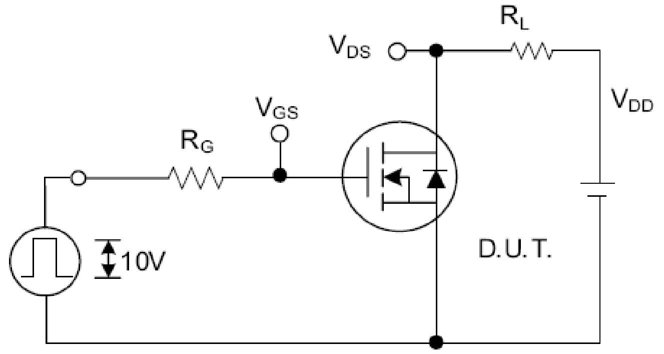

Fig. 2.1 Switching Test Circuit

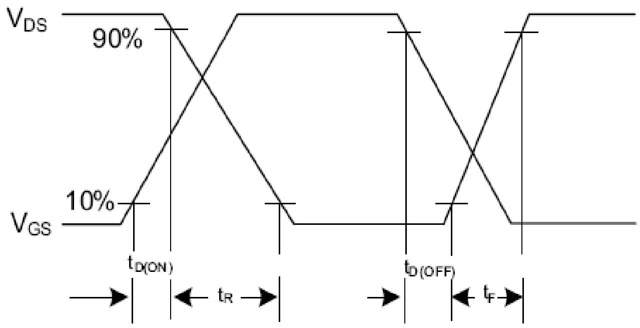

Fig. 2.2 Switching Waveforms

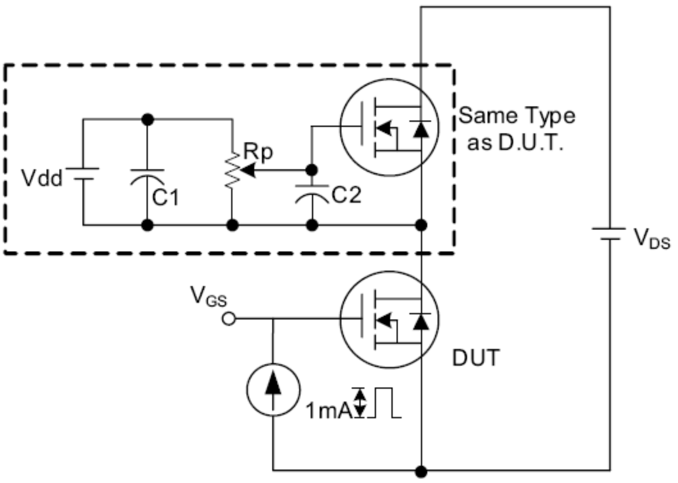

Fig. 3 . 1 Gate Charge Test Circuit

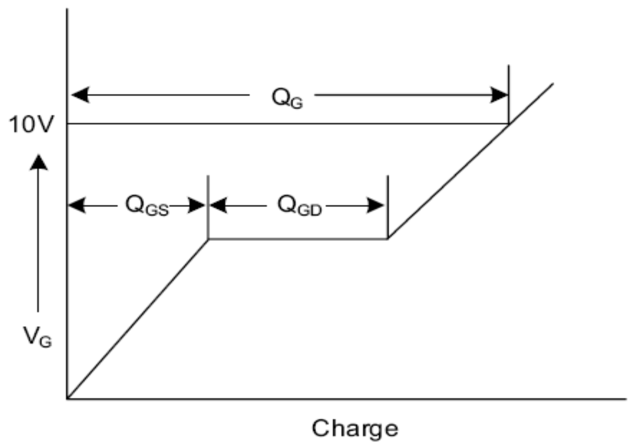

Fig. 3 . 2 Gate Charge Waveform

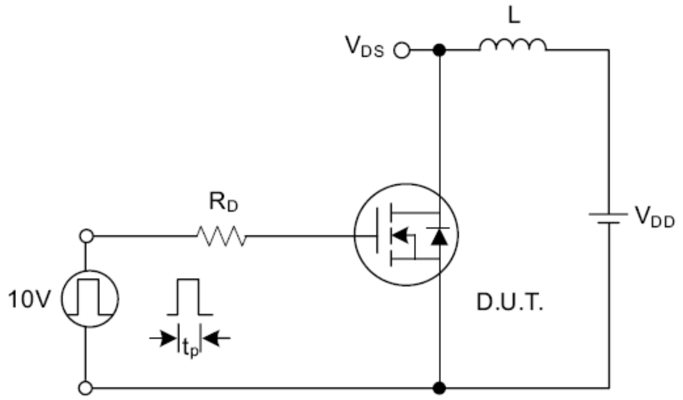

Fig. 4.1 Unclamped Inductive Switching Test Circuit

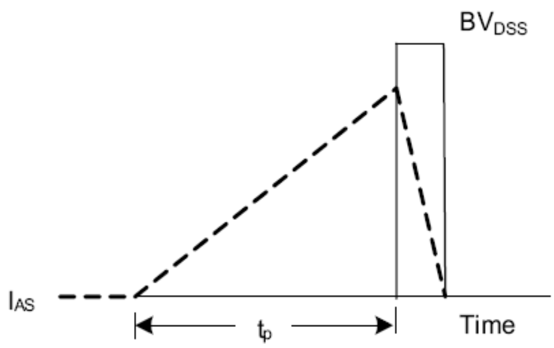

Fig. 4.2 Unclamped Inductive Switching Waveforms

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