

EXTREME LOW POWER RTC MODULE WITH I²C, 32-bit UNIX time counter, 43 bytes EEPROM, Battery Switchover and Trickle Charger



GENERAL DESCRIPTION

The EM3028-C7 engineered using the in-house analog low power (ALP) technology provides unmatched true ultra-low current consumption of typically 40nA while running on a standard 32'768 Hz tuning fork crystal. Thus allowing several hours of backup supply using cost effective MLCC capacitors.

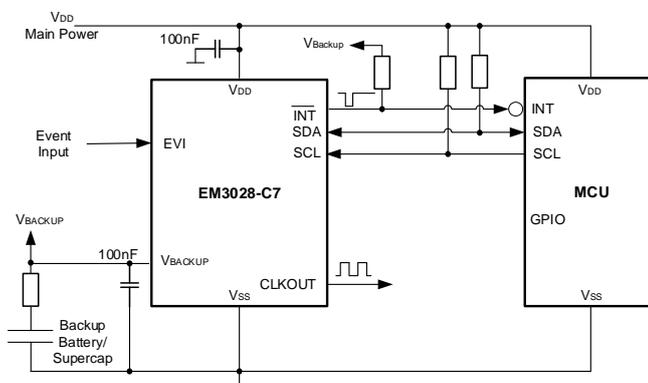
It provides full RTC function with programmable counters, alarm, selectable interrupt and clock output functions and also a 32-bit UNIX Time counter.

The internal EEPROM memory hosts all configuration settings and allows for additional 43 bytes of user memory.

All addresses and data are transferred over an I²C-bus interface for communication with a host controller.

This ultra-small RTC module has been specially designed for miniature and cost sensitive high volume applications.

TYPICAL APPLICATION



FEATURES

- | Extreme low power consumption: **40 nA @ 3 V**.
- | Wide operating voltage range: 1.2 V to 5.5 V.
- | Built-in tuning Fork crystal at 32'768 Hz
- | Time accuracy: Factory calibrated to **±1 ppm @ 25°C**
- | Non-volatile configuration settings with user programmable offset value.
- | Configuration stored in EEPROM and mirrored in RAM
- | Backup Switch and Trickle Charger function.
- | Provides year, month, date, weekday, hours, minutes and seconds.
- | Automatic leap year correction; 2000 to 2099
- | 32 bit UNIX time counter.
- | Timer, alarm and external event functions with time stamp.
- | Clock output: 32.768 kHz, 8192 Hz, 1024 Hz, 64 Hz, 32 Hz, 1 Hz.
- | 43 bytes non-volatile user memory, 2 bytes user RAM.
- | I²C-bus interface: 400 kHz.
- | Ultra small C7 package, RoHS compliant, 3.2x1.5x0.8mm
- | Also available in TSSOP14 with external Crystal, part number EM3028VxTP14

APPLICATIONS

The EM3028-C7 RTC module combines key functions with outstanding performance in an ultra-small ceramic package, special designed for:

- | IoT
- | Wearable systems
- | Multi-Solar cell platforms
- | Beacons and wireless sensor networks
- | Industrial and environmental monitoring
- | Battery operated platforms

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1. PRODUCT DESCRIPTION

The EM3028-C7 is an extreme-low power CMOS based Real-Time-Clock Module with embedded 32.768 kHz Crystal. It includes an Automatic Backup switchover function with a Trickle charger where the interrupt output on INT pin is also working in V_{BACKUP} Power state. The clock output on CLKOUT pin can be enabled normally via command over interface or can be interrupt driven and synchronized clock output enable/disable on CLKOUT pin can be freely selected. The configuration registers are stored permanently in non-volatile EEPROM and mirrored in RAM in order that the RTC module is still configured correctly even after power down. For safety against inadvertent change the time registers and configuration registers can be protected by a User Programmable Password. Additionally, there is an EEOffset value customer use for aging correction.

The EM3028-C7 provides standard Clock & Calendar function including seconds, minutes, hours (12 or 24 h), weekdays, date, months, years (with leap year correction) and interrupt functions for an External Event, Periodic Countdown Timer, Periodic Time Update and Alarm. All is accessible via I²C-bus (2-wire Interface). The interrupt functions and the Time Stamp of the External Event function are also working in V_{BACKUP} Power state. Beside the standard RTC functions a 32 bit UNIX Time counter and 43 Bytes of non-volatile User Memory EEPROM and 2 Bytes of User RAM are provided. A further Byte can be used as User RAM when the Periodic Countdown Timer is not used (Timer Value register 0Ah) and a further Byte when the Alarm function is not used (Alarm register 07h).

The registers are accessed by selecting a register address and then performing read or write operations. Multiple reads or writes may be executed in a single access, with the address automatically incrementing after each byte. When address is automatically incremented, wrap around occurs from address 3Fh to address 00h (see figure below). All registers are designed as addressable 8-bit registers despite the fact that not all registers and bits are implemented (reserved).

1.1. BLOCK DIAGRAM

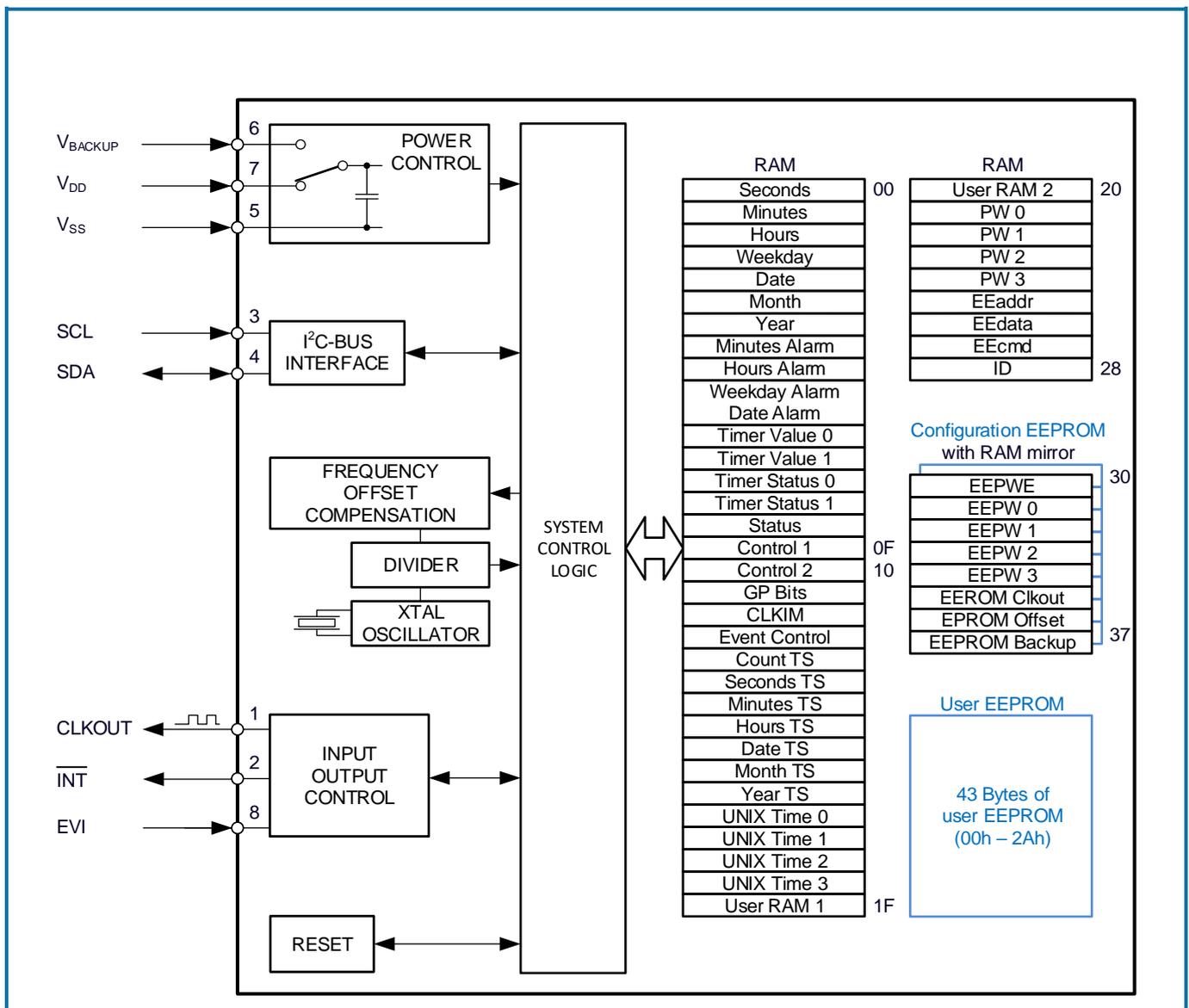


Figure 1-1 EM3028 Block Diagram

1.2. OPERATING MODES

The registers are accessed by selecting a register address and then performing read or write operations. Multiple reads or writes may be executed in a single access, with the address automatically incrementing after each byte. When address is automatically incremented, wrap around occurs from address 3Fh to address 00h (see [Figure 1-2 Address register auto-increment](#)). All registers are designed as addressable 8-bit registers despite the fact that not all registers and bits are implemented (reserved).

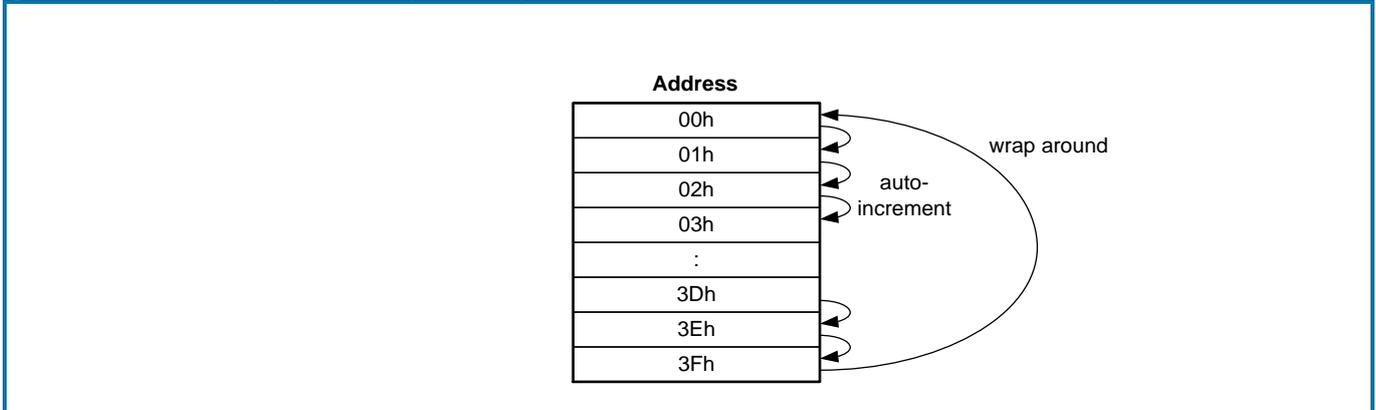


Figure 1-2 Address register auto-increment

1.2.1. DEVICE PROTECTION

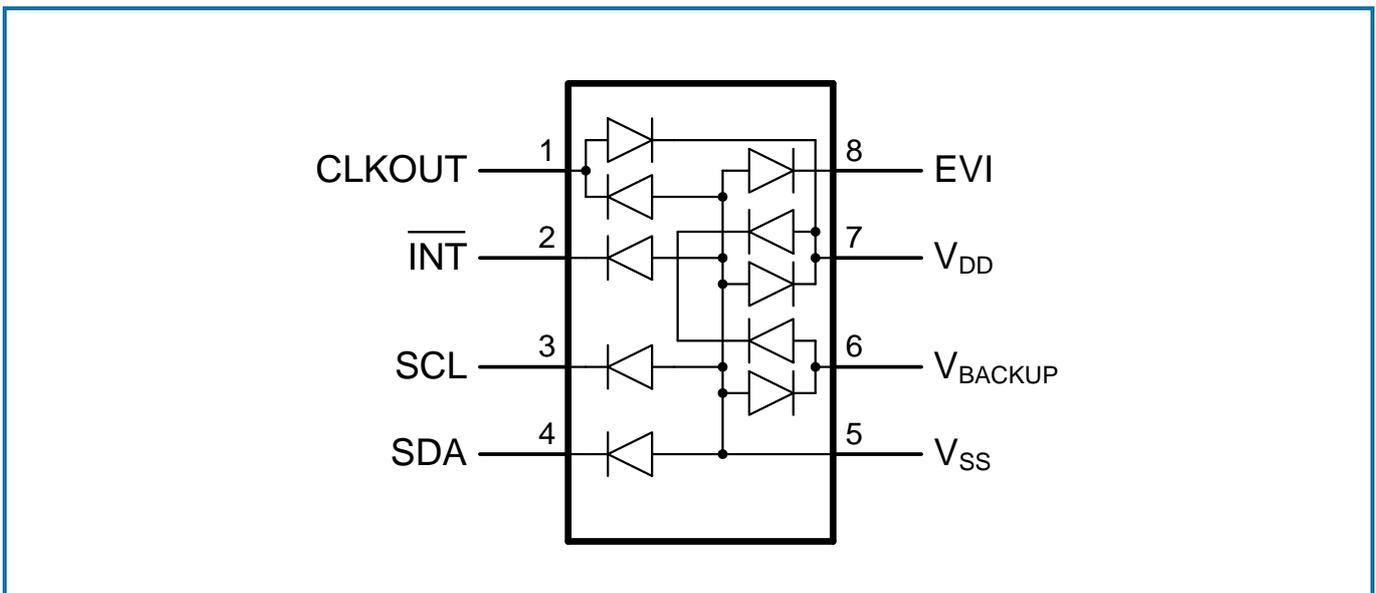


Figure 1-3 Device Diode Protection Diagram

1.2.2. REGISTER ORGANIZATION

- RAM Registers at addresses 00h to 28h are accessed by selecting a register address and then performing read or write operations. Multiple reads or writes may be executed in a single access, with the address automatically incrementing after each byte.
- The Configuration Registers at addresses 2Bh and 30h to 37h are memorized in EEPROM and mirrored in RAM.
- There are 43 bytes of non-volatile user memory EEPROM at addresses 00h to 2Ah for general use.

The following tables summarize the function of each register.

1.2.3. REGISTER CONVENTIONS

The conventions in this table serve as a key for the register overview and individual register diagrams:

| Convention (Conv.) | Description |
|--------------------|---|
| R | Read only. Writing to this register has no effect. |
| W | Write only. Returns 0 when read. |
| R/WP | Read: Always readable. Write: Can be write-protected by password. |
| WP | Write only. It can be write-protected by password. |
| Prot. | Protected. Not readable, but normal address pointer incrementing. |

1.2.4. REGISTER OVERVIEW

After reset, all registers are set according to Table in section [Register Reset Values Summary](#).

Register Definitions; RAM, Address 00h to 3Fh:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------------------|-------|----------------|-------|-------|-------|-------|-------|-------|-------|
| 00h | Seconds | R/WP | 0 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 01h | Minutes | R/WP | 0 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 02h | Hours (24 hour) | R/WP | 0 | 0 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Hours (12 hour) | | | | AMPM | 10 | 8 | 4 | 2 | 1 |
| 03h | Weekday | R/WP | 0 | 0 | 0 | 0 | 0 | 4 | 2 | 1 |
| 04h | Date | R/WP | 0 | 0 | 20 | 10 | 8 | 4 | 2 | 1 |
| 05h | Month | R/WP | 0 | 0 | 0 | 10 | 8 | 4 | 2 | 1 |
| 06h | Year | R/WP | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 07h | Minutes Alarm | R/WP | AE_M | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 08h | Hours Alarm (24h) | R/WP | AE_H | 0 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Hours Alarm (12h) | | | | AMPM | 10 | 8 | 4 | 2 | 1 |
| 09h | Weekday Alarm | R/WP | AE_WD | 0 | 0 | 0 | 0 | 4 | 2 | 1 |
| | Date Alarm | | | | 20 | 10 | 8 | 4 | 2 | 1 |
| 0Ah | Timer Value 0 | R/WP | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| 0Bh | Timer Value 1 | R/WP | 0 | 0 | 0 | 0 | 2048 | 1024 | 512 | 256 |
| 0Ch | Timer Status 0 | R | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| 0Dh | Timer Status 1 shadow | R | 0 | 0 | 0 | 0 | 2048 | 1024 | 512 | 256 |
| 0Eh | Status | R/WP | EEbusy | CLKF | BSF | UF | TF | AF | EVF | PORF |
| 0Fh | Control 1 | R/WP | TRPT | - | WADA | USEL | EERD | TE | TD | |
| 10h | Control 2 | R/WP | TSE | CLKIE | UIE | TIE | AIE | EIE | 12_24 | RESET |
| 11h | GP Bits | R/WP | - | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 |
| 12h | Clock Int. Mask | R/WP | - | - | - | - | CEIE | CAIE | CTIE | CUIE |
| 13h | Event Control | R/WP | 0 | EHL | ET | | 0 | TSR | TSOW | TSS |
| 14h | Count TS | R | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| 15h | Seconds TS | R | 0 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 16h | Minutes TS | R | 0 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 17h | Hours TS | R | 0 | 0 | 20 | 10 | 8 | 4 | 2 | 1 |
| | | | | | AMPM | 10 | 8 | 4 | 2 | 1 |
| 18h | Date TS | R | 0 | 0 | 20 | 10 | 8 | 4 | 2 | 1 |
| 19h | Month TS | R | 0 | 0 | 0 | 10 | 8 | 4 | 2 | 1 |
| 1Ah | Year TS | R | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 1Bh | UNIX Time 0 | R/WP | UNIX 0 [7:0] | | | | | | | |
| 1Ch | UNIX Time 1 | R/WP | UNIX 1 [15:8] | | | | | | | |
| 1Dh | UNIX Time 2 | R/WP | UNIX 2 [23:16] | | | | | | | |
| 1Eh | UNIX Time 3 | R/WP | UNIX 3 [31:24] | | | | | | | |
| 1Fh | User RAM 1 | R/WP | RAM 1 data | | | | | | | |
| 20h | User RAM 2 | R/WP | RAM 2 data | | | | | | | |
| 21h | Password 0 | W | PW 0 [7:0] | | | | | | | |
| 22h | Password 1 | W | PW 1 [15:8] | | | | | | | |
| 23h | Password 2 | W | PW 2 [23:16] | | | | | | | |

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|--------------|-------|--|-------|-------|-------|-------|-------|-------|-------|
| 24h | Password 3 | W | PW 3 [31:24] | | | | | | | |
| 25h | EEPROM Addr. | R/WP | EEaddr | | | | | | | |
| 26h | EEPROM Data | R/WP | EEdata | | | | | | | |
| 27h | EEPROM Com. | WP | EEcmd | | | | | | | |
| 28h | ID | R | HID | | | | VID | | | |
| 29h and 2Ah | Non-existing | | Non-existing RAM address (will be skipped by address pointer) | | | | | | | |
| 2Ch to 2Fh | RESERVED | Prot. | RESERVED (not readable, but normal address pointer incrementing) | | | | | | | |
| 38h to 3Fh | RESERVED | Prot. | RESERVED (not readable, but normal address pointer incrementing) | | | | | | | |

o Read only. Always 0.
- Bit not implemented. Will return a 0 when read.

Register Definitions; Configuration EEPROM with RAM mirror, Address 2Bh and 30h to 37h:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------------------|-------|------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 2Bh | EEPROM RESERVED | R/WP | RESERVED (Must not be overwritten) | | | | | | | |
| 30h | EEPROM PW Enable | R/WP | EEPWE | | | | | | | |
| 31h | EEPROM Password 0 | WP | EEPW 0 [7:0] | | | | | | | |
| 32h | EEPROM Password 1 | WP | EEPW 1 [15:8] | | | | | | | |
| 33h | EEPROM Password 2 | WP | EEPW 2 [23:16] | | | | | | | |
| 34h | EEPROM Password 3 | WP | EEPW 3 [31:24] | | | | | | | |
| 35h | EEPROM Clkout | R/WP | CLKOE | CLKSY | - | - | PORIE | FD | | |
| 36h | EEPROM Offset | R/WP | EEOffset [8:1] | | | | | | | |
| 37h | EEPROM Backup | R/WP | EEOffset [0] | BSIE | TCE | FEDE | BSM | | TCR | |

- Bit not implemented. Will return a 0 when read.

Register Definitions; User EEPROM, Address 00h to 2Ah:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|------------------------|-------|--------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 00h to 2Ah | User EEPROM (43 Bytes) | R/WP | 43 Bytes of non-volatile User EEPROM | | | | | | | |

Register Definitions; Manufacturer EEPROM, Address 2Ch to 2Fh and 38h to 3Fh:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-----------------|-------|----------|-------|-------|-------|-------|-------|-------|-------|
| 2Ch to 2Fh | EEPROM RESERVED | Prot. | RESERVED | | | | | | | |
| 38h to 3Fh | EEPROM RESERVED | Prot. | RESERVED | | | | | | | |

2. PIN DESCRIPTION

| PIN | | I/O TYPE | | DESCRIPTION |
|-----|-------------------------|-----------|--|--|
| NO. | NAME | DIRECTION | SUPPLY | |
| 1 | CLKOUT | O | V _{DD} | <p>Clock Output; push-pull; Normal and Interrupt driven clock output can be activated concurrently.</p> <ol style="list-style-type: none"> Normal clock output is controlled by the CLKOE bit. When CLKOE is set to 1 (default), the CLKOUT pin drives the square wave on the CLKOUT pin. When CLKOE bit is set to 0, the CLKOUT pin is LOW. Interrupt driven clock output is controlled by an interrupt event. When CLKIE is set to 1 the occurrence of the interrupt selected in the Clock Interrupt Mask Register (12h) allows the square wave output on the CLKOUT pin. Writing 0 to CLKIE will disable new interrupts from driving square wave on CLKOUT. When CLKF flag is cleared, the CLKOUT pin is LOW. <p>Depending of the settings in the XO field, the CLKOUT pin can drive the square wave of 32.768 kHz (default), 8192 Hz, 1024 Hz, 64 Hz, 32 Hz or 1 Hz, or the predefined periodic countdown timer interrupt. When XO field is 111 the CLKOUT pin is LOW.</p> <p>When CLKS_Y bit set to 1, the enabling and disabling of the clock output is synchronized. CLKS_Y has no effect on the timer interrupt signal.</p> <p>In V_{BACKUP} Power state, the CLKOUT pin is LOW.</p> |
| 2 | $\overline{\text{INT}}$ | O | V _{DD} or V _{BACKUP} | <p>Interrupt Output; open-drain; active LOW; requires pull-up resistor; used to output Periodic Countdown Timer, Periodic Time Update, Alarm, External Event, Automatic Backup Switchover and Power On Reset Interrupt signals. Interrupt output also in V_{BACKUP} Power state.</p> |
| 3 | SCL | I | V _{DD} | <p>I²C Serial Clock Input; requires pull-up resistor. In V_{BACKUP} Power state, the SCL pin is disabled.</p> |
| 4 | SDA | I/O | V _{DD} | <p>I²C Serial Data Input-Output; open-drain; requires pull-up resistor. In V_{BACKUP} Power state, the SDA pin is disabled (high impedance).</p> |
| 5 | V _{SS} | | V _{SS} | Ground |
| 6 | V _{BACKUP} | | | Battery Supply Voltage. When the backup switchover function is not needed, V _{BACKUP} must be tied to V _{SS} with a 10 kΩ resistor. |
| 7 | V _{DD} | | | Positive power supply |
| 8 | EVI | I | V _{DD} or V _{BACKUP} | <p>External Event Input; used for interrupt generation, interrupt driven clock output and time stamp function. Remains active also in V_{BACKUP} Power state. This pin should not be left floating.</p> |

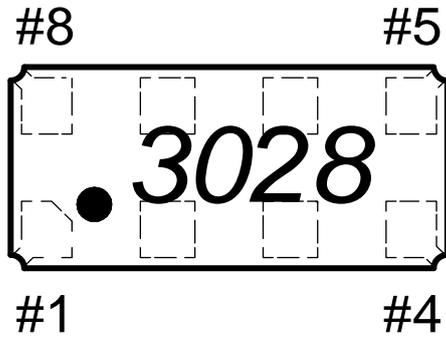
Table 1 Pin Out description

3. HANDLING PROCEDURES

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

4. PACKAGE / PIN OUT / MARKING

EM3028-C7 Package: (top view)



| | |
|----|-------------------------|
| #1 | CLKOUT |
| #2 | $\overline{\text{INT}}$ |
| #3 | SCL |
| #4 | SDA |
| #5 | V _{SS} |
| #6 | V _{BACKUP} |
| #7 | V _{DD} |
| #8 | EVI |

Figure 4-1 8 Id C7

Laser marking EM3028-C7 Package: (top view)

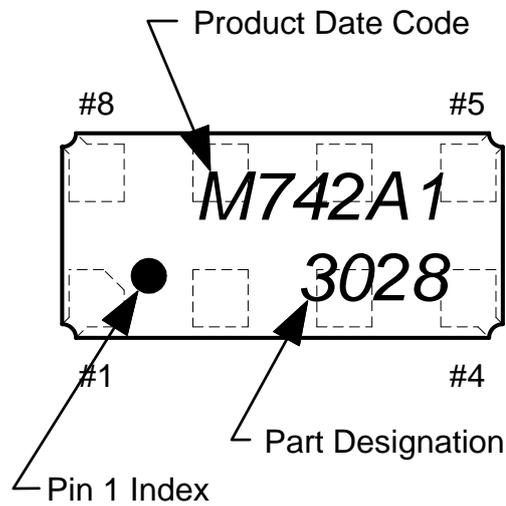


Figure 4-2 Package marking

5. ELECTRICAL SPECIFICATIONS

5.1. ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings according to IEC 60134:

| SYMBOL | PARAMETER | CONDITIONS | MIN | MAX | UNIT |
|--|--------------------------|----------------------|------|----------------------|------|
| V _{DD} | Power Supply Voltage | | -0.3 | 6.0 | V |
| V _I | Input voltage | Input Pin | -0.3 | V _{DD} +0.3 | V |
| V _O | Output voltage | Output Pin | -0.3 | V _{DD} +0.3 | V |
| I _I | Input current | | -10 | 10 | mA |
| I _O | Output current | | -10 | 10 | mA |
| V _{ESD} | ESD Voltage | HBM ⁽¹⁾ | | ±2000 | V |
| I _{LU} | Latch-up Current | JeDEC ⁽²⁾ | | ±100 | mA |
| T _{OPR} | Operating Temperature | | -40 | 85 | °C |
| T _{STO} | Storage Temperature | | -55 | 125 | °C |
| T _{PEAK} | Maximum reflow condition | JEDEC J-STD-020C | | 265 | °C |
| ⁽¹⁾ HBM: Human Body Model, according to JESD22-A114. ⁽²⁾ Latch-up testing, according to JESD78., Class I (room temperature), level A (100 mA) | | | | | |

Table 2 Absolute maximum ratings

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

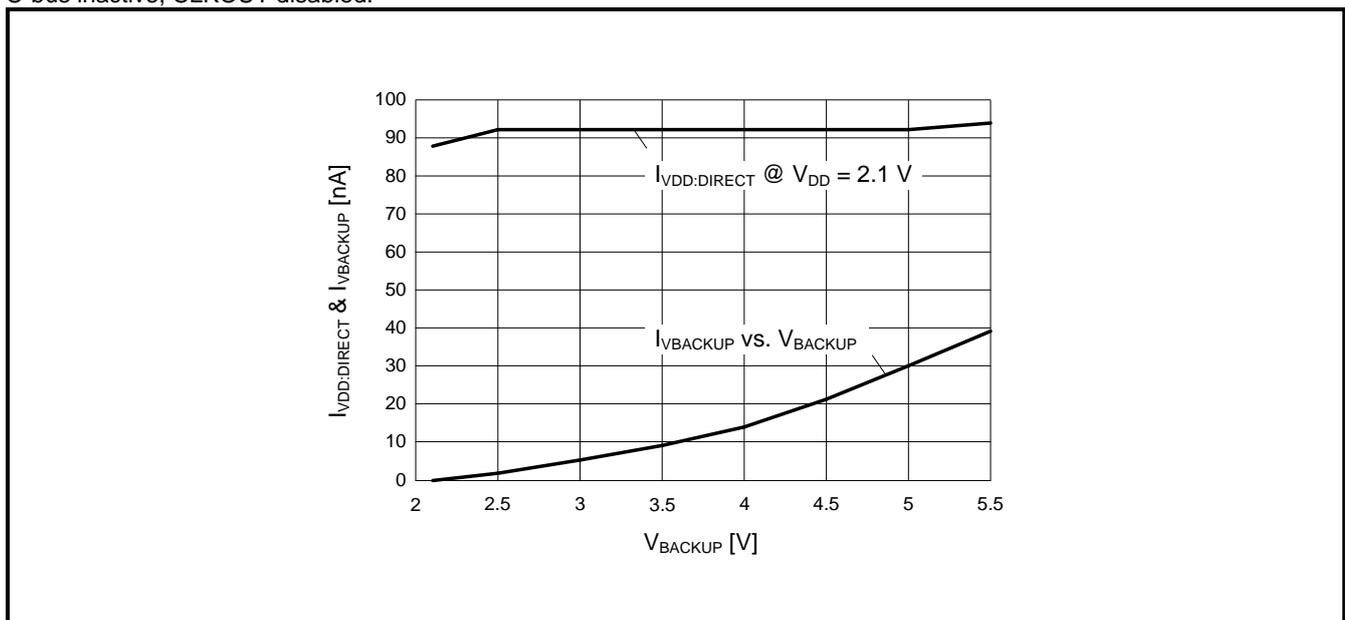
5.2. OPERATING PARAMETERS

For this Table, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ unless otherwise indicated. $V_{DD} = 1.2$ to 5.5 V , TYP values at $25\text{ }^\circ\text{C}$ and 3.0 V . Operating Parameters:

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|-----|------|-----|---------------|
| Supplies | | | | | | |
| V_{DD} | Power Supply Voltage | Time-keeping mode ⁽¹⁾ | 1.1 | | 5.5 | V |
| | | I ² C-bus (100 kHz) | 1.2 | | 5.5 | |
| | | I ² C-bus (400 kHz) | 2.0 | | 5.5 | |
| V_{BACKUP} | Backup Supply Voltage | | 1.1 | | 5.5 | V |
| I_{VDD} | V_{DD} supply current timekeeping I ² C-bus inactive, CLKOUT disabled, average current | $V_{DD} = 1.1\text{ V}$ ⁽²⁾ | | 40 | 300 | nA |
| | | $V_{DD} = 3.0\text{ V}$ ⁽²⁾ | | 40 | 330 | |
| | | $V_{DD} = 5.0\text{ V}$ ⁽²⁾ | | 40 | 400 | |
| $I_{VDD:I2C}$ | V_{DD} supply current during I ² C burst read/write, CLKOUT disabled | $V_{DD} = 1.2\text{ V}$, SCL = 100 kHz ⁽³⁾ | | 2 | 15 | μA |
| | | $V_{DD} = 3.0\text{ V}$, SCL = 400 kHz ⁽³⁾ | | 5 | 40 | |
| | | $V_{DD} = 5.0\text{ V}$, SCL = 400 kHz ⁽³⁾ | | 7 | 60 | |
| $I_{VDD:LEVEL}$ | V_{DD} supply current in level switching mode I ² C-bus inactive, CLKOUT disabled | $V_{DD} = 3.0\text{ V}$ | | 115 | 180 | nA |
| $I_{VDD:DIRECT}$ | V_{DD} supply current in direct switching mode I ² C-bus inactive, CLKOUT disabled | $V_{DD} = 3.0\text{ V}$ | | 95 | 150 | nA |
| $\Delta I_{VDD:CK32}$ | Additional V_{DD} supply current ⁽⁴⁾ | $V_{DD} = 3.0\text{ V}$, $F_{CLKOUT} = 32.768\text{ kHz}$, $C_L = 10\text{ pF}$ | | 1 | | μA |
| $\Delta I_{VDD:CK1024}$ | | $V_{DD} = 3.0\text{ V}$, $F_{CLKOUT} = 1024\text{ Hz}$, $C_L = 10\text{ pF}$ | | 30 | | nA |
| $\Delta I_{VDD:CK1}$ | | $V_{DD} = 3.0\text{ V}$, $F_{CLKOUT} = 1\text{ Hz}$, $C_L = 10\text{ pF}$ | | 0.03 | | nA |
| <p>(1) Clocks operating and RAM registers retained.</p> <p>(2) All inputs and outputs are at 0 V or V_{DD}.</p> <p>(3) 2.2k pull-up resistors on SCL/SDA, excluding external peripherals and pull-up resistor current. All other inputs (besides SDA and SCL) are at 0 V or V_{DD}. Test conditions: Continuous burst read/write, 55h data pattern, 25 μs between each data byte, 20 pF load on each bus pin.</p> <p>(4) When CLKOUT is enabled the additional V_{DD} supply current ΔI_{VDD} can be calculated as follows: $\Delta I_{VDD} = C_L \times V_{DD} \times CLKOUT$, e.g. $\Delta I_{VDD} = 10\text{ pF} \times 3.0\text{ V} \times 32.768\text{ Hz} = 980\text{ nA} \approx 1\text{ }\mu\text{A}$</p> | | | | | | |

Table 3 Operating Parameters, supplies

Typical characteristics in direct switching mode: $I_{VDD:DIRECT}$ @ $V_{DD} = 2.1\text{ V}$ and $I_{VBACKUP}$ vs. V_{BACKUP} , $T_A = 25\text{ }^\circ\text{C}$, I²C-bus inactive, CLKOUT disabled.



For this Table, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ unless otherwise indicated. $V_{DD} = 1.2$ to 5.5 V , TYP values at $25\text{ }^\circ\text{C}$ and 3.0 V .

Operating Parameters (continued):

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|--|--|---------------|------|--------------|---------------|
| Inputs | | | | | | |
| V_{IL} | LOW level input voltage | $V_{DD} = 1.1\text{ V}$ to 5.5 V Pins: SCL, SDA, EVI | | | $0.2 V_{DD}$ | V |
| V_{IH} | HIGH level input voltage | | $0.8 V_{DD}$ | | | V |
| I_{LEAK} | Input leakage current | $V_{SS} \leq V_I \leq V_{DD}$ | -0.5 | | 0.5 | μA |
| C_I | Input capacitance | $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$ $f = 1\text{ MHz}$ | | | 7 | pF |
| Outputs | | | | | | |
| $V_{OL:CLK}$ | LOW level output voltage CLKOUT | $V_{DD} = 1.1\text{ V}$, $I_{OL} = -0.1\text{ mA}$ | | | 0.1 | V |
| | | $V_{DD} = 3.0\text{ V}$, $I_{OL} = -1.0\text{ mA}$ | | | 0.3 | |
| | | $V_{DD} = 5.0\text{ V}$, $I_{OL} = -1.0\text{ mA}$ | | | 0.5 | |
| $V_{OH:CLK}$ | HIGH level output voltage CLKOUT | $V_{DD} = 1.1\text{ V}$, $I_{OH} = 0.1\text{ mA}$ | 1.0 | | | V |
| | | $V_{DD} = 3.0\text{ V}$, $I_{OH} = 1.0\text{ mA}$ | 2.7 | | | |
| | | $V_{DD} = 5.0\text{ V}$, $I_{OH} = 1.0\text{ mA}$ | 4.5 | | | |
| V_{OL} | LOW level output voltage Pins: SDA, INT | $V_{DD} = 1.2\text{ V}$, $I_{OL} = -0.5\text{ mA}$ | | | 0.4 | V |
| | | $V_{DD} = 3.0\text{ V}$, $I_{OL} = -3.0\text{ mA}$ | | | 0.4 | |
| | | $V_{DD} = 5.0\text{ V}$, $I_{OL} = -3.0\text{ mA}$ | | | 0.3 | |
| I_{OLEAK} | Output leakage current | $V_O = V_{DD}$ or V_{SS} | -0.5 | | 0.5 | μA |
| C_{OUT} | Output capacitance | $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$ $f = 1\text{ MHz}$ | | | 7 | pF |
| Power On Reset | | | | | | |
| V_{POR} | POR detection threshold | | 0.75 | 0.8 | 0.85 | V |
| Trickle charger | | | | | | |
| TCR 1 k Ω | Current limiting resistors | $V_{DD} = 5.0\text{ V}$, $V_{BACKUP} = 3.0\text{ V}$, including internal schottky diode | 2 | 3 | 4 | k Ω |
| TCR 3 k Ω | | | 4.5 | 5.5 | 6.25 | |
| TCR 6 k Ω | | | 7.5 | 9.3 | 11.6 | |
| TCR 11 k Ω | | | 12.5 | 15.7 | 17.4 | |
| Switchover | | | | | | |
| $V_{HYST:DSM}$ | Switchover hysteresis in direct switching mode | V_{DD} with respect to $V_{BACKUP}=3\text{ V}$, V_{DD} slew rate = $\pm 1\text{ V/ms}$, $T_{OPR} = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | | 60 | | mV |
| $V_{TH:LSM}$ | Backup switchover threshold voltage | V_{DD} falls below $V_{TH:LSM}$ | 1.8 | 2.0 | 2.2 | V |
| $V_{HYST:LSM}$ | Switchover hysteresis in level switching mode | V_{DD} with respect to $V_{BACKUP} = 3\text{ V}$, V_{DD} slew rate = $\pm 1\text{ V/ms}$, $T_{OPR} = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | | 100 | | mV |
| EEPROM Characteristics | | | | | | |
| $V_{DD:READ}$ | V_{DD} Read voltage | V_{DD} Power state | 1.1 | | | V |
| $V_{DD:WRITE}$ | V_{DD} write voltage | | 1.5 | | | |
| V_{WRITE} | Write voltage, only for voltage $\geq V_{TH:LSM}$ | | $V_{TH:LSM}$ | | | |
| t_{PREFR} | POR refresh | At power up | | 66 | | ms |
| t_{AREFR} | Automatic refresh | Each 24 hours, EERD = 0 | | 3.5 | | |
| t_{UPDATE} | Update | EECMD = 11h | | 63 | | |
| t_{REFR} | Refresh | EECMD = 12h | | 3.5 | | |
| t_{PROG} | Write to one EEPROM byte | EECMD = 21h | 4 | 16 | 30 | |
| t_{READ} | Read one EEPROM byte | EECMD = 22h | | 1.4 | | |
| n_{CYCLE} | Write cycle endurance ⁽⁵⁾ | $V_{DD} = 5.5\text{ V}$, $T_A = 85^\circ\text{C}$ $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$ | 100 10'000 | | | cycle |
| t_{RET} | Data retention time | $T_A = 55^\circ\text{C}$ | 10 | | | years |

⁽⁵⁾ Not 100% tested

Table 4 Operating Parameters, continued

5.3. OSCILLATOR PARAMETERS

For this Table, T_A = -40 °C to +85 °C unless otherwise indicated. V_{DD} = 1.2 to 5.5 V, TYP values at 25 °C and 3.0 V.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|---|--|--|--------|-------------------|-------|
| Xtal General | | | | | | |
| F | Crystal Frequency | | | 32.768 | | kHz |
| t _{START} | Oscillator start-up time at V _{DD} = 3.0 V | T _A = 25°C | | 0.5 | 1 | s |
| | | | | | 3 | |
| V _{START} | Oscillator start-up voltage | | 1.3 | | | V |
| Δf/V | Frequency vs. voltage characteristics | V _{DD} = 1.1 V to 5.5 V T _A = 25°C | | 0.5 | 1 | ppm/V |
| V _{DDR} | V _{DD} rising slew rate | V _{DD} = 1.1 V to 3.6 V | | | 2.5 | V/ms |
| | | V _{DD} = 3.6 V to 5.5 V | | | 3.8 | |
| V _{DDF} | V _{DD} falling slew rate | V _{DD} = 5.5 V to 1.1 V | | | 2.2 | |
| δ _{CLKOUT} | CLKOUT duty cycle | V _{DD} = 1.1 V to 5.5 V F _{CLKOUT} = 32.768 kHz | | 50 ±10 | | % |
| Xtal Frequency Characteristics | | | | | | |
| ΔF/F | Frequency accuracy | T _A = 25°C | | ±5 | | ppm |
| ΔF/F _{TOPR} | Frequency vs. temperature characteristics | T _{OPR} = -40°C to +85°C V _{DD} = 3.0 V | $-0.035^{ppm/°C^2} (T_{OPR}-T_0)^2 \pm 10\%$ | | | ppm |
| T ₀ | Turnover temperature | | +25 ±5 | | | °C |
| ΔF/F | Aging first year max. | T _A = 25°C, V _{DD} = 3.0 V | | | ±3 | ppm |
| Frequency Offset Correction | | | | | | |
| Δt/t | OFFSET correction: Min. corr. step (LSB) and Max. corr. range | T _A = -40°C to +85°C | ±0.954 | | +243.2/ -244.1 | ppm |
| Δt/t | Achievable time accuracy | Calibrated at an initial temperature and voltage | -0.48 | | +0.48 | ppm |

Table 5 Operating Parameters, Oscillator

5.3.1. XTAL FREQUENCY VS. TEMPERATURE CHARACTERISTICS

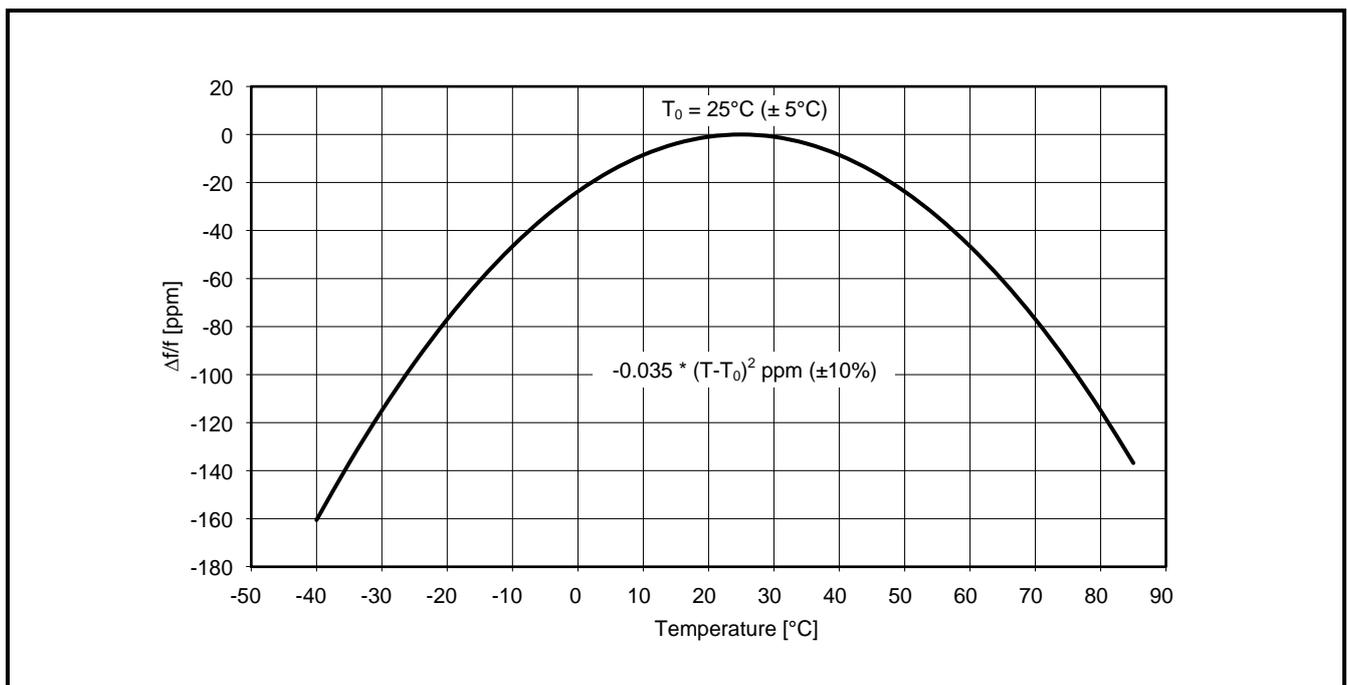


Figure 5-1 Xtal Frequency Characteristics

5.4. POWER-ON AC ELECTRICAL CHARACTERISTICS

The following Figure describes the power on AC electrical characteristics for the CLKOUT pin. The clock output signal on CLKOUT pin is enabled by the CLKOE bit (EEPROM 35h), see also [Use of the Configuration EEPROM WITH RAM MIRROR Registers](#).

Power-On AC Electrical Characteristics:

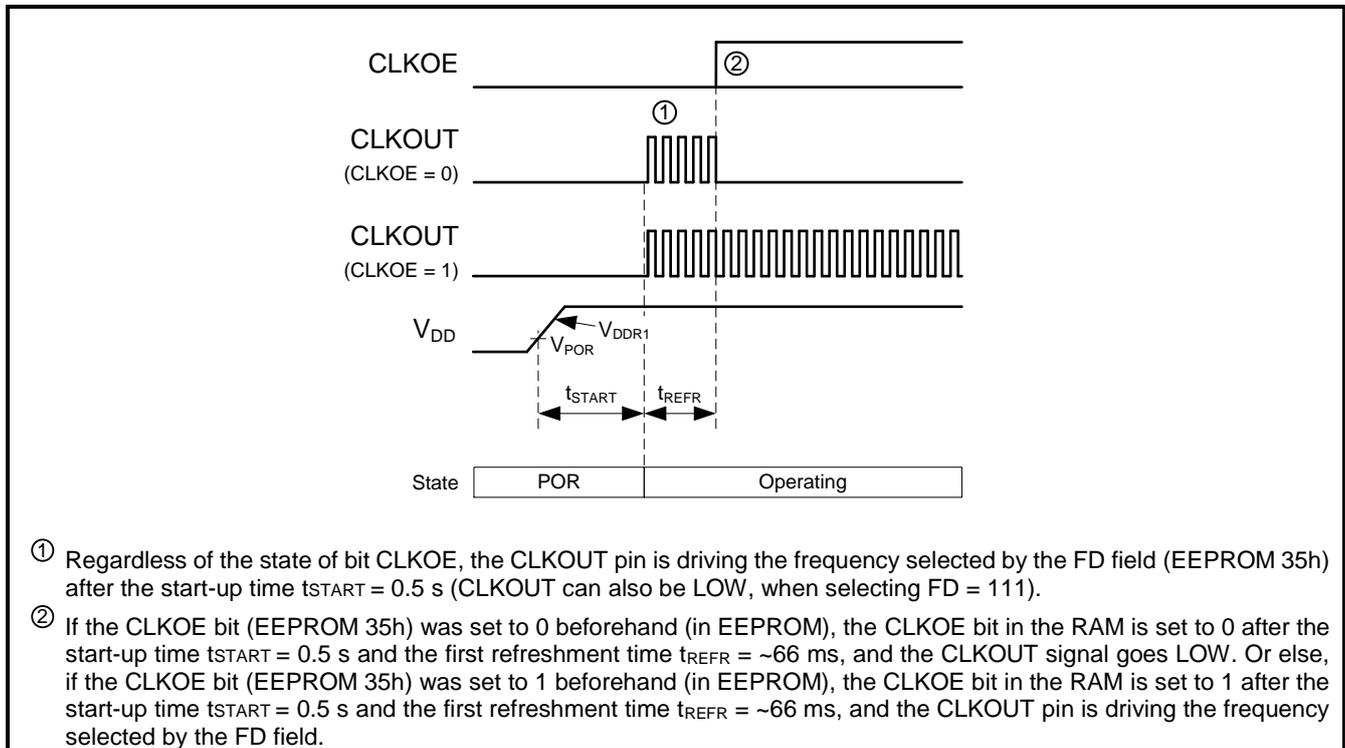


Figure 5-2 Power-On, AC Characteristics

For this Table, $T_A = -40$ °C to $+85$ °C and $V_{DD} = 1.2$ to 5.5 V, TYP values at 25 °C and 3.0 V.

Power On AC Electrical Parameters:

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|---|----------------------------|-----|-----|-----|------|
| V_{DDR1} | V_{DD} rising slew rate at initial power on reset (POR) | CLKOUT enabled (CLKOE = 1) | 0.1 | | 1 | V/ms |
| t_{START} | Oscillator start-up time at $V_{DD} = 3.0$ V | | | 0.5 | 3 | s |
| t_{REFR} | First refreshment time | | | 66 | | ms |

Table 6 Power-On Electrical Parameters

5.5. I²C-BUS CHARACTERISTICS

The following Figure and Table describe the I²C AC electrical parameters.
I²C AC Parameter Definitions:

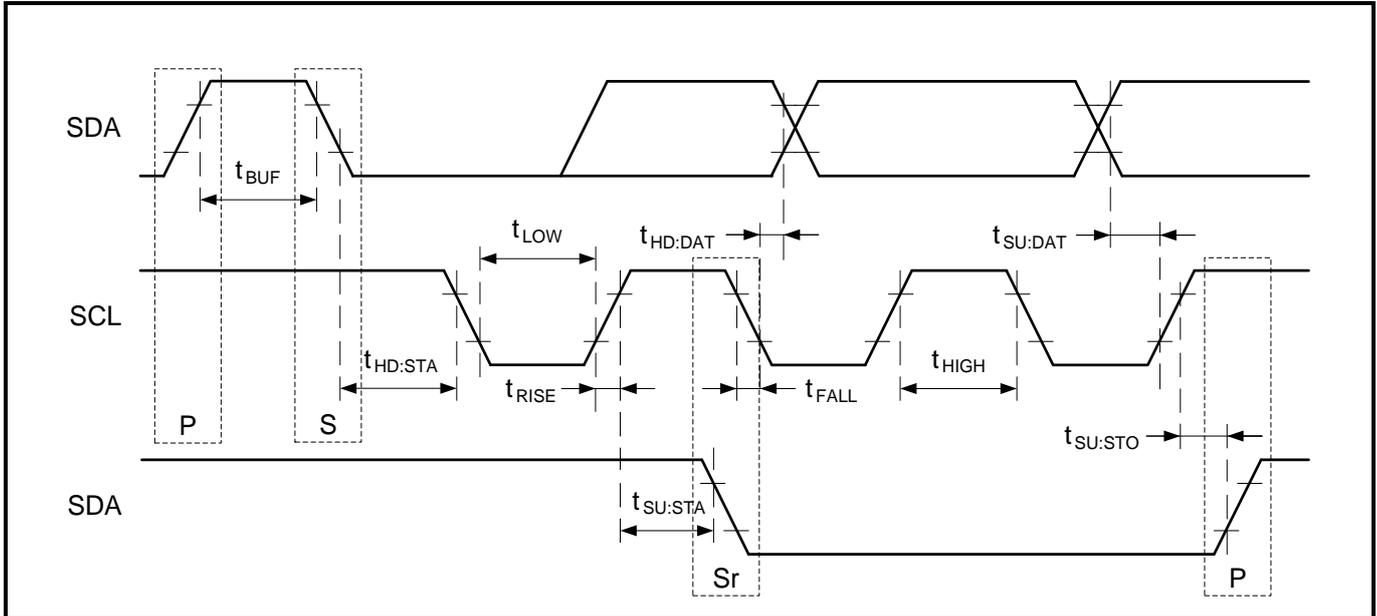


Figure 5-3 I²C Parameter definitions

For the following Table, $T_A = -40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$, TYP values at $25\text{ }^\circ\text{C}$.
I²C AC Electrical Parameters:

| SYMBOL | PARAMETER | Conditions | MIN | TYP | MAX | UNIT |
|---------------------|---|----------------------------|-----|-----|------|---------------|
| f _{SCL} | SCL input clock frequency | $V_{DD} \geq 1.2\text{ V}$ | 0 | | 100 | kHz |
| | | $V_{DD} \geq 2.0\text{ V}$ | 0 | | 400 | |
| t _{LOW} | Low period of SCL clock | $V_{DD} \geq 1.2\text{ V}$ | 4.7 | | | μs |
| | | $V_{DD} \geq 2.0\text{ V}$ | 1.3 | | | |
| t _{HIGH} | High period of SCL clock | $V_{DD} \geq 1.2\text{ V}$ | 4.0 | | | μs |
| | | $V_{DD} \geq 2.0\text{ V}$ | 0.6 | | | |
| t _{RISE} | Rise time of SDA and SCL | $V_{DD} \geq 1.2\text{ V}$ | | | 1000 | ns |
| | | $V_{DD} \geq 2.0\text{ V}$ | | | 300 | |
| t _{FALL} | Fall time of SDA and SCL | $V_{DD} \geq 1.2\text{ V}$ | | | 300 | ns |
| | | $V_{DD} \geq 2.0\text{ V}$ | | | 300 | |
| t _{HD:STA} | START condition hold time | $V_{DD} \geq 1.2\text{ V}$ | 4.0 | | | μs |
| | | $V_{DD} \geq 2.0\text{ V}$ | 0.6 | | | |
| t _{SU:STA} | START condition setup time | $V_{DD} \geq 1.2\text{ V}$ | 4.7 | | | μs |
| | | $V_{DD} \geq 2.0\text{ V}$ | 0.6 | | | |
| t _{SU:DAT} | SDA setup time | $V_{DD} \geq 1.2\text{ V}$ | 250 | | | ns |
| | | $V_{DD} \geq 2.0\text{ V}$ | 100 | | | |
| t _{HD:DAT} | SDA hold time | $V_{DD} \geq 1.2\text{ V}$ | 0 | | | μs |
| | | $V_{DD} \geq 2.0\text{ V}$ | 0 | | | |
| t _{SU:STO} | STOP condition setup time | $V_{DD} \geq 1.2\text{ V}$ | 4.0 | | | μs |
| | | $V_{DD} \geq 2.0\text{ V}$ | 0.6 | | | |
| t _{BUF} | Bus free time before a new transmission | $V_{DD} \geq 1.2\text{ V}$ | 4.7 | | | μs |
| | | $V_{DD} \geq 2.0\text{ V}$ | 1.3 | | | |

S = Start condition, Sr = Repeated Start condition, P = Stop condition

Table 7 Operating Parameters, I²C

Caution:

When accessing the EM3028-C7, all communication from transmitting the Start condition to transmitting the Stop condition after access should be completed within 950 ms.
If such communication requires 950 ms or longer, the I²C bus interface is reset by the internal bus timeout function.

6. PRODUCT CONFIGURATION

6.1. CLOCK REGISTERS

00h – Seconds. This register holds the count of seconds, in two binary coded decimal (BCD) digits. Values will be from 00 to 59. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|---|-------|-------|-------|-------|-------|-------|-------|
| 00h | Seconds | R/WP | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 6:0 | Seconds | 00 to 59 | Holds the count of seconds, coded in BCD format. When 1 is written to the RESET bit the Seconds register value remains unchanged. | | | | | | | |

Table 8 Seconds (0x00h).

01h – Minutes. This register holds the count of minutes, in two binary coded decimal (BCD) digits. Values will be from 00 to 59. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 01h | Minutes | R/WP | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 6:0 | Minutes | 00 to 59 | Holds the count of minutes, coded in BCD format. | | | | | | | |

Table 9 Minutes (0x01h).

02h – Hours. This register holds the count of hours, in two binary coded decimal (BCD) digits. If the 12_24 bit is cleared (default) (see [Configuration Registers](#), 10h – Control 2) the values will be from 0 to 23. If the 12_24 bit is set, the hour values will range from 1 to 12 and the AMPM bit will be 0 for AM hours and 1 for PM hours. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|--------------------------------------|---------|--|-------|-------|-------|-------|-------|-------|-------|
| 02h | Hours (24 hour mode) – default value | R/WP | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| | Hours (12 hour mode) | | | | AMPM | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Hours (24 hour mode), 12_24 = 0 – default value | | | | | | | | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:6 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 5:0 | Hours (24 hour mode) – default value | 0 to 23 | Holds the count of hours, coded in BCD format. | | | | | | | |
| Hours (12 hour mode), 12_24 = 1 | | | | | | | | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:6 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 5 | AMPM | 0 | AM hours. | | | | | | | |
| | | 1 | PM hours. | | | | | | | |
| 4:0 | Hours (12 hour mode) | 1 to 12 | Holds the count of hours, coded in BCD format. | | | | | | | |

Table 10 Hours (0x02h).

6.2. CALENDAR REGISTERS

03h – Weekday. This register holds the current day of the week. Each value represents one weekday that is assigned by the user. Values will range from 0 to 6. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------------|----------|--------|----------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 03h | Weekday | R/WP | ○ | ○ | ○ | ○ | ○ | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:3 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 2:0 | Weekday | 0 to 6 | Holds the weekday counter value. | | | | | | | |
| Weekday | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Weekday 1 – Default value | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Weekday 2 | | | | | | | | 0 | 0 | 1 |
| Weekday 3 | | | | | | | | 0 | 1 | 0 |
| Weekday 4 | | | | | | | | 0 | 1 | 1 |
| Weekday 5 | | | | | | | | 1 | 0 | 0 |
| Weekday 6 | | | | | | | | 1 | 0 | 1 |
| Weekday 7 | | | | | | | | 1 | 1 | 0 |

Table 11 Weekday (0x03h).

04h – Date. This register holds the current day of the month, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 2000 to 2099. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 04h | Date | R/WP | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:6 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 5:0 | Date | 01 to 31 | Holds the current date of the month, coded in BCD format. – Default value = 01 | | | | | | | |

Table 12 Date (0x04h).

05h – Month. This register holds the current month, in two binary coded decimal (BCD) digits. Values will range from 01 to 12. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|-------------------------|----------|----------|---|-------|-------|-------|-------|-------|-------|-------|--|
| 05h | Month | R/WP | ○ | ○ | ○ | 10 | 8 | 4 | 2 | 1 | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |
| Bit | Symbol | Value | Description | | | | | | | | |
| 7:5 | ○ | 0 | Read only. Always 0. | | | | | | | | |
| 4:0 | Month | 01 to 12 | Holds the current month, coded in BCD format. | | | | | | | | |
| Months | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | | | |
| January – Default value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | |
| February | | | | 0 | 0 | 0 | 1 | 0 | | | |
| March | | | | 0 | 0 | 0 | 1 | 1 | | | |
| April | | | | 0 | 0 | 1 | 0 | 0 | | | |
| May | | | | 0 | 0 | 1 | 0 | 1 | | | |
| June | | | | 0 | 0 | 1 | 1 | 0 | | | |
| July | | | | 0 | 0 | 1 | 1 | 1 | | | |
| August | | | | 0 | 1 | 0 | 0 | 0 | | | |
| September | | | | 0 | 1 | 0 | 0 | 1 | | | |
| October | | | | 1 | 0 | 0 | 0 | 0 | | | |
| November | | | | 1 | 0 | 0 | 0 | 0 | 1 | | |
| December | | | | 1 | 0 | 0 | 1 | 0 | | | |

Table 13 Month (0x05h).

06h – Year. This register holds the current year, in two binary coded decimal (BCD) digits. Values will range from 00 to 99. Leap years are correctly handled from 2000 to 2099. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|---|-------|-------|-------|-------|-------|-------|-------|
| 06h | Year | R/WP | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | Year | 00 to 99 | Holds the current year, coded in BCD format. – Default value = 00 | | | | | | | |

Table 14 Year (0x06h).

6.3. ALARM REGISTERS

07h – Minutes Alarm. This register holds the Minutes Alarm Enable bit AE_M and the alarm value for minutes, in two binary coded decimal (BCD) digits. Values will range from 00 to 59. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------|---|---|-------|-------|-------|-------|-------|-------|-------|
| 07h | Minutes Alarm | R/WP | AE_M | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | AE_M | Minutes Alarm Enable bit. Enables alarm together with AE_H and AE_WD (see Use of The Alarm Interrupt). | | | | | | | | |
| | | 0 | Minutes Alarm is enabled. | | | | | | | |
| | | 1 | Minutes Alarm is disabled. – Default value | | | | | | | |
| 6:0 | Minutes Alarm | 00 to 59 | Holds the alarm value for minutes, coded in BCD format. | | | | | | | |

Table 15 Minutes Alarm (0x07h).

08h – Hours Alarm. This register holds the Hours Alarm Enable bit AE_H and the alarm value for hours, in two binary coded decimal (BCD) digits. If the 12_24 bit is cleared (default value) (see [Configuration Registers](#), 10h – Control 2) the values will range from 0 to 23. If the 12_24 bit is set, the hour values will be from 0 to 12 and the AMPM bit will be 0 for AM hours and 1 for PM hours. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|--|---|---|-------|-------|-------|-------|-------|-------|-------|
| 08h | Hours Alarm (24 hour mode) – default value | R/WP | AE_H | ◦ | 20 | 10 | 8 | 4 | 2 | 1 |
| | Hours Alarm (12 hour mode) | | | | AMPM | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Hours Alarm (24 hour mode), 12_24 = 0 – default value | | | | | | | | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | AE_H | Hours Alarm Enable bit (see Use of The Alarm Interrupt). | | | | | | | | |
| | | 0 | Enabled | | | | | | | |
| | | 1 | Disabled – Default value | | | | | | | |
| 6 | ◦ | 0 | Read only. Always 0. | | | | | | | |
| 5:0 | Hours Alarm (24 hour mode) – default value | 0 to 23 | Holds the alarm value for hours, coded in BCD format. | | | | | | | |
| Hours Alarm(12 hour mode), 12_24 = 1 | | | | | | | | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | AE_H | Hours Alarm Enable bit (see Use of The Alarm Interrupt). | | | | | | | | |
| | | 0 | Enabled | | | | | | | |
| | | 1 | Disabled – Default value | | | | | | | |
| 6 | ◦ | 0 | Read only. Always 0. | | | | | | | |
| 5 | AMPM | 0 | AM hours. | | | | | | | |
| | | 1 | PM hours. | | | | | | | |
| 4:0 | Hours Alarm (12 hour mode) | 1 to 12 | Holds the alarm value for hours, coded in BCD format. | | | | | | | |

Table 16 Hours Alarm (0x08h).

09h – Weekday/Date Alarm. This register holds the Weekday/Date Alarm Enable bit AE_WD. If the WADA bit is 0 (Bit 5 in Register 0Fh), it holds the alarm value for the weekday (weekdays assigned by the user), in two binary coded decimal (BCD) digits. Values will range from 0 to 6. If the WADA bit is 1, it holds the alarm value for the date, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 2000 to 2099. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|-------------------------------|---|---|-------|-------|-------|-------|-------|-------|-------|
| 09h | Weekday Alarm – default value | R/WP | AE_WD | ○ | ○ | ○ | ○ | 4 | 2 | 1 |
| | Date Alarm | | | | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Weekday Alarm, WADA = 0 – default value | | | | | | | | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | AE_WD | Weekday/Date Alarm Enable bit. Enables alarm together with AE_M and AE_H (see Use of The Alarm Interrupt). | | | | | | | | |
| | | 0 | Enabled | | | | | | | |
| | | 1 | Disabled – Default value | | | | | | | |
| 6:3 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 2:0 | Weekday Alarm | 0 to 6 | Holds the weekday alarm value, coded in BCD format. | | | | | | | |
| Date Alarm, WADA = 1 | | | | | | | | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | AE_WD | Weekday/Date Alarm Enable bit. Enables alarm together with AE_M and AE_H (see Use of The Alarm Interrupt). | | | | | | | | |
| | | 0 | Enabled | | | | | | | |
| | | 1 | Disabled – Default value | | | | | | | |
| 6 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 5:0 | Date Alarm | 01 to 31 | Holds the alarm value for the date, coded in BCD format. The Reset value 00 after POR has to be replaced by a valid value (01 to 31). | | | | | | | |

Table 17 Weekday/Date Alarm (0x09h).

6.4. PERIODIC COUNTDOWN TIMER CONTROL REGISTERS

0Ah – Timer Value 0. This register is used to set the lower 8 bits of the Timer Value (preset value) for the Periodic Countdown Timer. This value will be reloaded into the Countdown Timer when it reaches zero if the TRPT bit is 1. This allows for periodic timer interrupts (see calculation below). Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------|------------|---|-------|-------|-------|-------|-------|-------|-------|
| 0Ah | Timer Value 0 | R/WP | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | Timer Value 0 | 00h to FFh | The Timer Value for the Periodic Countdown Timer in binary format (lower 8 bit) (see Use of the Periodic Countdown Timer Interrupt). When read, only the preset value is returned and not the actual value. When the Periodic Countdown Timer Interrupt function is not used, register 0Ah can be used as RAM byte. | | | | | | | |

Table 18 Timer Value 0 (0x0Ah).

0Bh – Timer Value 1. This register is used to set the upper 4 bits of the Timer Value (preset value) for the Periodic Countdown Timer. This value will be reloaded into the Countdown Timer when it reaches zero if the TRPT bit is a 1. This allows for periodic timer interrupts (see calculation below). Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------|----------|---|-------|-------|-------|-------|-------|-------|-------|
| 0Bh | Timer Value 1 | R/WP | ○ | ○ | ○ | ○ | 2048 | 1024 | 512 | 256 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:4 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 3:0 | Timer Value 1 | 0h to Fh | The Timer Value for the Periodic Countdown Timer in binary format (upper 4 bit) (see Use of the Periodic Countdown Timer Interrupt). When read, only the preset value is returned and not the actual value. | | | | | | | |

Table 19 Timer Value 1 (0x0Bh).

Countdown Period in seconds:

$$\text{Countdown Period} = \frac{\text{Timer Value}}{\text{Timer Clock Frequency}}$$

0Ch – Timer Status 0. This register holds the lower 8 bits of the current value of the Periodic Countdown Timer. It is read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 0Ah | Timer Value 0 | R/WP | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | Timer Value 0 | 00h to FFh | The Timer Value for the Periodic Countdown Timer in binary format (lower 8 bit) (see Use of the Periodic Countdown Timer Interrupt). When read, only the preset value is returned and not the actual value. When the Periodic Countdown Timer Interrupt function is not used, register 0Ah can be used as RAM byte. | | | | | | | |

Table 20 Timer Status 0 (0x0Ch).

0Dh – Timer Status 1 shadow. This register holds the upper 4 bits of the current value of the Periodic Countdown Timer. It is read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 0Dh | Timer Status 1 | R | ○ | ○ | ○ | ○ | 2048 | 1024 | 512 | 256 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:4 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 3:0 | Timer Status 1 | 0h to Fh | The current value of the Periodic Countdown Timer in binary format (upper 4 bit) (see Use of the Periodic Countdown Timer Interrupt). | | | | | | | |

Table 21 Timer Status 1 shadow (0x0Dh).

When TE bit is set to 1, reading the Timer Status 0 value updates the Timer Status 1 shadow register. Reading Timer Status 1 will return the Timer Status 1 shadow register value, memorized during Timer Status 0 read. When a 0 is written to the TE bit, the Timer Status 0 and Timer Status 1 registers store the last updated value.

6.5. CONFIGURATION REGISTERS

0Eh – Status. This register is used to detect the occurrence of various interrupt events and reliability problems in internal data. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | | |
|---------|----------|--|--|-------|-------|-------|-------|-------|-------|-------|--|--|
| 0Eh | Status | R/WP | EEbusy | CLKF | BSF | UF | TF | AF | EVF | PORF | | |
| | Reset | | 1 → 0 | 0 | 0 | 0 | 0 | 0 | X | 1 | | |
| Bit | Symbol | Value | Description | | | | | | | | | |
| 7 | EEbusy | EEPROM Memory Busy Status Bit – (Read Only) (see EEPROM READ/WRITE) | | | | | | | | | | |
| | | 0 | The transfer is finished. | | | | | | | | | |
| | | 1 | Indicates that the EEPROM is currently handling a read or write request and will ignore any further commands until the current one is finished. At power up a refresh is automatically generated. The time of this first refreshment is ~66 ms. After the refreshment is finished; EEbusy is cleared to 0 automatically. | | | | | | | | | |
| 6 | CLKF | Clock Output Interrupt Flag (see Programmable Clock Output) | | | | | | | | | | |
| | | 0 | No event detected. When cleared to 0 the frequency output will stop depending on CLKS _Y and CLKOUT settings. | | | | | | | | | |
| | | 1 | If set to 0 beforehand, indicates the occurrence of an interrupt driven clock output on CLKOUT pin. The value 1 is retained until a 0 is written by the user. | | | | | | | | | |
| 5 | BSF | Backup Switch Flag (see Automatic Backup Switchover Function) | | | | | | | | | | |
| | | 0 | No backup switchover detected. At power up (POR) this flag is automatically cleared to 0. When the backup switchover function is disabled (PM field = 00) BSF is always logic 0. | | | | | | | | | |
| | | 1 | If set to 0 beforehand, indicates that a switchover from main power V _{DD} to V _{BACKUP} has occurred. The value 1 can be cleared by writing a 0 to the bit if RTC module is in VDD Power state. Caution: The EVF flag is also set by an event of the Backup Switchover function when bits TSS and TSE are set to 1. | | | | | | | | | |
| 4 | UF | Periodic Time Update Flag (see Periodic Time Update Interrupt Function) | | | | | | | | | | |
| | | 0 | No event detected. | | | | | | | | | |
| | | 1 | If set to 0 beforehand, indicates the occurrence of a Periodic Time Update Interrupt event. The value 1 is retained until a 0 is written by the user. | | | | | | | | | |
| 3 | TF | Periodic Countdown Timer Flag (see Periodic Countdown Timer Interrupt Function) | | | | | | | | | | |
| | | 0 | No event detected. | | | | | | | | | |
| | | 1 | If set to 0 beforehand, indicates the occurrence of a Periodic Countdown Timer Interrupt event. The value 1 is retained until a 0 is written by the user. | | | | | | | | | |
| 2 | AF | Alarm Flag (see Alarm Interrupt Function) | | | | | | | | | | |
| | | 0 | No event detected. | | | | | | | | | |
| | | 1 | If set to 0 beforehand, indicates the occurrence of an Alarm Interrupt event. The value 1 is retained until a 0 is written by the user. | | | | | | | | | |
| 1 | EVF | Event Flag (see External Event Function) | | | | | | | | | | |
| | | X | At POR, the default value depends on the voltage on the EVI pin and has to be cleared by writing a 0 to the bit. At POR EHL = 0, the low level is regarded as an External Event Interrupt. At POR, EVF = 0, no LOW level was detected on EVI pin. At POR, EVF = 1, LOW level was detected on EVI pin. | | | | | | | | | |
| | | 0 | No event detected. | | | | | | | | | |
| 0 | PORF | Power On Reset Flag | | | | | | | | | | |
| | | 0 | No voltage drop detected. | | | | | | | | | |
| | | 1 | If set to 0 beforehand, indicates a voltage drop below V _{POR} . The data in the device are no longer valid and all registers must be initialized. The value 1 is retained until a 0 is written by the user. At startup (POR) the value is set to 1, the user has to write 0 to the flag to use it. | | | | | | | | | |

Table 22 Status (0x0Eh).

0Fh – Control 1. This register is used to specify the target for the Alarm Interrupt function and the Periodic Time Update Interrupt function and to select or set operations for the Periodic Countdown Timer. Read: Always readable. Write: Can be write-protected by password. Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|-------------------------|------------------|---|-------|-------|-------------|--|-------|-------|-------|
| 0Fh | Control 1 | R/WP | TRPT | - | WADA | USEL | EERD | TE | TD | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | TRPT | | Timer Repeat bit. Specifies either Single or Repeat Mode for the Periodic Countdown Timer Interruption function (see Periodic Countdown Timer Interrupt Function) | | | | | | | |
| | | 0 | Single Mode is selected. When the Countdown Timer is enabled (TE = 1) it will halt when it reaches zero and TE is automatically cleared.– Default value | | | | | | | |
| | | 1 | Repeat Mode is selected. When the Countdown Timer is enabled (TE = 1) it reloads the value from the Timer Value registers upon reaching 0, and continues counting. | | | | | | | |
| 6 | - | 0 | Bit not implemented. Will return a 0 when read. | | | | | | | |
| 5 | WADA | | Weekday Alarm / Date Alarm selection bit. This bit is used to specify either the Weekday or Date as the source for the Alarm Interrupt function (see Alarm Interrupt Function). | | | | | | | |
| | | 0 | Weekday is the source for the Alarm Interrupt function. – Default value | | | | | | | |
| | | 1 | Date is the source for the Alarm Interrupt function. | | | | | | | |
| 4 | USEL | | Update Interrupt Select bit. Specifies either Second or Minute update for the Periodic Time Update Interrupt function. When 1 is written to the RESET bit the interrupt function is retarded (see Periodic Time Update Interrupt Function). | | | | | | | |
| | | 0 | Second update (Auto reset time $t_{RTN2} = 500$ ms). – Default value | | | | | | | |
| | | 1 | Minute update (Auto reset time $t_{RTN2} = 7.813$ ms). | | | | | | | |
| 3 | EERD | | EEPROM Memory Refresh Disable bit. When 1, disables the automatic refresh of the Configuration Registers from the non-volatile EEPROM Memory (see Refresh (All Configuration EEPROM → RAM)). | | | | | | | |
| | | 0 | Refresh is active. All data in the Configuration Registers are refreshed by the data stored in the EEPROM each 24 hours, at date increment (at the beginning of the last second before midnight). The time of this automatic refreshment is $t_{AREFR} = \sim 3.5$ ms. Refresh is only active when RTC is not in VBACKUP mode.– Default value | | | | | | | |
| | | 1 | Refresh is disabled. | | | | | | | |
| 2 | TE | | Periodic Countdown Timer Enable bit. This bit controls the start/stop setting for the Periodic Countdown Timer Interruption function (see Periodic Countdown Timer Interrupt Function). | | | | | | | |
| | | 0 | Stops the Periodic Countdown Timer Interrupt function. TE is also automatically cleared when Single Mode is selected (TRPT = 0) and when the Countdown Timer reaches zero. – Default value | | | | | | | |
| | | 1 | Starts the Periodic Countdown Timer Interrupt function (a countdown starts from the preset value set in Timer Value registers). | | | | | | | |
| 1:0 | TD | 00 to 11 | Timer Clock Frequency selection. Sets the countdown source clock for the Periodic Countdown Timer Interrupt function. With this setting the Auto reset time t_{RTN1} is also defined. When the clock source has been set to Second update (1 Hz) or Minute update (1/60 Hz), the timing of both, countdown and interrupts, is coordinated with the clock update timing. When 1 is written to the RESET bit, the interrupt function is retarded. See Table 23 Control 1 (0x0Fh) (see also Periodic Countdown Timer Interrupt Function). | | | | | | | |
| TD Value | Timer Clock Frequency | Countdown period | | | | t_{RTN1} | RESET bit | | | |
| 00 | 4096 Hz – Default value | 244.14 μ s | | | | 122 μ s | When 1 is written to the RESET bit, the interrupt function is retarded | | | |
| 01 | 64 Hz | 15.625 ms | | | | 7.813 ms | | | | |
| 10 | 1 Hz | 1 s | | | | | | | | |
| 11 | 1/60 Hz | 60 s | | | | | | | | |

Table 23 Control 1 (0x0Fh)

10h – Control 2. This register is used to control the interrupt event output for the $\overline{\text{INT}}$ pin, the stop/start status of clock and calendar operations, the interrupt controlled clock output on CLKOUT pin, the hour mode and the time stamp enable. Read: Always readable. Write: Can be write-protected by password. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 10h | Control 2 | R/WP | TSE | CLKIE | UIE | TIE | AIE | EIE | 12_24 | RESET |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Value | Description |
|-----|--------|-------|---|
| 7 | TSE | | Time Stamp Enable bit (see TIME STAMP Function) |
| | | 0 | Disables the time stamp function. – Default value |
| | | 1 | Enables the Time stamp function. |
| 6 | CLKIE | | Interrupt Controlled Clock Output Enable bit. When enabled, it is possible to wake-up an external system by outputting a frequency. (see Programmable Clock Output) |
| | | 0 | Disabled – Default value |
| 1 | | 1 | When set to 1, the clock output on CLKOUT pin is automatically enabled when an interrupt occurs, based on the Clock Interrupt Mask Register (12h) and according to clock setting defined by the FD field. This function is disabled in VBACKUP Power state. |
| | | | |
| 5 | UIE | | Periodic Time Update Interrupt Enable bit (see Periodic Time Update Interrupt Function) |
| | | 0 | No interrupt signal is generated on $\overline{\text{INT}}$ pin when a Periodic Time Update event occurs or the signal is cancelled on $\overline{\text{INT}}$ pin. – Default value |
| 1 | | 1 | An interrupt signal is generated on $\overline{\text{INT}}$ pin when a Periodic Time Update event occurs. The low-level output signal is automatically cleared after $t_{\text{RTN2}} = 500$ ms (Second update) or $t_{\text{RTN2}} = 7.813$ ms (Minute update). |
| | | | |
| 4 | TIE | | Periodic Countdown Timer Interrupt Enable bit(see Periodic Time Update Interrupt Function) |
| | | 0 | No interrupt signal is generated on $\overline{\text{INT}}$ pin when a Periodic Countdown Timer event occurs or the signal is cancelled on $\overline{\text{INT}}$ pin. – Default value |
| 1 | | 1 | An interrupt signal is generated on $\overline{\text{INT}}$ pin when a Periodic Countdown Timer event occurs. The low-level output signal is automatically cleared after $t_{\text{RTN1}} = 122$ μs (TD = 00) or $t_{\text{RTN1}} = 7.813$ ms (TD = 01, 10, 11). |
| | | | |
| 3 | AIE | | Alarm Interrupt Enable bit (see Alarm Interrupt Function) |
| | | 0 | No interrupt signal is generated on $\overline{\text{INT}}$ pin when an Alarm event occurs or the signal is cancelled on $\overline{\text{INT}}$ pin. – Default value |
| 1 | | 1 | An interrupt signal is generated on $\overline{\text{INT}}$ pin when an Alarm event occurs. This setting is retained until the AF flag is cleared to 0 (no automatic cancellation). |
| | | | |
| 2 | EIE | | Event Interrupt Enable bit(see External Event Function and Interrupt Scheme) |
| | | 0 | No interrupt signal is generated on $\overline{\text{INT}}$ pin when an External Event on EVI pin occurs, or when an Automatic Backup Switchover occurs when TSS and TSE are set to 1, or the signal on $\overline{\text{INT}}$ pin is cleared. – Default value |
| 1 | | 1 | An interrupt signal is generated on $\overline{\text{INT}}$ pin when an External Event on EVI pin occurs, or when an Automatic Backup Switchover occurs when TSS and TSE are set to 1. The signal on $\overline{\text{INT}}$ pin is retained until the EVF flag is cleared to 0 (no automatic cancellation). |
| | | | |
| 1 | 12_24 | | 12 or 24 hour mode (see Clock Registers and Alarm Registers) |
| | | 0 | 24 hour mode is selected (0 to 23). – Default value |
| 1 | | 1 | 12 hour mode is selected (1 to 12). |
| | | | |
| 0 | RESET | | Reset bit. This bit is used for a software-based time adjustment (synchronizing)(see RESET bit Function). |
| | | 1 | When 1 is written to the RESET bit, the clock prescaler from 4096 Hz to 1 Hz is reset. An eventual present memorized 1 Hz update is also reset. The RESET bit is then automatically cleared. Because the upper two stages of the prescaler are not reset (16.384 kHz and 8192 Hz) and the I ² C interface is asynchronous, the first 1 Hz period after synchronization will be 0 to 244 μs shorter than 1 second. Resetting the prescaler will have an influence on the length of the current clock period on all subsequent peripherals (clock and calendar, CLKOUT, timer clock, update timer clock, UNIX clock, EVI input filter). |

Table 24 Control 2 (0x10h).

11h – GP Bits. This register holds the bits for general purpose use (7 bits). Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|---|-------|-------|-------|-------|-------|-------|-------|
| 11h | GP Bits | R/WP | - | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | - | 0 | Bit not implemented. Will return a 0 when read. | | | | | | | |
| 6:0 | GPx | 0 or 1 | Register bits for general purpose use (7 bits). | | | | | | | |

Table 25 GP bits (0x11h).

12h – Clock Interrupt Mask. This register is used to select a predefined interrupt for automatic clock output. Setting a bit to 1 selects the corresponding interrupt. Multiple interrupts can be selected. After power on, no interrupt is selected (see [Clock Output Scheme](#)). Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------------|---|---|-------|-------|-------|-------|-------|-------|-------|
| 12h | Clock Interrupt Mask | R/WP | - | - | - | - | CEIE | CAIE | CTIE | CUIE |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:4 | | 0 | Bit not implemented. Will return a 0 when read. | | | | | | | |
| 3 | CEIE | Clock output when Event Interrupt bit. The source for the Event Interrupt can be the External Event from EVI pin or the Automatic Backup Switchover (see Interrupt Scheme). | | | | | | | | |
| | | 0 | Disabled – Default value | | | | | | | |
| | | 1 | Enabled. Internal signal EI is selected. | | | | | | | |
| 2 | CAIE | Clock output when Alarm Interrupt bit. | | | | | | | | |
| | | 0 | Disabled – Default value | | | | | | | |
| | | 1 | Enabled. Internal signal AI is selected. | | | | | | | |
| 1 | CTIE | Clock output when Periodic Countdown Timer Interrupt bit. | | | | | | | | |
| | | 0 | Disabled – Default value | | | | | | | |
| | | 1 | Enabled: Internal signal TI is selected. | | | | | | | |
| 0 | CUIE | Clock output when Periodic Time Update Interrupt bit. | | | | | | | | |
| | | 0 | Disabled – Default value | | | | | | | |
| | | 1 | Enabled: Internal signal TI is selected. | | | | | | | |

Table 26 Clock Interrupt Mask (0x12h).

6.6. EVENT CONTROL REGISTER

13h – Event Control. This register controls the event detection on the EVI pin. Depending of the EHL bit a high or a low signal can be detected. Moreover a digital glitch filtering can be applied to the EVI signal by selecting a sampling period in the ET field. Furthermore this register holds control functions for the Time Stamp data. And the switching over to VBACKUP Power state can be selected as source for an event. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|---------|---|---|--|-------|-------|-------|-------|-------|-------|-------|--|
| 13h | Event Control | R/WP | ○ | EHL | ET | | ○ | TSR | TSOW | TSS | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Bit | Symbol | Value | Description | | | | | | | | |
| 7 | ○ | 0 | Read only. Always 0. | | | | | | | | |
| 6 | EHL | Event High/Low detection Select (see External Event Function) | | | | | | | | | |
| | | 0 | The low level (negative edge) is regarded as the External Event on pin EVI. – Default value | | | | | | | | |
| 1 | The high level (positive edge) is regarded as the External Event on pin EVI. | | | | | | | | | | |
| 5:4 | ET | Event Filtering Time set. Applies a digital filtering to the EVI pin by sampling the EVI signal. Edge and stable steady state are detected when ET = 01, 10 or 11 (see Use of the External Event Function) | | | | | | | | | |
| | | 00 | No filtering. Edge detection (minimal pulse time is 30.5 μs). – Default value | | | | | | | | |
| | | 01 | 3.9 ms sampling period (256 Hz). | | | | | | | | |
| | | 10 | 15.6 ms sampling period (64 Hz). | | | | | | | | |
| 11 | 125 ms sampling period (8 Hz). | | | | | | | | | | |
| 3 | ○ | 0 | | | | | | | | | |
| 2 | TSR | Time Stamp Reset bit (see TIME STAMP Function) | | | | | | | | | |
| | | 0 | Disables the Time Stamp Reset. – Default value | | | | | | | | |
| 1 | When this bit is set to 1, all seven time stamp registers (Count TS to Year TS) are cleared to 00h. The TSR bit is automatically cleared to 0 after performing the reset. | | | | | | | | | | |
| 1 | TSOW | Time Stamp Overwrite bit. Controls the overwrite function of the TS registers. Exception: The counter Count TS is always working, independent of the settings of the overwrite bit TSOW. (see TIME STAMP Function) | | | | | | | | | |
| | | 0 | The time stamp of the first occurred event is recorded and remains in TS registers. To initialize or reinitialize the first event detection function, the EVF has to be cleared. – Default value | | | | | | | | |
| 1 | The time stamp of the last occurred event is recorded and TS registers are overwritten. The EVF flag does not need to be cleared. | | | | | | | | | | |
| 0 | TSS | Time Stamp Source Selection bit (see TIME STAMP Function) | | | | | | | | | |
| | | 0 | A time stamp is generated (if TSE = 1) when an External Event on EVI pin occurs – Default value | | | | | | | | |
| 1 | A time stamp is generated (if TSE = 1) when the circuit goes to VBACKUP Power state. | | | | | | | | | | |

Table 27 Event Control (0x13h).

6.7. TIME STAMP REGISTERS

14h – Count TS. This register contains the number of occurrences of the corresponding event in standard binary format. The values range from 0 to 255. It is read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 14h | Count TS | R | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | Count TS | 0 to 255 | Number of occurrences of the corresponding event, coded in binary. In case of an overflow the counter starts again with 00h When bit TSE = 0, the counter stops counting events. When bit TSE = 1, the counter is increased when event occurs. The counter Count TS is always working, independent of the settings of the overwrite bit TSOW. The Count TS register is cleared to 00h when a 1 is written to the reset bit TSR (see TIME STAMP Function) | | | | | | | |

Table 28 Count TS (0x14h).

15h – Seconds TS. This register holds a recorded Time Stamp of the Seconds register, in two binary coded decimal (BCD) digits. The values are from 00 to 59. It is read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 15h | Seconds TS | R | 0 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | 0 | 0 | Read only. Always 0. | | | | | | | |
| 6:0 | Seconds TS | 00 to 59 | Holds a recorded Time Stamp of the Seconds register, coded in BCD format. When enabled (bit TSE = 1), Depending on the setting of the TSOW bit it contains the time stamp of the first or last occurred event. The Seconds TS register is cleared to 00h when a 1 is written to the reset bit TSR. | | | | | | | |

Table 29 Seconds TS (0x15h).

16h – Minutes TS. This register holds a recorded Time Stamp of the Minutes register, in two binary coded decimal (BCD) digits. The values are from 00 to 59. It is read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 16h | Minutes TS | R | 0 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | 0 | 0 | Read only. Always 0. | | | | | | | |
| 6:0 | Minutes TS | 00 to 59 | Holds a recorded Time Stamp of the Minutes register, coded in BCD format. When enabled (bit TSE = 1), Depending on the setting of the TSOW bit it contains the time stamp of the first or last occurred event. The Minutes TS register is cleared to 00h when a 1 is written to the reset bit TSR. | | | | | | | |

Table 30 Minutes TS (0x16h).

17h – Hours TS. This register holds a recorded Time Stamp of the Hours register, in two binary coded decimal (BCD) digits. If the 12_24 bit is cleared (default) (see **Configuration Registers**, 10h – Control 2) the values will be from 0 to 23. If the 12_24 bit is set, the hour values will range from 1 to 12 and the AMPM bit will be 0 for AM hours and 1 for PM hours. It is read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 17h | Hours TS (24 hour mode) – default value | R | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| | Hours TS (12 hour mode) | | AMPM | 10 | 8 | 4 | 2 | 1 | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Hours TS (24 hour mode) – default value | | | |
|---|---|---------|--|
| Bit | Symbol | Value | Description |
| 7:6 | ○ | 0 | Read only. Always 0. |
| 5:0 | Hours TS (24 hour mode) – default value | 0 to 23 | Holds a recorded Time Stamp of the Hours register, coded in BCD format. When enabled (bit TSE = 1), Depending on the setting of the TSOW bit it contains the time stamp of the first or last occurred event. The Hours TS register is cleared to 00h when a 1 is written to the reset bit TSR. |

| Hours TS (12 hour mode) | | | |
|-------------------------|-------------------------|---------|--|
| Bit | Symbol | Value | Description |
| 7:6 | ○ | 0 | Read only. Always 0. |
| 5 | AMPM | 0 | AM hours, from the recorded Time Stamp of the Hours register. |
| | | 1 | PM hours, from the recorded Time Stamp of the Hours register. |
| 4:0 | Hours TS (12 hour mode) | 1 to 12 | Holds a recorded Time Stamp of the Hours register, coded in BCD format. When enabled (bit TSE = 1), Depending on the setting of the TSOW bit it contains the time stamp of the first or last occurred event. The Hours TS register is cleared to 00h when a 1 is written to the reset bit TSR. |

Table 31 Hours TS (0x17h).

18h – Date TS. This register holds a recorded Time Stamp of the Date register, in two binary coded decimal (BCD) digits. The values will range from 01 to 31. It is read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 18h | Date TS | R | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Value | Description |
|-----|---------|----------|---|
| 7:6 | ○ | 0 | Read only. Always 0. |
| 5:0 | Date TS | 01 to 31 | Holds a recorded Time Stamp of the Date register, coded in BCD format. When enabled (bit TSE = 1), Depending on the setting of the TSOW bit it contains the time stamp of the first or last occurred event. The Date TS register is cleared to 00h when a 1 is written to the reset bit TSR. After POR or when reset with bit TSR and when a Time Stamp is recorded, the value 00 will be automatically replaced by a valid value (01 to 31). |

Table 32 Date TS (0x18h).

19h – Month TS. This register holds a recorded Time Stamp of the Month register, in two binary coded decimal (BCD) digits. The values will range from 01 to 12. It is read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 19h | Month TS | R | ○ | ○ | ○ | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:5 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 4:0 | Month TS | 01 to 12 | Holds a recorded Time Stamp of the Month register, coded in BCD format. When enabled (bit TSE = 1), Depending on the setting of the TSOW bit it contains the time stamp of the first or last occurred event. The Month TS register is cleared to 00h when a 1 is written to the reset bit TSR. After POR or when reset with bit TSR and when a Time Stamp is recorded, the value 00 will be automatically replaced by a valid value (01 to 12). | | | | | | | |

Table 33 Month TS (0x19h).

1Ah – Year TS. This register holds a recorded Time Stamp of the Year register, in two binary coded decimal (BCD) digits. Values will range from 00 to 99. It is read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 1Ah | Year TS | R | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | Year TS | 00 to 99 | Holds a recorded Time Stamp of the Year register, coded in BCD format. When enabled (bit TSE = 1), Depending on the setting of the TSOW bit it contains the time stamp of the first or last occurred event. The Year TS register is cleared to 00h when a 1 is written to the reset bit TSR. | | | | | | | |

Table 34 Year TS (0x1Ah).

6.8. UNIX TIME REGISTERS

The UNIX Time counter is a 32-bit counter with the value in binary format. The counter will roll-over to 00000000h when reaching FFFFFFFFh. The 4 counter registers are fully readable and writable. The counter source clock is the digitally tuned 1 Hz clock frequency. The UNIX Time counter increment is inhibited during I²C write access to the 4 UNIX Time registers to allow coherent data values (see **Setting and Reading the Time**). Read: Always readable. Write: Can be write-protected by password.

1Bh – UNIX Time 0. Bit 0 to 7 from 32-bit UNIX Time counter.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------------|------------|--------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 1Bh | UNIX Time 0 | R/WP | UNIX 0 [7:0] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | UNIX 0 [7:0] | 00h to FFh | Bit 0 to 7 from 32-bit UNIX counter. | | | | | | | |

Table 35 UNIX Time 0 (0x1Bh).

1Ch – UNIX Time 1. Bit 8 to 15 from 32-bit UNIX Time counter.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------|------------|---------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 1Ch | UNIX Time 1 | R/WP | UNIX 1 [15:8] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | UNIX 1 [15:8] | 00h to FFh | Bit 8 to 15 from 32-bit UNIX counter. | | | | | | | |

Table 36 UNIX Time 1 (0x1Ch).

1Dh – UNIX Time 2. Bit 16 to 23 from 32-bit UNIX Time counter.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 1Dh | UNIX Time 2 | R/WP | UNIX 2 [23:16] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | UNIX 2 [23:16] | 00h to FFh | Bit 16 to 23 from 32-bit UNIX counter. | | | | | | | |

Table 37 UNIX Time 2 (0x1Dh).

1Eh – UNIX Time 3. Bit 24 to 31 from 32-bit UNIX Time counter.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 1Eh | UNIX Time 3 | R/WP | UNIX 3 [31:24] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | UNIX 3 [31:24] | 00h to FFh | Bit 24 to 31 from 32-bit UNIX counter. | | | | | | | |

Table 38 UNIX Time 3 (0x1Eh).

6.9. RAM REGISTERS

Two free RAM bytes, which can be used for any purpose, for example, status bytes of the system.

1Fh – User RAM 1. This register holds the bits for general purpose use. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|------------|-------------|-------|-------|-------|-------|-------|-------|-------|
| 1Fh | User RAM 1 | R/WP | RAM 1 | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | RAM 1 | 00h to FFh | RAM 1 data | | | | | | | |

Table 39 User RAM 1 (0x1Fh)

20h – User RAM 2. This register holds the bits for general purpose use. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|------------|-------------|-------|-------|-------|-------|-------|-------|-------|
| 20h | User RAM 2 | R/WP | RAM 2 | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | RAM 2 | 00h to FFh | RAM 2 data | | | | | | | |

Table 40 User RAM 2 (0x20h)

6.10. PASSWORD REGISTERS

After a Power up and the first refreshment of ~66 ms, the PW 0 to PW 3 registers are reset to 00h.

When enabled by writing 255 into the EEPROM Password Enable register EEPWE (EEPROM 30h), the Password registers are used to be written with the 32-Bit Password necessary to be able to write into all writable registers (for time and configuration registers). This 32-Bit Password is compared to the 32 bits stored in the EEPROM Password registers EEPW 0 to EEPW 3 (EEPROM 31h to 34h) (see [EEPROM Password Registers](#)).

21h – Password 0. Bit 0 to 7 from 32-bit Password. Write only. Returns 0 when read.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|------------|---------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 21h | Password 0 | W | PW 0 [7:0] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | PW 0 [7:0] | 00h to FFh | Bit 0 to 7 from 32-bit Password | | | | | | | |

Table 41 Password 0 (0x21h)

22h – Password 1. Bit 8 to 15 from 32-bit Password. Write only. Returns 0 when read.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------------|------------|----------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 22h | Password 1 | W | PW 1 [15:8] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | PW 1 [15:8] | 00h to FFh | Bit 8 to 15 from 32-bit Password | | | | | | | |

Table 42 Password 1 (0x22h)

23h – Password 2. Bit 16 to 23 from 32-bit Password. Write only. Returns 0 when read.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------------|------------|-----------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 23h | Password 2 | W | PW 2 [23:16] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | PW 2 [23:16] | 00h to FFh | Bit 16 to 23 from 32-bit Password | | | | | | | |

Table 43 Password 2 (0x23h)

24h – Password 3. Bit 24 to 31 from 32-bit Password. Write only. Returns 0 when read.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------------|------------|-----------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 24h | Password 3 | W | PW 3 [31:24] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | PW 3 [31:24] | 00h to FFh | Bit 24 to 31 from 32-bit Password | | | | | | | |

Table 44 Password 3 (0x24h)

6.11. EEPROM MEMORY CONTROL REGISTERS

See also [EEPROM READ/WRITE](#).

25h –EEPROM Address. This register holds the Address used for read or write from/to a single EEPROM Memory byte. Read: Always readable. Write: Can be write-protected by password

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 25h | EEPROM Address | R/WP | EEaddr | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEaddr | 00h to FFh | Address for direct read or write one EEPROM Memory byte. | | | | | | | |

Table 45 EEPROM Address (0x25h)

26h –EEPROM Data. This register holds the Data that are read from, or that are written to a single EEPROM Memory byte. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 26h | EEPROM Data | R/WP | EEdata | | | | | | | |
| | Reset | | X | X | X | X | X | X | X | X |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEdata | 00h to FFh | Data from direct read or for direct write to one EEPROM Memory byte. | | | | | | | |

Table 46 EEPROM Data (0x26h)

27h –EEPROM Commands. This register must be written with specific values, in order to read or write all (readable/writeable) configuration registers or to read or write from/to a single EEPROM Memory byte.

Before using this commands, the automatic refresh function has to be disabled (EERD = 1) and the busy status bit EEbusy has to indicate, that the last transfer has been finished (EEbusy = 0). Before entering the command 11h, 12h, 21h or 22h, EEcmd has to be written with 00h. Write only. It can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--|---|--|-------|-------|-------|-------|-------|-------|-------|
| 27h | EEPROM Commands | WP | EEcmd | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEcmd | Commands for EEPROM Memory (see EEPROM READ/WRITE) | | | | | | | | |
| | | 00h | First command must be 00h. – Default value | | | | | | | |
| | | 11h | Write to all Configuration EEPROM registers (Update). When writing a value of 11h, data from all (readable/writeable) configuration RAM bytes (address 30h to 37h) are written (stored) into the corresponding EEPROM bytes. | | | | | | | |
| | | 12h | Read all Configuration EEPROM registers (Refresh). When writing a value of 12h, data from all Configuration EEPROM bytes are read and copied into the corresponding RAM bytes (address 30h to 37h). | | | | | | | |
| | | 21h | Write to one EEPROM byte (Configuration or User EEPROM). When writing a value of 21h, data from EEdata byte is written (stored) into the EEPROM byte with the address specified in EEaddr. (For Configuration EEPROM bytes (address 30h to 37h) and User EEPROM bytes (address 00h to 2Ah)). | | | | | | | |
| 22h | Read one EEPROM byte (from Configuration or User EEPROM). When writing a value of 22h, data from the EEPROM byte with the address specified in EEaddr is read and copied into the EEdata byte. (For Configuration EEPROM bytes (address 30h to 37h) and User EEPROM bytes (address 00h to 2Ah)). | | | | | | | | | |

Table 47 EEPROM Commands (0x27h)

6.12. ID REGISTER

28h – ID. This register holds the 4 bit Hardware Identification number (HID) and the 4 bit Version Identification number (VID).

The ID can be used to monitor a hardware modification and the version in the production line. It is read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|---------|---------------------------------|-------|-------|-------|---------------------|-------|-------|-------|
| 28h | ID | R | HID | | | | VID | | | |
| | Reset | | Preconfigured Value | | | | Preconfigured Value | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:4 | HID | 0 to 15 | Hardware Identification number. | | | | | | | |
| 3:0 | VID | 0 to 15 | Version Identification number. | | | | | | | |

Table 48 ID Register (0x28h)

6.13. CONFIGURATION EEPROM WITH RAM MIRROR REGISTERS

All Configuration EEPROM at addresses 2Bh and 30h to 37h are memorized in the EEPROM and mirrored in the RAM.

6.13.1. EEPROM RESERVED

2Bh – EEPROM Reserved. Read: Always readable. Write: Can be write-protected by password. It must not be overwritten.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------------|-------|---|-------|-------|-------|-------|-------|-------|-------|
| 2Bh | EEPROM RESERVED | R/WP | RESERVED (Must not be overwritten) | | | | | | | |
| | Default value on delivery | | Preconfigured Value | | | | | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | RESERVED | | Preconfigured Value – It must not be overwritten. | | | | | | | |

Table 49 EEPROM Reserved (0x2Bh)

6.13.2. EEPROM PASSWORD ENABLE REGISTER

After a Power up and the first refreshment of ~66 ms, the Password Enable value EEPWE is copied from the EEPROM. The default value preset on delivery is 00h.

30h – EEPROM Password Enable. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 30h | EEPROM Password Enable | R/WP | EEPWE | | | | | | | |
| | Default value on delivery | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEPWE | | EEPROM Password Enable | | | | | | | |
| | | 0 to 254 | Password function disabled. When writing a value not equal 255, the password function is disabled. – 00h is default value preset on delivery | | | | | | | |
| | | 255 | Password function enabled. When writing a value of 255, the Password registers (21h to 24h) can be used to enter the 32-bit Password. | | | | | | | |

Table 50 EEPROM Password Enable (0x30h)

6.14. EEPROM PASSWORD REGISTERS

After a Power up and the first refreshment of ~66 ms, the EEPROM Password values EEPW 0 to EEPW 3 are copied from the EEPROM. The default values preset on delivery are 00h.

31h – EEPROM Password 0. Bit 0 to 7 from 32-bit EEPROM Password. Write only. It can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 31h | EEPROM Password 0 | WP | EEPW 0 [7:0] | | | | | | | |
| | Default value on delivery | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEPW 0 [7:0] | 00h to FFh | Bit 0 to 7 from 32-bit EEPROM Password | | | | | | | |

Table 51 EEPROM Password 0 (0x31h)

32h – EEPROM Password 1. Bit 8 to 15 from 32-bit EEPROM Password. Write only. It can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------------|------------|---|-------|-------|-------|-------|-------|-------|-------|
| 32h | EEPROM Password 1 | WP | EEPW 1 [15:8] | | | | | | | |
| | Default value on delivery | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEPW 1 [15:8] | 00h to FFh | Bit 8 to 15 from 32-bit EEPROM Password | | | | | | | |

Table 52 EEPROM Password 1 (0x32h)

33h – EEPROM Password 2. Bit 16 to 23 from 32-bit EEPROM Password. Write only. It can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 33h | EEPROM Password 2 | WP | EEPW 2 [23:16] | | | | | | | |
| | Default value on delivery | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEPW 2 [23:16] | 00h to FFh | Bit 16 to 23 from 32-bit EEPROM Password | | | | | | | |

Table 53 EEPROM Password 2 (0x33h)

34h – EEPROM Password 3. Bit 24 to 31 from 32-bit EEPROM Password. Write only. It can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 34h | EEPROM Password 3 | WP | EEPW 3 [31:24] | | | | | | | |
| | Default value on delivery | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEPW 3 [31:24] | 00h to FFh | Bit 24 to 31 from 32-bit EEPROM Password | | | | | | | |

Table 54 EEPROM Password 3 (0x34h)

6.15. EEPROM CLKOUT REGISTER

35h – EEPROM CLKOUT. A programmable square wave output is available at CLKOUT pin. Operation is enabled by the CLKOE bit (see [Programmable Clock](#)). Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|--|-------|-------|-------|-------|-------|-------|-------|
| 35h | EEPROM CLKOUT | R/WP | CLKOE | CLKSY | - | - | PORIE | FD | | |
| | Default value on delivery | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | CLKOE | CLKOUT Enable bit (see Programmable Clock Output) | | | | | | | | |
| | | 0 | The CLKOUT pin is LOW. | | | | | | | |
| | | 1 | The clock output signal on CLKOUT pin is enabled. – Default value on delivery | | | | | | | |
| 6 | CLKSY | CLKOUT Synchronized enable/disable (see Synchronized Enable/Disable) | | | | | | | | |
| | | 0 | Disabled | | | | | | | |
| | | 1 | Enables the Synchronized enable/disable (by CLKOE) of the CLKOUT frequency. – Default value on delivery | | | | | | | |
| 5:4 | - | 0 | Bit not implemented. Will return a 0 when read. | | | | | | | |
| 3 | PORIE | Power On Reset Interrupt Enable bit(see POWER ON RESET Interrupt Function) | | | | | | | | |
| | | 0 | No interrupt signal is generated on \overline{INT} pin when a Power On Reset occurs or the signal is cancelled on \overline{INT} pin. – Default value on delivery | | | | | | | |
| | | 1 | An interrupt signal is generated on \overline{INT} pin when a Power On Reset occurs. This setting is retained until the PORF flag is cleared to 0 (no automatic cancellation). | | | | | | | |
| 2:0 | FD | 000 to 111 | CLKOUT Frequency Selection (see CLKOUT Frequency Selection) | | | | | | | |
| FD | CLKOUT Frequency Selection | | Effect when 1 is written to the RESET bit | | | | | | | |
| 000 | 32.768 kHz – Default value on delivery | | No effect | | | | | | | |
| 001 | 8192 Hz (1) | | No effect | | | | | | | |
| 010 | 1024 Hz (1) | | CLKOUT goes LOW | | | | | | | |
| 011 | 64 Hz (1) | | CLKOUT goes LOW | | | | | | | |
| 100 | 32 Hz (1) | | CLKOUT goes LOW | | | | | | | |
| 101 | 1 Hz (1) | | CLKOUT goes LOW | | | | | | | |
| 110 | Predefined periodic countdown timer interrupt (1) (2) | | CLKOUT goes LOW | | | | | | | |
| 111 | CLKOUT = LOW | | No effect | | | | | | | |
| (1) 8192 Hz to 1 Hz clock pulses and the timer interrupt pulses can be affected by compensation pulses (Frequency OFFSET Correction). (2) CLKSY bit has no effect. | | | | | | | | | | |

Table 55 EEPROM CLKOUT Register (0x35h).

6.16. EEPROM OFFSET REGISTER

The registers EEPROM Offset and EEPROM Backup hold the EEOffset value to digitally compensate the initial frequency deviation of the 32.768 kHz oscillator or for aging adjustment (see [Frequency OFFSET Correction](#)).

Caution: Bit EEOffset [0] is in the [EEPROM Backup](#) .

36h – EEPROM Offset. This register holds the upper 8 bits of the EEOffset value. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 36h | EEPROM Offset | R/WP | EEOffset [8:1] | | | | | | | |
| | Default value on delivery | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEOffset [8:1] | 00h to FFh | Bits 8 to 1 of the EEOffset [8:0] value. EEOffset defines correction pulses in steps. Each pulse introduces a deviation of 0.9537 ppm, the maximum range is from +243.2 ppm to -244.1 ppm. The value of 0.9537 ppm is based on a nominal 32.768 kHz clock (see Frequency OFFSET Correction) | | | | | | | |

Table 56 EEPROM Offset (0x36h)

6.17. EEPROM BACKUP REGISTER

37h – EEPROM Backup. This register is used to control the switchover function and the trickle charger and it holds bit 0 (LSB) of the EEOffset value. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------------|--|---|-------|-------|-------|-------|-------|-------|-------|
| 37h | EEPROM Backup | R/WP | EEOffset [0] | BSIE | TCE | FEDE | BSM | | TCR | |
| | Default value on delivery | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | EEOffset [0] | 0 to 1 | Bit 0 of the EEOffset [8:0] value. EEOffset defines correction pulses in steps. Each pulse introduces a deviation of 0.9537 ppm, the maximum range is from +243.2 ppm to -244.1 ppm. The value of 0.9537 ppm is based on a nominal 32.768 kHz clock (see Frequency OFFSET Correction) | | | | | | | |
| 6 | BSIE | Backup Switchover Interrupt Enable bit(see Automatic Backup Switchover Function and Automatic BACKUP Switchover Interrupt Function) | | | | | | | | |
| | | 0 | No interrupt signal is generated on $\overline{\text{INT}}$ pin when an Automatic Backup Switchover occurs or the signal is cancelled on $\overline{\text{INT}}$ pin.– Default value on delivery | | | | | | | |
| | | 1 | An interrupt signal is generated on $\overline{\text{INT}}$ pin when an Automatic Backup Switchover occurs. This setting is retained until the BSF flag is cleared to 0 (no automatic cancellation). | | | | | | | |
| 5 | TCE | Trickle Charger Enable bit (see Trickle Charger) | | | | | | | | |
| | | 0 | Disabled – Default value on delivery | | | | | | | |
| | | 1 | Enabled | | | | | | | |
| 4 | FEDE | Fast Edge Detection Enable bit (see Automatic Backup Switchover Function and Automatic BACKUP Switchover Interrupt Function) | | | | | | | | |
| | | 0 | Disabled. | | | | | | | |
| | | 1 | FEDE should always be set to 1. When the FEDE bit is 1, the Fast Edge Detection for the Automatic Backup Switchover function is enabled. A voltage with a rising or falling edge with a slew rate typically bigger than 7 V/ms can be recorded correctly on V_{DD} power supply pin and the Automatic Backup Switchover function is adapted to this specific situation. – Default value on delivery | | | | | | | |
| 3:2 | BSM | Backup Switchover Mode(see Automatic Backup Switchover Function and Automatic BACKUP Switchover Interrupt Function) To read/write to/from the EEPROM, the user has to disable the Backup Switchover function by setting the BSM field to 00 or 10 (see routine in EEPROM Read/Write Conditions) | | | | | | | | |
| | | 00 | Switchover Disabled. The automatic backup switchover function is disabled. Used when only one power supply is available (V_{DD}). V_{BACKUP} pin should be connected to ground. – Default value on delivery | | | | | | | |
| | | 01 | Enables the Direct Switching Mode (DSM). Switchover when $V_{DD} < V_{BACKUP}$. | | | | | | | |
| | | 10 | Standby Mode. When $V_{DD} < V_{BACKUP}$ the device enters the standby mode and does not draw any current from the backup source before it is powered up again from main supply V_{DD} . | | | | | | | |
| | | 11 | Enables the Level Switching Mode (LSM). Switchover when $V_{DD} < V_{BACKUP}$ AND $V_{DD} < V_{TH_LSM}$ (AND $V_{BACKUP} > V_{TH_LSM}$). | | | | | | | |
| 1:0 | TCR | Trickle Charger Series Resistance (see Trickle Charger) | | | | | | | | |
| | | 00 | TCR = 1 k Ω – Default value on delivery | | | | | | | |
| | | 01 | TCR = 3 k Ω | | | | | | | |
| | | 10 | TCR = 6 k Ω | | | | | | | |
| | | 11 | TCR = 11 k Ω | | | | | | | |

Table 57 EEPROM Backup Register (0x37h).

| EEOffset [8:0] | EEOffset correction value in decimal | Correction pulses in steps | CLKOUT frequency correction in ppm ^(*) |
|---------------------|--------------------------------------|----------------------------|---|
| 011111111 | 255 | 255 | 243.187 |
| 011111110 | 254 | 254 | 242.233 |
| : | : | : | : |
| 000000001 | 1 | 1 | 0.954 |
| 000000000 (default) | 0 | 0 | 0.000 |
| 111111111 | 511 | -1 | -0.954 |
| 111111110 | 510 | -2 | -1.907 |
| : | : | : | : |
| 100000001 | 257 | -255 | -243.187 |
| 100000000 | 256 | -256 | -244.141 |

(*)Each correction pulse corresponds to $1 / (32768 \times 32) = 0.9537$ ppm. The frequency deviation measured at CLKOUT pin can be compensated by computing the correction value EEOffset and writing it into the EEPROM Offset and EEPROM Backup registers (see **Frequency OFFSET Correction**).

Table 58 EEOffset Value (0x36h, 0x37h)

6.18. USER EEPROM

00h – 2Ah – User EEPROM.

43 Bytes of User EEPROM for general purpose storage are provided. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-------------|-------|--------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 00h to 2Ah | User EEPROM | R/WP | 43 Bytes of non-volatile User EEPROM | | | | | | | |

Table 59 User EEPROM (0x00h to 2Ah).

6.19. MANUFACTURER EEPROM

2Ch – 2Fh and 38h to 3Fh – Manufacturer EEPROM.

This registers are Protected. Not readable, but normal address pointer incrementing.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-----------------|-------|---|-------|-------|-------|-------|-------|-------|-------|
| 2Ch to 2Fh | EEPROM RESERVED | Prot. | 4 Bytes of non-volatile Manufacturer EEPROM | | | | | | | |
| 38h to 3Fh | EEPROM RESERVED | Prot. | 8 Bytes of non-volatile Manufacturer EEPROM | | | | | | | |

Table 60 Manufacturer EEPROM (0x2Ch to 2Fh and 38h to 3Fh).

6.20. REGISTER RESET VALUES SUMMARY
Reset values; RAM, Address 00h to 3Fh:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|----------------------------|-------|--|-------|-------|-------|---------------------|-------|-------|-------|
| 00h | Seconds | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01h | Minutes | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 02h | Hours (24h / 12h) | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 03h | Weekday | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 04h | Date | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 05h | Month | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 06h | Year | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 07h | Minutes Alarm | R/WP | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 08h | Hours Alarm (24h / 12h) | R/WP | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 09h | Weekday Alarm / Date Alarm | R/WP | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Ah | Timer Value 0 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Bh | Timer Value 1 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Ch | Timer Status 0 | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Dh | Timer Status 1 shadow | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Eh | Status | R/WP | 1 → 0 | 0 | 0 | 0 | 0 | 0 | X | 1 |
| 0Fh | Control 1 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10h | Control 2 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11h | GP Bits | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 12h | Clock Int. Mask | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 13h | Event Control | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14h | Count TS | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15h | Seconds TS | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16h | Minutes TS | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 17h | Hours TS | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 18h | Date TS | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 19h | Month TS | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Ah | Year TS | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Bh | UNIX Time 0 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Ch | UNIX Time 1 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Dh | UNIX Time 2 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Eh | UNIX Time 3 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Fh | User RAM 1 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 20h | User RAM 2 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 21h | Password 1 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 22h | Password 2 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 23h | Password 3 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 24h | Password 4 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 25h | EEPROM Addr. | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 26h | EEPROM Data | R/WP | X | X | X | X | X | X | X | X |
| 27h | EEPROM Com. | WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 28h | ID | R | Preconfigured Value | | | | Preconfigured Value | | | |
| 29h and 2Ah | Non-existing | | Non-existing RAM address (will be skipped by address pointer) | | | | | | | |
| 2Ch to 2Fh | RESERVED | Prot. | RESERVED (not readable, but normal address pointer incrementing) | | | | | | | |
| 38h to 3Fh | RESERVED | Prot. | RESERVED (not readable, but normal address pointer incrementing) | | | | | | | |

X = not defined

Table 61 Reset Values; RAM (00h to 3Fh).

Default values on delivery; Configuration EEPROM with RAM mirror, Address 2Bh and 30h to 37h:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 2Bh | EEPROM RESERVED | R/WP | X | X | X | X | X | X | X | X |
| 30h | EEPROM PW Enable | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 31h | EEPROM Password 0 | WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 32h | EEPROM Password 1 | WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 33h | EEPROM Password 2 | WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 34h | EEPROM Password 3 | WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 35h | EEPROM CLKOUT | R/WP | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 36h | EEPROM Offset | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 37h | EEPROM Backup | R/WP | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

X = not defined

Table 62 Configuration EEPROM (0x2Bh and 0x30h to 37h).

Default values on delivery; User EEPROM, Address 00h to 2Ah:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 00h to 2Ah | User EEPROM | R/WP | 00h | | | | | | | |

Table 63 Default values: User EEPROM (0x00h to 2Ah).

Default values on delivery; Manufacturer EEPROM, Address 2Ch to 2Fh and 38h to 3Fh:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-----------------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| 2Ch to 2Fh | EEPROM RESERVED | Prot.. | XXh | | | | | | | |
| 38h to 3Fh | EEPROM RESERVED | Prot.. | XXh | | | | | | | |

X = not defined

Table 64 Default values: Manufacturer EEPROM (0x2Ch to 2Fh and 38h to 3Fh).

EM3028 reset values after power on (RAM) and default values on delivery (EEPROM):

RAM, reset values:

| | | |
|-----------------------|---|--|
| Time (hh:mm:ss) | = | 00:00:00 |
| Date (YY-MM-DD) | = | 00-01-01 |
| Weekday | = | 0 |
| Hour mode | = | 24 hour mode (0 to 23) |
| Count TS | = | 0 (read only) |
| Time TS (hh:mm:ss) | = | 00:00:00 (read only) |
| Date TS (YY-MM-DD) | = | 00-00-00 (read only) |
| UNIX Time | = | 00000000h |
| Alarm function | = | disabled, weekday is selected |
| Timer function | = | disabled, Timer Frequency = 4096 Hz, Single Mode selected |
| Update function | = | Second update is selected |
| Ext. Event function | = | LOW level is regarded as External Event on pin EVI, filtering on EVI pin disabled, first event recorded is enabled |
| Time Stamp function | = | disabled, Ext. Event selected, Time Stamp overwrite disabled, Time Stamp Reset disabled |
| EEPROM Memory Refresh | = | enabled |
| Reset function | = | disabled |
| Interrupts | = | disabled |
| EEbusy status bit | = | 1 → 0 (1 for the time of ~66 ms, then it is cleared to 0 automatically) |
| EVF Flag | = | 0 or 1 (0 if High level is detected on EVI pin; 1 if Low level is detected) |
| PORF Flag | = | 1 (can be cleared by writing 0 to the bit) |
| Int. Controlled Clock | = | disabled, no interrupt selected |
| Password | = | 00000000h (write only) |
| EEPROM Address | = | 00h |
| EEPROM Data | = | XXh |
| EEPROM Commands | = | 00h (first command) (write only) |
| ID | = | Preconfigured Value (read only) |
| General Purpose Bit | = | 0 (7 bits) |
| User RAM 1, 2 | = | 00h (2 bytes) |

Configuration EEPROM with RAM mirror, default values on delivery:

| | | |
|--------------------------|---|---|
| EEPROM RESERVED | = | Preconfigured Value (must not be overwritten) |
| EEPROM Password Enable | = | disabled |
| EEPROM Password | = | 00000000h (write only) |
| CLKOUT | = | enabled, synchronization enabled, F = 32.768 kHz |
| Power On Reset Interrupt | = | disabled |
| EEOffset value | = | 0 (9 bits) |
| Backup Switchover | = | disabled, interrupt disabled, Fast Edge Detection enabled |
| Trickle charger | = | disabled, TCR = 1 kΩ selected |

User EEPROM, default values on delivery:

| | | |
|------------------------|---|-----|
| User EEPROM (43 Bytes) | = | 00h |
|------------------------|---|-----|

Manufacturer EEPROM, Address 2Ch to 2Fh and 38h to 3Fh, default values on delivery:

| | | |
|-----------------|---|-----------------|
| EEPROM RESERVED | = | XXh (protected) |
|-----------------|---|-----------------|

7. DETAILED FUNCTIONAL DESCRIPTION

7.1. POWER-ON-RESET (POR)

The power on reset (POR) is generated at start-up (see [Error! Reference source not found.](#)). All RAM registers including the Counter Registers are initialized to their reset values and the Configuration EEPROM registers with the RAM mirror registers are set to their preset default values. At power up a refresh of the RAM mirror values by the values in the Configuration EEPROM is automatically generated. The time of this first refreshment is ~66 ms. The EEbusy bit in the Status register (0Eh) can be used to monitor the status of the refreshment (see [Register Reset Values Summary](#)).

The Power On Reset Flag PORF indicates the occurrence of a voltage drop of the internal power supply voltage below V_{POR} threshold needed to cause the generation of the device POR. A PORF value of 1 indicates that the voltage had dropped below the threshold level V_{POR} and that the time information is corrupted. The value 1 is retained until a 0 is written by the user.

When PORIE bit (EEPROM 35h) is set and the PORF flag was cleared beforehand, an interrupt signal on \overline{INT} pin can be generated when a Power On Reset occurs (see [POWER ON RESET Interrupt Function](#)).

7.2. AUTOMATIC BACKUP SWITCHOVER FUNCTION

Basic Hardware Definitions:

- The EM3028 has two power supply pins.
 - V_{DD} is the main power supply input pin.
 - V_{BACKUP} is the backup power supply input pin.
- $V_{TH.LSM}$ is the backup switchover threshold voltage. The typical value is 2.0 V.
- A debounce logic provides a 122 μ s – 183 μ s debounce time t_{DEB} , which will filter V_{DD} oscillation when the backup switchover will switch back from V_{BACKUP} to V_{DD} .
- The FEDE bit (EEPROM 37h) should always be set to 1, so that Fast Edge Detection (≥ 7 V/ms) is always enabled. – Default value on delivery

Switchover Modes:

The EM3028 has four backup switchover modes. The desired mode can be selected by the BSM field in the Configuration EEPROM, see [EEPROM Backup Register](#):

- BSM = 00. Backup switchover disabled (default value on delivery), see [SWITCHOVER Disabled](#).
- BSM = 01. Direct Switching Mode (DSM): when $V_{DD} < V_{BACKUP}$, switchover occurs from V_{DD} to V_{BACKUP} without requiring V_{DD} to drop below $V_{TH.LSM}$, see [Direct Switching Mode \(DSM\)](#).
- BSM = 10. Standby mode: when $V_{DD} < V_{BACKUP}$ (backup battery charged, no V_{DD}), the device enters the standby mode and draw any current from the backup source, see [STANDBY MODE](#).
- BSM = 11. Level Switching Mode (LSM): when $V_{DD} < V_{BACKUP}$ AND $V_{DD} < V_{TH.LSM}$ (AND $V_{BACKUP} > V_{TH.LSM}$), switchover occurs from V_{DD} to V_{BACKUP} , see [Level Switching Mode \(LSM\)](#).
-

Function Overview:

When a valid backup switchover condition occurs (direct or level switching mode) and the internal power supply switches to the V_{BACKUP} voltage (VBACKUP Power state) the following sequence applies:

- The Backup Switch Flag BSF is set and, if BSIE bit is 1 (EEPROM 37h), an interrupt will be generated on \overline{INT} pin and remains as long as BSF is not cleared to 0. If BSIE is 0 no interrupt will be generated (see [Automatic BACKUP Switchover Interrupt Function](#)).
- The I²C-bus interface is automatically disabled (high impedance) and reset.
- EVI input remains active for interrupt generation, interrupt driven clock output and time stamp function
- CLKOUT pin is held LOW during VBACKUP Power state.
- The interrupt output pin \overline{INT} remains active in VBACKUP Power state for any previously configured interrupt condition.
- Going into VBACKUP Power state can be used as a time stamp condition (see [TIME STAMP Function](#)).
- The backup switchover condition can also be used to enable the clock output on CLKOUT pin automatically, when again in VDD Power state (see [Automatic BACKUP Switchover Interrupt Function](#)).

The Backup Switch Flag BSF can be cleared using the I²C-bus interface as soon as the circuit resumes from V_{BACKUP} Power state and switched back to V_{DD}.

Note: After the device has switched back from V_{BACKUP} Power state to V_{DD} Power state the I²C interface has to be reinitialized by sending a STOP followed by a START (see also **I²C-BUS in Switchover Condition**).

7.2.1. SWITCHOVER DISABLED

The automatic backup switchover function is disabled when the BSM field (EEPROM 37h) is set to 00 (default value on delivery). Used when only one power supply is available.

- The power supply is applied on V_{DD} pin.
- V_{BACKUP} pin must be tied to V_{SS} with a 10 kΩ resistor.
- The battery flag BSF is always logic 0.

7.2.2. DIRECT SWITCHING MODE (DSM)

This mode is selected with BSM = 01 (EEPROM 37h).

- If V_{DD} > V_{BACKUP} the internal power supply is V_{DD}.
- If V_{DD} < V_{BACKUP} the internal power supply is V_{BACKUP}.

The Direct Switching Mode is useful in systems where V_{DD} is higher than V_{BACKUP} at all times (for example, V_{DD} = 5.0 V, V_{BACKUP} = 3.5 V). If the V_{DD} and V_{BACKUP} values are similar (for example, V_{DD} = 3.3 V, V_{BACKUP} ≥ 3.0V), the Direct Switching Mode is not recommended.

In Direct Switching Mode, the power consumption is reduced compared to the Level Switching Mode (LSM) because the monitoring of V_{BACKUP} and V_{TH:LSM} is not performed (typical I_{VDD:DIRECT} = 95 nA).

Note that the circuit needs in worst case 2 ms to react when the mode is changed from Standby Mode or Backup Switchover Disabled to DSM.

Backup switchover in Direct Switching Mode and with Backup Switchover Interrupt enabled with BSIE = 1 (EEPROM 37h):

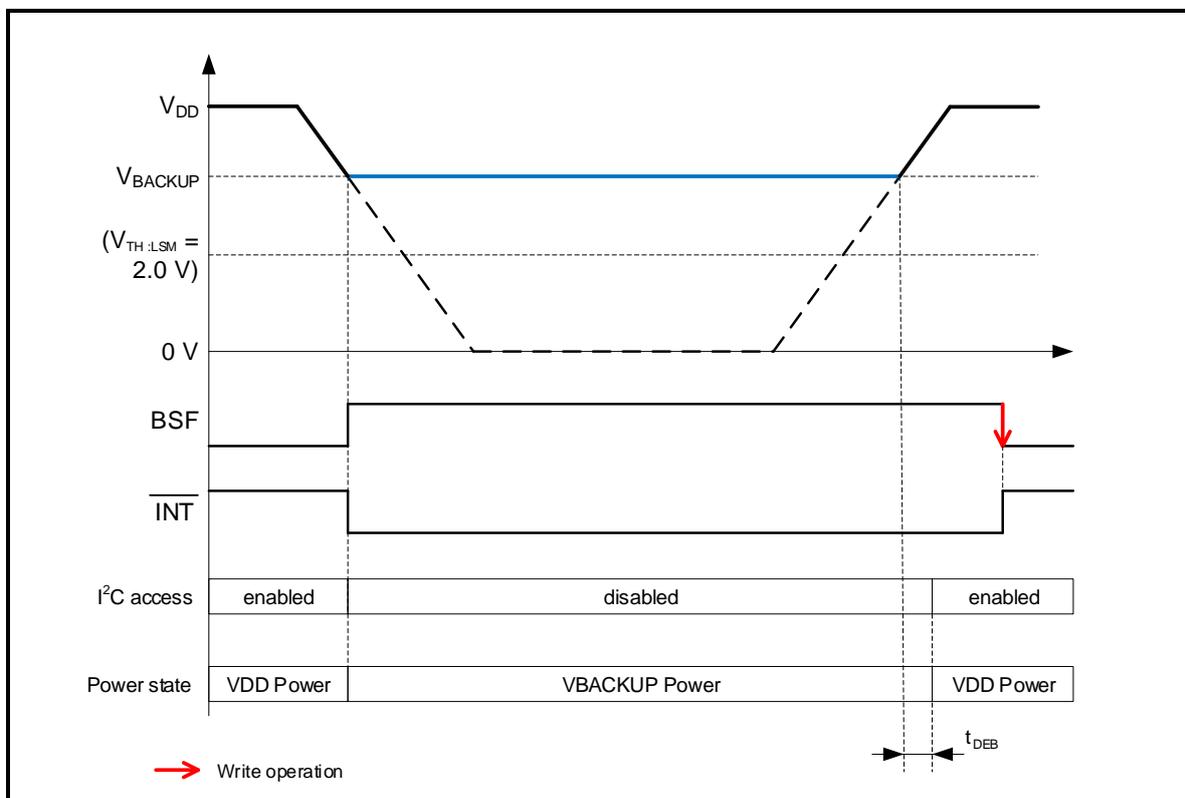


Figure 7-1 Direct Switching Mode

7.2.3. STANDBY MODE

When the device is first powered up from the backup supply (V_{BACKUP}) but without a main supply (V_{DD}), the device automatically enters the Standby Mode. In Standby Mode the device does not draw any power from the backup source until the device is powered up from the main power supply V_{DD} .

It is also possible to enter into Standby Mode when the device is already supplied by the main power supply V_{DD} and a backup supply V_{BACKUP} is connected. To enter the Standby Mode, the BSM field (EEPROM 37h) has to be set logic 10. Then the main power supply V_{DD} must be removed. As a result of it, the device enters the Standby Mode and does not draw any current from the backup supply before it is powered up again from main supply V_{DD} and set to a switchover mode.

7.2.4. LEVEL SWITCHING MODE (LSM)

This mode is selected with BSM = 11 (EEPROM 37h).

- If $V_{DD} > V_{BACKUP}$ OR $V_{DD} > V_{TH:LSM}$, the internal power supply is V_{DD} .
- If $V_{DD} < V_{BACKUP}$ AND $V_{DD} < V_{TH:LSM}$ (AND $V_{BACKUP} > V_{TH:LSM}$), the internal power supply is V_{BACKUP} .

In Level Switching Mode, the power consumption is increased compared to the Direct Switching Mode (DSM) because of the monitoring of V_{BACKUP} and $V_{TH:LSM}$ (typical $I_{VDD:LEVEL} = 115$ nA). See also typical characteristics in level switching mode in section Operating Parameters.

Note that the circuit needs in worst case 15.625 ms to react when the mode is changed from Standby Mode or Backup Switchover Disabled to LSM.

Backup switchover in Level Switching Mode and with Backup Switchover Interrupt enabled with BSIE = 1 (EEPROM 37h):

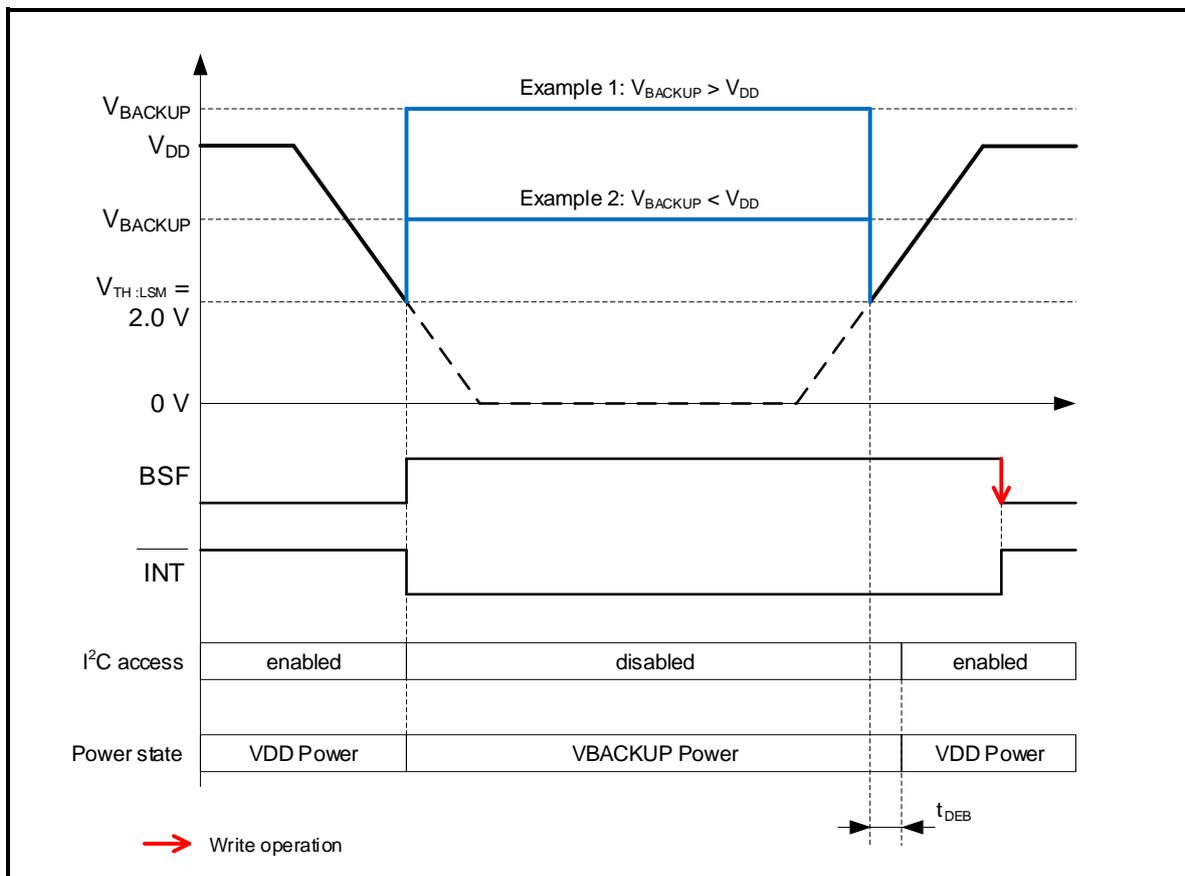


Figure 7-2 Level Switching Mode

7.3. TRICKLE CHARGER

The device supporting the V_{BACKUP} pin include a trickle charging circuit which allows a battery or supercapacitor connected to the V_{BACKUP} pin to be charged from the power supply connected to the V_{DD} pin. The circuit of the Trickle Charger is shown in the following Figure. The Trickle Charger is enabled with bit TCE (EEPROM 37h). The series current limiting resistor is selected by the TCR field (EEPROM 37h) as shown in the Figure (default value on delivery is 1 k Ω). A schottky diode, with a typical voltage drop of 0.25 V, is inserted in the charging path.

Trickle Charger:

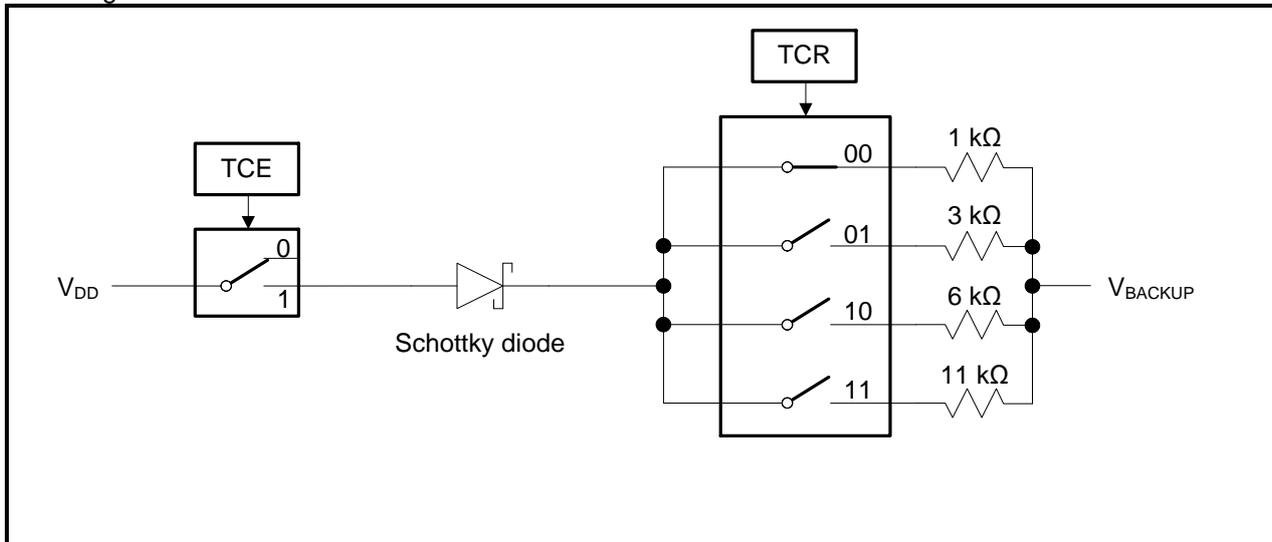


Figure 7-3 Trickle Charger configuration

The trickle charger is disabled when the device is in V_{BACKUP} Power state.

7.4. PROGRAMMABLE CLOCK OUTPUT

Six different frequencies or the countdown timer interrupt signal can be output on CLKOUT pin, the signal selection is done in the FD field (EEPROM 35h).

- 32.768 kHz, direct from Xtal oscillator, not tuned.
- 8192 Hz, 1024 Hz, 64 Hz, 32 Hz, 1 Hz; divided Xtal oscillator frequencies, digitally tuned according to the oscillator offset value EEOffset (EEPROM 36h and 37h).
- Timer interrupt is controlled by the Countdown Timer Control Registers and the Control 1 register.

The initial original clock signal (32.768 kHz) is initiated for switching on/off at his negative edge, a subsequently selected clock signal is taking over on his negative edge by controlling bits CLKF, CLKOE and FD field, in-between CLKOUT is tied to V_{SS} .

CLKOUT is tied to V_{SS} in V_{BACKUP} Power state independent of the CLKOUT configuration settings.

The frequency output can be controlled directly via the I²C-bus interface commands (normal operation) or can be interrupt driven to allow waking up an external system by supplying a clock.

At POR the synchronization function is active since the bit CLKS_Y is set to 1 (default), the 32.768 kHz frequency is output to CLKOUT pin since the bit CLKOE is set to 1 (default) and FD field is set to 000 (default). Hint: These are the default values on delivery, stored in the Configuration EEPROM with RAM mirror. To customize these POR values, the user can change the values in the Configuration EEPROM.

7.4.1. CLKOUT FREQUENCY SELECTION

A programmable square wave is available at pin CLKOUT. Operation is controlled by the FD field (EEPROM 35h). Frequencies from 32.768 kHz (Default value on delivery) to 1 Hz and countdown timer interrupt can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the crystal oscillator.

Pin CLKOUT is a push-pull output that is enabled at power on (Default value on delivery). CLKOUT can be disabled by setting CLKOE bit to 0 or FD field to 111. When disabled, the CLKOUT pin is LOW.

The RESET bit function can affect the CLKOUT signal depending on the selected frequency. When 1 is written to the RESET bit and the CLKOUT is enabled, the CLKOUT pin goes LOW for the frequencies 1024 Hz to 1 Hz (for more details, see **RESET bit Function**).

CLKOUT Frequency Selection:

| FD | CLKOUT Frequency Selection | When 1 is written to the RESET bit |
|-----|---|------------------------------------|
| 000 | 32.768 kHz –Default value on delivery | No effect |
| 001 | 8192 Hz (1) | No effect |
| 010 | 1024 Hz (1) | CLKOUT goes LOW |
| 011 | 64 Hz (1) | CLKOUT goes LOW |
| 100 | 32 Hz (1) | CLKOUT goes LOW |
| 101 | 1 Hz (1) | CLKOUT goes LOW |
| 110 | Predefined periodic countdown timer interrupt (1) (2) | CLKOUT goes LOW |
| 111 | CLKOUT = LOW | No effect |

(1) 8192 Hz to 1 Hz clock pulses and the timer interrupt pulses can be affected by correction pulses (see **Frequency OFFSET Correction**).

(2) CLKSYS bit has no effect.

Table 65 CLKOUT Frequency Selection

7.4.2. NORMAL CLOCK OUTPUT

Writing bit CLKOE to 1 will drive the selected frequency on CLKOUT, writing CLKOE to 0 will clear the selected frequency on CLKOUT.

7.4.3. INTERRUPT CONTROLLED CLOCK OUTPUT

Writing 1 to CLKIE the occurrence of the selected interrupt condition allows frequency output on CLKOUT. This function allows waking up an external system by outputting a clock.

Writing 0 to CLKIE will disable new interrupts from driving frequencies on CLKOUT, but if there is already an active interrupt driven frequency output (CLKF flag is set), the active frequency output will not be stopped. Writing the CLKF flag to 0 will clear the flag and frequency output will stop. Normal and Interrupt controlled clock output can be activated concurrently.

7.4.4. SYNCHRONIZED ENABLE/DISABLE

The enabled Synchronized CLKOUT Enable/Disable function (CLKSY = 1) consists of two sub-functions.

- Synchronized CLKOUT enable. For enabling clock output on CLKOUT pin the internal first negative clock edge of the selected clock source (FD field) is detected after CLKF or CLKOE are set.
- Synchronized CLKOUT disable. Clock output on CLKOUT will be disabled at the next negative clock edge of the selected clock source (FD field) after both CLKF and CLKOE are cleared and after the I²C-bus interface stop condition. When disabled, CLKOUT is tied to V_{SS}.

(CLKF and CLKOE = 0 → disable condition → next negative clock edge → CLKOUT driven to V_{SS})

Synchronized CLKOUT Enable/Disable times (CLKSY = 1):

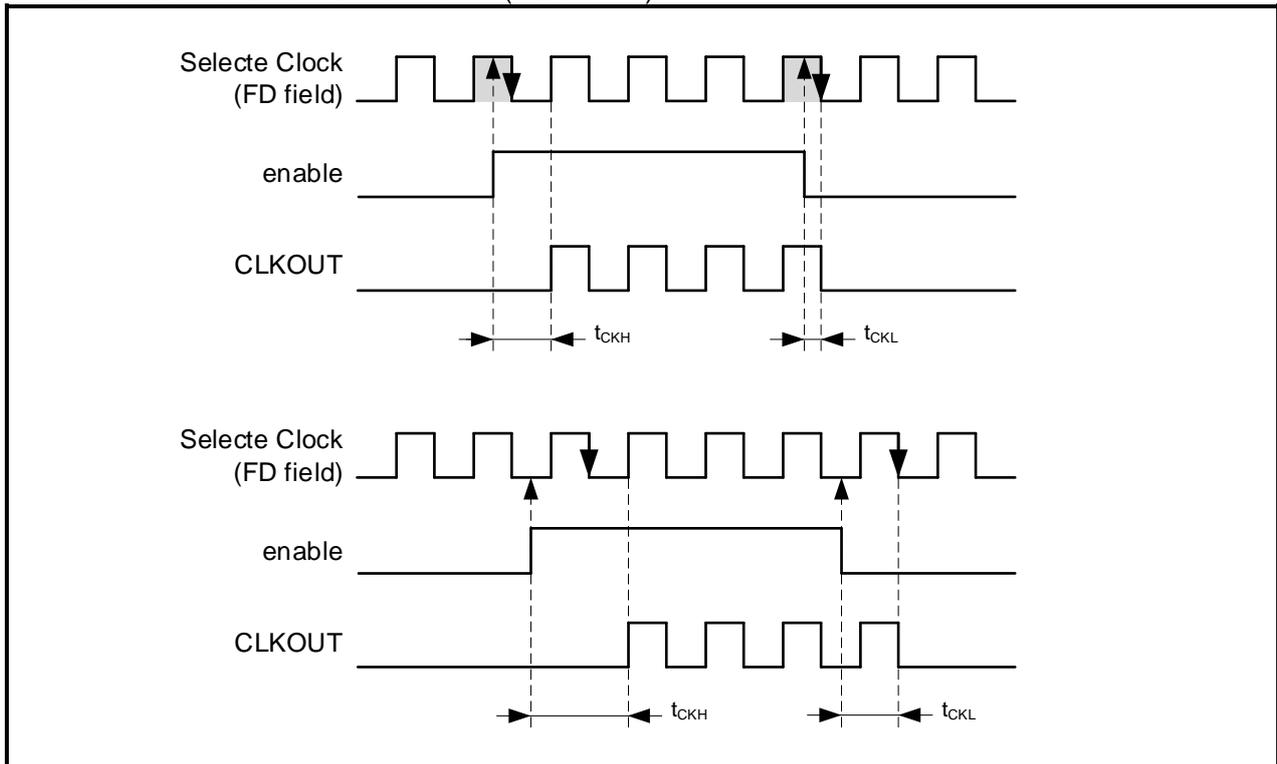


Figure 7-4 Frequency Output configuration

Hint: Glitch free frequency change on CLKOUT requires clearing flag CLKF and bit CLKOE to 0 before the new clock is selected in FD field.

(CLKF and CLKOE = 0 → disable condition → CLKOUT driven to V_{SS} → FD field selection → CLKF and/or CLKOE = 1 → enable condition → next negative clock edge)

7.4.5. CLOCK OUTPUT SCHEME

Complete frequency output scheme:

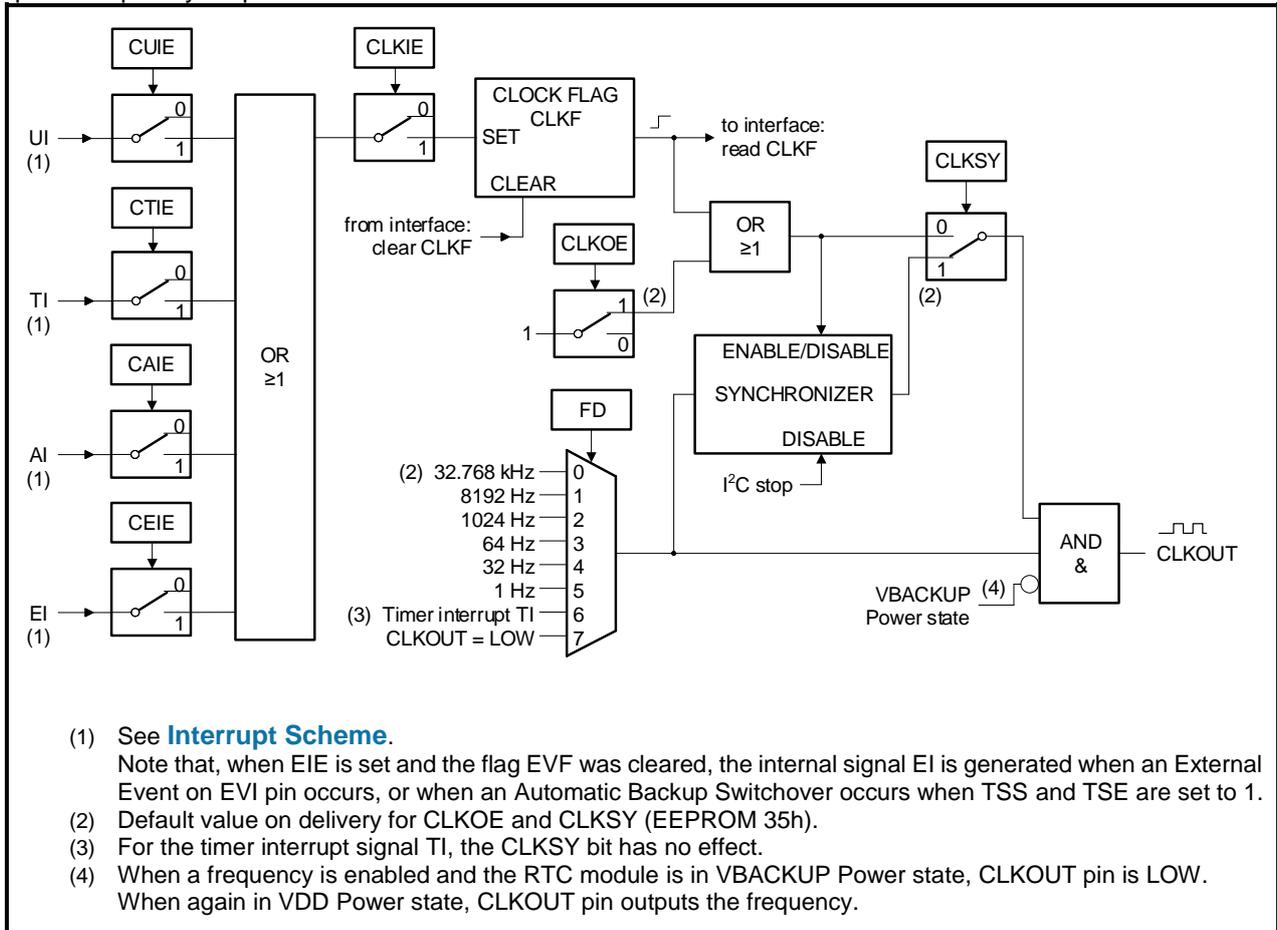


Figure 7-5 Frequency Output scheme

7.5. SETTING AND READING THE TIME

Data flow and data dependencies starting from the 1 Hz clock tick:

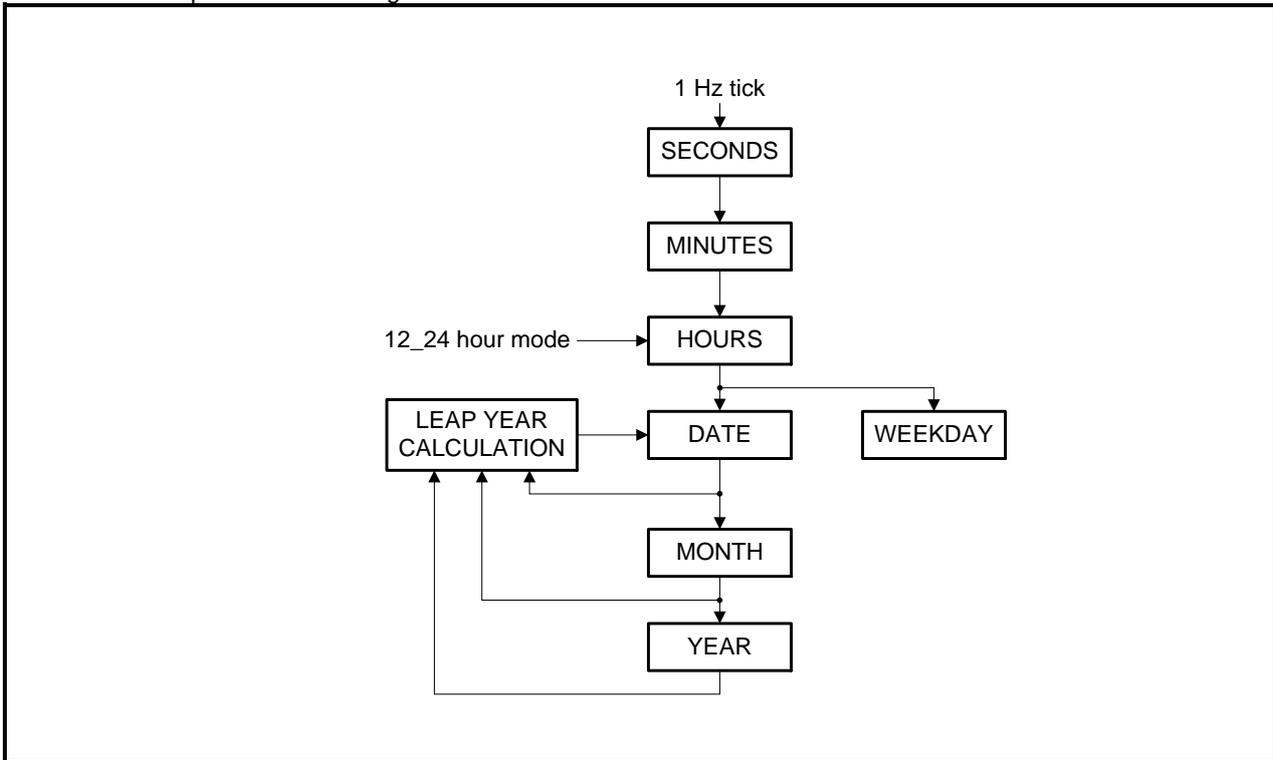


Figure 7-6 Setting and Reading the Time

During read/write operations, all clock and calendar registers (00h to 06h) are blocked for 950 ms second. The clock counter increment (1 Hz tick) is inhibited during I²C access to the EM3028 to allow coherent data values. A counter increment (maximum one 1 Hz tick) occurring during inhibition time is memorized and will be realized after the I²C stop condition.

Exception: If during the inhibition time the Seconds register was written by an I²C command the prescaler from 4096 Hz to 1 Hz will be reset. Resetting the prescaler will have an influence on the length of the current clock period on all subsequent peripherals (clock and calendar, CLKOUT, timer clock, update timer clock, UNIX clock, EVI input filter). Writing to the Seconds register has the same effect as setting RESET bit to 1 (see **RESET bit Function**).

When the read/write access has been terminated within 950 milliseconds ($t < 950$ ms), the time circuit is de-blocked immediately and any pending request to increment the time counters that occurred during a read access is correctly applied. Maximal one 1 Hz tick can be handled (see **Figure 7-7 Access time for Read/Write Operations**).

Access time for read/write operations:

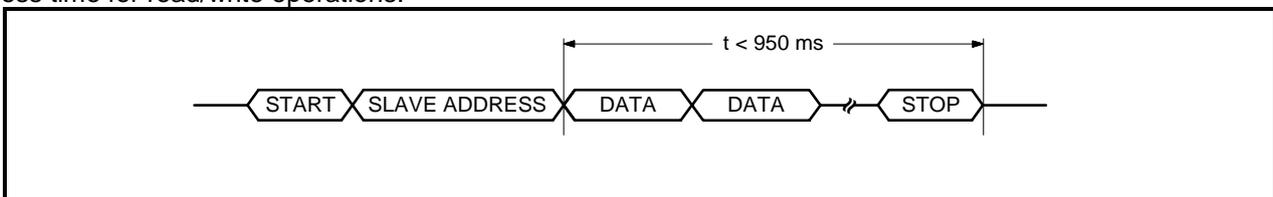


Figure 7-7 Access time for Read/Write Operations

Because of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

7.5.1. SETTING THE TIME

Advantage of register blocking during setting the time:

- Register blocking prevents faulty writing to the clock and calendar during an I²C write access (no incrementing of time registers during the write access).
- A possible 1 Hz tick occurring during the write access will be dropped.

The divider chain is reset whenever the Seconds register is written. This feature can be used to make a synchronized time setting. The other method is to use the [RESET bit Function](#)..

7.5.2. READING THE TIME

Advantage of register blocking and memorization of one 1 Hz tick during reading the time:

- Register blocking prevents faulty reading of the clock and calendar during an I²C read access (no incrementing of time registers during the read access).
- After reading, one memorized 1 Hz tick can be handled. Clock and calendar are updated.
- No second reading is needed. The read data are coherent.

Hint: The UNIX Time counter does not know such register blocking (see [UNIX Time Counter](#)).

7.6. EEPROM READ/WRITE

7.6.1. POR REFRESH (ALL CONFIGURATION EEPROM → RAM)

Read of all Configuration EEPROM registers at Power On Reset (POR):

At power up a refresh of the RAM mirror values by the values in the Configuration EEPROM is automatically generated (see [Register Reset Values Summary](#)). The time of this first refreshment is ~66 ms. The EEBusy bit in the register Status (0Eh) can be used to monitor the status of the refreshment.

7.6.2. AUTOMATIC REFRESH (ALL CONFIGURATION EEPROM → RAM)

Read all Configuration EEPROM registers automatically:

- To keep the integrity of the configuration data, all data of the Configuration RAM are refreshed by the data in the Configuration EEPROM each 24 hours, at date increment (1 second before midnight).
- Refresh is only active when EM3028 is not in VBACKUP mode and not disabled by EERD (EEPROM Memory Refresh Disable) bit.

7.6.3. REFRESH (ALL CONFIGURATION EEPROM → RAM)

Read all Configuration EEPROM registers:

- Before starting to read the configuration stored in the EEPROM, the auto refresh of the registers from the EEPROM has to be disabled by writing 1 into the EERD control bit.
- Then the actual configuration can be read from the Configuration EEPROM registers, writing the command 00h into the register EEcmd, and then the second command 12h into the register EEcmd will start the copy of the configuration into the RAM.
- When the transfer is finished (EEbusy = 0), the user can enable again the auto refresh of the registers by writing 0 into the EERD bit in the Control 1 register.

7.6.4. UPDATE (ALL CONFIGURATION RAM → EEPROM)

Write to all Configuration EEPROM registers:

- Before starting to change the configuration stored in the EEPROM, the auto refresh of the registers from the EEPROM has to be disabled by writing 1 into the EERD control bit.
- Then the new configuration can be written into the configuration RAM registers, when the whole new configuration is in the registers, writing the command 00h into the register EEcmd, then the second command 11h into the register EEcmd will start the copy of the configuration into the EEPROM.
- When the transfer is finished (EEbusy = 0), the user can enable again the auto refresh of the registers by writing 0 into the EERD bit in the Control 1 register.

7.6.5. READ ONE EEPROM BYTE (EEPROM → RAM-EEDATA)

Read one EEPROM byte from Configuration EEPROM or User EEPROM registers:

- Before starting to read a byte in the EEPROM, the auto refresh of the registers from the EEPROM has to be disabled by writing 1 into the EERD control bit.
- To read a single byte from EEPROM, the address to be read from is put in the EEaddr register, then the command 00h is written in the EEcmd register, then the second command 22h is written in the EEcmd register and the resulting byte can be read from the EEdata register.
- When the transfer is finished (EEbusy = 0), the user can enable again the auto refresh of the registers by writing 0 into the EERD bit in the Control 1 register.

7.6.6. WRITE TO ONE EEPROM BYTE (RAM-EEDATA → EEPROM)

Write to one EEPROM byte of the Configuration EEPROM or User EEPROM registers:

- Before starting to change data stored in the EEPROM, the auto refresh of the registers from the EEPROM has to be disabled by writing 1 into the EERD control bit.
- To write a single byte to EEPROM, the address to be written to is put in the EEaddr register and the data to be written is put in the EEdata register, then the command 00h is written in the EEcmd register, then a second command 21h is written in the EEcmd register to start the EEPROM write.
- When the transfer is finished (EEbusy = 0), the user can enable again the auto refresh of the registers by writing 0 into the EERD bit in the Control 1 register.

7.6.7. EEBUSY BIT

The set EEBusy status bit (bit 7 in the Status register 0Eh) indicates that the EEPROM is currently handling a read or write request and will ignore any further commands until the current one is finished. At power up a refresh is automatically generated. The time of this first refreshment is ~66 ms. After the refreshment is finished; EEBusy is cleared to 0 automatically. The cleared EEBusy status bit indicates that the EEPROM transfer is finished.

To prevent access collision between the internal automatic EEPROM refresh cycle (EERD = 0) and external EEPROM read/write access through interface the following procedures can be applied.

- Set EERD = 1 Automatic EEPROM Refresh needs to be disabled before EEPROM access.
- Check for EEBusy = 0 Access EEPROM only if not busy.
- Clear EERD = 0 It is recommended to enable Automatic EEPROM Refresh at the end of read/write access.
- Write EEPROM Wait 10 ms after each written EEPROM register before checking for EEBusy = 0 to allow internal data transfer.

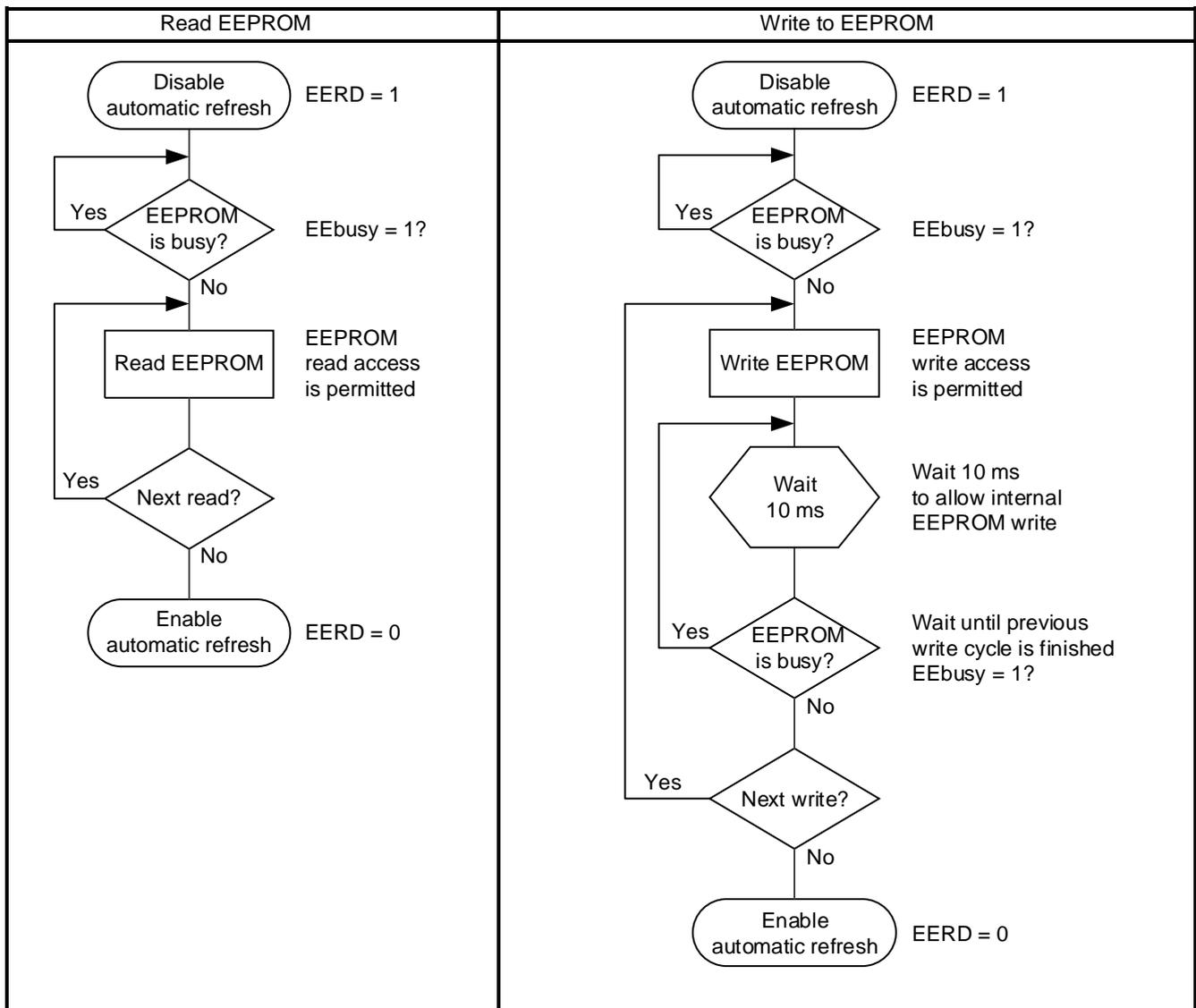


Figure 7-8 EEBusy bit

Note: In VDD Power state a minimum voltage of $V_{PROG} = 1.5\text{ V}$ during the whole EEPROM write procedure is required; i.e. until EEBusy = 0.

7.6.8. EEPROM READ/WRITE CONDITIONS

During a read/write of the EEPROM, if the V_{DD} supply drops, the device will continue to operate and communicate until a switchover to V_{BACKUP} occurs (in DSM or LSM mode). It is not recommended to operate during this time and all I²C communication should be halted as soon as V_{DD} failure is detected.

During the time that data is being written to the EEPROM, V_{DD} should remain above the minimum programming voltage $V_{PROG} = 1.5$ V. If at any time V_{DD} drops below this voltage, the data written to the device get corrupted.

To program the EEPROM, the backup switchover circuit must switch back to the main power supply V_{DD} . See also [Automatic BACKUP Switchover Interrupt Function](#).

7.7. USE OF THE CONFIGURATION EEPROM WITH RAM MIRROR REGISTERS

The best practice method to use the Configuration EEPROM with RAM mirror registers at addresses 2Bh and 30h to 37h is to make all Configuration settings in the RAM first and then to update all Configuration EEPROMs by the Update command EEcmd = 11h, see [Update \(All Configuration RAM → EEPROM\)](#).

Edit the Configuration settings:

1. Enter the correct password PW (PW = EEPW) to unlock write protection (PW0 to PW3)
2. Disable automatic refresh (EERD = 1)
3. Edit Configuration settings (RAM)
 - a. For changing Password EEPW, see [User Programmable Password](#)
4. Enter correct password PW (PW = EEPW) to unlock write protection (PW0 to PW3)
5. Update EEPROM (all Configuration RAM → EEPROM) with EEcmd = 00h followed by 11h
6. Enable automatic refresh (EERD = 0)
7. Enter an incorrect password PW (PW ≠ EEPW) to (PW0 to PW3) to lock the device

7.8. INTERRUPT OUTPUT

The interrupt pin $\overline{\text{INT}}$ can be triggered by six different functions:

- Periodic Countdown Timer Interrupt F
- Periodic Time Update Interrupt F
- Alarm Interrupt F
- External Event F
- Automatic BACKUP Switchover Interrupt F
- POWER ON RESET Interrupt F

7.8.1. SERVICING INTERRUPTS

The $\overline{\text{INT}}$ pin can indicate six types of interrupts. It outputs the logic OR operation result of these interrupt outputs. When an interrupt is detected (when $\overline{\text{INT}}$ pin produces a negative pulse or is at low level), the TF, UF, AF, EVF, BSF and PORF flags can be read to determine which interrupt event has occurred.

To keep $\overline{\text{INT}}$ pin from changing to low level, clear the TIE, UIE, AIE, EIE and BSIE (EEPROM 37h) and PORIE (EEPROM 35h) bits. To check whether an event has occurred without outputting any interrupts via the $\overline{\text{INT}}$ pin, software can read the TF, UF, AF, EVF, BSF and PORF interrupt flags (polling).

Caution: The EVF flag is also set by an event of the Backup Switchover function when bits TSS and TSE are set to 1.

7.8.2. INTERRUPT SCHEME

Interrupt Scheme (Part 1)

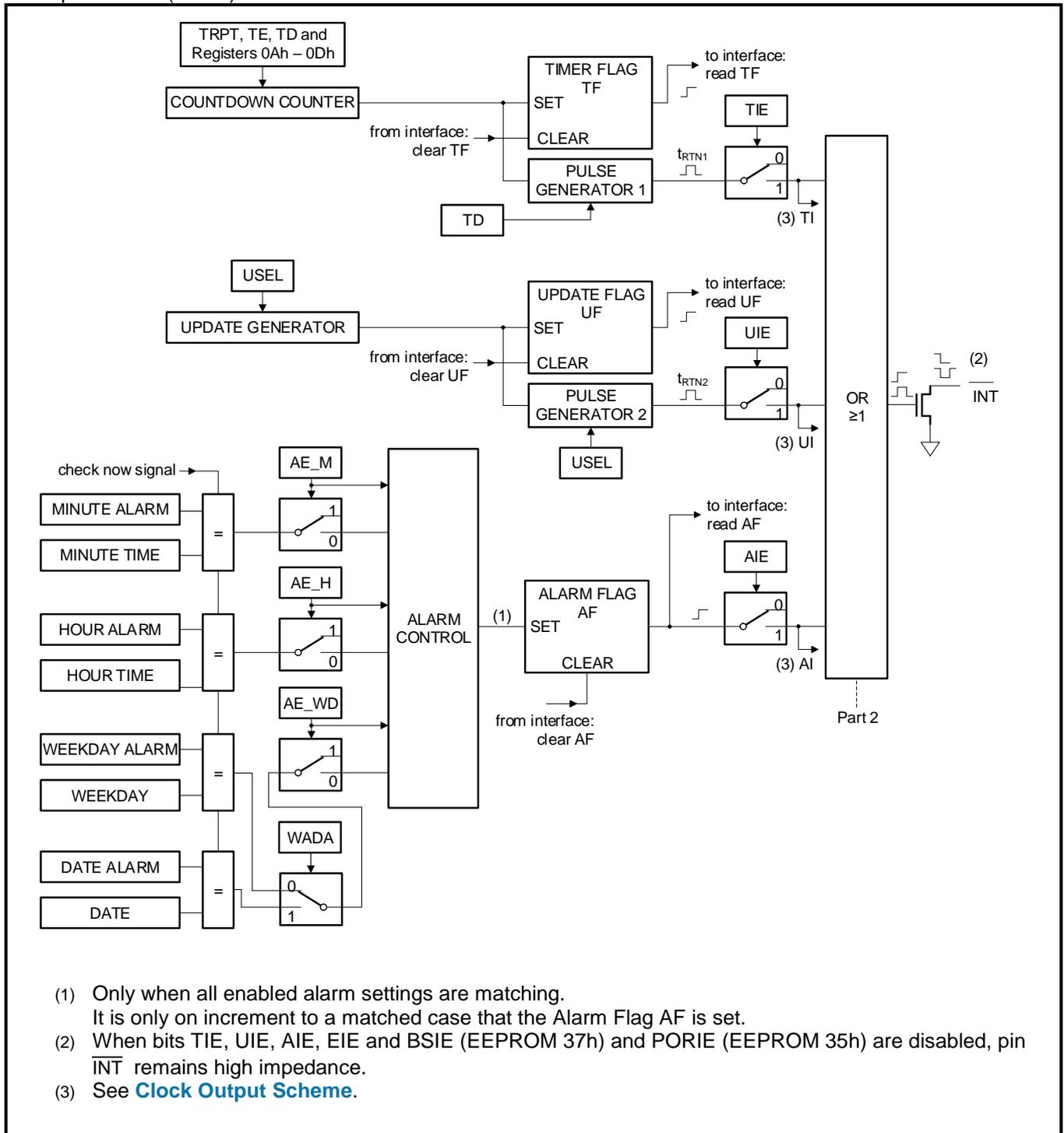
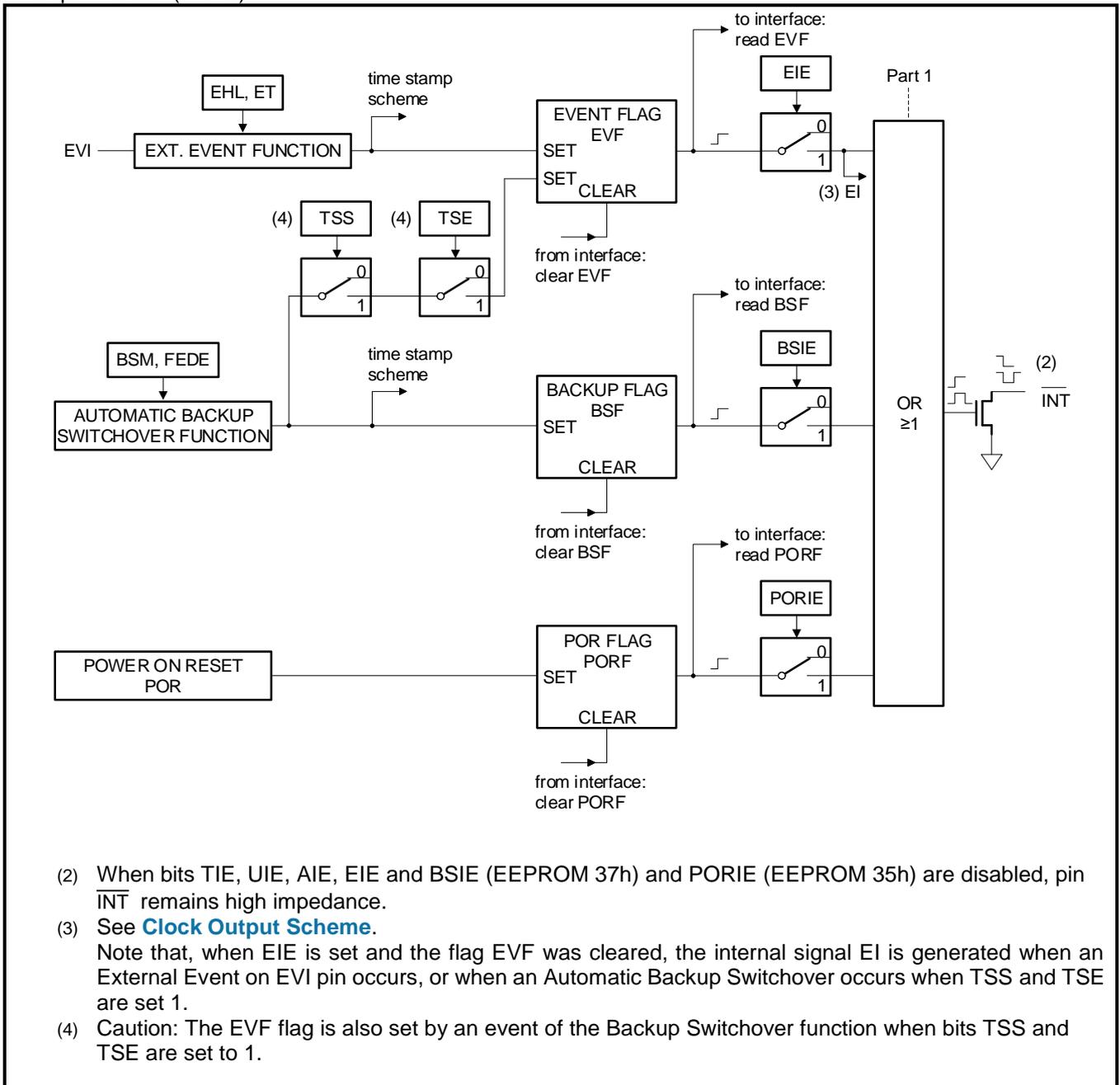


Figure 7-9 Interrupt Scheme (Part 1)

Interrupt Scheme (Part 2)



- (2) When bits TIE, UIE, AIE, EIE and BSIE (EEPROM 37h) and PORIE (EEPROM 35h) are disabled, pin $\overline{\text{INT}}$ remains high impedance.
- (3) See **Clock Output Scheme**.
Note that, when EIE is set and the flag EVF was cleared, the internal signal EI is generated when an External Event on EVI pin occurs, or when an Automatic Backup Switchover occurs when TSS and TSE are set to 1.
- (4) Caution: The EVF flag is also set by an event of the Backup Switchover function when bits TSS and TSE are set to 1.

Figure 7-10 Interrupt Scheme (Part 2)

7.9. PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION

The Periodic Countdown Timer Interrupt function generates an interrupt event once or periodically at any period set from 244.14 μ s to 4095 minutes.

If TRPT is set to 0 (default), Single Mode is selected. In Single Mode the counter will stop after reaching 0 and bit TE will be reset.

TRPT bit has to be set to 1 if periodic countdown is needed (Repeat Mode). In Repeat Mode the timer will be reloaded with the Timer Value from the Timer Value 0 and Timer Value 1 registers. This will repeat until TE is cleared or TRPT will be set to 0. In later case the countdown will stop when the timer reaches 0 for the next time and TE will be cleared. Loading the Timer Value with 0 stops the timer, interrupt is cleared and the flag TF is reset.

When starting the countdown timer for the first time, only the first period does not have a fixed duration. The amount of inaccuracy for the first timer period depends on the selected source clock (see **First Period Duration**).

When an interrupt event is generated, the $\overline{\text{INT}}$ pin goes to the low level and the TF flag is set to 1 to indicate that an event has occurred. The output on the $\overline{\text{INT}}$ pin is only effective if the TIE bit in the Control 2 register is set to 1. The low-level output signal on the $\overline{\text{INT}}$ pin is automatically cleared after the Auto reset time t_{RTN1} . $t_{\text{RTN1}} = 122 \mu\text{s}$ (TD = 00) or $t_{\text{RTN1}} = 7.813 \text{ ms}$ (TD = 01, 10, 11).

When bit TIE is set to 1, the internal countdown timer interrupt pulse (TI) can be used to enable the clock output on CLKOUT pin automatically, when bits CTIE, CLKIE and CLKOE are set to 1 and a frequency is selected in the FD field. The interrupt pulses (TI) can even be used as CLKOUT frequency, when selecting 110 in the FD field (see **Clock Output Scheme**).

7.9.1. PERIODIC COUNTDOWN TIMER DIAGRAM

Diagram of the Periodic Countdown Timer Interrupt function: In Repeat Mode (TRPT = 1). Countdown Timer Signal on CLKOUT (CLKOE = 1 and FD = 110).

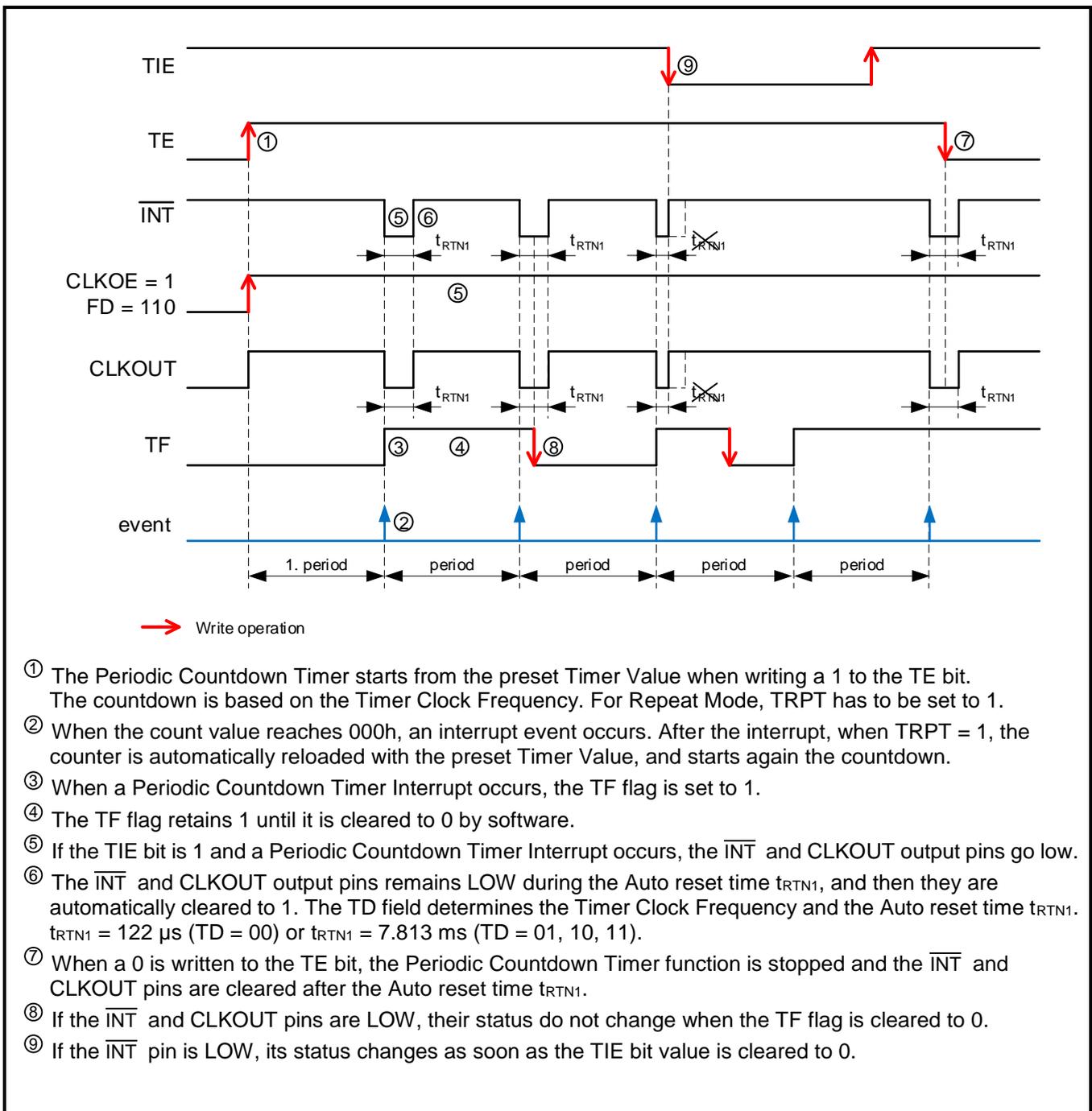


Figure 7-11 Periodic Countdown Timer Interrupt

7.9.2. USE OF THE PERIODIC COUNTDOWN TIMER INTERRUPT

The following registers, fields and bits are related to the Periodic Countdown Timer Interrupt and Automatic Clock output function:

- Timer Value 0 Register (0Ah) (see [Periodic Countdown Timer Control Registers](#))
- Timer Value 1 Register (0Bh) (see [Periodic Countdown Timer Control Registers](#))
- Timer Status 0 Register (0Ch) (see [Periodic Countdown Timer Control Registers](#))
- Timer Status 1 shadow Register (0Dh) (see [Periodic Countdown Timer Control Registers](#))
- TF flag (see [Configuration Registers](#), 0Eh – Status)
- TRPT bit, TE bit and TD field (see [Configuration Registers](#), 0Fh – Control 1)
- TIE bit (see [Configuration Registers](#), 10h – Control 2)
- CTIE bit (see [Configuration Registers](#), 12h – Clock Interrupt Mask)

For selecting Countdown Timer Signal for CLKOUT pin (CLKOE = 1 and FD = 110):

- CLKOE bit and FD field (see [EEPROM CLKOUT Register](#))

Prior to entering any timer settings for the Periodic Countdown Timer Interrupt, it is recommended to write a 0 to the TIE and TE bits to prevent inadvertent interrupts on $\overline{\text{INT}}$ pin. When 1 is written to the RESET bit, the Periodic Countdown Timer Interrupt function is retarded. When the Periodic Countdown Timer Interrupt function is not used, one Timer Value register (0Ah) can be used as RAM byte. The Timer Clock Frequency selection field TD is used to set the countdown period (source clock) for the Periodic Countdown Timer Interrupt function (four settings are possible).

Procedure to use the Periodic Countdown Timer Interrupt function and Automatic Clock output function:

1. Initialize bits TE, TIE and TF to 0. In that order, to prevent inadvertent interrupts on $\overline{\text{INT}}$ pin.
2. Set TRPT bit to 1 if periodic countdown is needed (Repeat Mode).
3. Choose the Timer Clock Frequency and write the corresponding value in the TD field.
4. Choose the Countdown Period based on the Timer Clock Frequency, and write the corresponding Timer Value to the registers Timer Value 0 (0Ah) and Timer Value 1 (0Bh). See following table.
5. Set the TIE bit to 1 if you want to get a hardware interrupt on $\overline{\text{INT}}$ pin.
6. Set CTIE bit to 1 to enable clock output when a timer interrupt occurs. See also [Clock Output S](#).
7. Set the TIE and CLKOE bits to 1 and the FD field to 110 if you want to get the timer signal on CLKOUT.
8. Set the TE bit from 0 to 1 to start the Periodic Countdown Timer. The countdown starts at the rising edge of the SCL signal after Bit 0 of the Address 0Fh is transferred. See subsequent Figure that shows the start timing.

Countdown Period in seconds:

$$\text{Countdown Period} = \frac{\text{Timer Value}}{\text{Timer Clock Frequency}}$$

| Timer Value (0Ah and 0Bh) | Countdown Period | | | |
|------------------------------|-------------------|-----------------|----------------|-------------------|
| | TD = 00 (4096 Hz) | TD = 01 (64 Hz) | TD = 10 (1 Hz) | TD = 11 (1/60 Hz) |
| 0 | - | - | - | - |
| 1 | 244.14 μ s | 15.625 ms | 1 s | 1 min |
| 2 | 488.28 μ s | 31.25 ms | 2 s | 2 min |
| : | : | : | : | : |
| 41 | 10.010 ms | 640.63 ms | 41 s | 41 min |
| 205 | 50.049 ms | 3.203 s | 205 s | 205 min |
| 410 | 100.10 ms | 6.406 s | 410 s | 410 min |
| 2048 | 500.00 ms | 32.000 s | 2048 s | 2048 min |
| : | : | : | : | : |
| 4095 (FFFh) | 0.9998 s | 63.984 s | 4095 s | 4095 min |

Table 66 Timer, Countdown Period

General countdown timer behavior:

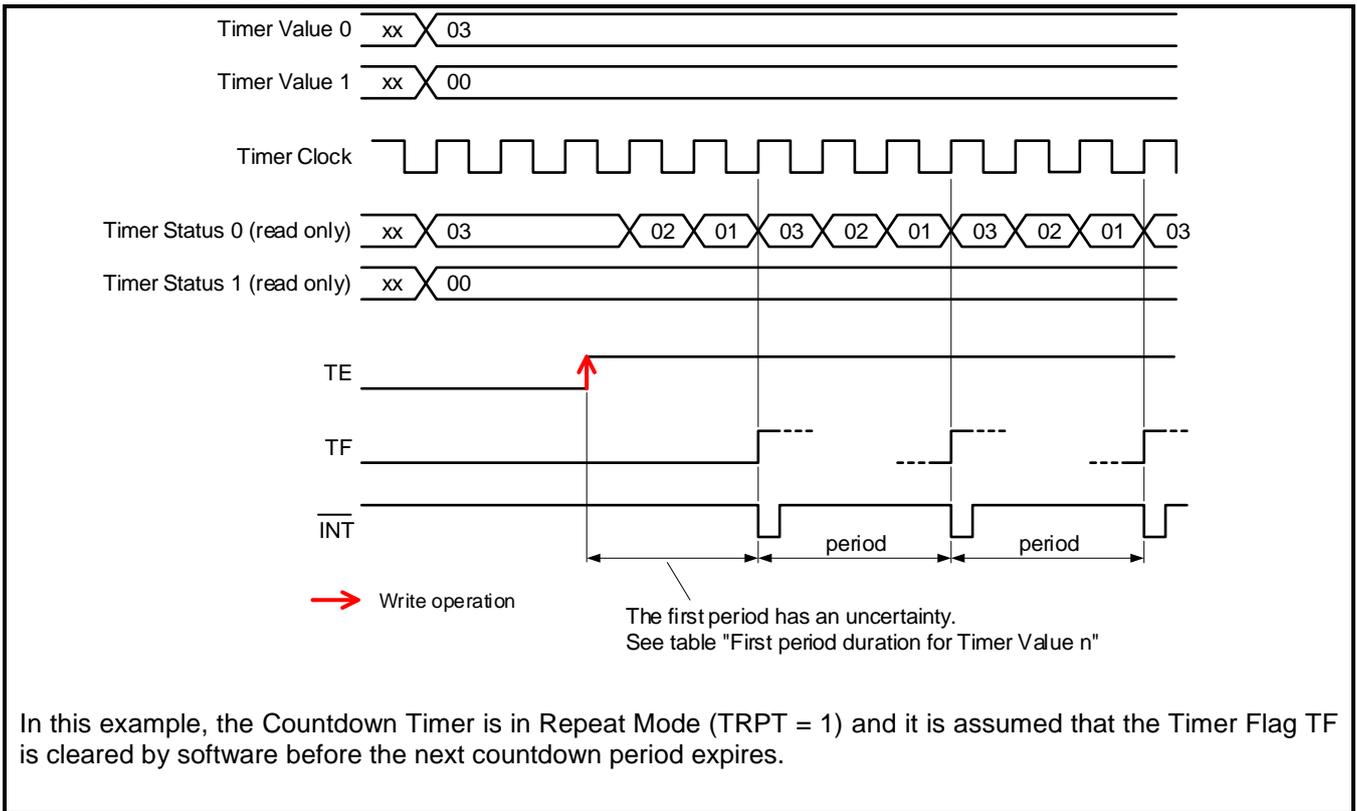


Figure 7-12 Periodic Countdown Timer Interrupt

Start timing of the Periodic Countdown Timer:

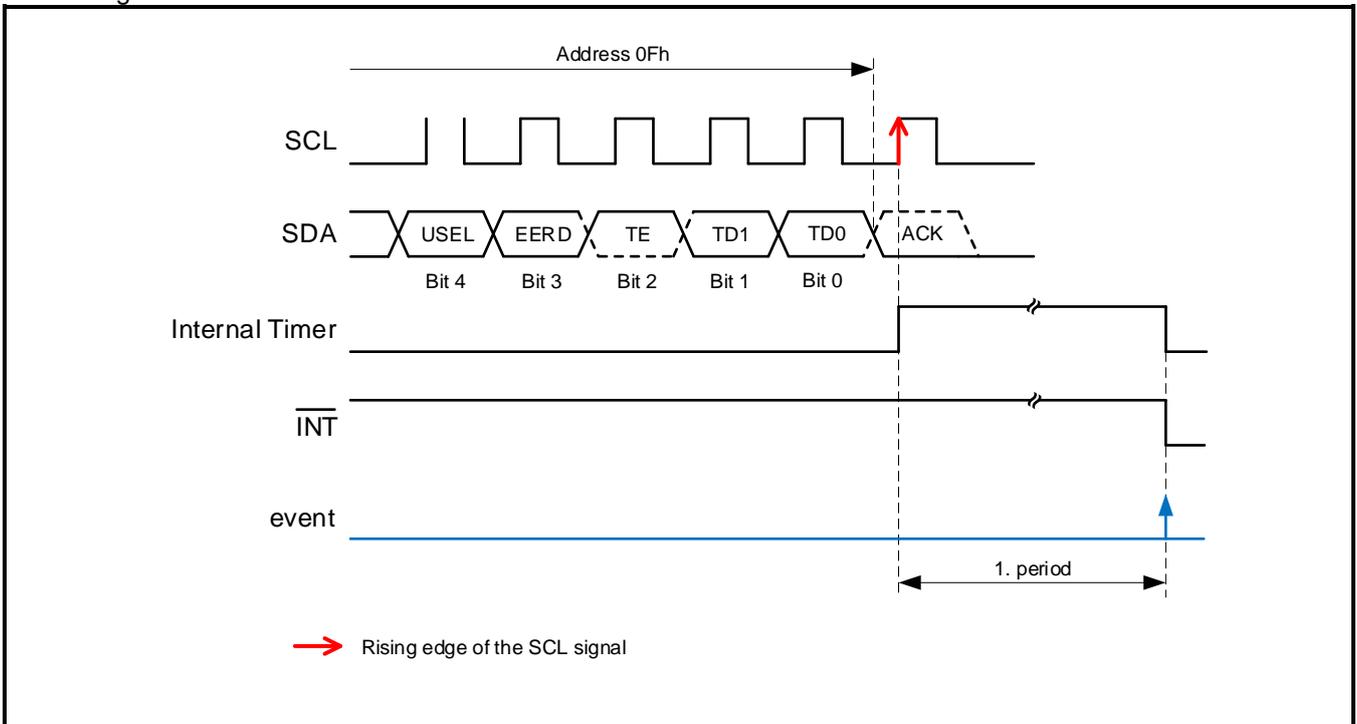


Figure 7-13 Periodic Countdown Timer Interrupt, countdown starting synchronization

7.9.3. FIRST PERIOD DURATION

When the TF flag is set, it indicates that an interrupt signal on \overline{INT} is generated if this mode is enabled. See Section **Interrupt Output** for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period has an uncertainty. The uncertainty is a result of the enable instruction being generated from the interface clock which is asynchronous from the Timer Clock Frequency. Subsequent timer periods do not have such deviation. The amount of deviation for the first timer period depends on the chosen Timer Clock Frequency, see following Table.

First period duration for Timer Value $n^{(1)}$:

| TD | Timer Clock Frequency | First period duration | | Subsequent periods duration |
|----|-----------------------|-------------------------|--|-----------------------------|
| | | Minimum Period | Maximum Period | |
| 00 | 4096 Hz | $n * 244 \mu\text{s}$ | $(n + 1) * 244 \mu\text{s}$ | $n * 244 \mu\text{s}$ |
| 01 | 64 Hz | $n * 15.625 \text{ ms}$ | $(n + 1) * 15.625 \text{ ms}$ | $n * 15.625 \text{ ms}$ |
| 10 | 1 Hz | $n * 1 \text{ s}$ | $n * 1 \text{ s} + 15.625 \text{ ms}$ | $n * 1 \text{ s}$ |
| 11 | 1/60 Hz | $n * 60 \text{ s}$ | $n * 60 \text{ s} + 15.625 \text{ ms}$ | $n * 60 \text{ s}$ |

⁽¹⁾ Timer Values n from 1 to 4095 are valid. Loading the counter with 0 stops the timer.

Table 67 Timer, First Period Duration

At the end of every countdown, the timer sets the Periodic Countdown Timer Flag (bit TF in Status Register). Bit TF can only be cleared by command. When enabled, a pulse is generated at the interrupt pin \overline{INT} .

When reading the Timer Value (Timer Value 0 and Timer Value 1), the preset value is returned and not the actual value. The actual value of the Periodic Countdown Timer can be read in the registers Timer Status 0 and Timer Status 1.

7.10. PERIODIC TIME UPDATE INTERRUPT FUNCTION

The Periodic Time Update Interrupt function generates an interrupt event periodically at the One-Second or the One-Minute update time, according to the selected timer source with bit USEL.

When an interrupt event is generated, the $\overline{\text{INT}}$ pin goes to the low level and the UF flag is set to 1 to indicate that an event has occurred. The output on $\overline{\text{INT}}$ pin is only effective if UIE bit in Control 2 register is set to 1. The low-level output signal on the $\overline{\text{INT}}$ pin is automatically cleared after the Auto reset time t_{RTN2} . $t_{\text{RTN2}} = 500 \text{ ms}$ (Second update) or $t_{\text{RTN2}} = 7.813 \text{ ms}$ (Minute update).

When bit UIE is set to 1, the internal update interrupt pulse (UI) can be used to enable the clock output on CLKOUT pin automatically, when bits CUIE, CLKIE and CLKOE are set to 1 and a frequency is selected in the FD field (see [Clock Output Scheme](#)).

7.10.1. PERIODIC TIME UPDATE DIAGRAM

Diagram of the Periodic Time Update Interrupt function:

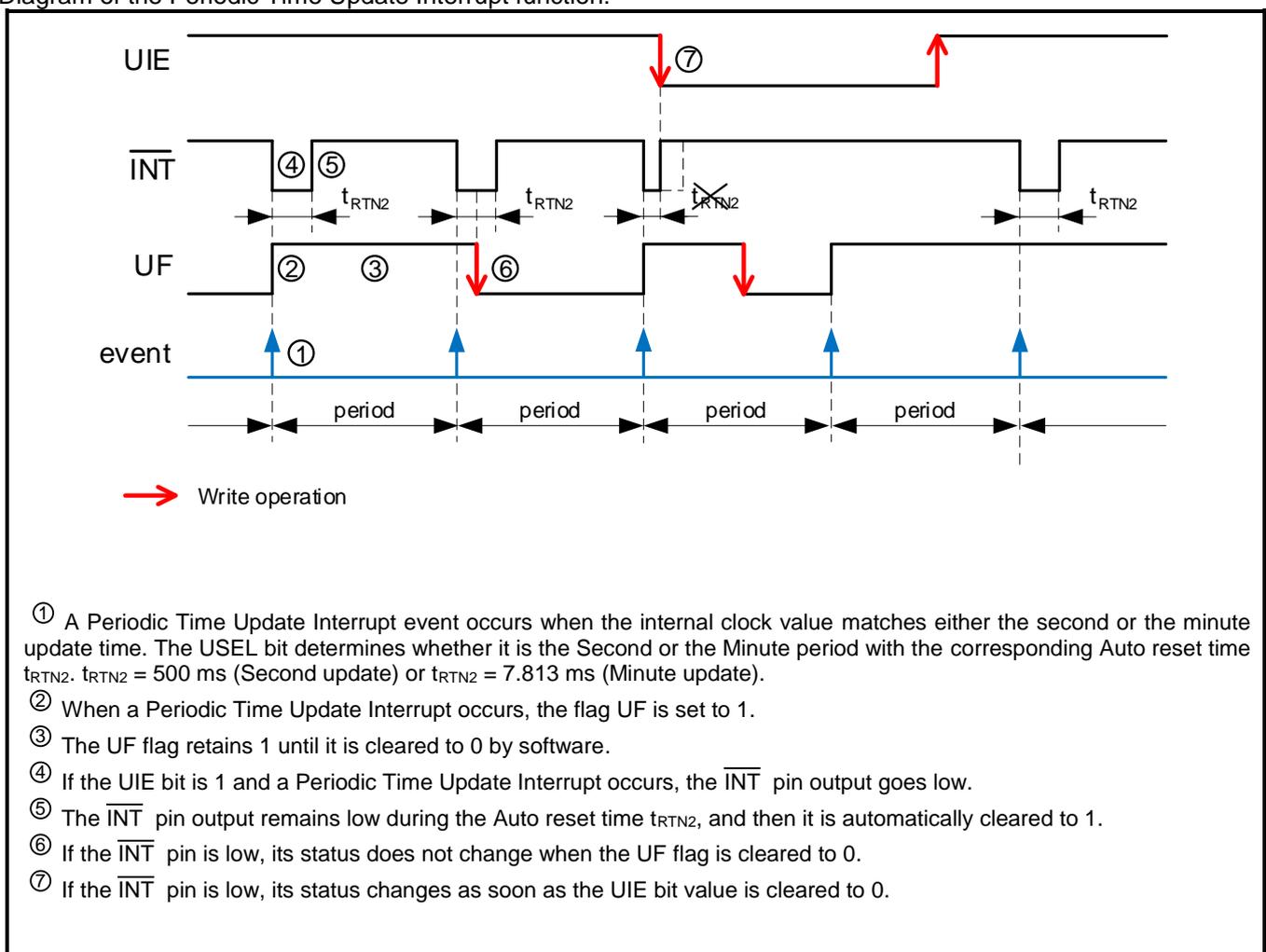


Figure 7-14 Periodic Time Update Interrupt

7.10.2. USE OF THE PERIODIC TIME UPDATE INTERRUPT

The following bits are related to the Periodic Time Update Interrupt and Automatic Clock output function:

- UF flag (see [Configuration Registers](#), 0Eh – Status)
- USEL bit (see [Configuration Registers](#), 0Fh – Control 1)
- UIE bit (see [Configuration Registers](#), 10h – Control 2)
- CUIE bit (see [Configuration Registers](#), 12h – Clock Interrupt Mask)

Prior to entering any other settings, it is recommended to write a 0 to the UIE bit to prevent inadvertent interrupts on $\overline{\text{INT}}$ pin. The Periodic Time Update Interrupt function cannot be fully stopped, but by writing a 0 in the UIE bit, it prevents the occurrence of a hardware interrupt on the $\overline{\text{INT}}$ pin.

When 1 is written to the RESET bit (see [Configuration Registers](#), 10h – Control 2) the divider chain is reset and the Periodic Time Update Interrupt will be retarded. The reset function only interrupts the Periodic Time Update Interrupt function but does not turn it off.

Procedure to use the Periodic Time Update Interrupt and Automatic Clock output function:

1. Initialize bits UIE and UF to 0.
2. Choose the timer source clock and write the corresponding value in the USEL bit.
3. Set the UIE bit to 1 if you want to get a hardware interrupt on $\overline{\text{INT}}$ pin.
4. Set CUIE bit to 1 to enable clock output when a time update interrupt occurs. See also [Clock Output Scheme](#).
5. The first interrupt will occur after the next event, either second or minute change.

7.11. ALARM INTERRUPT FUNCTION

The Alarm Interrupt function generates an interrupt for alarm settings such as weekday/date, hour and minute settings.

When an interrupt event is generated, the $\overline{\text{INT}}$ pin goes to the low level and the AF flag is set to 1 to indicate that an event has occurred. The output on the $\overline{\text{INT}}$ pin is only effective if the AIE bit in the Control 2 register is set to 1.

When bit AIE is set to 1, the internal alarm interrupt signal (AI) can be used to enable the clock output on CLKOUT pin automatically, when bits CAIE, CLKIE and CLKOE are set to 1 and a frequency is selected in the FD field (see [Clock Output Scheme](#)).

7.11.1. ALARM DIAGRAM

Diagram of the Alarm Interrupt function:

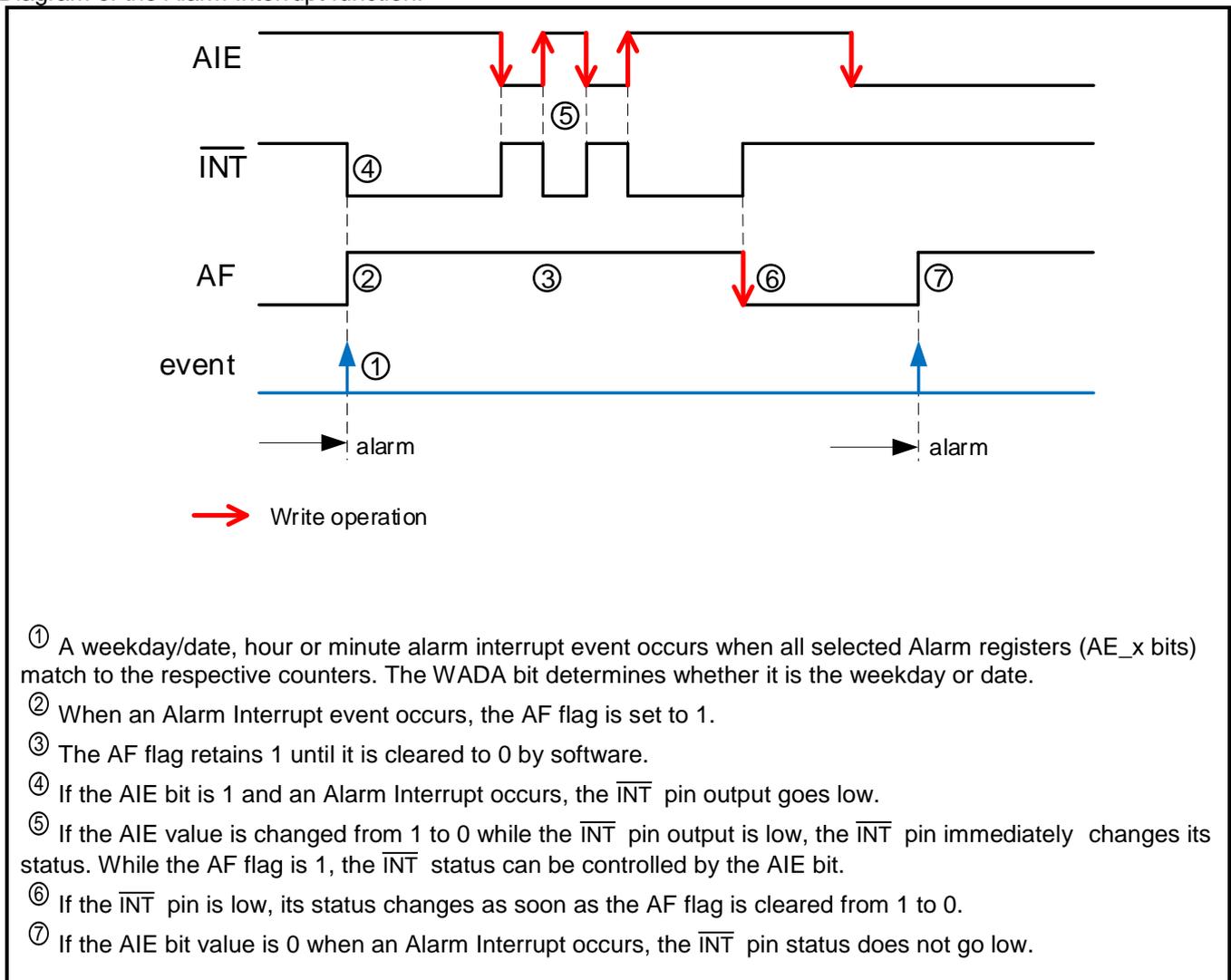


Figure 7-15 Alarm Interrupt

7.11.2. USE OF THE ALARM INTERRUPT

The following registers and bits are related to the Alarm Interrupt and Automatic Clock output function:

- Minutes Register (01h) (see [Clock Registers](#))
- Hours Register (02h) (see [Clock Registers](#))
- Weekday Register (03h) (see [Calendar Registers](#))
- Date Register (04h) (see [Calendar Registers](#))
- Minutes Alarm Register and AE_M bit (07h) (see [Alarm Registers](#))
- Hours Alarm Register and AE_H bit (08h) (see [Alarm Registers](#))
- Weekday/Date Alarm Register and AE_WD bit (09h) (see [Alarm Registers](#))
- AF flag (see [Configuration Registers](#), 0Eh – Status)
- WADA bit (see [Configuration Registers](#), 0Fh – Control 1)
- AIE bit (see [Configuration Registers](#), 10h – Control 2)
- CAIE bit (see [Configuration Registers](#), 12h – Clock Interrupt Mask)

Prior to entering any timer settings for the Alarm Interrupt, it is recommended to write a 0 to the AIE bit to prevent inadvertent interrupts on $\overline{\text{INT}}$ pin. When 1 is written to the RESET bit, an Alarm Interrupt function event can be retarded. When the Alarm Interrupt function is not used, one Byte (07h) of the Alarm registers can be used as RAM byte. In such case, be sure to write a 0 to the AIE bit (if the AIE bit value is 1 and the Alarm register is used as RAM register, $\overline{\text{INT}}$ may change to low level unintentionally).

Procedure to use the Alarm Interrupt and Automatic Clock output function:

1. Initialize bits AIE and AF to 0.
2. Choose weekday alarm or date alarm (weekday/date) by setting the WADA bit. WADA = 0 for weekday alarm or WADA = 1 for date alarm.
3. Write the desired alarm settings in registers 07h to 09h. The three alarm enable bits, AE_M, AE_H and AE_WD, are used to select the corresponding register that has to be taken into account for match or not. See the following table.
4. Set CAIE bit to 1 to enable clock output when an alarm occurs. See also [Clock Output S](#).
5. Set the AIE bit to 1 if you want to get a hardware interrupt on $\overline{\text{INT}}$ pin.

Alarm Interrupt:

| Alarm enable bits | | | Alarm event |
|-------------------|------|------|--|
| AE_WD | AE_H | AE_M | |
| 0 | 0 | 0 | When minutes, hours and weekday/date match (once per weekday/date) |
| 0 | 0 | 1 | When hours and weekday/date match (once per weekday/date) |
| 0 | 1 | 0 | When minutes and weekday/date match (once per hour per weekday/date) |
| 0 | 1 | 1 | When weekday/date match (once per weekday/date) |
| 1 | 0 | 0 | When hours and minutes match (once per day) |
| 1 | 0 | 1 | When hours match (once per day) |
| 1 | 1 | 0 | When minutes match (once per hour) |
| 1 | 1 | 1 | All disabled – Default value |

AE_x bits (where x is WD, H or M)
 AE_x = 0: Alarm is enabled
 AE_x = 1: Alarm is disabled – Default value

Table 68 Alarm Interrupt

7.12. EXTERNAL EVENT FUNCTION

The External Event Interrupt and the Time Stamp function are enabled by the control bits EIE, TSS and TSE. Depending of the EHL bit a high level (positive edge) or low level (negative edge) signal can be regarded as an event and furthermore a digital glitch filtering is applied to the EVI signal when selecting a sampling period in the ET field.

If enabled (EIE = 1, TSS = 0, TSE = 1 and EVF flag was cleared to 0 before) and an External Event on EVI pin is detected, the clock and calendar registers are captured and copied into the Time Stamp registers, the \overline{INT} is issued and the EVF flag is set to 1 to indicate that an external event has occurred.

When bit EIE is set to 1, the internal event interrupt signal (EI) can be used to enable the clock output on CLKOUT pin automatically, when bits CEIE, CLKIE and CLKOE are set to 1 and a frequency is selected in the FD field (see [Clock Output Scheme](#)).

Caution: The EVF flag is also set by an event of the Backup Switchover function when bits TSS and TSE are set to 1.

7.12.1. EXTERNAL EVENT DIAGRAM

Diagram of the External Event function. Example with positive edge/level detection (EHL = 1):

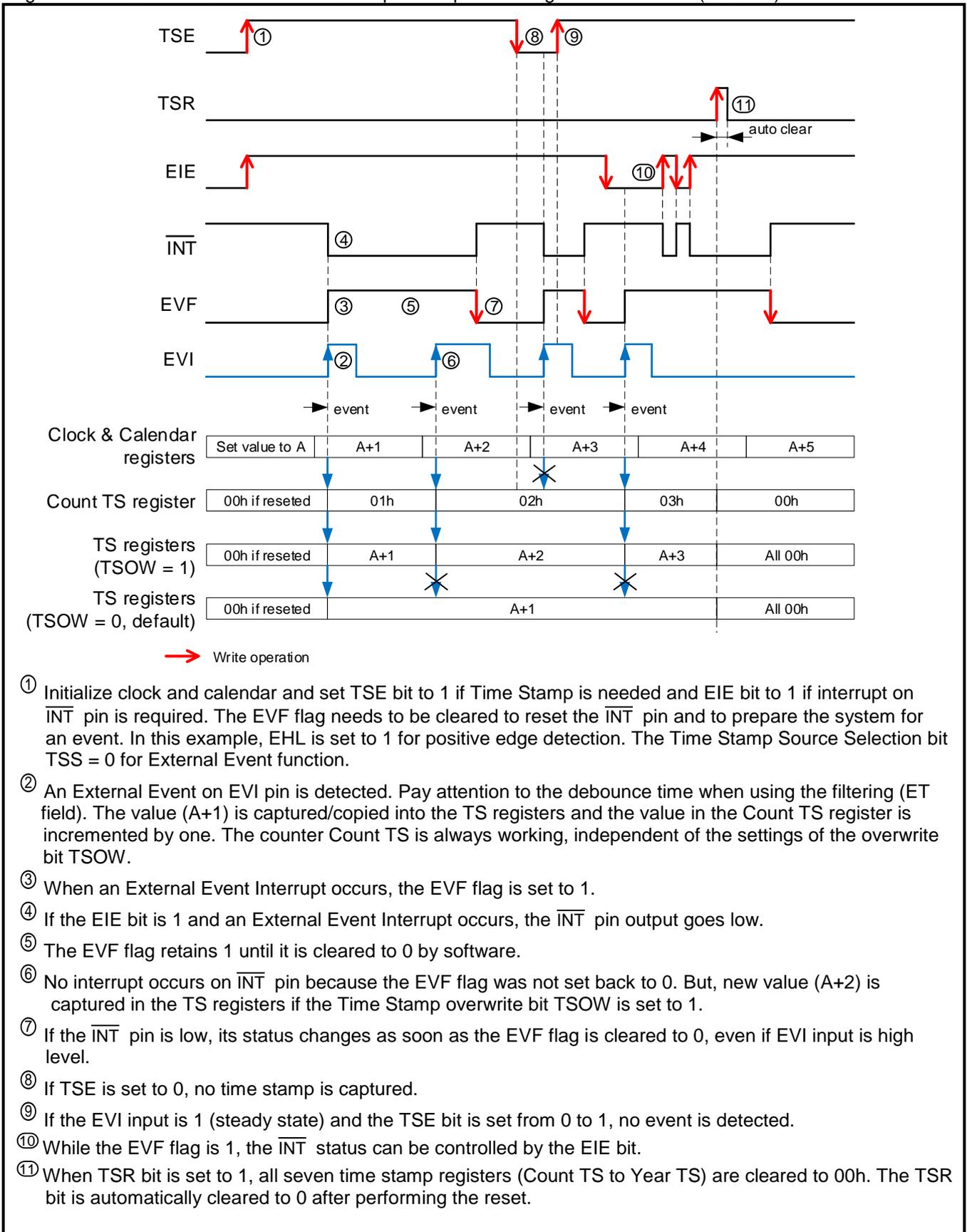


Figure 7-16 External Event

7.12.2. USE OF THE EXTERNAL EVENT FUNCTION

The following registers and bits are related to the External Event Interrupt, Time Stamp and Automatic Clock output function:

- Seconds Register (00h) (see [Clock Registers](#))
- Minutes Register (01h) (see [Clock Registers](#))
- Hours Register (02h) (see [Clock Registers](#))
- Date Register (04h) (see [Calendar Registers](#))
- Month Register (05h) (see [Calendar Registers](#))
- Year Register (06h) (see [Calendar Registers](#))
- Count TS Register (14h) (see [Time Stamp Registers](#))
- Seconds TS (15h) (see [Time Stamp Registers](#))
- Minutes TS (16h) (see [Time Stamp Registers](#))
- Hours TS (17h) (see [Time Stamp Registers](#))
- Date TS (18h) (see [Time Stamp Registers](#))
- Month TS (19h) (see [Time Stamp Registers](#))
- Year TS (1A) (see [Time Stamp Registers](#))
- EVF flag (see [Configuration Registers](#), 0Eh – Status)
- TSE and EIE bits (see [Configuration Registers](#), 10h – Control 2)
- CEIE bit (see [Configuration Registers](#), 12h – Clock Interrupt Mask)
- EHL bit, ET field, TSR bit, TSOW bit and TSS bit (see [Event Control Register](#))

Prior to entering any timer settings for the event interrupt, it is recommended to write a 0 to the EIE bit to prevent inadvertent interrupts on $\overline{\text{INT}}$ pin.

Procedure to use the External Event Interrupt, Time Stamp and Automatic Clock output function:

1. Initialize bits TSE, EIE and flag EVF to 0.
2. Set TSR bit to 1, to reset all Time Stamp registers to 00h. After reset the TSR bit is automatically cleared.
3. Set EHL bit to 1 or 0 to choose high or low level detection on pin EVI.
4. Set ET field to apply filtering to the EVI pin. See following two diagrams.
5. Set TSS bit to 0 to select External Event on EVI pin as Time Stamp source.
6. Set TSOW bit to 1 if the last occurred event has to be recorded and TS registers are overwritten.
Hint: The counter Count TS is always working, independent of the settings of the overwrite bit TSOW.
7. Set CEIE bit to 1 to enable clock output when external event occurs. See also [Clock Output Scheme](#).
8. Set TSE bit to 1 if you want to enable the Time Stamp function.
9. Set EIE bit to 1 if you want to get a hardware interrupt on $\overline{\text{INT}}$ pin.

Example with no filtering (ET = 00), with positive edge detection (EHL = 1) and enabled interrupt (EIE = 1):

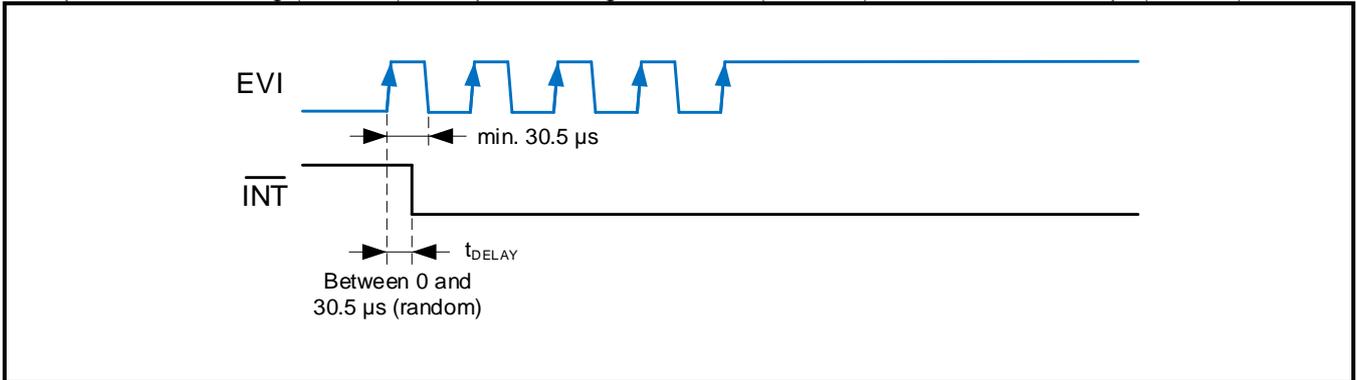
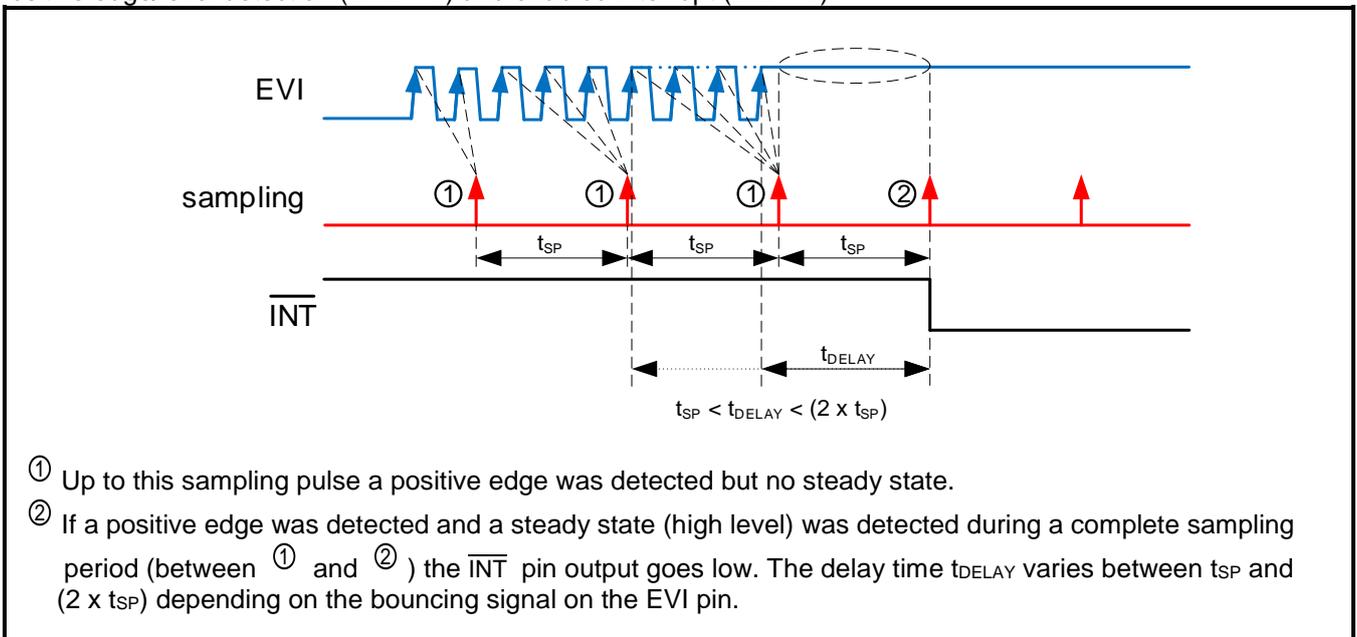


Figure 7-17 External Event function, No filtering example, EIE = 1

Example with digital debounce filtering (ET = 01, 10 or 11; sampling period $t_{\text{SP}} = 3.9 \text{ ms}$, 15.6 ms or 125 ms), with positive edge/level detection (EHL = 1) and enabled interrupt (EIE = 1):



- ① Up to this sampling pulse a positive edge was detected but no steady state.
- ② If a positive edge was detected and a steady state (high level) was detected during a complete sampling period (between ① and ②) the $\overline{\text{INT}}$ pin output goes low. The delay time t_{DELAY} varies between t_{SP} and $(2 \times t_{\text{SP}})$ depending on the bouncing signal on the EVI pin.

Figure 7-18 External Event function, with Filtering example, EIE = 1

7.13. AUTOMATIC BACKUP SWITCHOVER INTERRUPT FUNCTION

The Automatic Backup Switchover Interrupt function generates an interrupt event when the BSM field (EEPROM 37h) is set to 01 (DSM) or 11 (LSM) and a switchover from VDD Power state to VBACKUP Power state occurs.

When an interrupt event is generated, the $\overline{\text{INT}}$ pin goes to the low level and the BSF flag is set to 1 to indicate that an event has occurred. The output on the $\overline{\text{INT}}$ pin is only effective if the BSIE bit (EEPROM 37h) is set to 1.

When bit EIE is set to 1 and when the bits TSS and TSE are set to 1, the internal event interrupt signal (EI) created by the Automatic Backup Switchover function can be used to enable the clock output on CLKOUT pin automatically, when bits CEIE, CLKIE and CLKOE are set to 1 and a frequency is selected in the FD field. When again in VDD Power state, CLKOUT pin outputs the frequency (see [Clock Output Scheme](#)).

Hint: A debounce logic provides a 122 μs – 183 μs debounce time t_{DEB} , which will filter V_{DD} oscillation when the backup switchover will switch back from V_{BACKUP} to V_{DD} (see [Automatic Backup Switchover Function](#)).

Hint: The FEDE bit (EEPROM 37h) should always be set to 1, so that Fast Edge Detection ($\geq 7 \text{ V/ms}$) is always enabled (see [EEPROM Backup Register](#)). – Default value on delivery

7.13.1. AUTOMATIC BACKUP SWITCHOVER DIAGRAM

Diagram of the Automatic Backup Switchover Interrupt function:

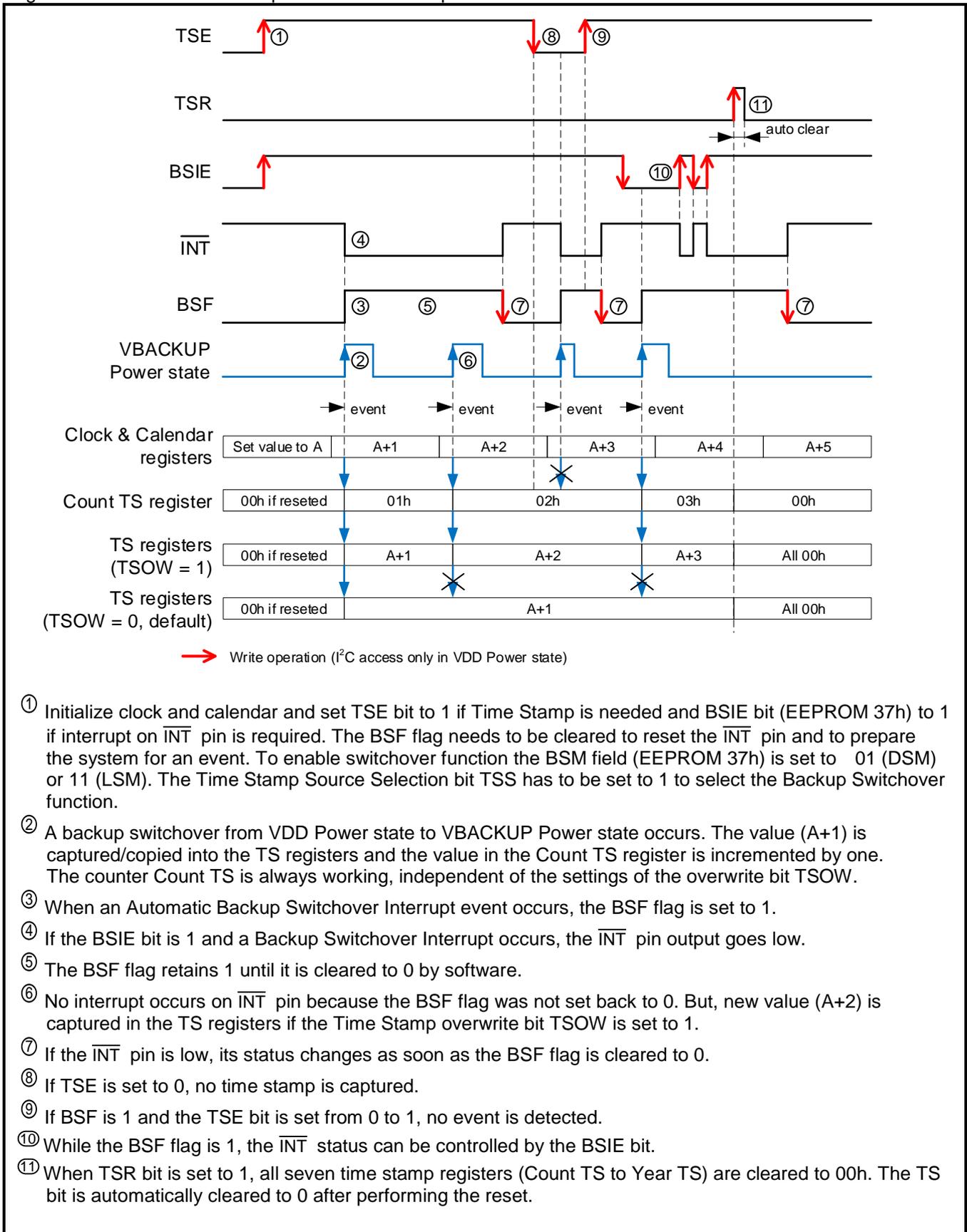


Figure 7-19 Automatic Backup Switchover

7.13.2. USE OF THE AUTOMATIC BACKUP SWITCHOVER INTERRUPT

The following registers and bits are related to the Automatic Backup Switchover Interrupt, Time Stamp and Automatic Clock output function:

- Seconds Register (00h) (see [Clock Registers](#))
- Minutes Register (01h) (see [Clock Registers](#))
- Hours Register (02h) (see [Clock Registers](#))
- Date Register (04h) (see [Calendar Registers](#))
- Month Register (05h) (see [Calendar Registers](#))
- Year Register (06h) (see [Calendar Registers](#))
- Count TS (14h) (see [Time Stamp Registers](#))
- Seconds TS (15h) (see [Time Stamp Registers](#))
- Minutes TS (16h) (see [Time Stamp Registers](#))
- Hours TS (17h) (see [Time Stamp Registers](#))
- Date TS (18h) (see [Time Stamp Registers](#))
- Month TS (19h) (see [Time Stamp Registers](#))
- Year TS (1A) (see [Time Stamp Registers](#))
- BSF flag (see [Configuration Registers](#), 0Eh – Status)
- CEIE bit (see [Configuration Registers](#), 12h – Clock Interrupt Mask)
- TSR bit, TSOW bit and TSS bit (see [Event Control Register](#))
- BSIE bit, FEDE bit and BSM field (see [EEPROM Backup Register](#))

Prior to entering any other settings, it is recommended to write a 0 to the BSIE bit to prevent inadvertent interrupts on $\overline{\text{INT}}$ pin.

Procedure to use the Automatic Backup Switchover Interrupt, Time Stamp and Automatic Clock output function:

1. Initialize bits TSE, BSIE and BSF to 0.
2. Set TSR bit to 1, to reset all Time Stamp registers to 00h. After reset, the TSR bit is automatically cleared.
3. Set TSS bit to 1 to select Backup Switchover as Time Stamp source.
4. Set TSOW bit to 1 if the last occurred event has to be recorded and TS registers are overwritten.
Hint: The counter Count TS is always working, independent of the settings of the overwrite bit TSOW.
5. Set TSE bit to 1 if you want to enable the Time Stamp function.
6. Set CEIE bit to 1 to enable clock output when a backup switchover occurs.
Caution: This function is only working with the Automatic Backup Switchover function when the bits TSS and TSE are set to 1. See also [Clock Output Scheme](#).
7. The FEDE bit (EEPROM 37h) should always be set to 1, so that Fast Edge Detection (≥ 7 V/ms) is always enabled.
8. Set the BSIE bit to 1 (EEPROM 37h) if you want to get a hardware interrupt on $\overline{\text{INT}}$ pin.
9. Choose the switchover mode (DSM or LSM) and write the corresponding value in the BSM field.

See also [EEPROM Read/Write Conditions](#).

7.14. POWER ON RESET INTERRUPT FUNCTION

The Power On Reset Interrupt function is enabled by the PORIE bit (EEPROM 35h).

The PORIE bit has to be set beforehand in the EEPROM not in the RAM (see [EEPROM READ/WRITE](#))

When voltage drop below V_{POR} is detected ($V_{DD} < V_{POR}$) the PORF flag is set to 1 to indicate that a Power On Reset has occurred and when the PORIE bit is 1 the \overline{INT} pin goes to low level.

A PORF value of 1 indicates also that the time information is corrupted. The value 1 is retained until a 0 is written by the user.

7.14.1. POWER ON RESET DIAGRAM

Diagram of the Power On Reset Interrupt function:

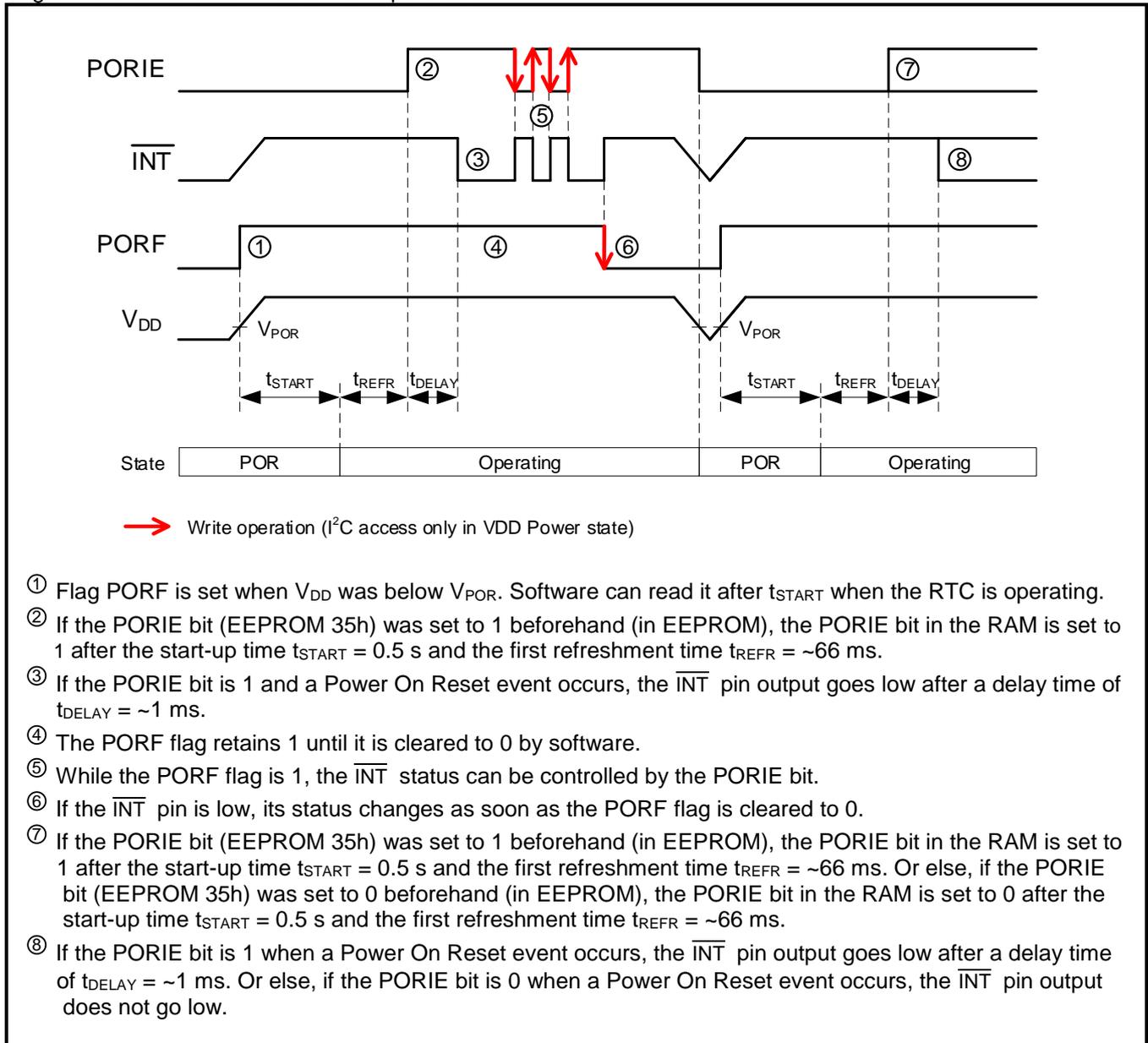


Figure 7-20 Power On Reset Interrupt

7.14.2. USE OF THE POWER ON RESET INTERRUPT

The following registers and bits are related to the Power On Reset Interrupt function (including EEPROM handling):

- PORF flag and EEbusy bit (see [Configuration Registers](#), 0Eh – Status)
- EERD bit (see [Configuration Registers](#), 0Fh – Control 1)
- EEaddr register (see [EEPROM Memory Control Registers](#), 25h –EEPROM Address)
- EEdata register (see [EEPROM Memory Control Registers](#), 26h –EEPROM Data)
- EEcmd register (see [EEPROM Memory Control Registers](#), 27h –EEPROM Commands)
- PORIE bit (see [EEPROM CLKOUT Register](#), 35h – EEPROM CLKOUT)

The PORIE bit has to be set beforehand in the EEPROM not in the RAM (see [EEPROM READ/WRITE](#)).

Procedure to use the Power On Reset Interrupt function:

1. In the EEPROM, set the PORIE bit to 1 if you want to get a hardware interrupt on $\overline{\text{INT}}$ pin at the next Power On Reset event. Procedure according to [EEPROM READ/WRITE](#).
2. The first interrupt will occur after the next POR event.

7.15. TIME STAMP FUNCTION

The Time Stamp function is enabled by the control bit TSE. Sources are the External Event function (TSS = 0) or the Automatic Backup Switchover function (TSS = 1).

If a source is enabled and an event is detected, the Time Stamp (TS) registers are recorded. When the TSOW bit is set to 0 and the EVF flag was cleared to 0 before, only one (the first) event is recorded. When the TSOW bit is set to 1, the last event is recorded (EVF flag does not need to be cleared). The counter Count TS is always working, independent of the settings of the overwrite bit TSOW.

- When the TSR bit value is 1, the data of the time stamp in TS registers and Count TS are reset.
- Before writing settings for TS, it is recommended to write a 0 in the TSE bit and a 1 to EVR bit.
- When 1 is written to the RESET bit, the TS event can be retarded.

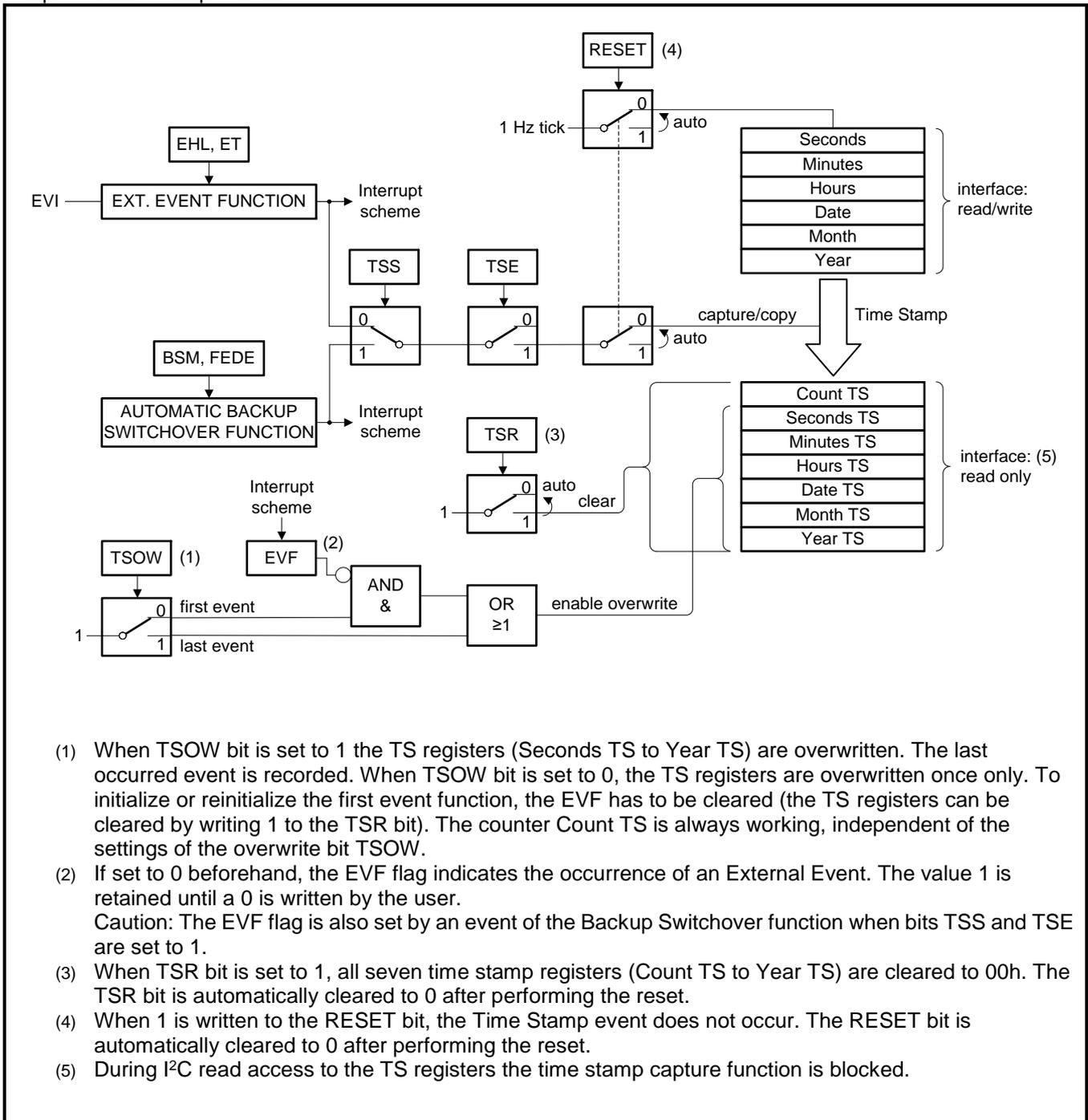
Procedures to use the Time Stamp function with the External Event Interrupt function or with the Automatic Backup Switchover function:

1. Write 0 in TSS and TSE bits. Select TSOW (0 or 1), clear EVF and BSF.
2. Write 1 in TSR bit then it is automatically cleared after performing the reset.
3. Write the desired external event or backup switchover settings (enabling function and interrupt on $\overline{\text{INT}}$ pin):
 - a. See [External Event Function](#)
 - b. See [Automatic BACKUP Switchover Interrupt Function](#)
4. Set the TSE bit to 1 to enable the Time Stamp function.

Hint: The $\overline{\text{INT}}$ signal is issued when EIE (RAM) or BSIE (EEPROM 37h) bit is set to 1. The EVF or BSF flag is set to 1 to indicate that a corresponding event has occurred.

Caution: Because the EVF flag is internally used for the identification of a First Event detection it is set by an event from the External Event function (TSS = 0, TSE = 1) or by an event of the Backup Switchover function (TSS = 1, TSE = 1). See also following scheme.

Complete Time Stamp scheme:



- (1) When TSO bit is set to 1 the TS registers (Seconds TS to Year TS) are overwritten. The last occurred event is recorded. When TSO bit is set to 0, the TS registers are overwritten once only. To initialize or reinitialize the first event function, the EVF has to be cleared (the TS registers can be cleared by writing 1 to the TSR bit). The counter Count TS is always working, independent of the settings of the overwrite bit TSO.
- (2) If set to 0 beforehand, the EVF flag indicates the occurrence of an External Event. The value 1 is retained until a 0 is written by the user.
Caution: The EVF flag is also set by an event of the Backup Switchover function when bits TSS and TSE are set to 1.
- (3) When TSR bit is set to 1, all seven time stamp registers (Count TS to Year TS) are cleared to 00h. The TSR bit is automatically cleared to 0 after performing the reset.
- (4) When 1 is written to the RESET bit, the Time Stamp event does not occur. The RESET bit is automatically cleared to 0 after performing the reset.
- (5) During I²C read access to the TS registers the time stamp capture function is blocked.

Figure 7-21 Time Stamp Scheme

7.16. FREQUENCY OFFSET CORRECTION

An aging adjustment or accuracy tuning can be done with the EEOffset value. The correction is purely digitally and has only the effect of shifting the time vs. temperature curve vertically up or down. It has no effect on the time vs. temperature characteristics of the final frequency. The EEOffset value contains a two's complement number with a range of +255 to -256 adjustment steps. The minimal correction step (one LSB) is $\pm 1 / (32768 * 32) = \pm 0.9537$ ppm. The compensation period is 32 seconds. The maximum correction range is from +243.2 ppm to -244.1 ppm.

Note that the signed offset value EEOffset corresponds to the correction value of the measured frequency (32.768 kHz). The user has access to this field (see [EEPROM Offset Register](#)).

7.16.1. EEOFFSET VALUE DETERMINATION

The EEOffset value is determined by the following process:

1. Select the 32.768 kHz frequency on the CLKOUT pin.
(If another frequency than 32.768 kHz is selected, the EEOffset value has to be set to 0 so that the uncorrected frequency can be measured, and the following calculations have to be adapted.)
2. Measure the frequency F_{meas} at CLKOUT pin in Hz.
3. Compute the offset value required in ppm: $P_{offset} = ((F_{meas} - 32768) / 32768 * 1'000'000)$
4. Compute the offset value in steps: $Offset = P_{offset} / (1 / (32768 * 32))$ in ppm) = $P_{offset} / (0.9537$ ppm)
5. If $Offset > 256$, the frequency is too high to be corrected.
6. Else if $1 \leq Offset \leq 256$ (correction is $-1 \geq Offset_{Corr.} \geq -256$), \rightarrow set $EEOffset = 512 - Offset$
7. Else if $-255 \leq Offset \leq 0$ (correction is $+255 \leq Offset_{Corr.} \leq 0$), \rightarrow set $EEOffset = - Offset$
8. Else the frequency is too low to be corrected.

Examples:

- If 32768.48 Hz is measured when the 32.768 kHz clock is selected, the offset is +0.48 Hz, which is $+0.48 \text{ Hz} / 32768 \text{ Hz} * 1'000'000 = +14.648$ ppm. The Offset value in steps is then calculated as follows: $+14.648 \text{ ppm} / 0.9537 \text{ ppm} = +15.36$, the rounded integral part is 15 (the offset correction is -15 steps). The unsigned EEOffset value is then: $512 - 15 = +497$. In binary, $EEOffset = 111110001$.
- If 32767.52 Hz is measured when the 32.768 kHz clock is selected, the offset is -0.48 Hz, which is $-0.48 \text{ Hz} / 32768 \text{ Hz} * 1'000'000 = -14.648$ ppm. The Offset value in steps is then calculated as follows: $-14.648 \text{ ppm} / 0.9537 \text{ ppm} = -15.36$, the rounded integral part is -15 (the offset correction is +15 steps). The EEOffset value is then: $-(-15) = +15$. In binary, $EEOffset = 000001111$.

7.16.2. VERIFICATION OF THE CORRECTED TIME ACCURACY

The offset correction can be verified by the following process:

1. Enter the calculated EEOffset value (see [EEOFFSET Value Determination](#)).
2. Select the 1 Hz frequency on the CLKOUT pin (if another frequency is selected the following calculations have to be adapted).
3. Measure every period during one compensation period of 32 seconds at CLKOUT pin.
4. Calculate the average frequency F_{meas_aver} in Hz.
5. Compute the new achieved offset value in ppm: $P_{offset} = ((F_{meas_aver} - 1) / 1 * 1'000'000)$

7.17. UNIX TIME COUNTER

The UNIX Time counter is a 32-bit counter, unsigned integer, which rolls over to 00000000h when reaching the value FFFFFFFFh. The 4 bytes are fully readable and writable. The counter source clock is the digitally tuned 1 Hz clock frequency of the prescaler.

After writing the required time value into the UNIX Time registers, the write access can be synchronized by the RESET bit function. When 1 is written to the RESET bit in control 2 register, the associated I²C stop condition will synchronize the 1 Hz counter clock to the desired accurate time. The RESET bit is then automatically cleared. The first 1 Hz period after synchronization will be 0 to 244 μ s shorter than 1 second. The 32-bit counter value itself is not changed at the moment when 1 is written to the RESET bit.

When reading the counter, the current value is returned. Since it is not possible to block the counter during read, it is recommended to read the four registers (UNIX Time 0 to UNIX Time 3) twice and to check for consistent results.

Write to UNIX Time counter and synchronization by using RESET bit:

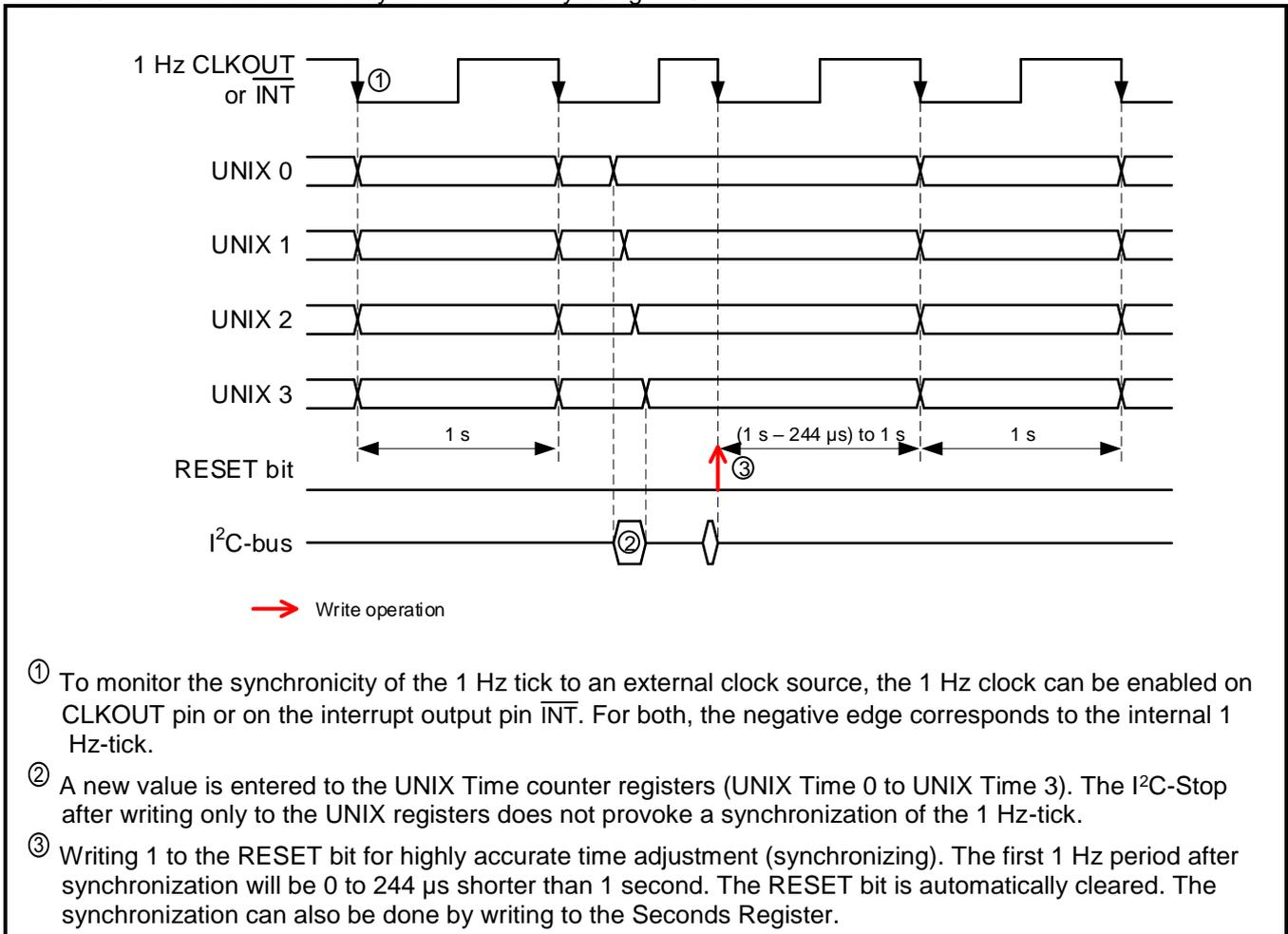


Figure 7-22 Unix Time Counter

7.18. RESET BIT FUNCTION

The RESET bit is used for a software-based accurate and safe starting of the time circuits.

When 1 is written to the RESET bit, the clock prescaler for 4096 Hz to 1Hz is reset and an eventual present memorized 1 Hz update is also reset. This bit is then automatically cleared. Because the upper two stages of the prescaler are not reset and the I²C interface is asynchronous, the next 1 Hz clock will be between (1 second – 244 μs) and 1 second. Resetting the prescaler will have an influence on the length of current clock period on all subsequent peripherals (clock and calendar, CLKOUT clock, timer clock, update timer clock, UNIX clock, EVI input filter).

The RESET bit function will not affect the CLKOUT of 32.768 kHz and 8192 Hz (see also **CLKOUT Frequency Selection**).

RESET bit functional diagram:

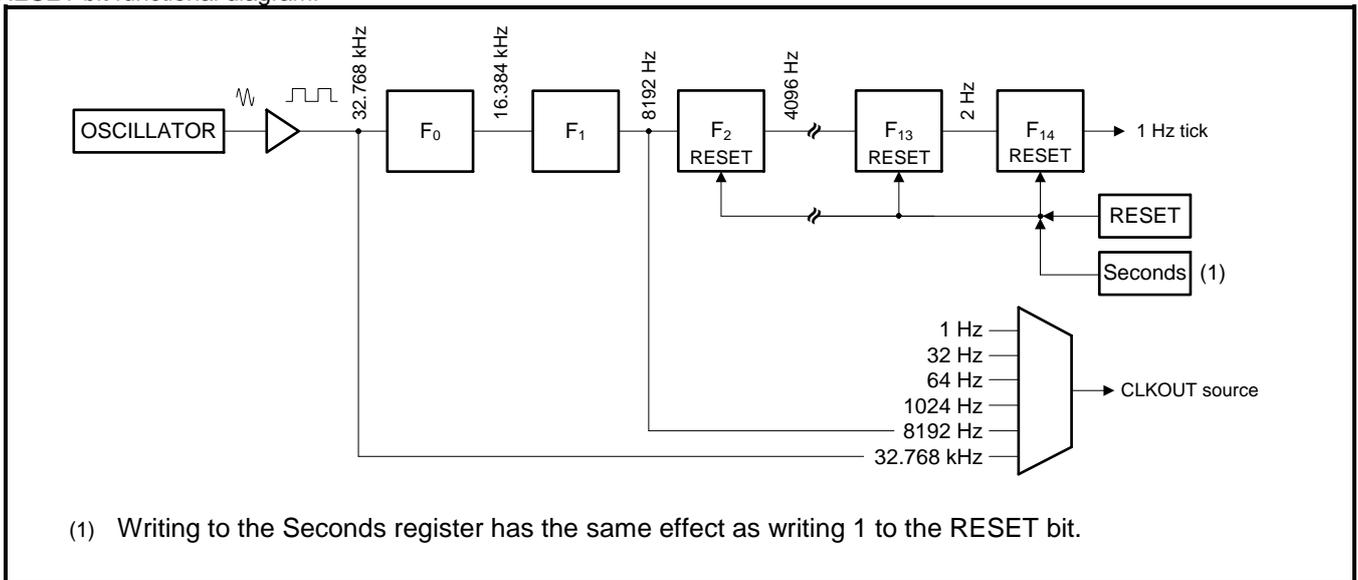


Figure 7-23 Reset bit Function

The clock and calendar can be set (in < 950 ms) and then synchronized by writing 1 to the RESET bit.

Setting the clock and calendar values using the RESET bit function:

1. Write the desired clock and calendar values to the registers (seconds, minutes, hours, weekday, date, month and year).
2. Write 1 to the RESET bit for a synchronized start of the time circuits (1 Hz tick). The RESET bit is automatically cleared.

7.19. USER PROGRAMMABLE PASSWORD

After a Power up and the first refreshment of ~66ms, the PW0 to PW3 registers are reset to 00h and the EEPWE (EEPROM 30h) and EEPW 0 to EEPW 3 values (EEPROM 31h to 34h) are copied from the EEPROM.

The first four Password registers (PW0 to PW3), in case of the use of the function (enabled by writing 255 into the EEPROM Password Enable register EEPWE), are used to write the 32-Bit Password necessary to be able to write in all writable registers (time and configuration registers). This 32-Bit Password is compared to the 32 bits stored in EEPROM Password registers EEPW 0 to EEPW 3 (see [PASSWORD Registers](#), [EEPROM Password Enable Register](#) and [EEPROM Password Registers](#)).

Caution: The number of possible passwords is $2^{32} \approx 4.3 * 10^9 = 4.3$ billion.

7.19.1. ENABLING/DISABLING WRITE PROTECTION

If the write protection function is enabled by writing 255 in register EEPWE (EEPROM 30h), it remains possible to read all the registers except the EEPROM registers. If the function is not enabled, read and write are possible for all corresponding registers.

If the write protection function is enabled, it is necessary to first write the 32-Bit Password before any attempt to write in the RAM registers, and to read and write in the EEPROM registers.

Once the user is finished with the write access and subsequently the write protection is enabled again (by writing 255 in EEPROM register EEPWE), it is necessary to write an incorrect password (PW \neq EEPW) into the Password registers PW0 to PW3 in order to write-protect the registers. See complete program sequences below and [Flowchart](#).

Enable write protection:

1. Registers are Not write-protected (EEPWE \neq 255)
2. Reference password is stored here (EEPW 0 to EEPW 3)
3. Disable automatic refresh (EERD = 1)
4. Enable password function (EEPWE = 255) (RAM)
5. Enter the correct password PW (PW = EEPW) to unlock write protection (PW0 to PW3)
6. Update EEPROM (all Configuration RAM \rightarrow EEPROM) with EEcmd = 00h followed by 11h
7. Enable automatic refresh (EERD = 0)
8. Enter an incorrect password PW (PW \neq EEPW) to (PW0 to PW3) to lock the device
9. Registers are Write-protected by password (EEPWE = 255)

Disable write protection:

1. Registers are write protected by password (EEPWE = 255)
2. Reference password is stored here (EEPW 0 to EEPW 3)
3. Enter the correct password PW (PW = EEPW) to unlock write protection (PW0 to PW3)
4. Disable automatic refresh (EERD = 1)
5. Disable password function (EEPWE \neq 255) (RAM)
6. Update EEPROM (all Configuration RAM \rightarrow EEPROM) with EEcmd = 00h followed by 11h
7. Enable automatic refresh (EERD = 0)
8. Registers are Not write-protected (EEPWE \neq 255)

7.19.2. CHANGING PASSWORD

To code a new password, the user has to first enter the current (correct) password into the Password registers (PW0 to PW3) if the registers are write protected, and writing a value not equal to all 1 (value \neq 255) in the EEPWE register (EEPROM 30h) to unlock write protection, and then write the new one in the registers EEPW 0 to EEPW 3 (EEPROM 31h to 34h) and writing all 1 (value = 255) in the EEPWE register to enable password function. See complete program sequences below and Figure 7-24 User Programmable Password Flowchart.

Change password if password function is enabled (EEPWE = 255):

1. Registers are Write-protected by old password (EEPW 0 to EEPW 3)
2. Enter old password PW (PW = EEPW) to unlock write protection (PW0 to PW3)
3. Disable automatic refresh (EERD = 1)
4. Disable password function (EEPWE \neq 255)
5. Define a new password EEPW (EEPW 0 to EEPW 3) (RAM), and edit other configuration settings (RAM)
6. Enable the password function (EEPWE = 255) (RAM)
7. Enter correct password PW (PW = EEPW) to unlock write protection (PW0 to PW3)
8. Update EEPROM (all Configuration RAM \rightarrow EEPROM) with EEcmd = 00h followed by 11h
9. Enable automatic refresh (EERD = 0)
10. Enter an incorrect password PW (PW \neq EEPW) to (PW0 to PW3) to lock the device
11. Registers are Write-protected by new password (EEPW 0 to EEPW 3)

Change password if password function is disabled (EEPWE \neq 255):

1. Old password is stored here (EEPW 0 to EEPW 3)
2. Disable automatic refresh (EERD = 1)
3. Define a new password EEPW (EEPW 0 to EEPW 3) (RAM), and edit other configuration settings (RAM)
4. Update EEPROM (all Configuration RAM \rightarrow EEPROM) with EEcmd = 00h followed by 11h
5. Enable automatic refresh (EERD = 0)
6. New password is stored here (EEPW 0 to EEPW 3)

7.19.3. FLOWCHART

The following Flowchart describes the programming of the enabling and disabling of the register write protection by user password and the changing of the user password if write protection is enabled or disabled.

User programmable password for register write protection:

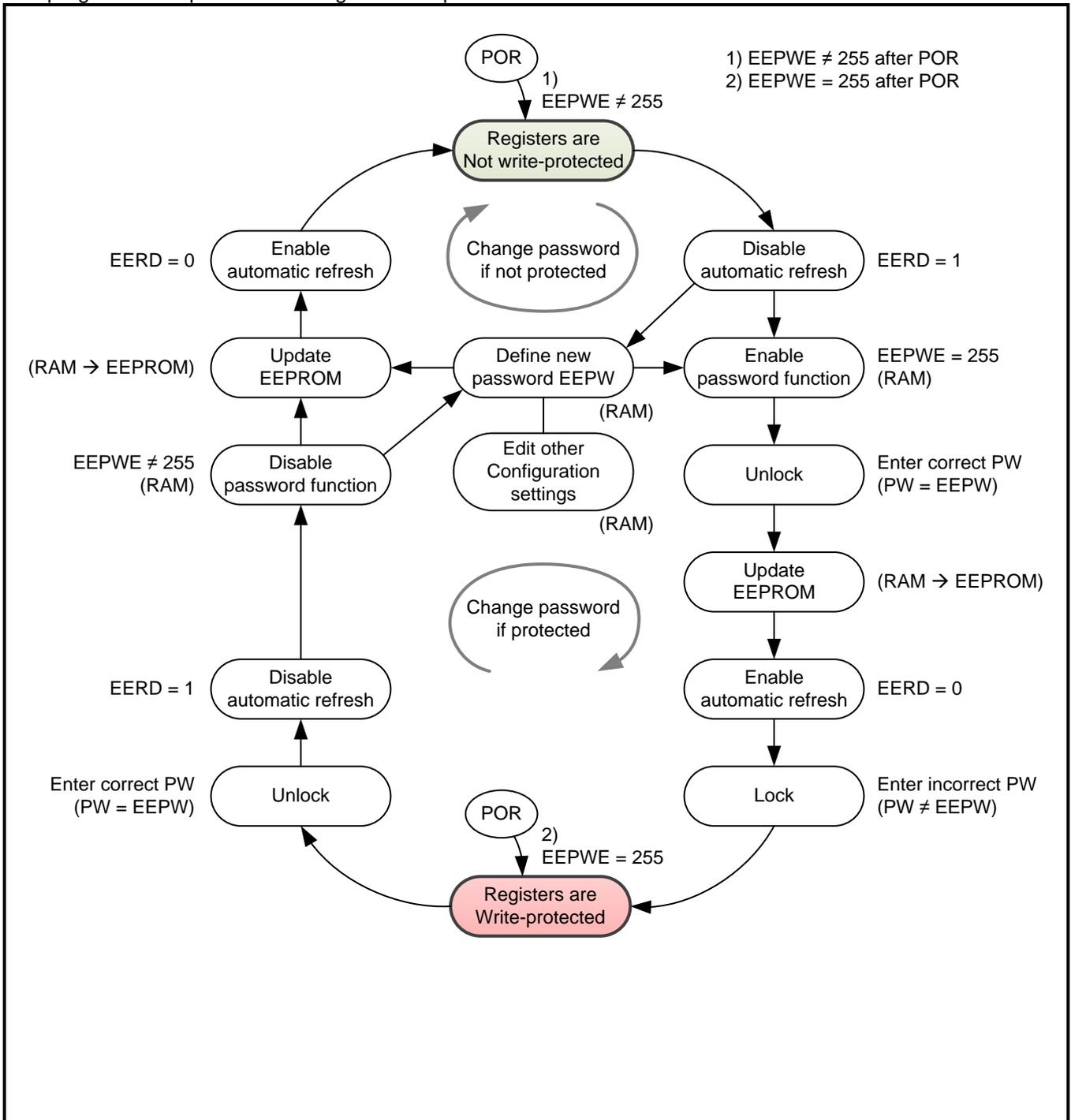


Figure 7-24 User Programmable Password Flowchart

7.20. I²C INTERFACE

The I²C interface is for bidirectional, two-line communication between different ICs or modules. The EM3028 is accessed at addresses A4h/A5h, and supports Fast Mode (up to 400 kHz). The I²C interface consists of two lines: one bi-directional data line (SDA) and one clock line (SCL). Both lines are connected to a positive supply via pull-up resistors. Data transfer is initiated only when the interface is not busy.

7.20.1. BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as a control signals. Data changes should be executed during the LOW period of the clock pulse (see [Figure 7-25 I²C Bit Transfer](#)).

Bit transfer:

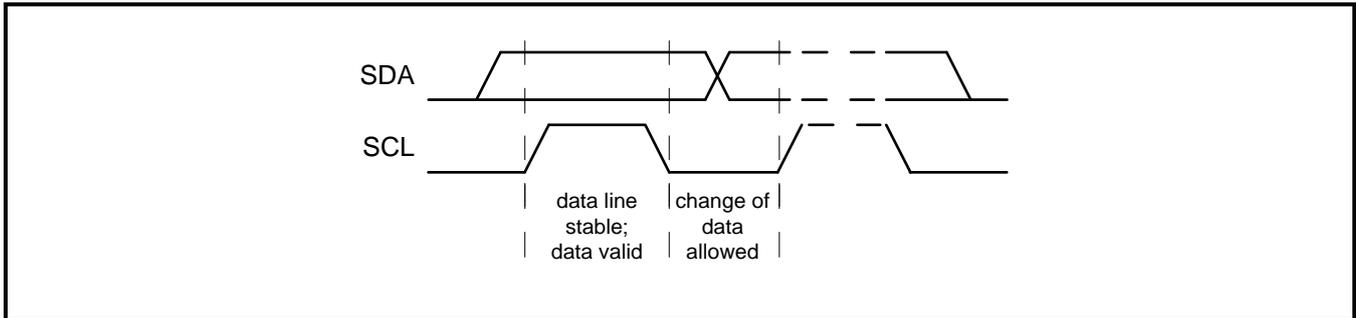


Figure 7-25 I²C Bit Transfer

7.20.2. START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (P) (see [Figure 7-26 I²C Start and Stop Conditions](#)).

Definition of START and STOP conditions:

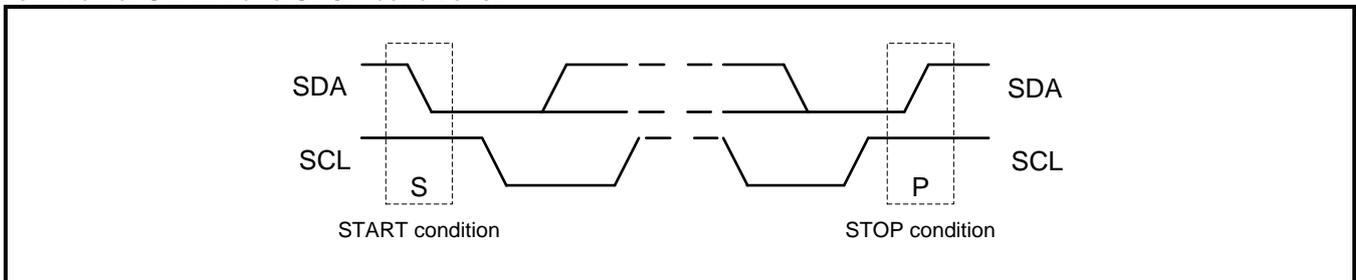


Figure 7-26 I²C Start and Stop Conditions

A START condition which occurs after a previous START but before a STOP is called a Repeated START condition, and functions exactly like a normal STOP followed by a normal START.

Caution:

When communicating with the EM3028, the series of operations from transmitting the START condition to transmitting the STOP condition should occur within **950 ms**.

If this series of operations requires **950 ms or longer**, the I²C bus interface will be automatically cleared and set to standby mode by the bus timeout function of the EM3028. Note with caution that both write and read operations are invalid for communications that occur during or after this auto clearing operation (when the read operation is invalid, all data that is read has a value of FFh).

Restarting of communications begins with transfer of the START condition again.

7.20.3. DATA VALID

After a START condition, SDA is stable for the duration of the high period of SCL. The data on SDA may be changed during the low period of SCL. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is not limited (however, the transfer time must be no longer than 950 ms). The information is transmitted byte-wide and each receiver acknowledges with a \overline{INT} bit.

7.20.4. SYSTEM CONFIGURATION

Since multiple devices can be connected with the I²C-bus, all I²C-bus devices have a fixed and unique device number built-in to allow individual addressing of each device.

The device that controls the I²C-bus is the Master; the devices which are controlled by the Master are the Slaves. A device generating a message is a Transmitter; a device receiving a message is the Receiver. The EM3028 acts as a Slave-Receiver or Slave-Transmitter.

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

System configuration:

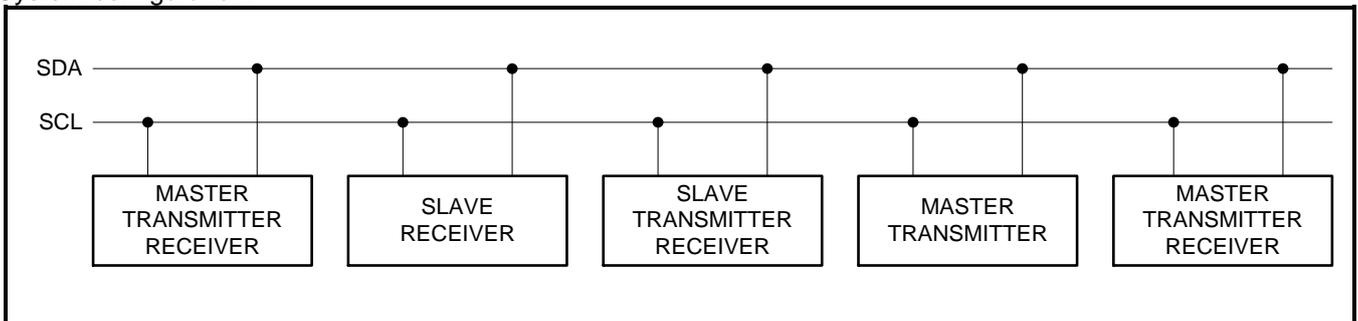


Figure 7-27 I²C System Configuration

7.20.5. ACKNOWLEDGE

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited (however, the transfer time must be no longer than 950 ms). Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge cycle after the reception of each byte.
- Also a master receiver must generate an acknowledge cycle after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge cycle on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Data transfer and acknowledge on the I²C-bus:

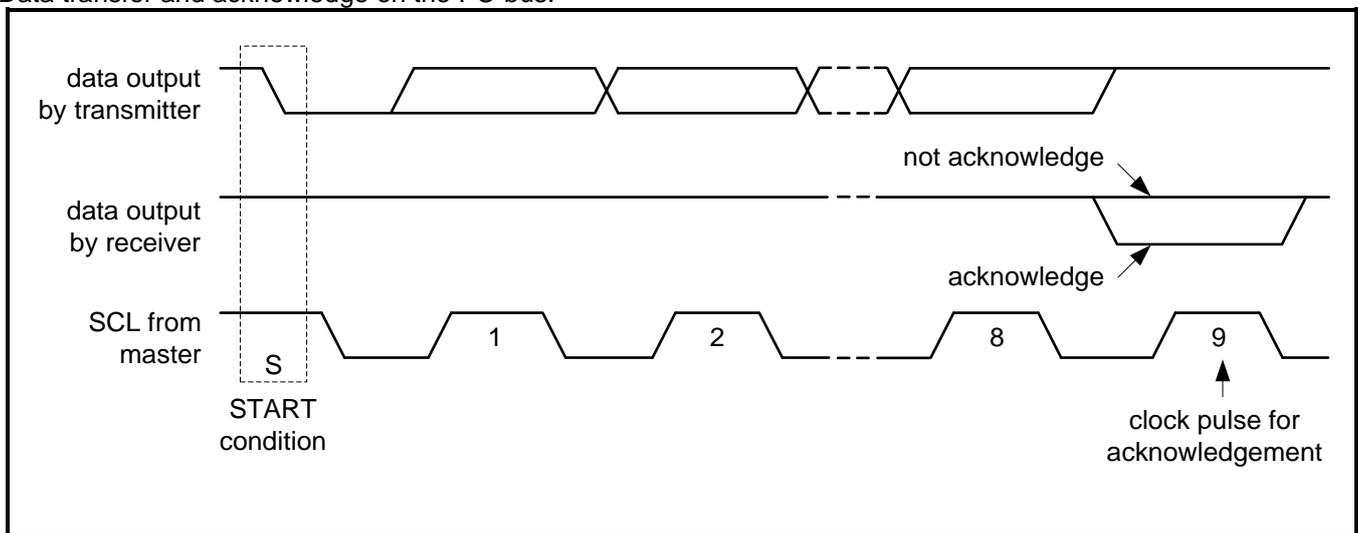


Figure 7-28 I²C Acknowledge

7.20.6. SLAVE ADDRESS

On the I²C-bus the 7-bit slave address 1010010b is reserved for the EM3028. The entire I²C-bus slave address byte is shown in the following table.

| Slave address | | | | | | | R/W | Transfer data |
|---------------|-------|-------|-------|-------|-------|-------|----------------------|---------------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 (R) | A5h (read) |
| | | | | | | | 0 (\overline{W}) | A4h (write) |

Table 69 I²C Slave Address

After a START condition, the I²C slave address has to be sent to the EM3028 device. The $\overline{R/W}$ bit defines the direction of the following single or multiple byte data transfer. The 7-bit address is transmitted MSB first. If this address is 1010010b, the EM3028 is selected, the eighth bit indicates a read ($\overline{R/W} = 1$) or a write ($\overline{R/W} = 0$) operation (results in A5h or A4h) and the EM3028 supplies the ACK. The EM3028 ignores all other address values and does not respond with an ACK.

In the write operation, a data transfer is terminated by sending either the STOP condition or the START condition of the next data transfer.

7.20.7. WRITE OPERATION

Master transmits to Slave-Receiver at specified address. The Register Address is an 8-bit value that defines which register is to be accessed next. After writing one byte, the Register Address is automatically incremented by 1.

Master writes to slave EM3028 at specific address:

- 1) Master sends out the START condition.
- 2) Master sends out Slave Address, A4h for the EM3028; the $\overline{R/W}$ bit is a 0 indicating a write operation.
- 3) Acknowledgement from EM3028.
- 4) Master sends out the Register Address to EM3028.
- 5) Acknowledgement from EM3028.
- 6) Master sends out the Data to write to the specified address in step 4).
- 7) Acknowledgement from EM3028.
- 8) Steps 6) and 7) can be repeated if necessary. The address is automatically incremented in the EM3028.
- 9) Master sends out the STOP Condition.

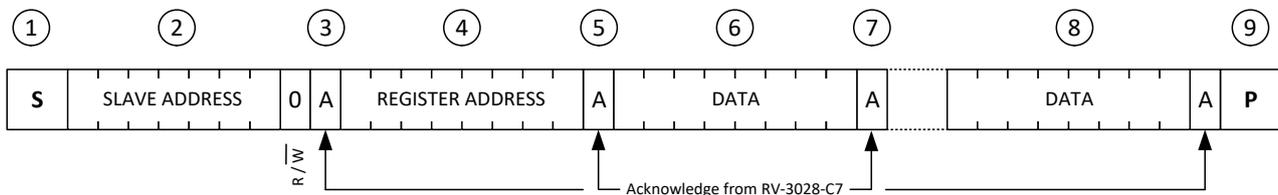


Figure 7-29 I²C Write Operation

7.20.8. READ OPERATION AT SPECIFIC ADDRESS

Master reads data from slave EM3028 at specific address:

- 1) Master sends out the START condition.
- 2) Master sends out Slave Address, A4h for the EM3028; the R/W bit is a 0 indicating a write operation.
- 3) Acknowledgement from EM3028.
- 4) Master sends out the Register Address to EM3028.
- 5) Acknowledgement from EM3028.
- 6) Master sends out the Repeated START condition (or STOP condition followed by START condition)
- 7) Master sends out Slave Address, A5h for the EM3028; the R/W bit is a 1 indicating a read operation.
- 8) Acknowledgement from EM3028.
At this point, the Master becomes a Receiver and the Slave becomes the Transmitter.
- 9) The Slave sends out the Data from the Register Address specified in step 4).
- 10) Acknowledgement from Master.
- 11) Steps 9) and 10) can be repeated if necessary. The address is automatically incremented in the EM3028.
- 12) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a STOP condition.
- 13) Master sends out the STOP condition.

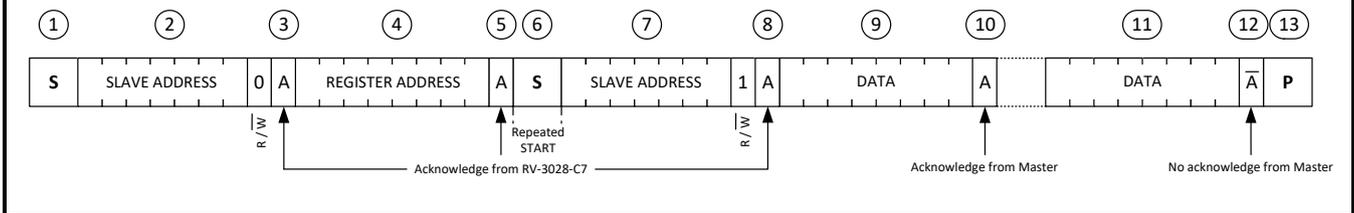


Figure 7-30 I²C Master reads data from slave EM3028 at specific address

7.20.9. READ OPERATION

Master reads data from slave EM3028 immediately after first byte:

- 1) Master sends out the START condition.
- 2) Master sends out Slave Address, A5h for the EM3028; the R/W bit is a 1 indicating a read operation.
- 3) Acknowledgement from EM3028.
At this point, the Master becomes a Receiver and the Slave becomes the Transmitter.
- 4) The EM3028 sends out the Data from the last accessed Register Address incremented by 1.
- 5) Acknowledgement from Master.
- 6) Steps 4) and 5) can be repeated if necessary. The address is automatically incremented in the EM3028.
- 7) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a STOP condition.
- 8) Master sends out the STOP condition.

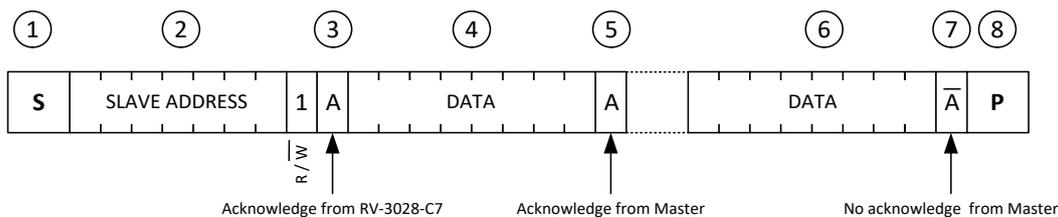


Figure 7-31 I²C Master reads data from slave EM3028 immediately after first byte

7.20.10. I²C-BUS IN SWITCHOVER CONDITION

To save power when the EM3028 is in V_{BACKUP} Power state the bus I²C-bus interface is automatically disabled (high impedance) and reset. Therefore the communication via I²C interface should be terminated before the supply is switched from V_{DD} to V_{BACKUP} . When the bus communication is not terminated in a proper way, the time counters get corrupted.

If the I²C communication was terminated uncontrolled, the I²C has to be reinitialized by sending a STOP followed by a START after the device switched back from V_{BACKUP} Power state to V_{DD} Power state.

8. TYPICAL APPLICATION

8.1. OPERATING EM3028-C7 WITH BACKUP SUPPLY VOLTAGE

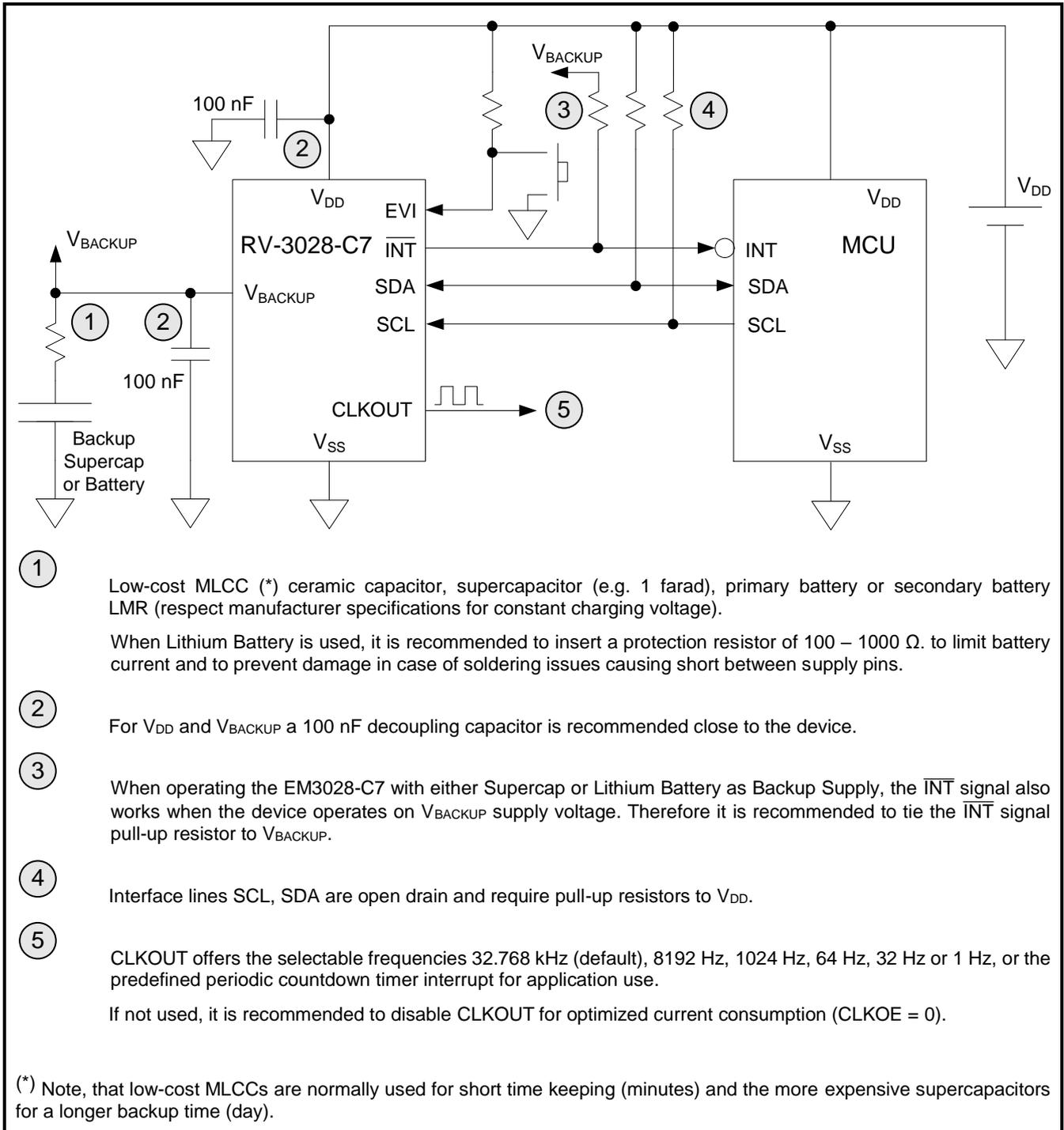


Figure 8-1 Example of Application

| CM7V-T1A | Crystal | 32768Hz |
|----------------------|--------------|-------------------------------------|
| Super capacitor | C_{BACKUP} | 1 F(supercap) or smaller value MLCC |
| Decoupling capacitor | C_D | 100 nF |
| Pullup resistor | R_{PULLUP} | 10kΩ |

Table 70 Component list

9. ORDERING INFORMATION

| Part Nb | Package form | Delivery form |
|------------|--------------|---------------------------------|
| EM3028C7B+ | SMD C7 | Tape & Reel 1000 IC per tape |

Table 71 Ordering Information

For other delivery formats please contact EM Microelectronics representative.

10. PACKAGING INFORMATION

10.1. C7 PACKAGE

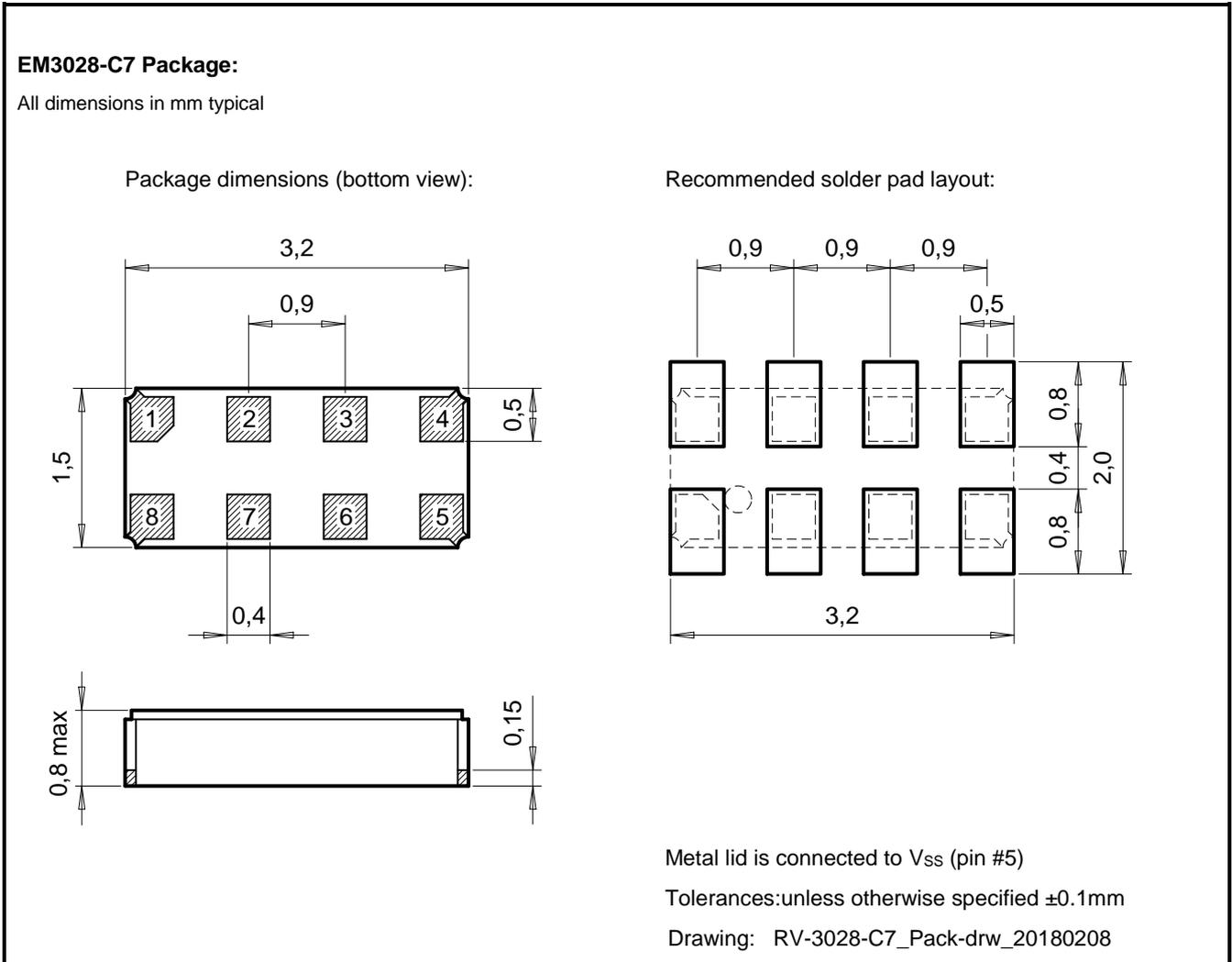


Figure 10-1 C7 Package Outline Drawing

10.2. RECOMMENDED THERMAL RELIEF

When connecting a pad to a copper plane, thermal relief is recommended.

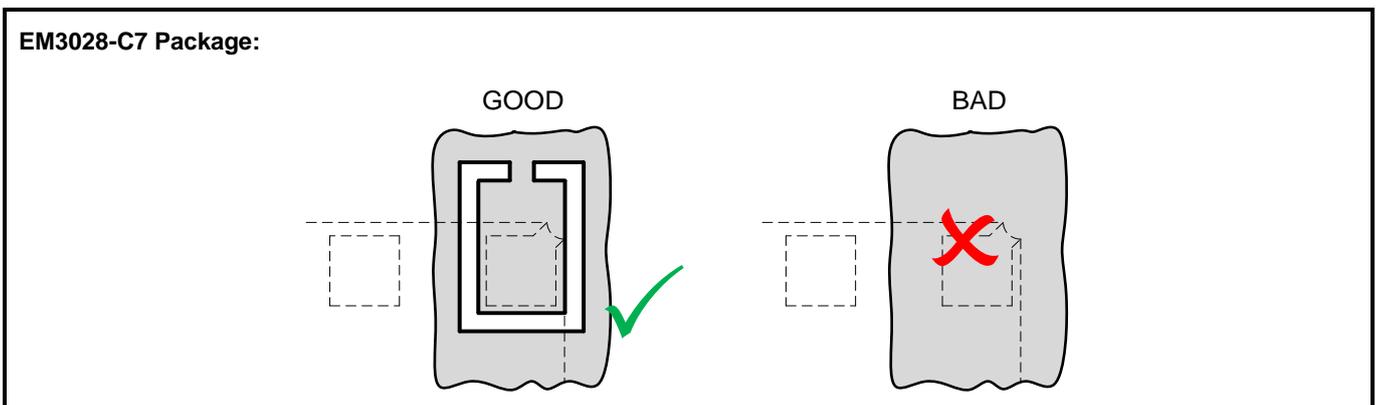
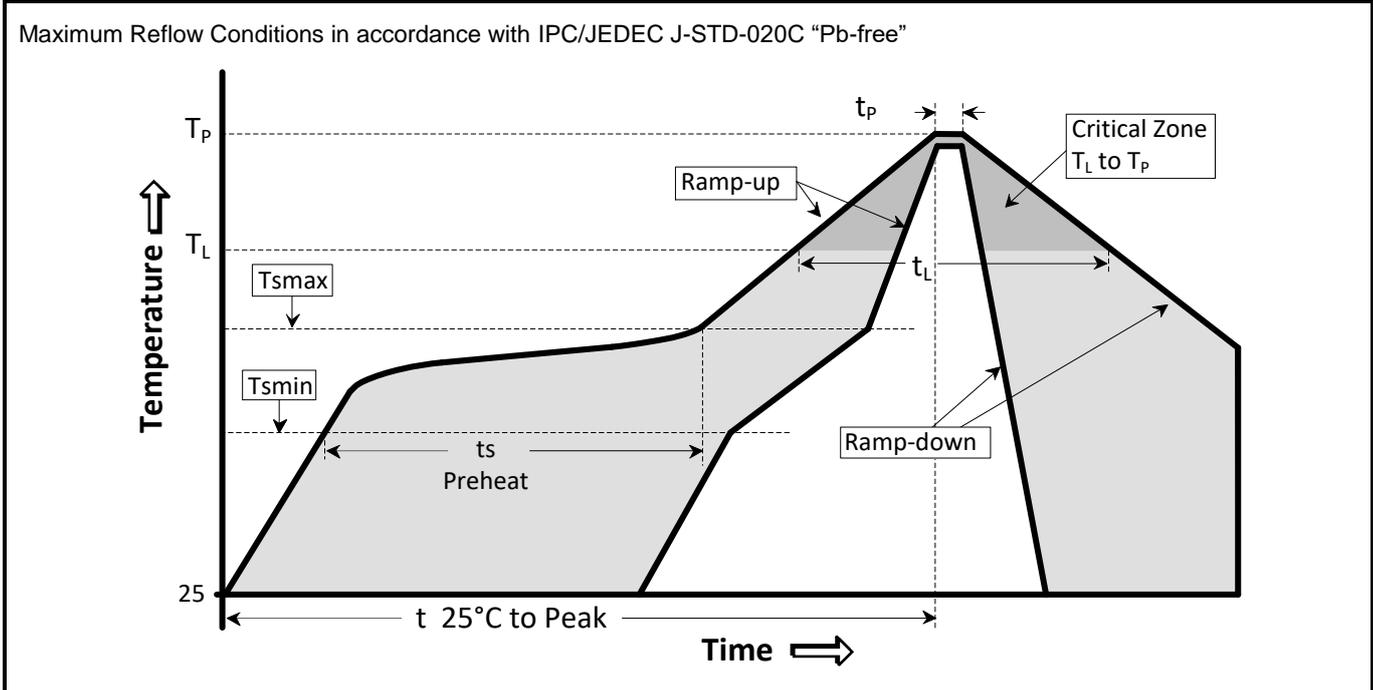


Figure 10-2 C7 Package Thermal Relief

11. SOLDERING INFORMATION



| Temperature Profile | Symbol | Condition | Unit |
|---|--|------------------|--------|
| Average ramp-up rate | (T _{Smax} to T _P) | 3°C / second max | °C / s |
| Ramp down Rate | T _{cool} | 6°C / second max | °C / s |
| Time 25°C to Peak Temperature | T _{to-peak} | 8 minutes max | min |
| Preheat | | | |
| Temperature min | T _{Smin} | 150 | °C |
| Temperature max | T _{Smax} | 200 | °C |
| Time T _{Smin} to T _{Smax} | t _s | 60 – 180 | sec |
| Soldering above liquidus | | | |
| Temperature liquidus | T _L | 217 | °C |
| Time above liquidus | t _L | 60 – 150 | sec |
| Peak temperature | | | |
| Peak Temperature | T _p | 260 | °C |
| Time within 5°C of peak temperature | t _p | 20 – 40 | sec |

12. HANDLING PRECAUTIONS FOR MODULES WITH EMBEDDED CRYSTALS

The built-in tuning-fork crystal consists of pure Silicon Dioxide in crystalline form. The cavity inside the package is evacuated and hermetically sealed in order for the crystal blank to function undisturbed from air molecules, humidity and other influences.

Shock and vibration:

Keep the crystal / module from being exposed to **excessive mechanical shock and vibration**. The crystal / module will bear a mechanical shock of 5000 g / 0.3 ms.

The following special situations may generate either shock or vibration:

Multiple PCB panels - Usually at the end of the pick & place process the single PCBs are cut out with a router. These machines sometimes generate vibrations on the PCB that have a fundamental or harmonic frequency close to 32.768 kHz. This might cause breakage of crystal blanks due to resonance. Router speed should be adjusted to avoid resonant vibration.

Ultrasonic cleaning - Avoid cleaning processes using ultrasonic energy. These processes can damage crystals due to mechanical resonance of the crystal blank.

Overheating, rework high temperature exposure:

Avoid overheating the package. The package is sealed with a seal ring consisting of 80% Gold and 20% Tin. The eutectic melting temperature of this alloy is at 280°C. Heating the seal ring up to >280°C will cause melting of the metal seal which then, due to the vacuum, is sucked into the cavity forming an air duct. This happens when using hot-air-gun set at temperatures >300°C.

Use the following methods for rework:

- Use a hot-air- gun set at 270°C.
- Use 2 temperature controlled soldering irons, set at 270°C, with special-tips to contact all solder-joints from both sides of the package at the same time, remove part with tweezers when pad solder is liquid.

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