

4525GEH-VB Datasheet

N- and P-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY		
	N-CHANNEL	P-CHANNEL
V_{DS} (V)	40	- 40
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 10$ V	0.014	0.014
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 4.5$ V	0.016	0.016
I_D (A)	50	- 50
Configuration	N- and P-Pair	

FEATURES

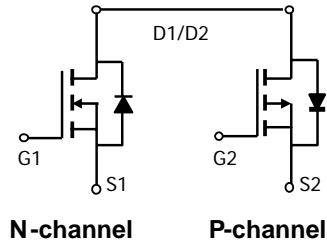
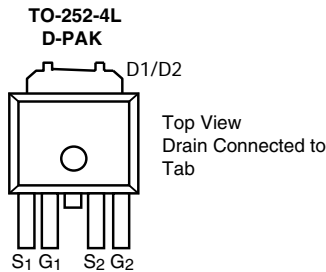
- Trench Power MOSFET
- 100 % R_g and UIS Tested



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- CCFL Inverter



ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)					
PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT	
Drain-Source Voltage	V_{DS}	40	- 40	V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ^a	I_D	$T_C = 25\text{ }^\circ\text{C}$	50	-50	A
		$T_C = 125\text{ }^\circ\text{C}$	35	-35	
Continuous Source Current (Diode Conduction) ^a	I_S	50	-50		
Pulsed Drain Current ^b	I_{DM}	150	-150		
Single Pulse Avalanche Current	I_{AS}	L = 0.1 mH	30	- 30	mJ
Single Pulse Avalanche Energy			E_{AS}	245	
Maximum Power Dissipation ^b	P_D	$T_C = 25\text{ }^\circ\text{C}$	108	108	W
		$T_C = 125\text{ }^\circ\text{C}$	32	32	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175		$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)		260			

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Junction-to-Ambient	R_{thJA}	85	85	$^\circ\text{C/W}$
Junction-to-Case (Drain)				

Notes

- Package limited.
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.

SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		N-Ch	40	-	-
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$		P-Ch	-40	-	-
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		N-Ch	1.0	-	3.0
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		P-Ch	-1.0	-	-3.0
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		N-Ch	-	-	± 100
				P-Ch	-	-	± 100
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}$	N-Ch	-	-	1
		$V_{GS} = 0\text{ V}$	$V_{DS} = -40\text{ V}$	P-Ch	-	-	-1
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$	N-Ch	-	-	50
		$V_{GS} = 0\text{ V}$	$V_{DS} = -40\text{ V}, T_J = 125\text{ }^\circ\text{C}$	P-Ch	-	-	-50
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 175\text{ }^\circ\text{C}$	N-Ch	-	-	150
		$V_{GS} = 0\text{ V}$	$V_{DS} = -40\text{ V}, T_J = 175\text{ }^\circ\text{C}$	P-Ch	-	-	-150
On-State Drain Current ^a	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	N-Ch	25	-	-
		$V_{GS} = -10\text{ V}$	$V_{DS} \leq 5\text{ V}$	P-Ch	-25	-	-
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 38\text{ A}$	N-Ch	-	0.014	-
		$V_{GS} = -10\text{ V}$	$I_D = -38\text{ A}$	P-Ch	-	0.014	-
		$V_{GS} = 10\text{ V}$	$I_D = 38\text{ A}, T_J = 125\text{ }^\circ\text{C}$	N-Ch	-	0.017	-
		$V_{GS} = -10\text{ V}$	$I_D = -38\text{ A}, T_J = 125\text{ }^\circ\text{C}$	P-Ch	-	0.017	-
		$V_{GS} = 10\text{ V}$	$I_D = 38\text{ A}, T_J = 175\text{ }^\circ\text{C}$	N-Ch	-	0.025	-
		$V_{GS} = -10\text{ V}$	$I_D = -38\text{ A}, T_J = 175\text{ }^\circ\text{C}$	P-Ch	-	0.025	-
		$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$	N-Ch	-	0.016	-
$V_{GS} = -4.5\text{ V}$	$I_D = -30\text{ A}$	P-Ch	-	0.016	-		
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 38\text{ A}$		N-Ch	-	40	-
		$V_{DS} = -15\text{ V}, I_D = -38\text{ A}$		P-Ch	-	18	-
Dynamic^b							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, f = 1\text{ MHz}$	N-Ch	-	1799	2248
		$V_{GS} = 0\text{ V}$	$V_{DS} = -20\text{ V}, f = 1\text{ MHz}$	P-Ch	-	2000	3500
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, f = 1\text{ MHz}$	N-Ch	-	282	352
		$V_{GS} = 0\text{ V}$	$V_{DS} = -20\text{ V}, f = 1\text{ MHz}$	P-Ch	-	320	550
Reverse Transfer Capacitance	C_{rss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, f = 1\text{ MHz}$	N-Ch	-	109	136
		$V_{GS} = 0\text{ V}$	$V_{DS} = -20\text{ V}, f = 1\text{ MHz}$	P-Ch	-	220	360
Total Gate Charge ^c	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 10\text{ A}$	N-Ch	-	310	-
		$V_{GS} = -10\text{ V}$	$V_{DS} = -20\text{ V}, I_D = -10\text{ A}$	P-Ch	-	420	-
Gate-Source Charge ^c	Q_{gs}	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 10\text{ A}$	N-Ch	-	5.7	-
		$V_{GS} = -10\text{ V}$	$V_{DS} = -20\text{ V}, I_D = -10\text{ A}$	P-Ch	-	5.5	-
Gate-Drain Charge ^c	Q_{gd}	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 10\text{ A}$	N-Ch	-	4.8	-
		$V_{GS} = -10\text{ V}$	$V_{DS} = -20\text{ V}, I_D = -10\text{ A}$	P-Ch	-	10.5	-
Gate Resistance	R_g	$f = 1\text{ MHz}$		N-Ch	2	4.11	6.2
				P-Ch	3.1	6.3	9.5

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.
 c. Independent of operating temperature.

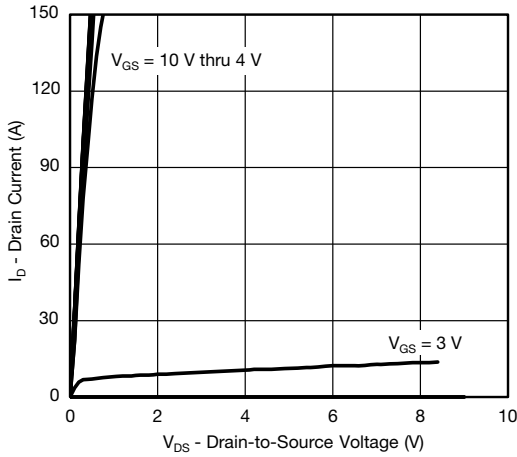
SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\ \Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch	-	7	11	ns
		$V_{DD} = -20\text{ V}, R_L = 2\ \Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\ \Omega$	P-Ch	-	11	17	
Rise Time ^c	t_r	$V_{DD} = 20\text{ V}, R_L = 2\ \Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch	-	21	32	
		$V_{DD} = -20\text{ V}, R_L = 2\ \Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\ \Omega$	P-Ch	-	9	14	
Turn-Off Delay Time ^c	$t_{d(off)}$	$V_{DD} = 20\text{ V}, R_L = 2\ \Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch	-	33	50	
		$V_{DD} = -20\text{ V}, R_L = 2\ \Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\ \Omega$	P-Ch	-	55	83	
Fall Time ^c	t_f	$V_{DD} = 20\text{ V}, R_L = 2\ \Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch	-	19	29	
		$V_{DD} = -20\text{ V}, R_L = 2\ \Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\ \Omega$	P-Ch	-	91	137	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I_{SM}		N-Ch	-	-	32	A
			P-Ch	-	-	-32	
Forward Voltage	V_{SD}	$I_S = 4\text{ A}$	N-Ch	-	0.79	1.2	V
		$I_S = -4\text{ A}$	P-Ch	-	-0.82	-1.2	

Notes

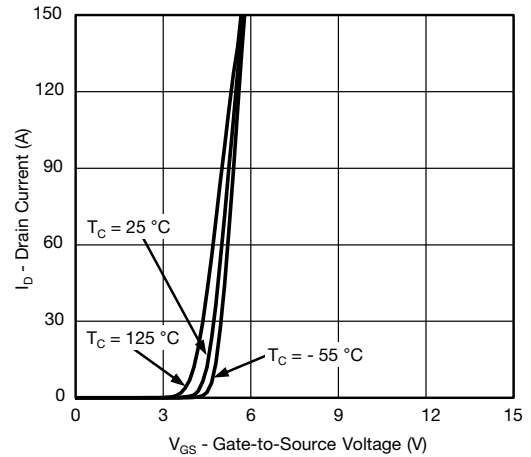
- Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

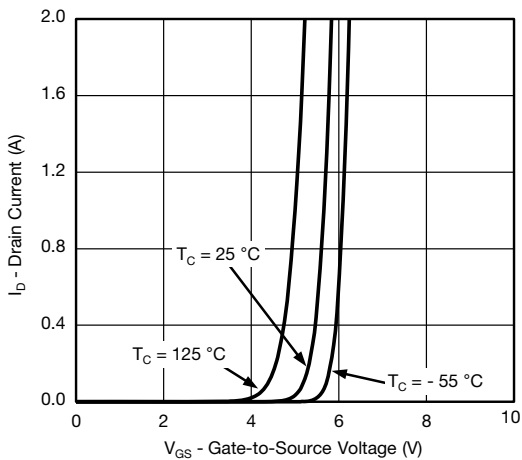
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



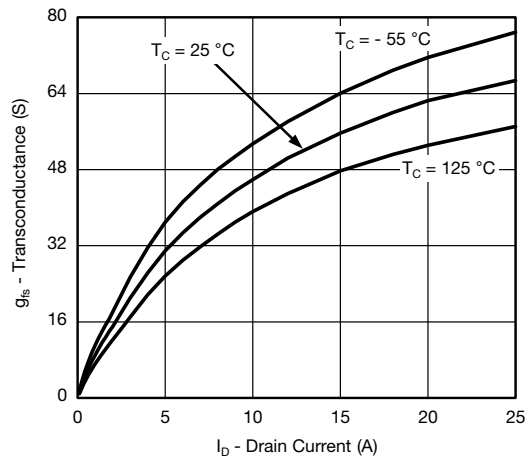
Output Characteristics



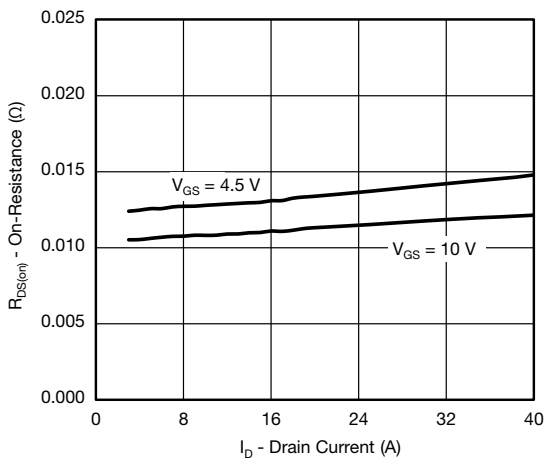
Transfer Characteristics



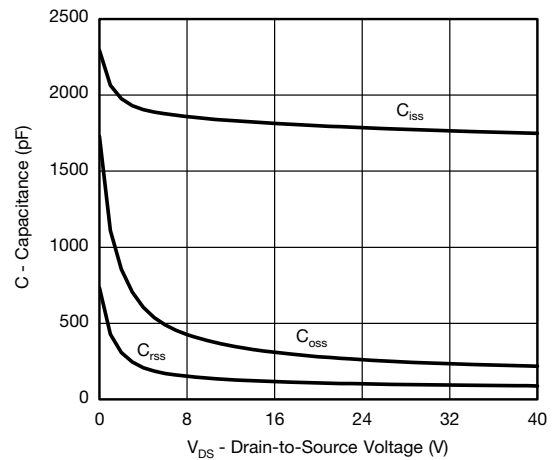
Transfer Characteristics



Transconductance

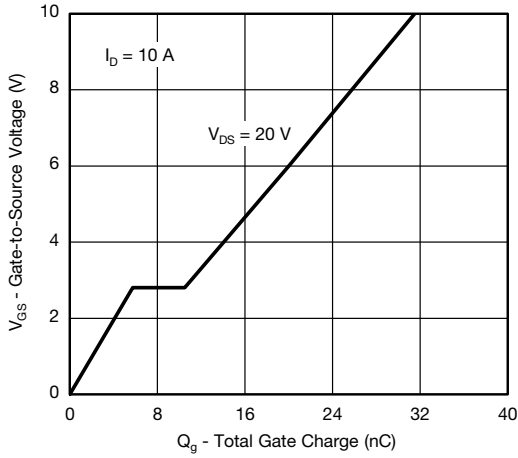


On-Resistance vs. Drain Current

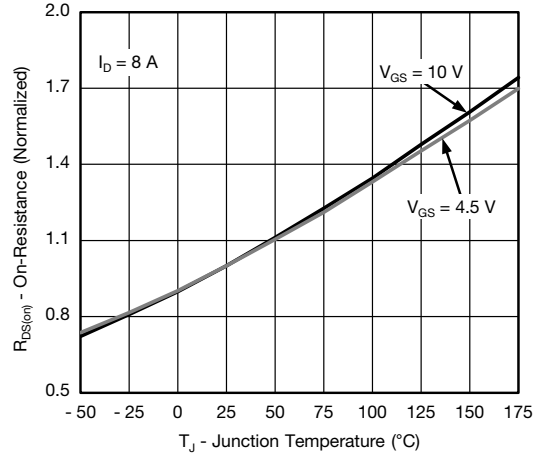


Capacitance

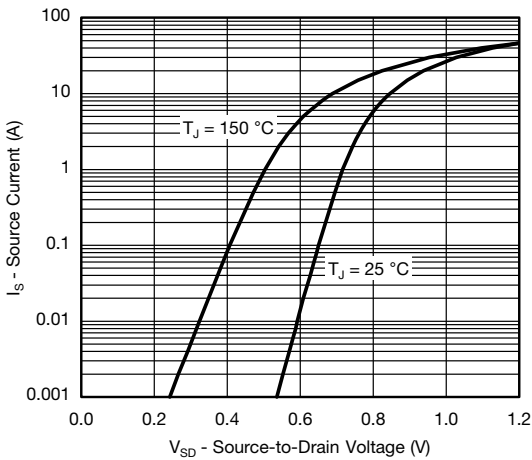
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



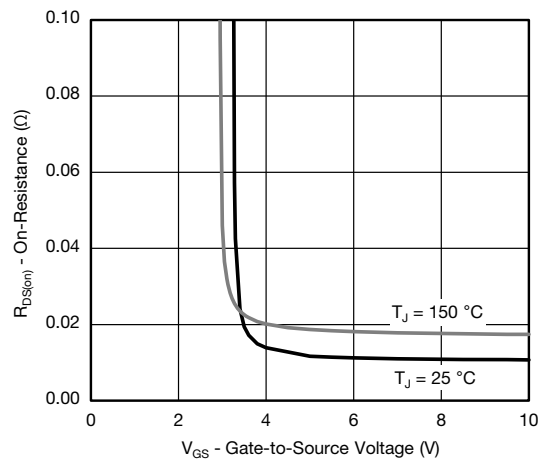
Gate Charge



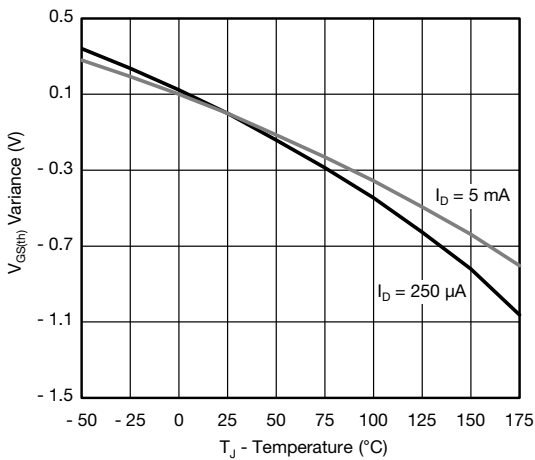
On-Resistance vs. Junction Temperature



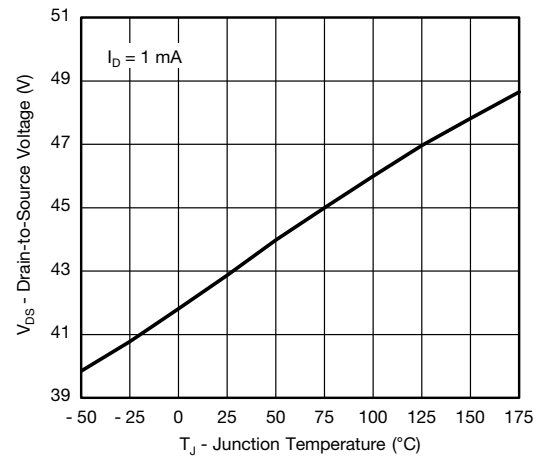
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

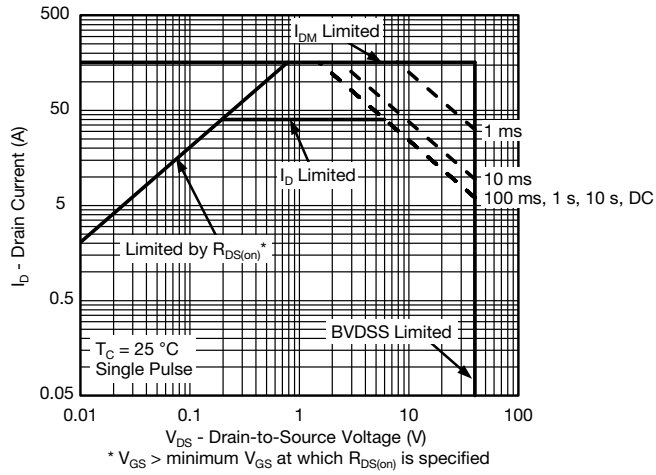


Threshold Voltage

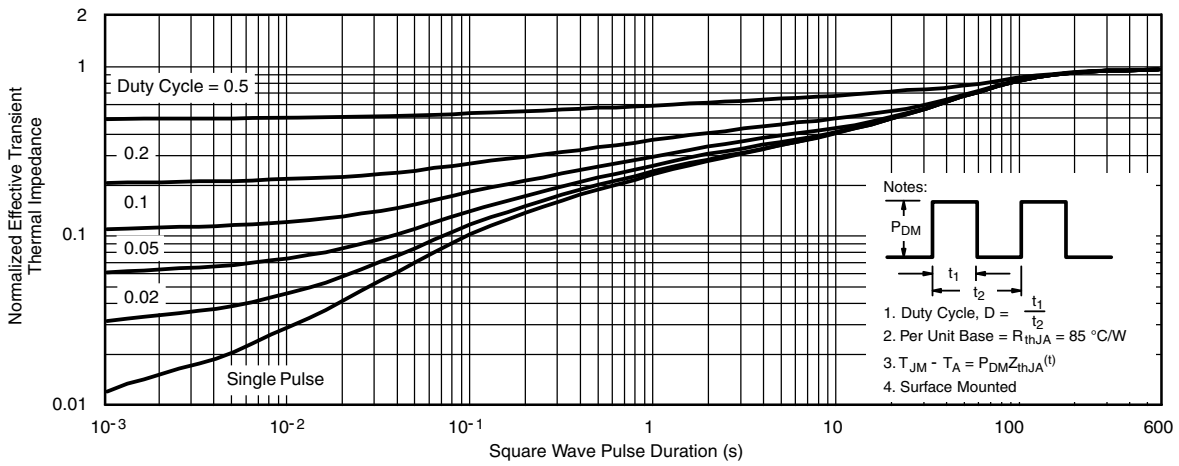


Drain Source Breakdown vs. Junction Temperature

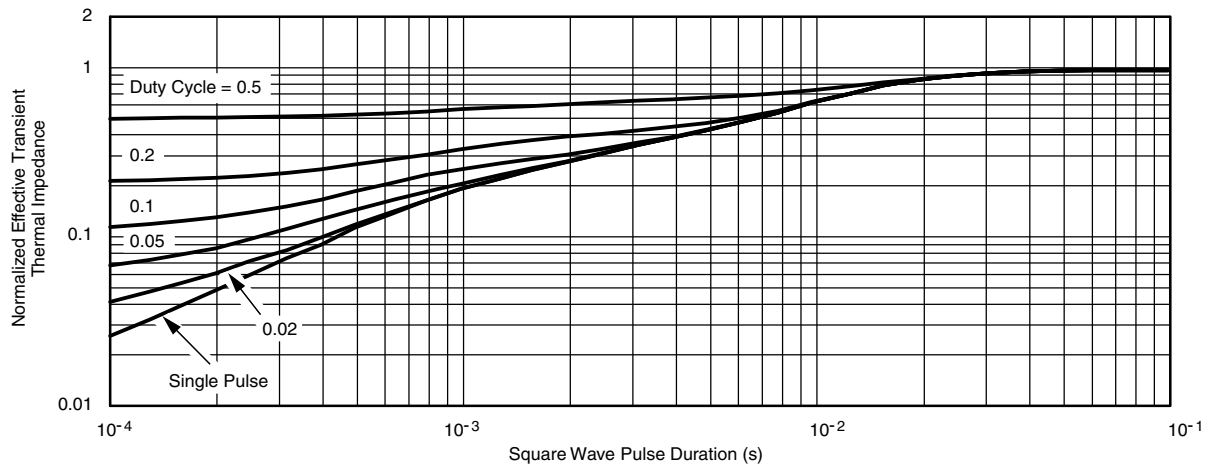
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Safe Operating Area

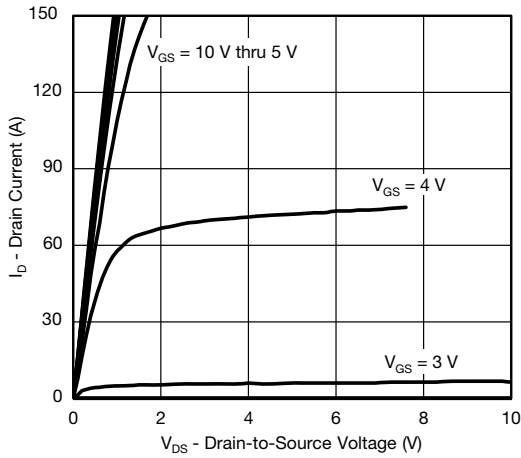


Normalized Thermal Transient Impedance, Junction-to-Ambient

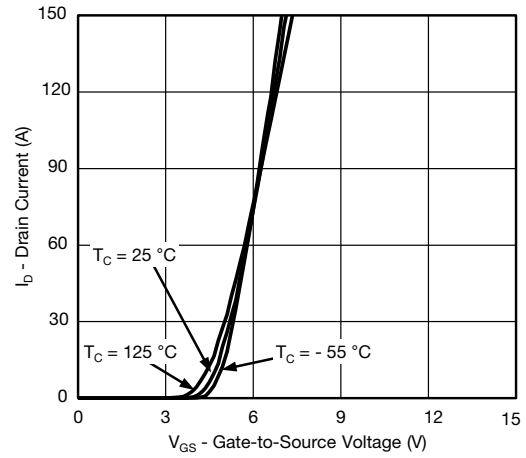
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Case
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^\circ\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^\circ\text{C}$)
 are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

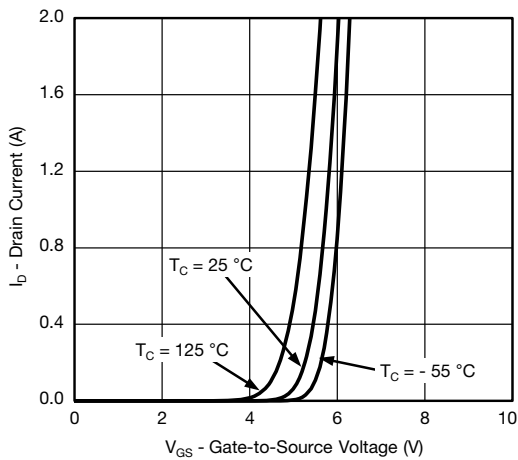
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



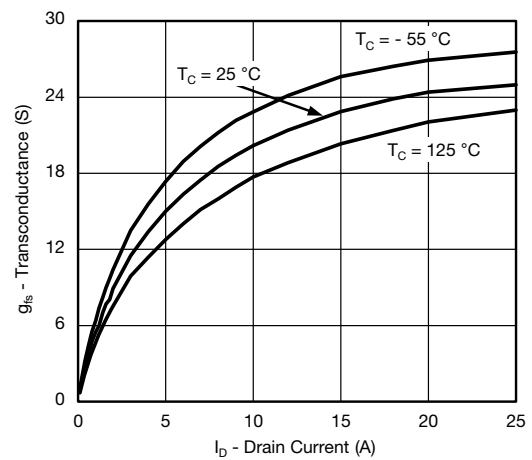
Output Characteristics



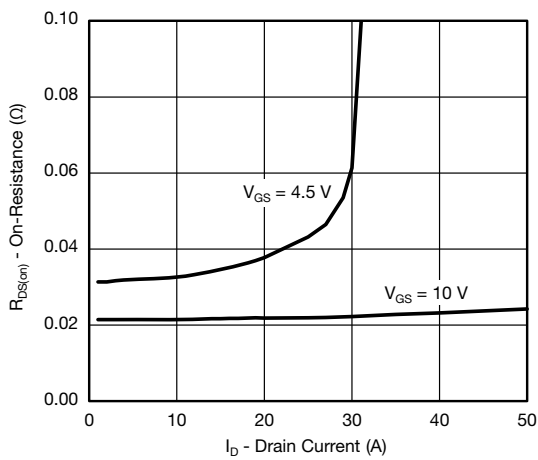
Transfer Characteristics



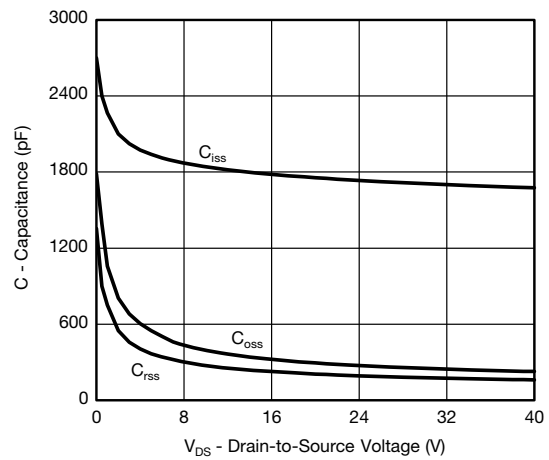
Transfer Characteristics



Transconductance

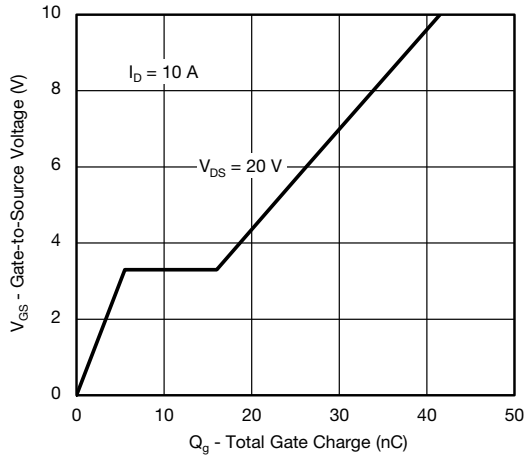


On-Resistance vs. Drain Current

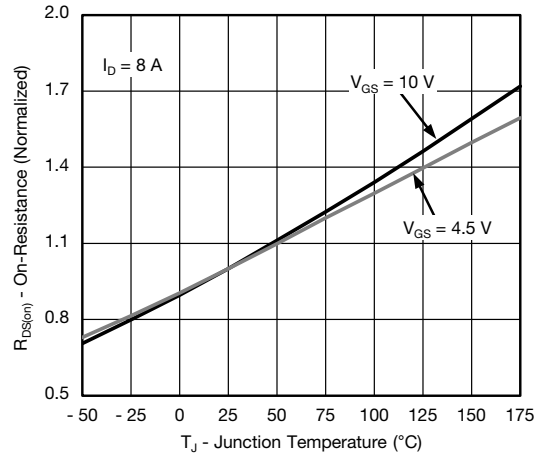


Capacitance

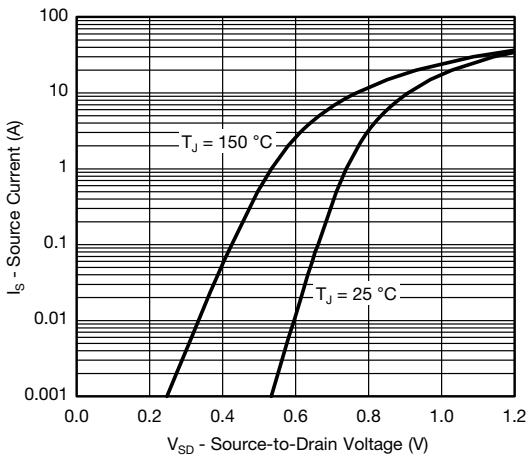
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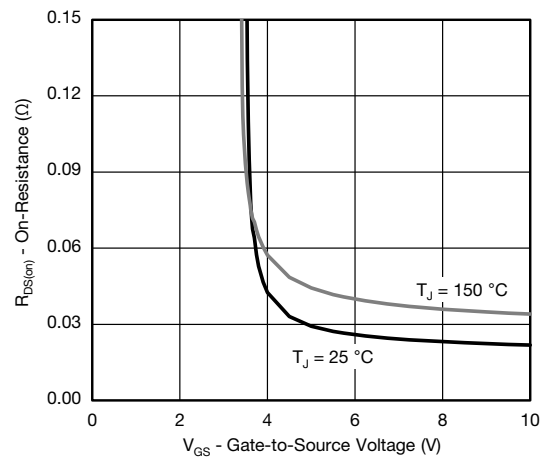
Gate Charge



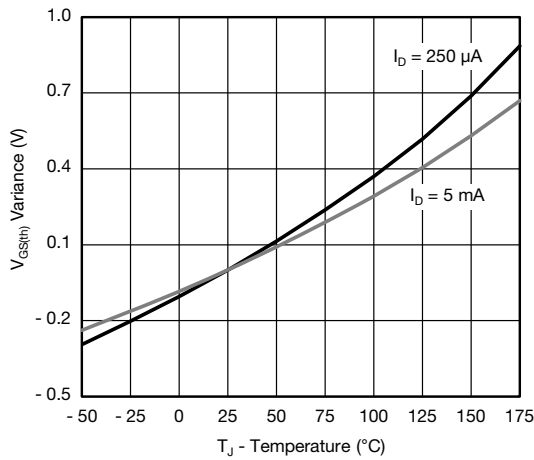
On-Resistance vs. Junction Temperature



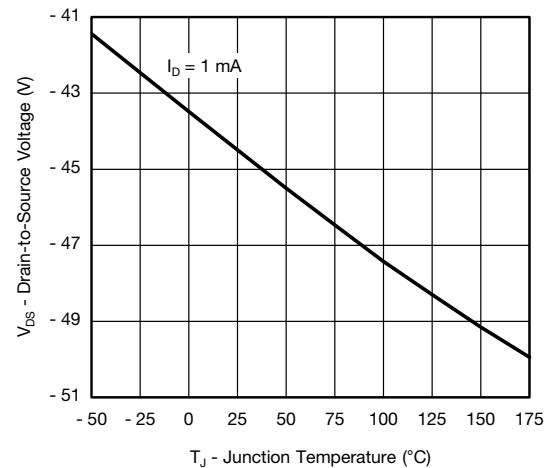
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

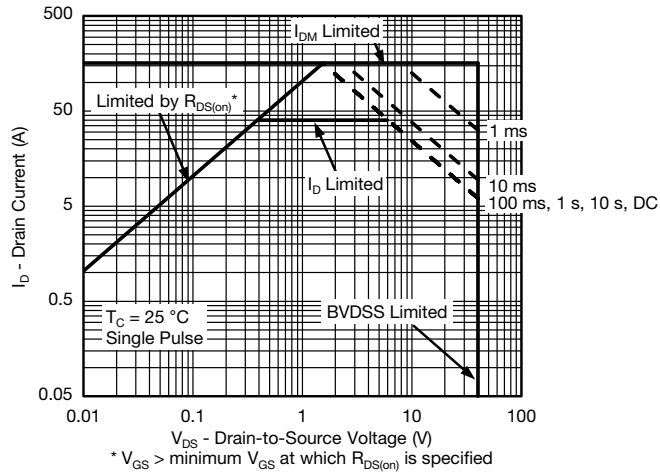


Threshold Voltage

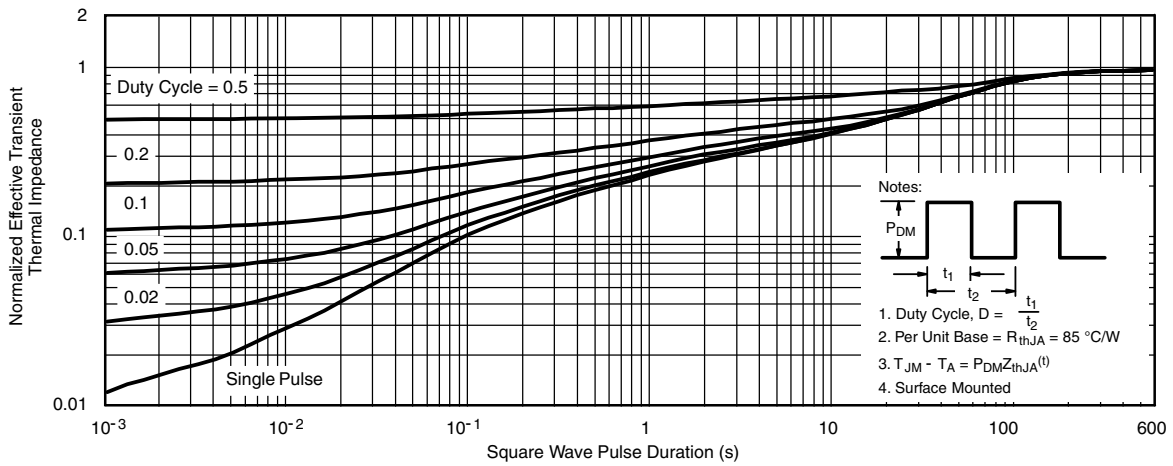


Drain Source Breakdown vs. Junction Temperature

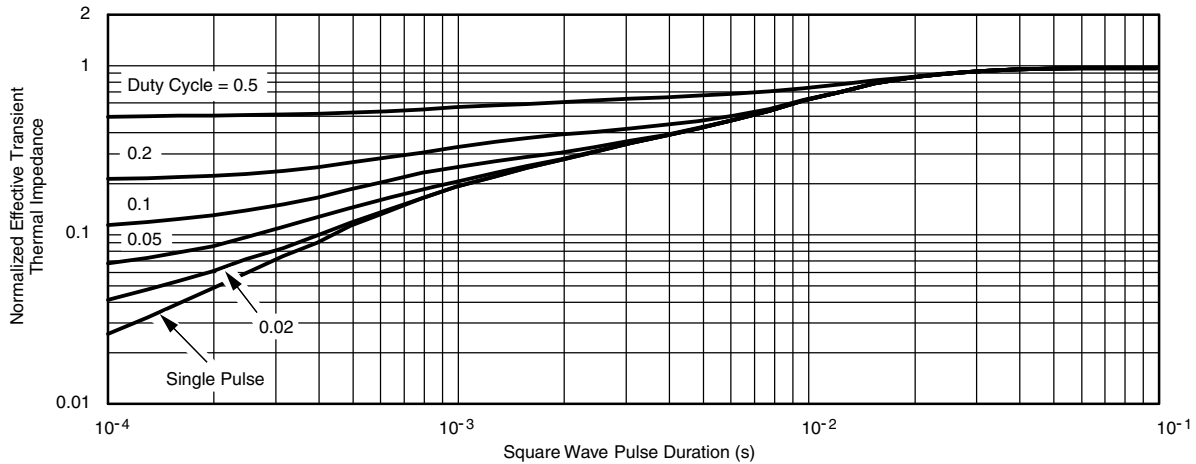
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Safe Operating Area

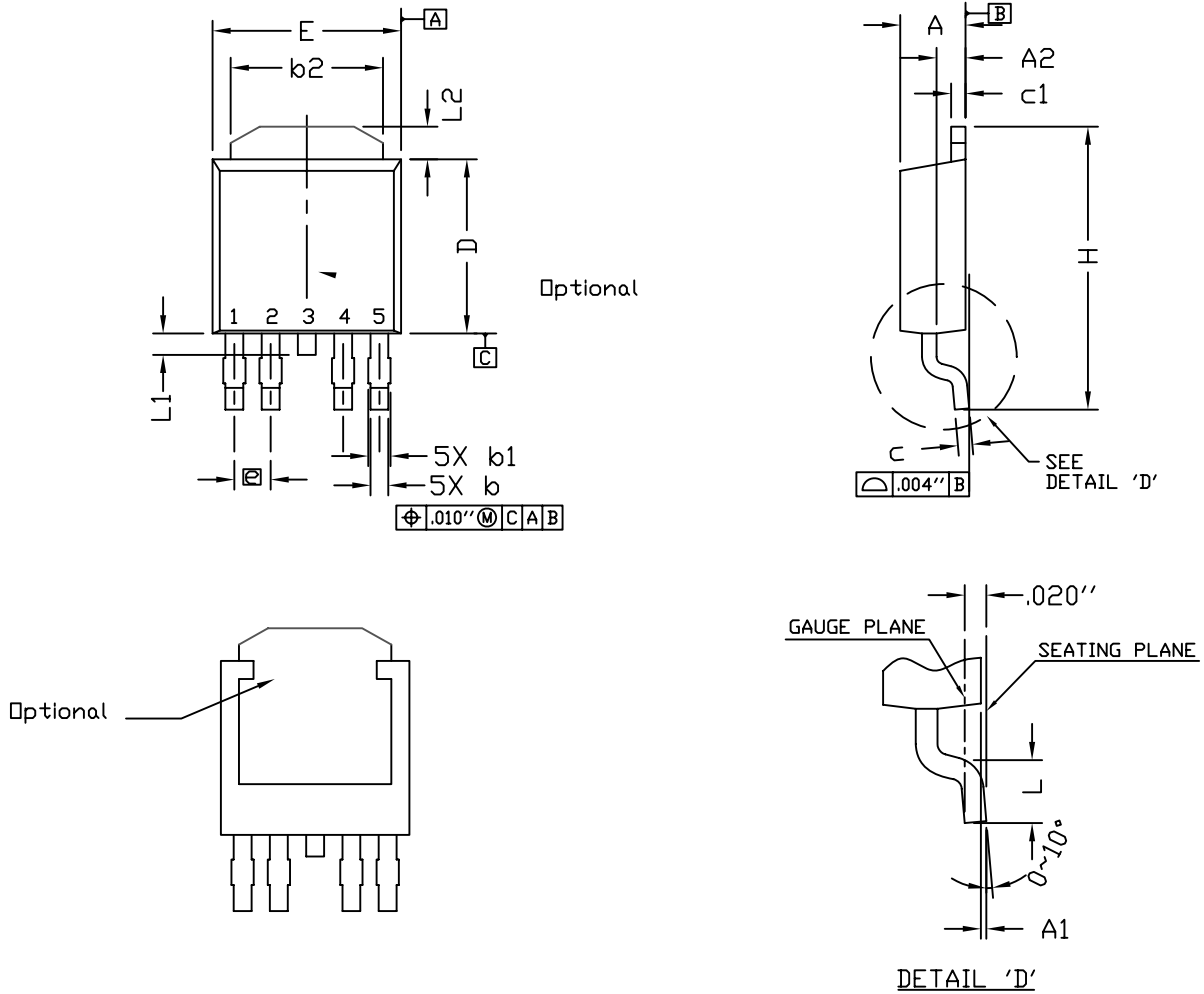


Normalized Thermal Transient Impedance, Junction-to-Ambient

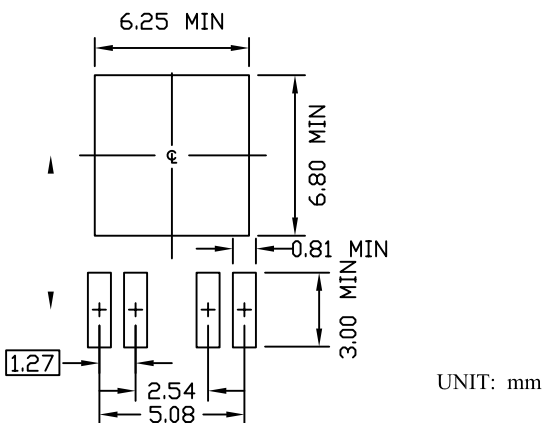
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Case
Note

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 are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

TO-252_4L Package Outline



RECOMMENDED LAND PATTERN



NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. DIMENSION L IS MEASURED IN GAUGE PLANE.
3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED.
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. REFER TO JEDEC TO-252 (AD).

SYMBOL	DIMENSION IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.184	2.286	2.388	0.086	0.090	0.094
A1	0.000	----	0.127	0.000	----	0.005
A2	0.889	----	1.143	0.035	----	0.045
b	0.508	----	0.711	0.020	----	0.028
b1	0.584	----	0.787	0.023	----	0.031
b2	4.953	----	5.461	0.195	----	0.215
c	0.457	0.508	0.610	0.018	0.020	0.024
c1	0.457	----	0.610	0.018	----	0.024
D	5.969	6.096	6.223	0.235	0.240	0.245
E	6.350	6.604	6.731	0.250	0.260	0.265
e	1.270 BSC.			0.050 BSC.		
H	9.398	----	10.414	0.370	----	0.410
L	1.270	----	2.032	0.050	----	0.080
L1	----	----	1.016	----	----	0.040
L2	0.889	----	1.270	0.035	----	0.050

Disclaimer

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