

DDL01

DDL Hex NOR Gate

Description

The DDL series of logic devices represents the first functionally complete logic family using silicon diodes as the sole active elements. The DDL01 Hex NOR contains six individual buffered DDL inverters with an input diode matrix configurable for six 2-input NOR gates, three positive-input SR latches, or a single negative-edge-triggered D flip-flop. Other logic functions are easily configured with pluggable jumper wires. The inputs are compatible with 3.3V and 5V TTL and CMOS logic families, and the outputs can directly drive LEDs or similar loads.

The DDL01 features a stackable design with integrated power distribution, and 25mil square header I/O pins allow for pluggable wiring using standard female jumpers. The generous pin-in and pin-out counts allow complex logic circuits to be constructed using only point-to-point wiring.

Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. Device may not function properly outside recommended operating conditions. Device lifetime may be affected by stresses exceeding recommended operating conditions.

Symbol	Parameter	Min	Max	Units
V_{RF} (note 1)	RF Supply Voltage	—	18	V_{P-P}
V_B	Bias Supply Voltage	-15	15	V
V_{IN}	Logic Input Voltage	-15	15	V

Notes: 1. Square wave. Different waveform of equivalent RMS allowed.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{RF}	RF Supply Voltage		12		V_{P-P}
V_B	Bias Supply Voltage		5		V
V_{IN}	Logic Input Voltage	-5		5	V
V_{IL}	Maximum LOW level input voltage			0	V
V_{IH}	Minimum HIGH level input voltage	1.5			V

Features

- Arbitrary logic functions using only diodes
- Unique logic technology
- Build-time configurable as:
 - Hex 2-input NOR gates
 - Triple positive-input SR latch
 - Single negative-edge-triggered D flip-flop
- NOR option easily jumpered for other functions
 - Triple 2-input OR gates
 - Dual 2-input AND gates
 - Single 2-input XOR gate
- Stackable design with power distribution
- Assemble complex designs with only female-female jumper wires
- Point-to-point wiring for most designs

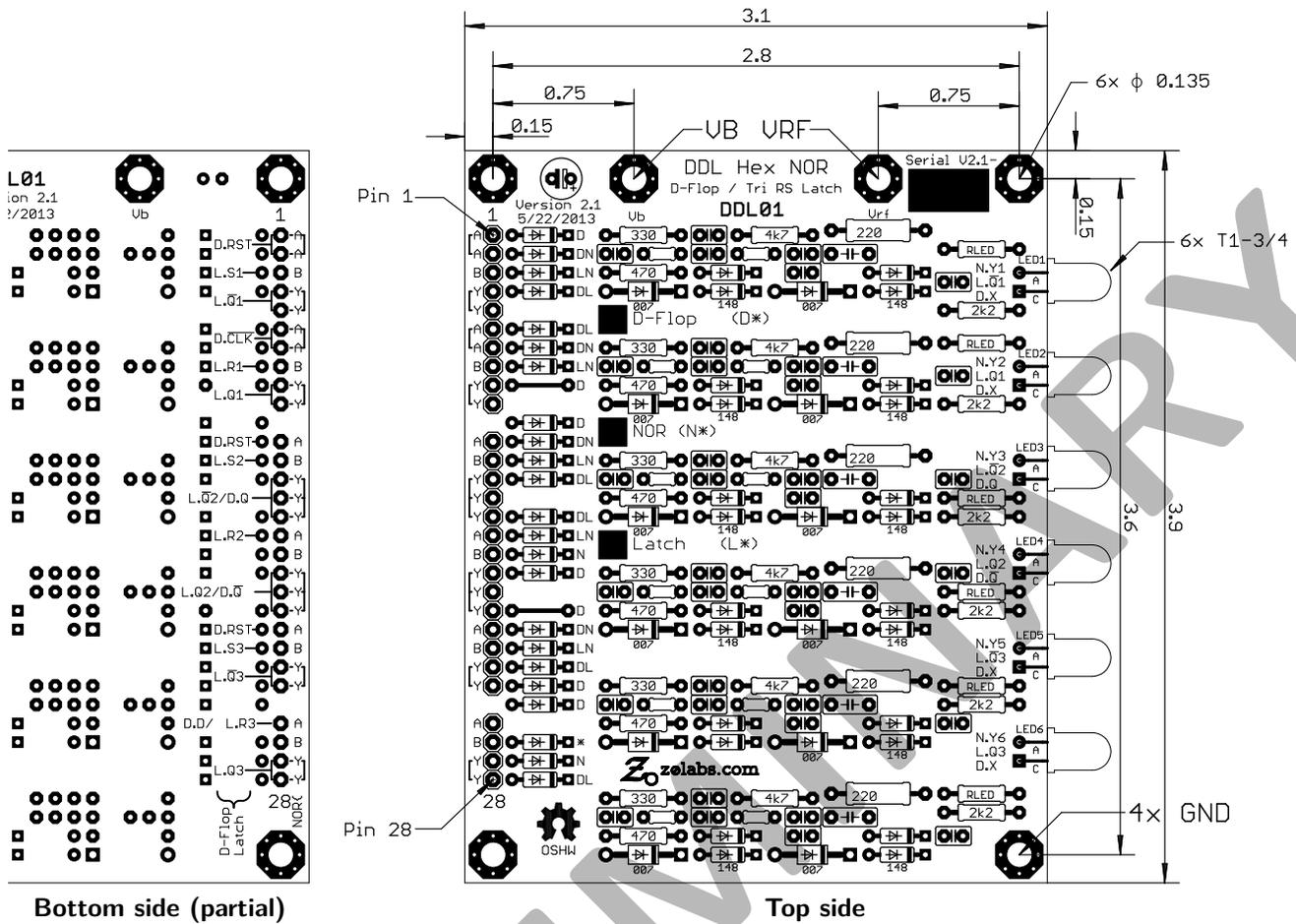


Figure 1: DDL01 Board dimensions and pin locations (1:1 scale on letter size paper)

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IL}	Maximum LOW level input voltage				0	V
V_{IH}	Minimum HIGH level input voltage		1.5			V
V_{OH}	HIGH level output voltage	output open		4.5		V
		1 DDL load		3		
		5 DDL loads		2		
V_{OL}	LOW level output voltage			0		V
I_{IL}	LOW level input current				-1	μ A
I_{IH} (note 2)	HIGH level input current				8	mA
I_{OS}	Short circuit output current			9.75		mA

Notes: 1. V_{RF} = 12Vp-p square wave at 4.5MHz; V_B = +5V
 2. Input voltage = 5V

Pin Description Table

Pin Number ^{1,2}	Direction	Signal Name	NOR Function ³	SR Latch Function ³	D-Flop Function ³
1	input	N.A1 / D.RST	A ₁	—	RST
2					
3	input	N.B1 / L.S1	B ₁	S ₁	—
4	output	N.Y1 / L.Q ₁	Y1	Q ₁	—
5					
6	input	N.A2/D.CLK	A ₂	—	CLK
7					
8	input	N.B2 / L.R1	B ₂	R ₁	—
9	output	N.Y2 / L.Q1	Y ₂	Q ₁	—
10					
11	input	N.A3 / D.RST	A ₃	—	RST
12	input	N.B3 / L.S2	B ₃	S ₂	—
13	output	N.Y3 / L.Q ₂ / D.Q	Y ₃	Q ₂	Q
14					
15					
16	input	N.A4 / L.R2	A ₄	R ₂	—
17	input	N.B4	B ₄	—	—
18	output	N.Y4 / L.Q2 / D.Q	Y ₄	Q ₂	Q
19					
20					
21	input	N.A5 / D.RST	A ₅	—	RST
22	input	N.B5 / L.S3	B ₅	S ₃	—
23	output	N.Y5 / L.Q ₃	Y ₅	Q ₃	—
24					
25	input	N.A6 / L.R3 / D.D	A ₆	R ₃	D
26	input	N.B6	B ₆	—	—
27	output	N.Y6 / L.Q3	Y ₆	Q ₃	—
28					

- Notes:
1. Inputs with multiple pins provided for “daisy-chaining” signals.
 2. Outputs with multiple pins provided for “fan-out” connections.
 3. D.RST appears on multiple pins; they may be used interchangeably.
 3. Input diodes and jumpers must be populated for specific function.

AC Electrical Characteristics

All Configurations^{1,2,4,5}

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V _{OH}	HIGH level output voltage	output open		4.5		V
		1 DDL load		3		
		5 DDL loads		2		
V _{OL}	LOW level output voltage	output open		0		V
		1 DDL load		0		
		5 DDL loads		0		

NOR Configuration^{1,2,3,4,5}

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t _{PLH}	Propagation time: output LOW-to-HIGH transition	output open		52		μs
		1 DDL load		45		
		5 DDL loads		39		
t _{PHL}	Propagation time: output HIGH-to-LOW transition	output open		54		μs
		1 DDL load		44		
		5 DDL loads		47		
t _r	Output rise time (10%, 90% points)	output open		54		μs
		1 DDL load		44		
		5 DDL loads		34		
t _f	Output fall time (90%, 10% points)	output open		96		μs
		1 DDL load		84		
		5 DDL loads		84		

Latch Configuration^{1,2,5}

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t _w	Input pulse width (minimum) for reliable latch	output open		106		μs
		1 DDL load		?		
		5 DDL loads		?		

D Flip-Flop Configuration^{1,2}

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f _{MAX}	Maximum clock frequency (÷2 circuit)	outputs open		3.3		kHz

- Notes:
1. V_{RF} = 12Vp-p square wave at 4.5MHz
 2. V_B = +5V
 3. Input waveform: 2kHz square wave, 2V amplitude
 4. Test circuit as shown in Figure 6

DDL Background

DDL gates implement standard logic functions using silicon diodes as active elements. In order to enable arbitrary logic functions, DDL gates must provide absolute gains greater than unity and a logical inversion function, both of which are absent from previous diode-based logic. To accomplish this, two different types of diode are used in DDL gates. Common switching diodes (1N4148 typ.) are used to implement traditional "diode-OR" functions at gate inputs. To achieve the required gain and inversion functions, PIN-type diodes are used to switch power from a radio-frequency (RF) supply, V_{RF} . The switched RF power is then rectified by a pair of switching diodes to produce a DC output signal. In the DDL01 device, common rectifier diodes (1N4007 typ.) are used as PIN diodes, achieving good performance at very low cost.

DDL Gate Design

A schematic diagram of a DDL NOR gate is shown in Figure 2. Each NOR gate is comprised of three major sections: a diode-OR input array, a buffer/pre-amp, and an inverting output driver. The two active-stage design of the DDL01 results in superior device gain and output drive, allowing much greater fan-out than single-stage designs.

Input Diode Array

The input section of a DDL gate comprises a diode-OR array with one switching diode per gate input (D1, D2 in Figure 2). A $470\ \Omega$ resistor (R1) is placed in series with the input diodes for current limiting. At signal frequencies (less than a few kHz, typical),

L1 can be treated as a short, and C1 and C2 as open circuits, so each input can be effectively modeled as a $470\ \Omega$ resistor in series with a 1N4148 and 1N4007 diode to ground. This equivalent model, shown in Figure 6, is used as a standard DDL load for testing. Additional diodes can be added to the input array of a DDL gate as required; the allowable fan-in is quite large, and the limit is not likely to be reached in practice.

Buffer Stage

The active element in the buffer stage is D3, a common rectifier diode used as a PIN diode RF switch. When all inputs to the gate are LOW, D3 acts as a relatively high impedance at RF, and RF current flows through R2, C1, and C2. A voltage doubler comprised of C2, D4 and D5 rectifies the RF into a negative DC output. The resulting negative voltage pulls the input to the driver stage negative, reverse biasing the driver PIN diode to ensure full turn-off. A relatively large negative bias is important to reduce junction capacitance in D6 and increase the off-state diode impedance.

In contrast, when one or more gate inputs are in the HIGH state, DC current flows through D3, causing it to assume a low impedance at RF. This low impedance shunts RF current away from the voltage doubler, so that the input of the driver stage is now biased positively from the bias supply, V_B , through R3.

Inverting Output Driver

D6 is the active element in the output driver stage. When D6 is reverse biased by the buffer-stage volt-

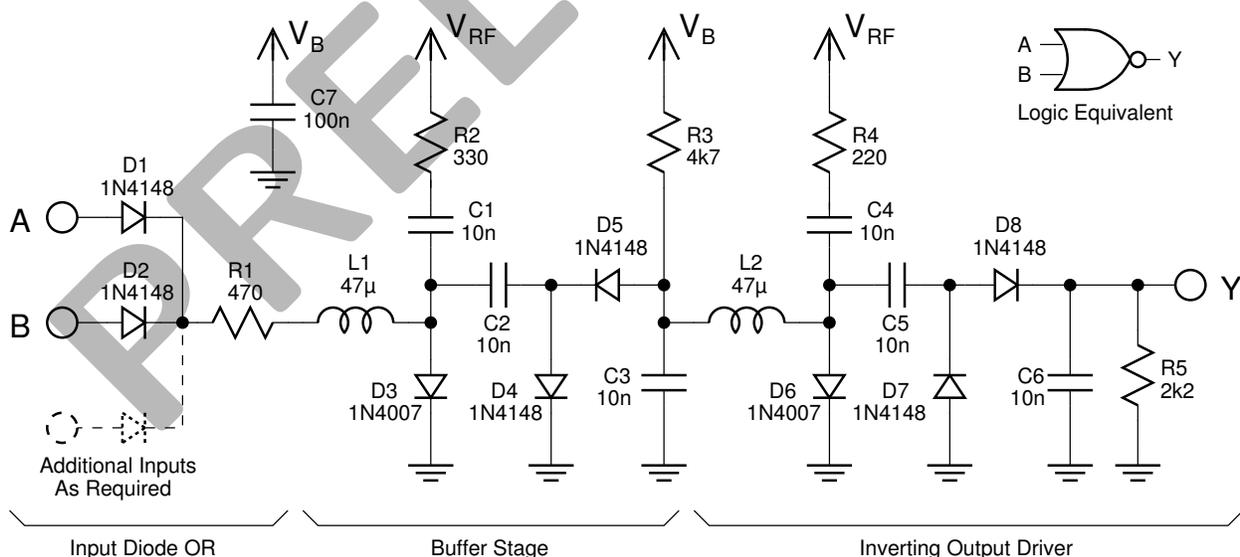


Figure 2: Buffered DDL NOR gate schematic (each gate)

age doubler (all gate inputs LOW), it presents a high impedance at RF. This allows RF current to flow through R4 and C4 to a second voltage doubler comprised of C5, D7, and D8. The positive voltage at the cathode of D8 is filtered by C6 to produce the NOR gate's HIGH output.

When D6 is forward biased through R3 (one or more gate inputs HIGH), it presents a low impedance at RF, and current through R4 and C4 is shunted to ground; the output voltage doubler delivers no current to C6. If the gate output was previously HIGH, R5 discharges C6 to a LOW state.

In cases where additional output current is required, the value of R4 can be decreased from its nominal value of 220 ohms. The main limitations are the allowable dissipation of R4 (LOW/HIGH output) and D6 (LOW output), and power supply limits.

Power Supplies

DDL gates require two power supplies: V_B , a DC bias supply, and V_{RF} , a radio-frequency supply. V_B is nominally +5V DC. As with any DC supply, V_B must be bypassed to reduce noise. The DDL01 provides 100nF of V_B bypass capacitance per gate, plus 10 μ F per device. This is sufficient for most designs; if additional (non-DDL) loads are also powered from the V_B supply, additional bypass capacitance may be necessary.

V_{RF} is a radio-frequency power supply, nominally a 12Vp-p square wave at 4.5MHz. Neither the V_{RF} frequency nor waveform is particularly critical; DDL devices work with frequencies roughly between 1MHz and 10MHz, and sine and square waveforms of similar RMS voltages work about equally well.

Particularly useful are spread-spectrum supplies. In large DDL systems, unintentional RF emissions may become an issue; using a spread-spectrum supply for V_{RF} can reduce emissions significantly.

Being an AC supply, V_{RF} cannot practically be bypassed. Theoretically, a fixed-frequency sine supply could be bypassed by an LC "tank" circuit tuned to the operating frequency, but this method doesn't work for square-wave or spread-spectrum supplies. The only solution is to use a low-impedance RF source as the supply for V_{RF} .

DDL devices may be "stacked" using standard #4-40 hardware. Stacked devices share V_B , V_{RF} and ground buses. More information on DDL Logic Stacks can be found in the Usage Information section.

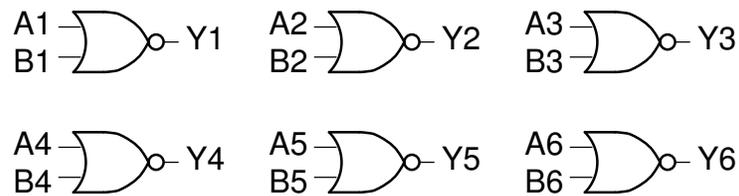
DDL02 Power Supply Device

The DDL02 RF power supply device is a standard DDL -sized board which provides a regulated DC bias supply (+5V DC), and a variable-voltage (8-15 Vp-p) RF supply based on an on-board square-wave oscillator, on-board spread-spectrum source, or external frequency input. Each DDL02 can power a stack of up to 20 DDL01 gate packages.

Applications

The NOR gate, like the NAND, is universal: it can be used to construct any arbitrary logic function. Therefore, the DDL01 Hex NOR devices can be used to construct any combinational or sequential logic circuit. Additional figures illustrate how the DDL01 can be used to construct a triple 2-input OR, a dual 2-input AND, and a single XOR gate. Four DDL01's can be used to construct a decoded modulo-6 Johnson counter.

Figure 3: Hex 2-Input NOR Configuration

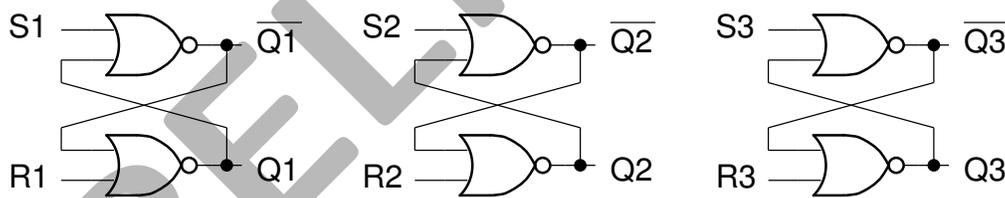


**Truth Table
(Each Gate)**

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH Level
L = LOW Level

Figure 4: Triple SR-Latch Configuration



**Truth Table
(Each Latch)**

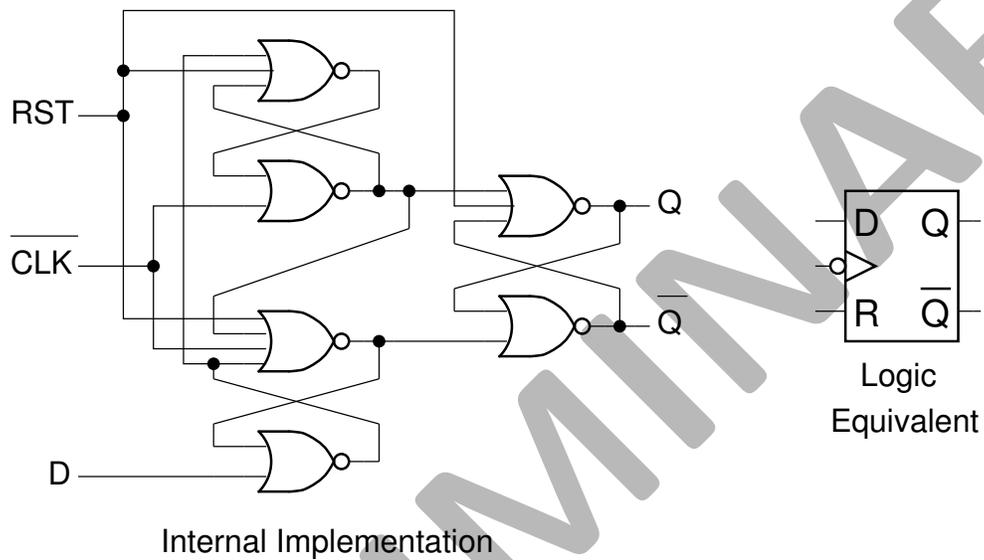
Inputs		Outputs	
S	R	Q	Q̄
H	L	H	L
L	H	L	H
L	L	Q ₀	Q̄ ₀
H	H	L*	L*

H = HIGH Level
L = LOW Level

Q₀, Q̄₀ = Stored state. The level of Q and Q̄, respectively, before specified input conditions are met.

L* = Unstable LOW level. Output is unspecified when both inputs return to LOW level.

Figure 5: Single Negative-Edge-Triggered D Flip-Flop Configuration



Truth Table
D Flip-Flop Configuration

Inputs		Outputs		
RST	CLK	D	Q	\bar{Q}
H	X	X	L	H
L	\neg	L	L	H
L	\neg	H	H	L
L	L	X	Q_0	\bar{Q}_0
L	H	X	Q_0	\bar{Q}_0

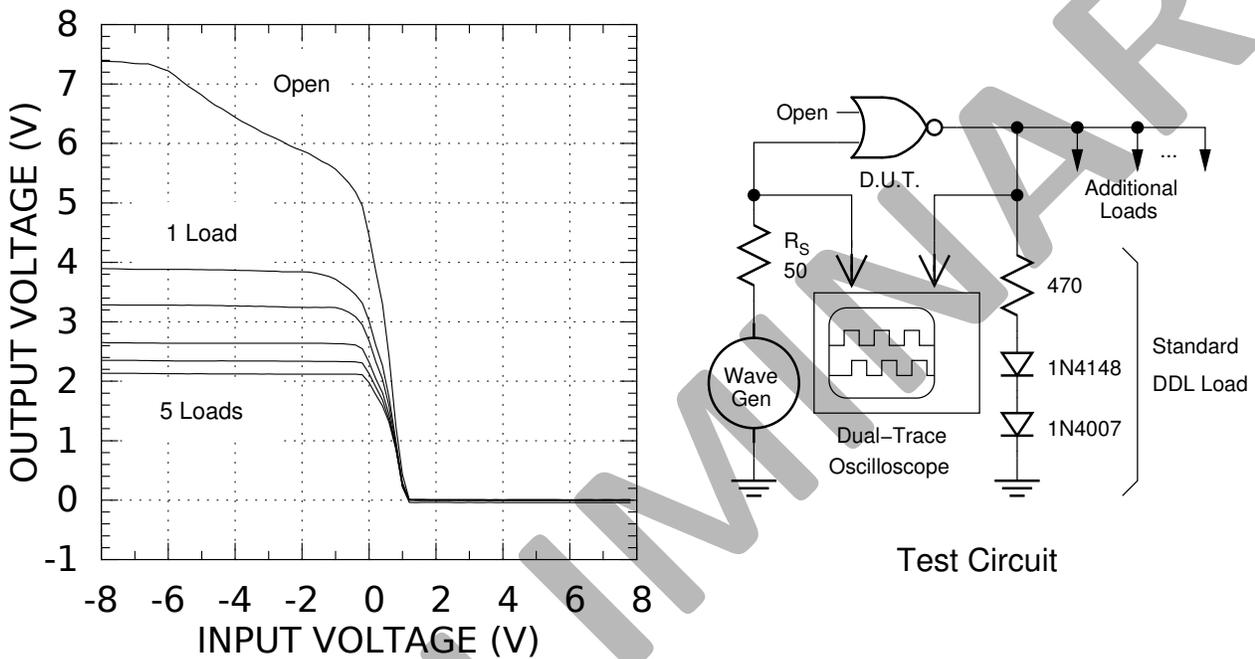
H = HIGH Level

L = LOW Level

X = Don't care

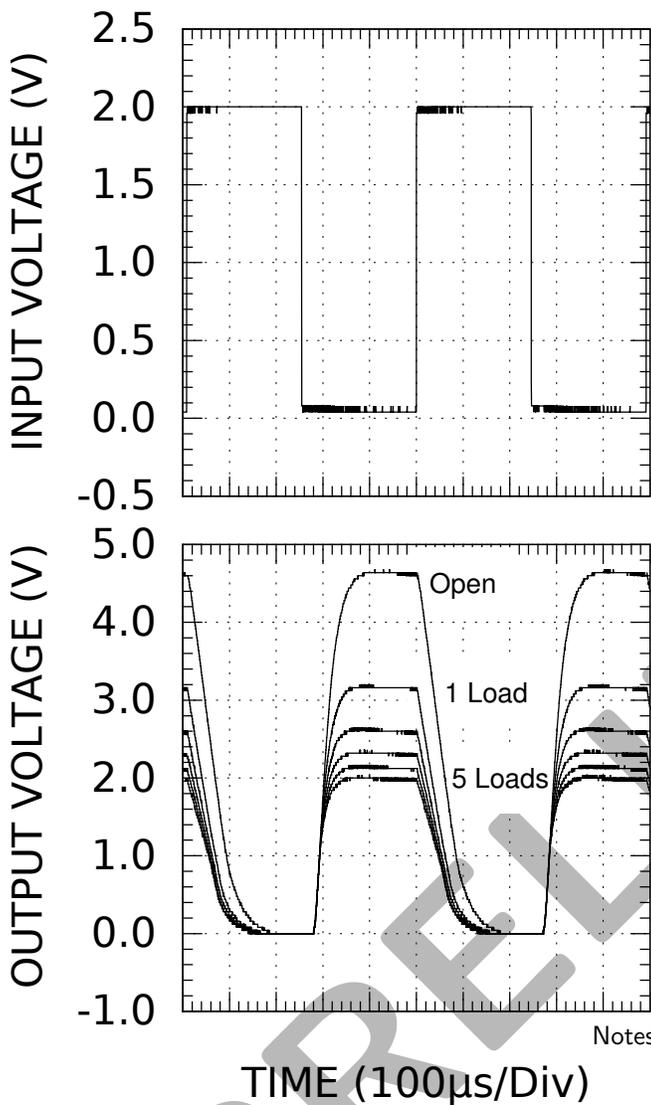
\neg = HIGH-to-LOW clock transition.

Q_0, \bar{Q}_0 = Stored state. The level of D and \bar{D} , respectively, before the last HIGH-to-LOW clock transition.



- Notes:
1. $V_{RF} = 12V_{p-p}$ square wave at 4.5MHz
 2. $V_B = +5V$
 3. Oscilloscope in X-Y mode
 4. Test circuit as shown
 5. Signals averaged from 128 samples

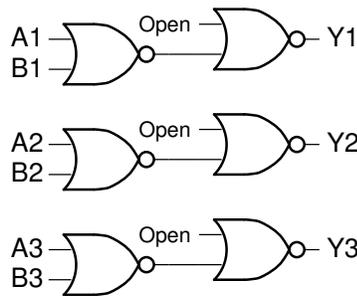
Figure 6: Typical DDL Gate Transfer Function for Various Fan-out



- Notes:
1. V_{RF} = 12Vp-p square wave at 4.5MHz
 2. V_B = +5V
 3. Input waveform: 2kHz square wave, 2V amplitude
 4. Test circuit as shown in Figure 6
 5. Signals averaged from 128 samples

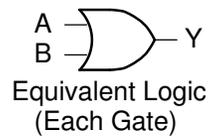
Figure 7: DLL Gate Transient Response for Various Fan-outs

DDL01 Wired as Triple 2-Input OR Gates



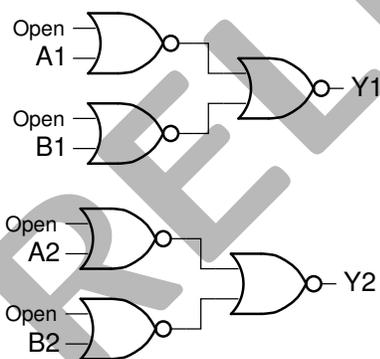
**Truth Table
(Each Gate)**

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H



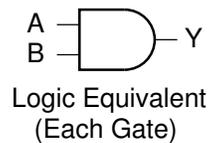
Note: Gates wired with external jumpers

DDL01 Wired as Dual 2-Input AND Gates



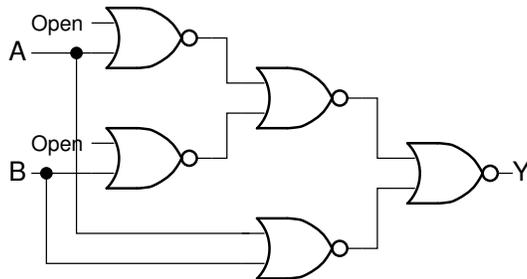
**Truth Table
(Each Gate)**

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H



Note: Gates wired with external jumpers

(5/6) DDL01 Wired as Single 2-Input XOR Gate



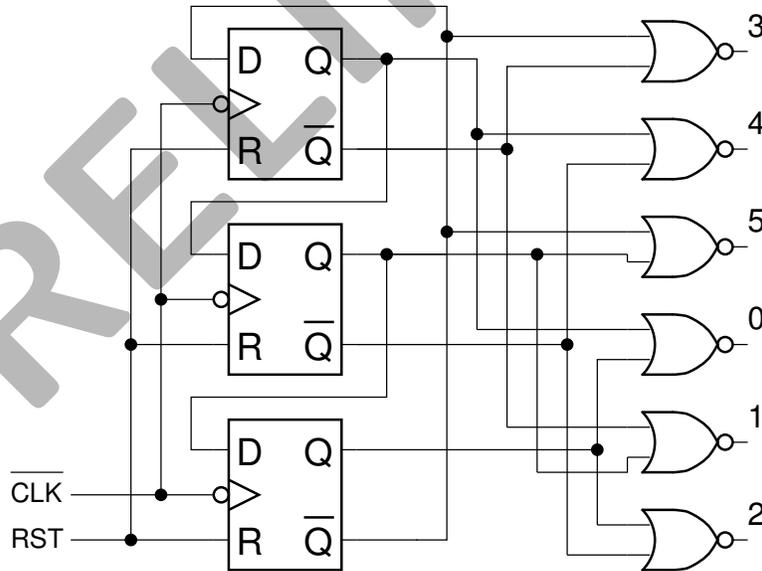
Truth Table (Each Gate)

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L



- Notes:
1. Gates wired with external jumpers
 2. Remaining NOR gate on DDL01 available

Decoded Modulo-6 Johnson Counter Built with (4) DDL01's



Note: Gates wired with external jumpers