M5M27404AK-10,-12,-15

4194304-BIT(524288-WORD BY 8-BIT/262144-WORD BY 16-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M27404AK is a high-speed 4194304-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5M27404AK is fabricated by N-channel double polysilicon gate for Memory and CMOS technology for peripheral circuits, and is available in a 40-pin DIP with a transparent lid.

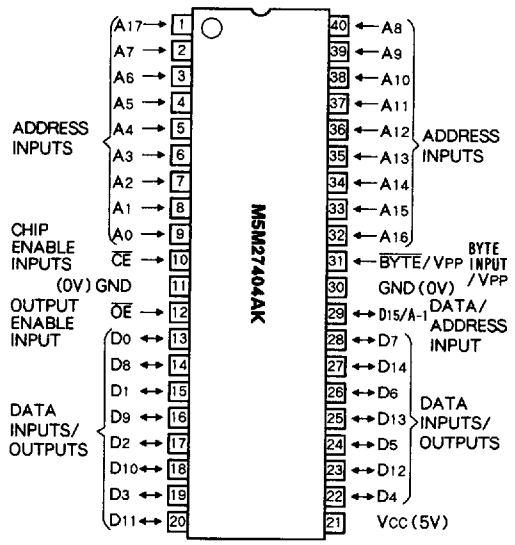
FEATURES

- 524288-word × 8-bit/262144-word × 16-bit organization
- Access time M5M27404AK-10 ..... 100ns (max.)
  M5M27404AK-12 ..... 120ns (max.)
  M5M27404AK-15 ..... 150ns (max.)
- Page access time
  M5M27404AK-10 ..... 50ns (max.)
  M5M27404AK-12 ..... 60ns (max.)
  M5M27404AK-15 ..... 60ns (max.)
- Single 5V power supply (read operation)
- Programming voltage 12.75V
- Input and output TTL-compatible in read and program mode
- Standard 40-pin DIP
- Word programming algorithm

APPLICATION

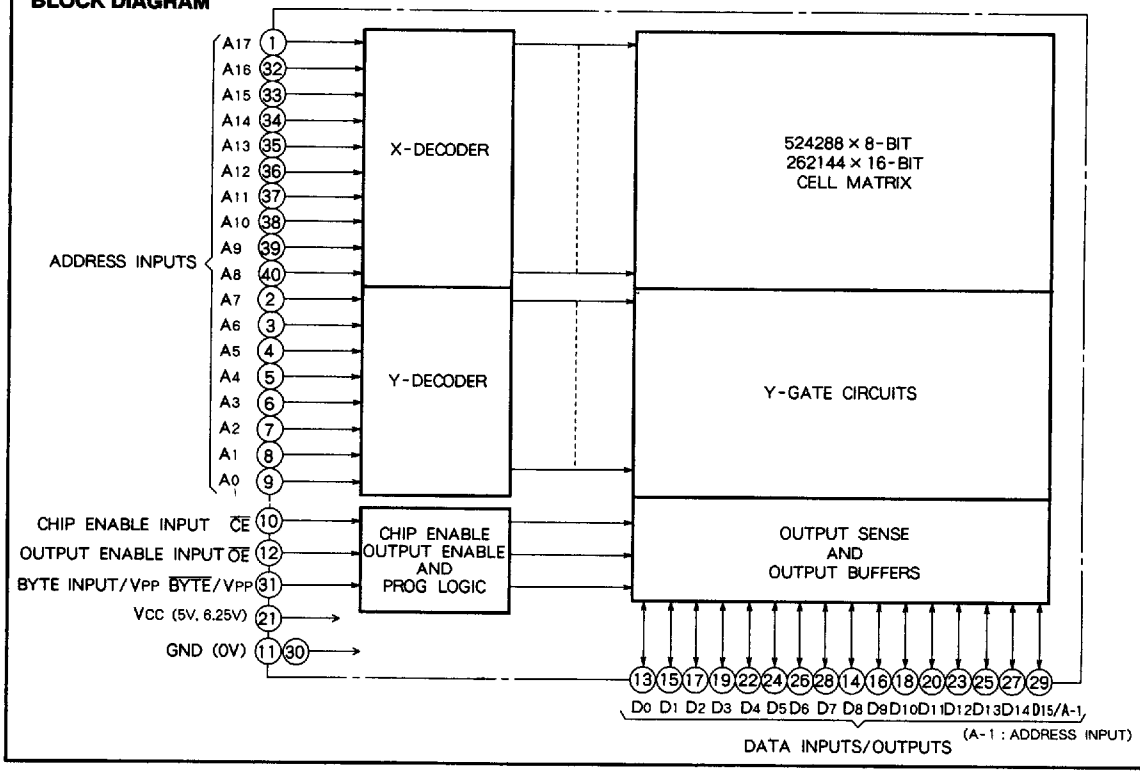
Microcomputer systems and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 40K4

BLOCK DIAGRAM



4194304-BIT(524288-WORD BY 8-BIT/262144-WORD BY 16-BIT)
CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

FUNCTION

Read

Read mode is initiated by $\overline{CE}$ and $\overline{OE}$ low. High level input to $\overline{BYTE}$ and address signals to the address inputs (A_0~A_{17}) make the data contents of the designated address location available at the data outputs (D_0~D_{15}).

When the $\overline{BYTE}$ signal is low, address inputs are A_{-1}, A_0 ~A_{17} and data outputs are D_0~D_7.

Page read mode allows two to eight bytes or four words of data to be read fast in the same page ; $\overline{CE}$ and A_2~A_{17} must not change.

When the $\overline{CE}$ ro $\overline{OE}$ signal is high, data outputs are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the stand by mode or power-down mode.

Programming

(Word programming algorithm)

The M5M27404AK enters the word programming mode when 12.75V is supplied to the $\overline{BYTE}$/V_{PP} power supply input and $\overline{OE}$ is at high level. A location is designated by address signals (A_0~A_{17}), and the data to be programmed must be applied at 16-bits in parallel to the data inputs (D_0~D_{15}). In this state, word programming is complated when $\overline{CE}$ is at low levle.

Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537 Å at an intensity of approximately 15WS /cm². Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

MODE SELECTION

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$/V_{PP}	V_{CC}	Data I/O D_0~$_7$	Data I/O D_8~$_{14}$	Data I/O D_{15}/A_{-1}
Read (Word mode)	V_{IL}	V_{IL}	V_{IH}	5V	Data out	Data out	Data out
Read (Byte mode)	V_{IL}	V_{IL}	V_{IL}	5V	Data out	Floating	A_{-1} input
Output disable	V_{IL}	V_{IH}	X *	5V	Floating	Floating	Floating
Standby (Power down)	V_{IH}	X*	X *	5V	Floating	Floating	Floating
Programming	V_{IL}	V_{IH}	12.75V	6.25V	Data in	Data in	Data in
Program verify	V_{IH}	V_{IL}	12.75V	6.25V	Data out	Data out	Data out
Program inhibit	V_{IH}	V_{IH}	12.75V	6.25V	Floating	Floating	Floating

* : X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Conditions	Ratings	Unit
V_{I1}	All input or output voltage except $\overline{BYTE}$/V_{PP}・A_9	With respect to Ground	− 0.6~7	V
V_{I2}	$\overline{BYTE}$/V_{PP} supply voltage		− 0.6~14.0	V
V_{I3}	A_9 supply voltage		− 0.6~13.5	V
T_{opr}	Operating tempersture		− 10~80	℃
T_{stg}	Storage temperature		− 65~125	℃

Note 1 : Stresses above those listed may cause parmanent damage to the device. This is a stress rating only and functional operation of the device at those or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

READ OPERATION

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 0~Vcc			10	μA
I_{LO}	Output leakage current	V_{OUT} = 0~Vcc			10	μA
I_{PP1}	Vpp current read/stand-by	Vpp = Vcc = 5.5V		1	100	μA
I_{SB1}	Vcc current stand-by	$\overline{CE}$ = V_{IH}			1	mA
I_{SB2}		$\overline{CE}$ = Vcc		1	100	μA
I_{CC1}	Vcc current active	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, DC, I_{OUT} = 0mA			50	mA
I_{CC2}		$\overline{CE}$ = V_{IL}, f = 10MHz, I_{OUT} = 0mA			120	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.2		Vcc+1	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH} = −400 μA	2.4			V

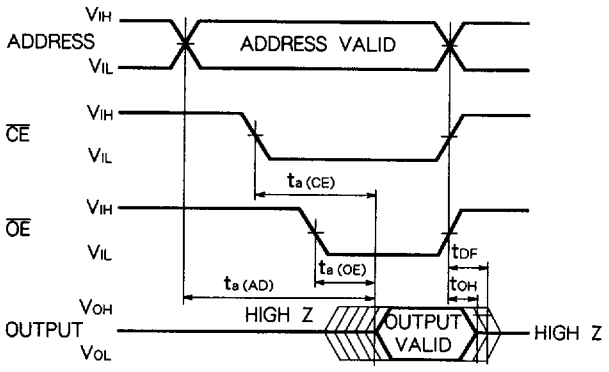
Note 2: Typical values are at Ta = 25℃ and nominal supply voltages.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits						Unit
			M5M27404AK-10		M5M27404AK-12		M5M27404AK-15		
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{a(AD)}$	Address to output delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		100		120		150	ns
$t_{a(CE)}$	$\overline{CE}$ to output delay	$\overline{OE}$ = V_{IL}		100		120		150	ns
$t_{a(OE)}$	$\overline{OE}$ to output delay	$\overline{CE}$ = V_{IL}		50		60		60	ns
t_{DF}	$\overline{OE}$ high to output float	$\overline{CE}$ = V_{IL}	0	45	0	50	0	50	ns
t_{OH}	Output hold from $\overline{CE}$, $\overline{OE}$ or address		0		0		0		ns
$t_{a(PA)}$	Page address access time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		50		60		60	ns

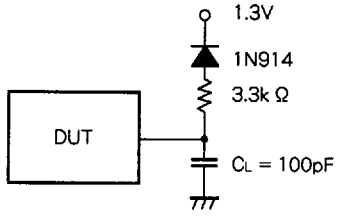
Note 3: PA: Page address (A-1, A0, A1 or A0, A1)

AC WAVEFORMS (Nomal mode)



Test conditions for A.C. characteristics
Input voltage : V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times : ≦ 10ns
Reference voltage at timing measurement : 1.5V

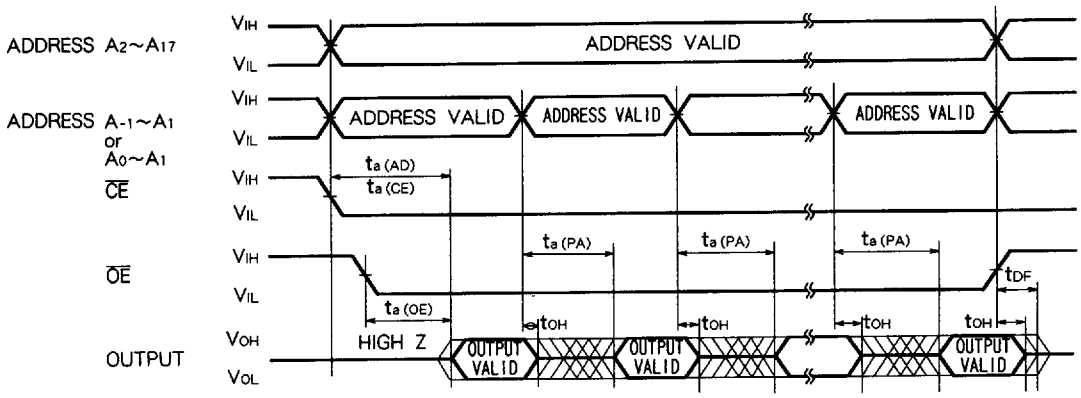
Output load : 1 TTL gate + C_L (= 100pF)
or



CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
C_{IN}	Input capacitance (Address, $\overline{CE}$, $\overline{OE}$)	Ta = 25℃, f = 1MHz, V_I = V_O = 0V			15	pF
C_{OUT}	Output capacitance				15	pF

AC WAVEFORMS (Page read mode)



Test conditions for A.C. characteristics

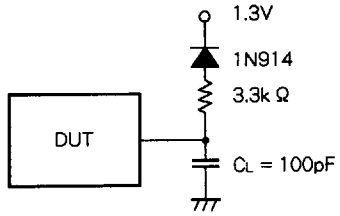
Input voltage : V_{IL} = 0.45V, V_{IH} = 2.4V

Input rise and fall times : ≦ 10ns

Reference voltage at timing measurement : 1.5V

Output load : 1 TTL gate + C_L (= 100pF)

or



PROGRAM OPERATION

First set V_{CC} = 6.25V, $\overline{BYTE}/V_{PP}$ = 12.75V and then set an address to first address to be programmed. After applying 0.1ms program pulse ($\overline{CE}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 0.1ms program pulse. The programmer continues 0.1ms pulse-then-verify routines until the device verify correctly or twenty five of these pulse-then-verify routines have been completed. When the programming procedure adove is finished, step to the next address and repeat this procedure till last address to be programmed. When the entire addresses have been programmed completely, all addresses should be verified with V_{CC} = $\overline{BYTE}/V_{PP}$ = 5V.

DC ELECTRICAL CHARACTERISTICS (T_a=25±5℃, V_{CC}=6.25V±0.25V, $\overline{BYTE}/V_{PP}$=12.75V±0.25V, unless otherwise noted)

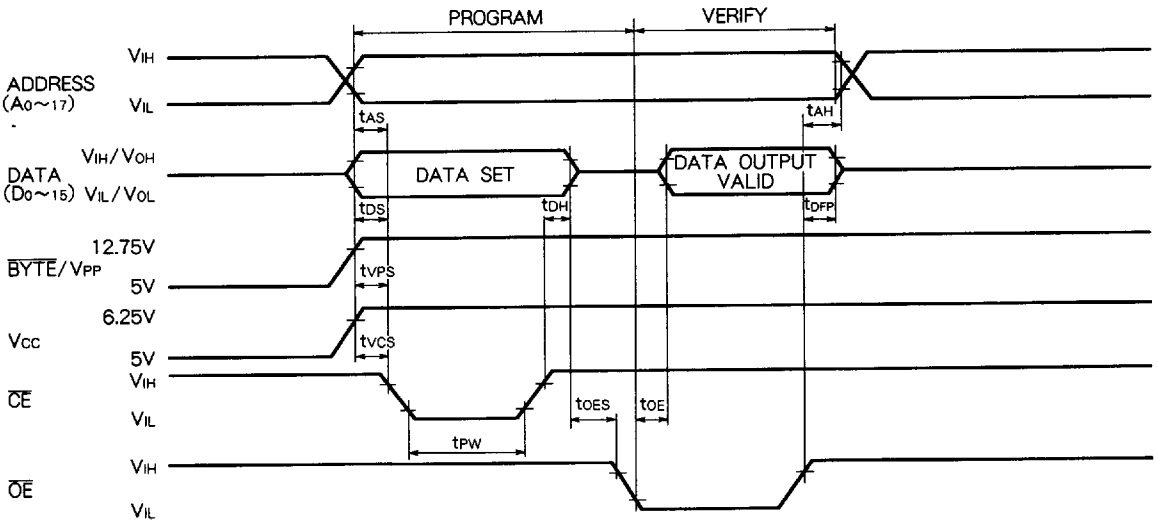
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 0~V_{CC}			10	μA
V_{OL}	Output low voltage (verify)	I_{OL} = 2.1mA			0.45	V
V_{OH}	Output high voltage (verify)	I_{OH} = −400 μA	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.2		V_{CC}	V
I_{CC}	V_{CC} supply current				50	mA
I_{PP}	V_{PP} supply current	$\overline{CE}$ = V_{IL}			50	mA

AC ELECTRICAL CHARACTERISTICS (T_a=25±5℃, V_{CC}=6.25V±0.25V, $\overline{BYTE}/V_{PP}$=12.75V±0.25V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ setup time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Chip enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	$\overline{BYTE}/V_{PP}$ setup time		2			μs
t_{PW}	$\overline{CE}$ initial program pulse width		95	100	105	μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

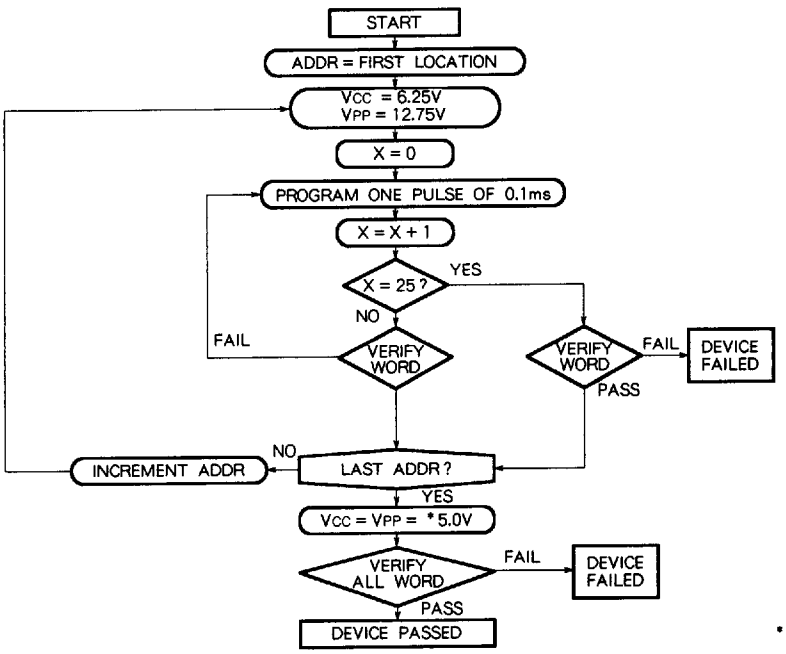
Note 4 : Vcc must be applied simultaneously $\overline{BYTE}/V_{PP}$ and removed simultaneously $\overline{BYTE}/V_{PP}$.

AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage : V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times : ≦ 20ns
Reference voltage at timing measurement : Input, Output
"L" = 0.8V, "H" = 2V.

PROGRAMMING ALGORITHM FLOW CHART



* 4.5V ≦ Vcc = VPP ≦ 5.5V

DEVICE IDENTIFIER MODE

The Device Identifier Mode allows the reading of a binary code from the EPROM that identifier the manufacturer and device type.

The EPROM Programmer reads the manufacturer code and the device code and automatically selects the corresponding programming algorithm.

M5M27404AK DEVICE IDENTIFIER CODE

Code \ Pin	A_0	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hex Data
Manufacturer code	V_{IL}	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	001C
Device code	V_{IH}	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0091

Note 5 : A_9 = 12.0V ± 0.5V
A_1~A_8, A_{10}~A_{17}, $\overline{CE}$, $\overline{OE}$ = V_{IL}, $\overline{BYTE}/V_{PP}$ = V_{IH}
V_{CC} = 5V ± 10%