FUJITSU
MICROELECTRONICS

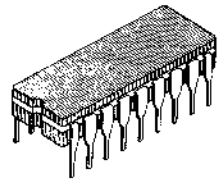
MBM2148-55L
MBM2148-70L

MOS 4096-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MBM2148L is a 1024 word by 4 bit static random access memory with automatic power down. It is fabricated using N-channel silicon gate MOS technology. The memory is fully static and requires no clock or timing strobe. All pins are TTL compatible and a single 5V power supply is required.

A separate chip select ($\overline{CS}$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied, and furthermore on selecting a single package by $\overline{CS}$ the other deselected packages automatically power down. Fujitsu's MBM2148L offers the advantages of low power dissipation, low cost and high performance.

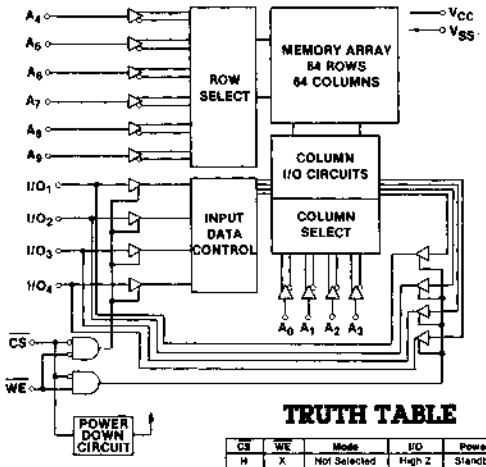


CERDIP PACKAGE
DIP-18C-C01

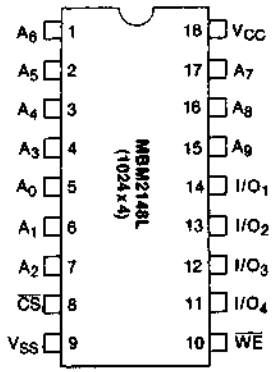
FEATURES

- **Organization: 1024 words x 4 bits**
- **Static operation; no clock or timing strobe required**
- **Fast access time:**
  MBM2148-55L: 55 ns max.
  MBM2148-70L: 70 ns max.
- **Low power consumption:**
  I_{CC} = 125mA max.
  I_{SB} = 20mA max.
- **Single +5V DC supply voltage (±10% tolerance)**
- **Common data input/output**
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Chip select for simplified memory expansion, automatic power down**
- **Standard 18-pin DIP package**
- **Pin compatible with Intel 2148**

MBM2148 BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	I/O	Power
H	X	Not Selected	High Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage On Any Pin with respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−3.5 to +7	V
Short Circuit Output Current	—	20	mA
Temperature Under Bias	T_A	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.2	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE[1]

(T_A = 25°C; f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Address/Control Capacitance (V_{IN} = 0V)	C_{IN}	—	5	pF
Input/Output Capacitance (V_{OUT} = 0V)	$C_{I/O}$	—	7	pF

NOTE: 1) This parameter is sampled and not 100% tested.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient[1] Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	V_{IL}	−3.0	—	0.8	V	
Input High Voltage	V_{IH}	2.1	—	6.0	V	

NOTE: 1. The operating ambient temperature range is guaranteed with transverse airflow exceeding 400 linear feet per minute.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC}, V_{CC} = Max)	I_{LI}	−10	10	μA
Output Leakage Current ($\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to 4.5V, V_{CC} = Max)	I_{LO}	−50	50	μA
Power Supply Current (V_{CC} = Max, $\overline{CS}$ = V_{IL}, I_{OUT} = 0mA)	I_{CC}	—	125	mA
Output Low Voltage (I_{OL} = 8mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4mA)	V_{OH}	2.4	—	V
Standby Current (V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}, I_{OUT} = 0mA)	I_{SB}	—	20	mA
Peak Power-On Current (V_{CC} = V_{SS} to V_{CC}, Min $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min)	I_{PO}	—	30	mA
Output Short Circuit Current (V_{OUT} = V_{SS} to V_{CC})	I_{OS}	−200	200	mA

AC CHARACTERISTICS

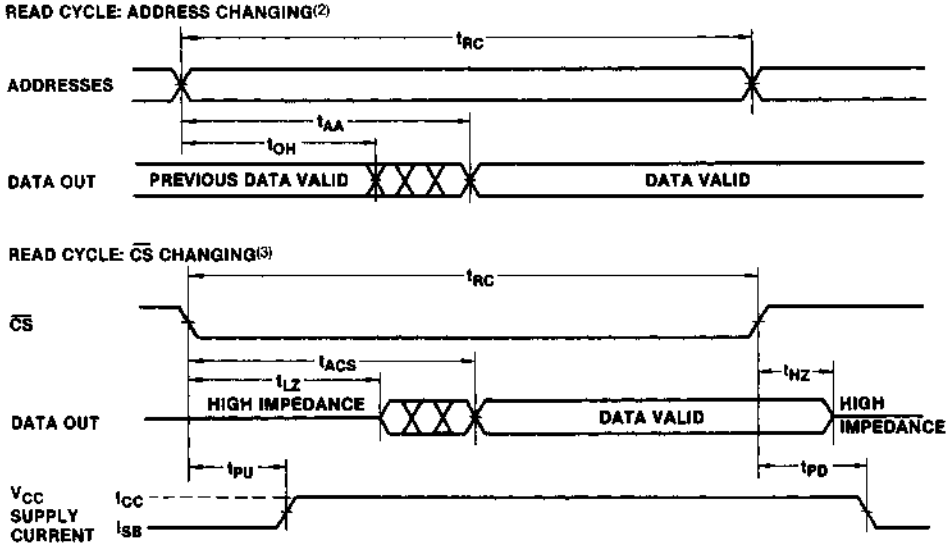
(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	NOTES	Symbol	MBM2148-55L			MBM2148-70L			Unit
			Min	Typ	Max	Min	Typ	Max	
Read Cycle Time		t_{RC}	55	—	—	70	—	—	ns
Address Access Time		t_{AA}	—	—	55	—	—	70	ns
Chip Select Access Time	1	t_{ACS1}	—	—	55	—	—	70	ns
Chip Select Access Time	2	t_{ACS2}	—	—	65	—	—	80	ns
Previous Read Data Valid After Change of Address		t_{OH}	5	—	—	5	—	—	ns
Chip Select to Power Up		t_{PU}	0	—	—	0	—	—	ns
Chip Select to Output Active	3	t_{LZ}	20	—	—	20	—	—	ns
Chip Select to Output Three-State	3	t_{HZ}	0	—	20	0	—	20	ns
Chip Select to Power Down		t_{PD}	—	—	30	—	—	30	ns

NOTE: 1. Chip deselected for greater than 55 ns prior to selection
2. Chip deselected for a finite time that is less than 55 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle: Address Changing.)
3. Transition is measured ±500 mV from high impedance voltage with LOAD B. This parameter is sampled and not 100% tested.

READ CYCLE (1)



NOTE: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincindent with $\overline{CS}$ low transition.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

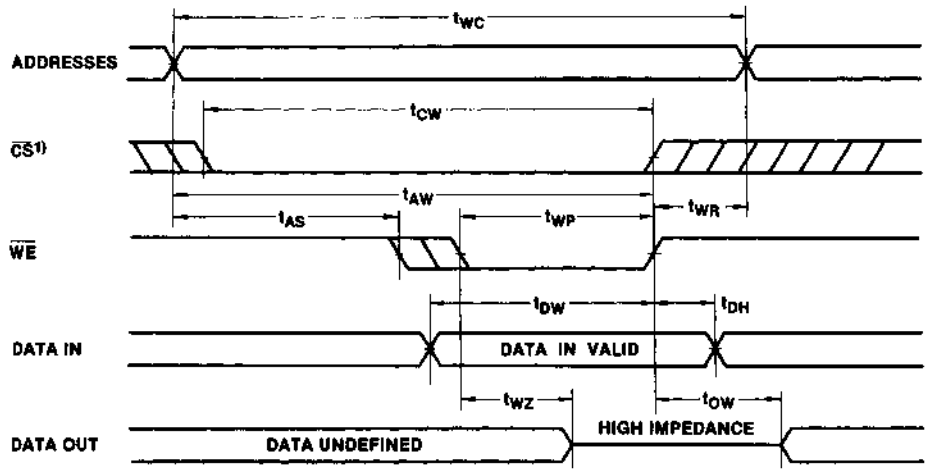
WRITE CYCLE

Parameter	NOTES	Symbol	MBM2148-55L			MBM2148-70L			Unit
			Min	Typ	Max	Min	Typ	Max	
Write Cycle Time		t_{WC}	55	—	—	70	—	—	ns
Address Valid to End of Write		t_{AW}	50	—	—	65	—	—	ns
Chip Select to End of Write		t_{CW}	50	—	—	65	—	—	ns
Data Valid to End of Write		t_{DW}	20	—	—	25	—	—	ns
Data Hold Time		t_{DH}	0	—	—	0	—	—	ns
Write Pulse Width		t_{WP}	40	—	—	50	—	—	ns
Write Recovery Time		t_{WR}	5	—	—	5	—	—	ns
Address Setup Time		t_{AS}	0	—	—	0	—	—	ns
Output Active From End of Write	1	t_{OW}	0	—	—	0	—	—	ns
Write Enabled to Output Three-State	1	t_{WZ}	0	—	20	0	—	25	ns

NOTE: 1. Transition is measured ±500 mV from high impedance voltage with LOAD B. This parameter is sampled and not 100% tested.

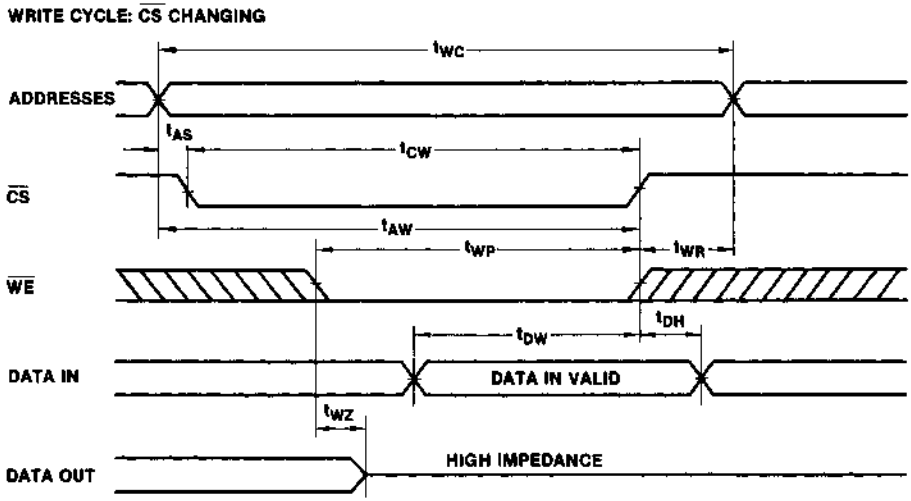
WRITE CYCLE

WRITE CYCLE: $\overline{WE}$ CHANGING



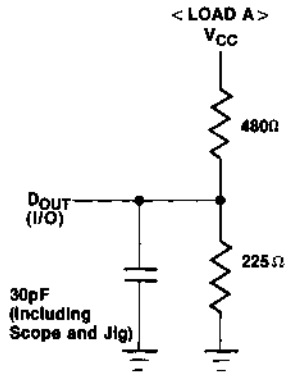
NOTE: 1. If $\overline{CS}$ goes high simulataneously with $\overline{WE}$ high, the output remains in a high impedance state.

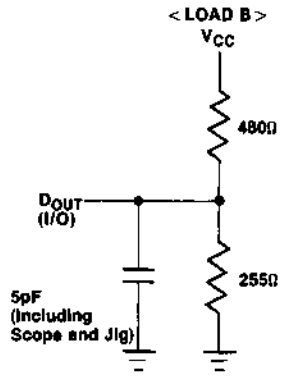
WRITE CYCLE



AC TEST CONDITIONS

Input Pulse Level:	0V to 3.0V
Input Pulse Rise and Fall Times:	5ns
Timing Measurement Reference Levels:	Inputs: 1.5V
	Outputs: 1.5V





OVERVIEW

The MBM2148 family from Fujitsu are high performance parts. They are designed for high speed and low power system requirements.

The high speed is obtained by advanced NMOS processing. The low power system requirements are achieved by the use of the MBM2148's chip select (active low). The MBM2148 automatically enters stand-by (drawing only I_{SB}) whenever the chip select is high. Upon activation of chip select ($\overline{CS}$ = LOW) the MBM2148 automatically powers up and draws I_{CC}.

This automatic power up/down is an extremely useful feature. PC board layout with proper V_{CC} decoupling will minimize power line glitches.

Input and data bus lines are an additional area of concern. Unless bus lines are properly designed and terminated, cross coupling, cross talk and reflections can occur. Of particular importance is the undershoot on address line. Once again, careful attention to good PC board layout and proper termination techniques will yield a well designed and reliable memory system.