# FUJITSU
## MICROELECTRONICS

# MBM27C64-25
# MBM27C64-30

## CMOS 65,536-BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

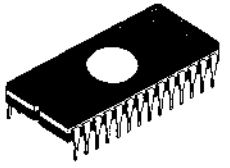
PRELIMINARY

### DESCRIPTION

The Fujitsu MBM27C64 is a high speed 65,536-bit static Complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially suited for applications where the extremely low power consumption of CMOS is essential. The device dissipates only 40 mW/MHz when active, typically 5μW when in standby, yet it provides the same high performance as the NMOS MBM2764-type devices.

A 28-pin dual in-line package with a transparent lid is used to package the MBM27C64. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can be programmed into the memory.

The MBM27C64 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 8192 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

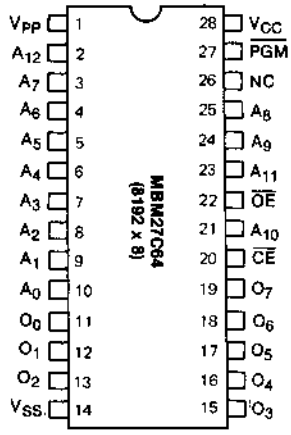


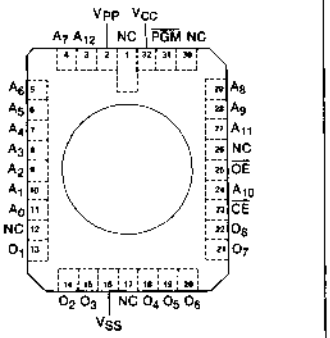
**CERDIP PACKAGE**
**DIP-28C-C01**
**ALSO AVAILABLE IN 32-PAD**
**CERAMIC LEADLESS CHIP CARRIER**
**LCC-32C-A01**

### FEATURES

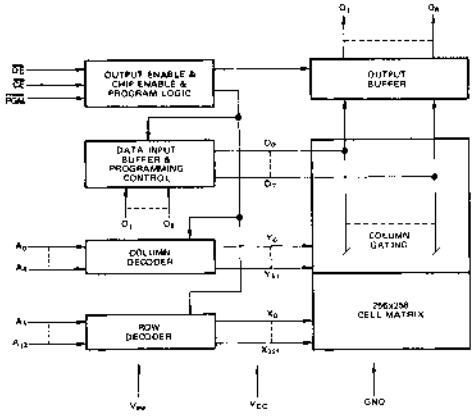
- **CMOS Power Consumption:**
  **500μW max. (Standby)**
  **5μW typ. (Standby)**
  **40mW/MHz (Active)**
- **Organized as 8192 words by 8-bits, fully decoded**
- **Utilizes the same simple programming requirements as MBM2764**
- **Single location programming**
- **Programming pulse may be reduced to 25 ns to cut programming time in half**
- **No clock required, fully static operation**
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Output Enable ($\overline{OE}$) pin simplifies memory expansion**
- **Fast Access Time:**
  **MBM27C64-25 250 ns max.**
  **MBM27C64-30 300 ns max.**
- **Single +5V operation**
- **Jedec standard 28-pin DIP package**
- **Pin and function compatible with 2764-type devices**

### PIN ASSIGNMENTS




### MBM27C64 BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS (See Note)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Temperature Under Bias | $T_A$ | −25 to +85 | °C |
| Storage Temperature | $T_{stg}$ | −65 to +125 | °C |
| Inputs/Outputs with Respect to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | −0.6 to +7 | V |
| $V_{CC}$ with Respect to $V_{SS}$ | $V_{CC}$ | −0.6 to +7 | V |
| $V_{PP}$ with Respect to $V_{SS}$ | $V_{PP}$ | −0.6 to +22 | V |

**Note:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

## FUNCTIONS AND PIN CONNECTIONS ($V_{CC}$(28) = +5, $V_{SS}$(14) = GND)

| Function (Pin No.) / Mode | Address Input (2 ~ 10, 21, 23 ~ 25) | Data I/O (11 ~ 13, 15 ~ 19) | $\overline{CE}$ (20) | $\overline{OE}$ (22) | $\overline{PGM}$ (27) | $I_{CC}$ Supply (28) | $V_{PP}$ (1) |
|---|---|---|---|---|---|---|---|
| Read | $A_{IN}$ | $D_{OUT}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $I_{CC1}$ | $V_{CC}$ |
| Output Disable | $A_{IN}$ | High Z | $V_{IL}$ | $V_{IH}$ | Don't Care | $I_{CC1}$ | $V_{CC}$ |
| | | | | Don't Care | $V_{IL}$ | | |
| Stand By | Don't Care | High Z | $V_{IH}$ | Don't Care | Don't Care | $I_{SB1}$ | $V_{CC}$ |
| Program | $A_{IN}$ | $D_{IN}$ | $V_{IL}$ | Don't Care | $V_{IL}$ | $I_{CC1}$ | $V_{PP}$ |
| Program Verify | $A_{IN}$ | $D_{OUT}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $I_{CC1}$ | $V_{PP}$ |
| Program Inhibit | Don't Care | High Z | $V_{IH}$ | Don't Care | Don't Care | $I_{SB1}$ | $V_{PP}$ |

## CAPACITANCE

($T_A$ = 25°C, f = 1 MHz)

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Input Capacitance ($V_{IN}$ = 0V) | $C_{IN}$ | 4 | 6 | pF |
| Output Capacitance ($V_{OUT}$ = 0V) | $C_{OUT}$ | 8 | 12 | pF |

## RECOMMENDED OPERATING CONDITIONS

(Referenced to $V_{SS}$ = GND)

| Parameter | Symbol | Min | Typ | Max | Unit | Operating Temperature |
|---|---|---|---|---|---|---|
| Supply Voltage[1] | $V_{CC}$ | 4.75 | 5.0 | 5.25 | V | 0°C to +70°C |
| Supply Voltage | $V_{PP}$ | $V_{CC}$ −0.6 | — | $V_{CC}$ +0.6 | V | |
| Supply Voltage | $V_{SS}$ | — | GND | — | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | — | $V_{CC}$ +0.3 | V | |
| Input Low Voltage | $V_{IL}$ | −0.1 | — | 0.8 | V | |

**Note:** 1. $V_{CC}$ must be applied either before or coincident with $V_{PP}$ and removed either after or coincident with $V_{PP}$.

PRELIMINARY

## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Load Current ($V_{IN}$ = 5.25V) | $I_{LI}$ | — | — | 10 | μA |
| Output Leakage Current ($V_{OUT}$ = 5.25V) | $I_{LO}$ | — | — | 10 | μA |
| $V_{PP}$ Supply Current | $I_{PP1}$ | — | 1 | 100 | μA |
| $V_{CC}$ Standby Current ($\overline{CE}$ = $V_{IH}$) | $I_{SB1}$ | — | — | 1 | mA |
| $V_{CC}$ Standby Current ($\overline{CE}$ = $V_{CC}$ −0.3V to $V_{CC}$ + 0.3V, $I_{OUT}$ = 0mA) | $I_{SB2}$ | — | 1 | 100 | μA |
| $V_{CC}$ Active Current ($\overline{CE}$ = $V_{IL}$) | $I_{CC1}$ | — | — | 30 | mA |
| $V_{CC}$ Operation Current (f = 4MHz, $I_{OUT}$ = 0mA) | $I_{CC2}$ | — | — | 30 | mA |
| Output Low Voltage ($I_{OL}$ = 2.1mA) | $V_{OL}$ | — | — | 0.45 | V |
| Output High Voltage ($I_{OH}$ = −400μA) | $V_{OH}$ | 2.4 | — | — | V |

## AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

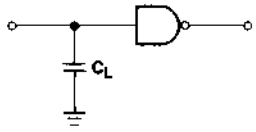
| Parameter | Symbol | MBM27C64-25 | | MBM27C64-30 | | | Unit |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Address Access Time ($\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, $\overline{PGM}$ = $V_{IH}$) | $t_{ACC}$ | — | — | 250 | — | — | 300 | ns |
| $\overline{CE}$ to Output Delay ($\overline{OE}$ = $V_{IL}$, $\overline{PGM}$ = $V_{IH}$) | $t_{CE}$ | — | — | 250 | — | — | 300 | ns |
| $\overline{OE}$ to Output Delay ($\overline{CE}$ = $V_{IL}$, $\overline{PGM}$ = $V_{IH}$) | $t_{OE}$ | 10 | — | 100 | 10 | — | 150 | ns |
| $\overline{PGM}$ to Output Delay ($\overline{CE}$ = $\overline{OE}$ = $V_{IL}$) | $t_{PGM}$ | 10 | — | 100 | 10 | — | 150 | ns |
| Output Enable High to Output Float (See Note) | $t_{DF}$ | 0 | — | 90 | 0 | — | 130 | ns |
| Address to Output Hold | $t_{OH}$ | 0 | — | — | 0 | — | — | ns |

**Note:** $t_{DF}$ is specified from $\overline{CE}$, $\overline{OE}$, or $\overline{PGM}$, whichever occurs first.

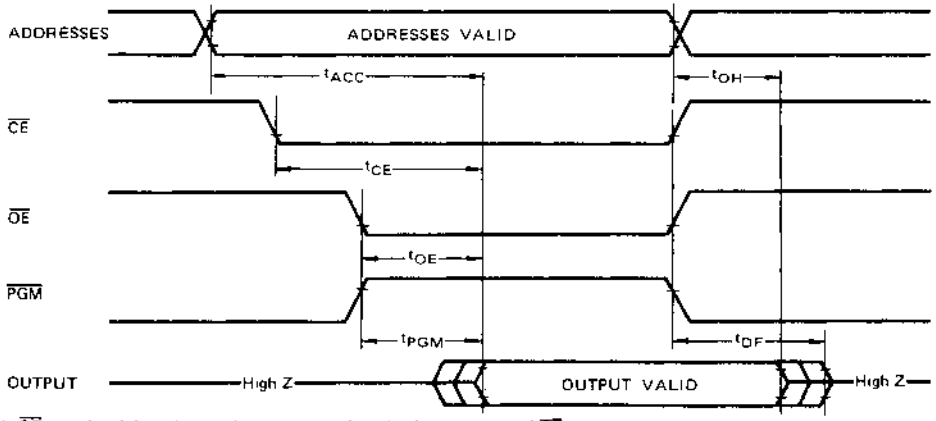
## AC TEST CONDITIONS

**Input Pulse levels:** 0.8V to 2.2V
**Input Rise and Fall Time:** ≤ 20nsec
**Timing Measurement Reference Levels:** 1.0V and 2.0V for inputs
0.8V and 2.0V for outputs
1 TTL gate and $C_L$ = 100 pF

**Output Load:**



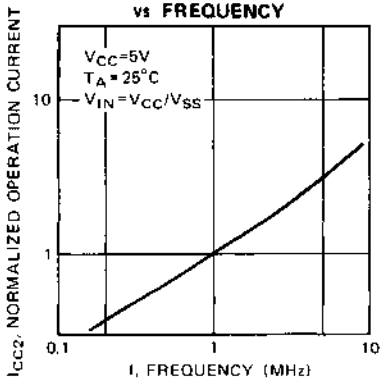

## OPERATION TIMING DIAGRAM



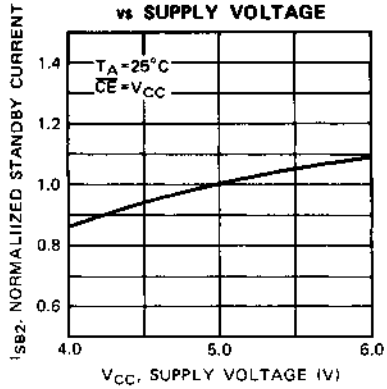

**Notes:** 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{ACC}$.

## TYPICAL CHARACTERISTICS CURVES

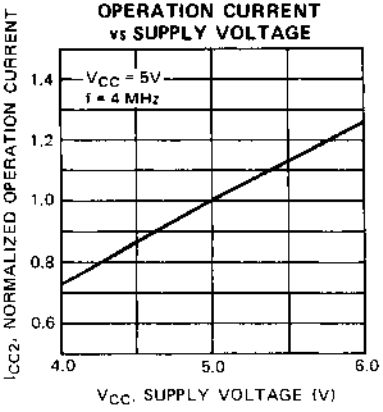
OPERATION CURRENT vs FREQUENCY



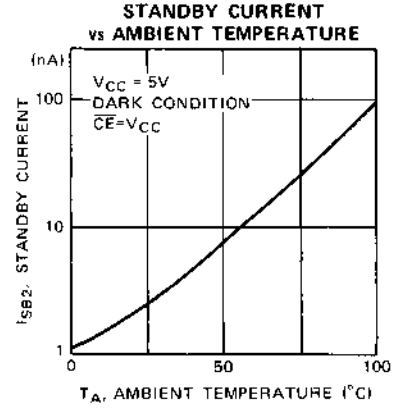

STANDBY CURRENT vs SUPPLY VOLTAGE



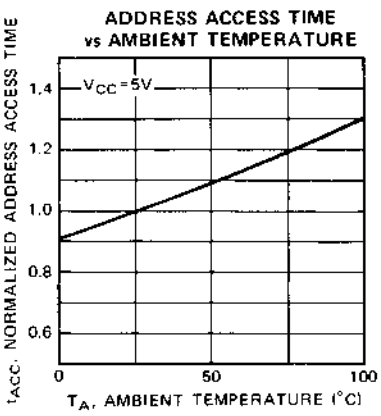

OPERATION CURRENT vs SUPPLY VOLTAGE



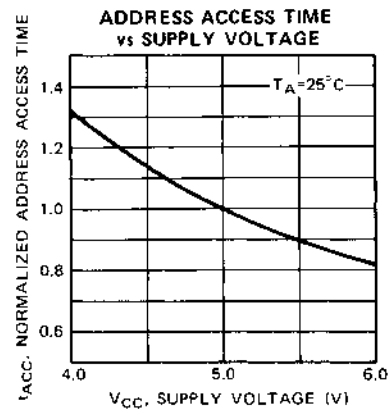

STANDBY CURRENT vs AMBIENT TEMPERATURE



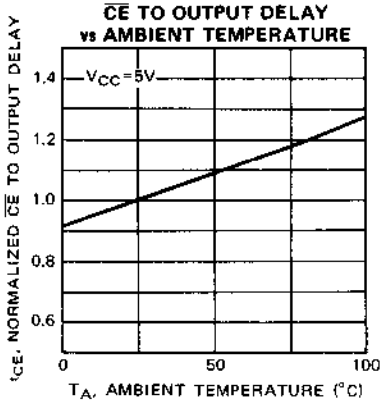

ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

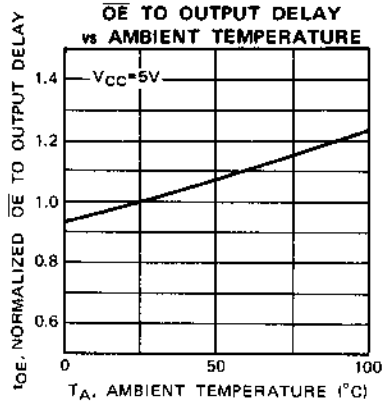


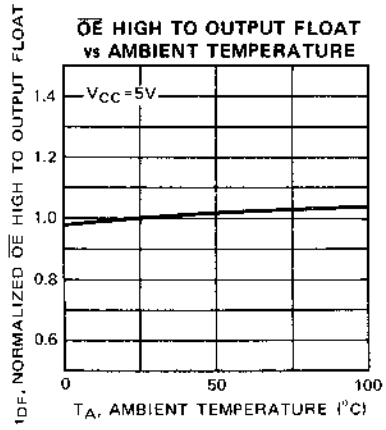

ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

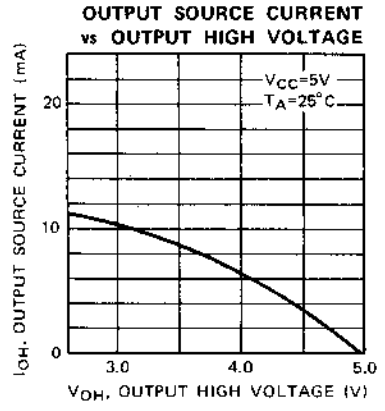


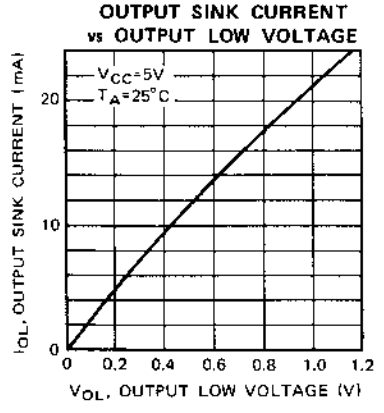
## TYPICAL CHARACTERISTICS CURVES (Continued)

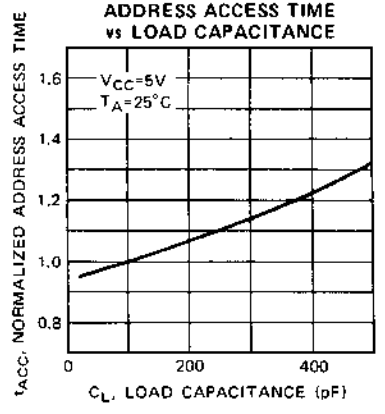


## PROGRAMMING / ERASING INFORMATION

### MEMORY CELL DESCRIPTION

The MBM27C64 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 1). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 2). In the initial state, the cell has a low threshold ($V_{TH1}$) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level ($V_{TH0}$), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold ($V_{THS}$), as indicated by the dotted line in Fig. 2.

**Fig. 1 — MEMORY CELL**

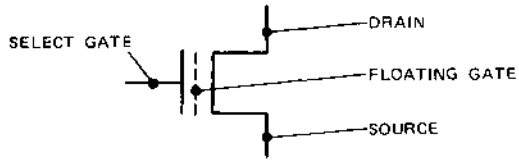
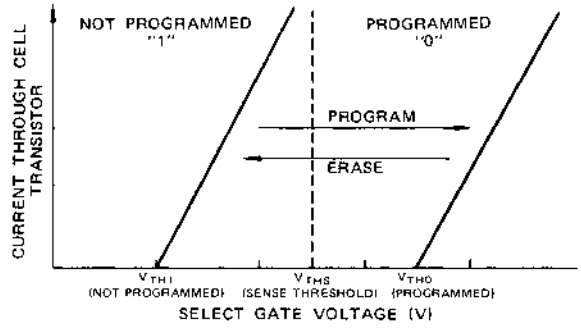



**Fig. 2 — MEMORY CELL THRESHOLD SHIFT**




### PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C64 has all 65,536 bits in the "1" or high state. "0's" are loaded into the MBM27C64 through the procedure of programming.

The programming mode is entered when +21V is applied to the $V_{PP}$ pin and CE and PGM are both at $V_{IL}$. During programming, CE is kept at $V_{IL}$. A 0.1μF capacitor between $V_{PP}$ and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. Eight bit patterns are placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, 50 msec, TTL low level pulse is applied to the PGM input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the PGM input is prohibited when programming.

### ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27C64 to an ultraviolet light source. A dosage of 15W-seconds/cm$^2$ is required to completely erase an MBM27C64. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000μW/cm$^2$) for 15 to 20 minutes. The MBM27C64 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27C64 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27C64 and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PRELIMINARY

Note: This is not a final specification. Some parametric limits are subject to change.

## PROGRAMMING/ERASING INFORMATION (Continued)

### DC CHARACTERISTICS

($T_A$ = 25 ±3°C, $V_{CC}$ = 5V ±5%, $V_{PP}$ = 21V ±0.5V)

| Parameter | Symbol | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | — | 10 | μA | $V_{IN}$ = 0.45V–5.25V |
| Output Low Voltage During Verify | $V_{OL}$ | — | 0.45 | V | $I_{OL}$ = 2.1 mA |
| Output High Voltage During Verify | $V_{OH}$ | 2.4 | — | V | $I_{OH}$ = −400μA |
| $V_{CC}$ Supply Current | $I_{CC1}$ | — | 30 | mA | — |
| Input Low Voltage | $V_{IL}$ | −0.1 | 0.8 | V | — |
| Input High Voltage | $V_{IH}$ | 2.0 | $V_{CC}$ +0.3 | V | — |
| $V_{PP}$ Supply Current During Progamming Pulse | $I_{PP2}$ | — | 30 | mA | $\overline{CE}$ = $\overline{PGM}$ = $V_{IL}$ |

**Note:** 1. $V_{CC}$ must be applied either coincidently or before $V_{PP}$ and removed either coincidently or after $V_{PP}$.

2. $V_{PP}$ must not be greater than 21.5 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining $V_{PP}$ = 21 volts. Also, during $\overline{CE}$ = $\overline{PGM}$ = $V_{IL}$, $V_{PP}$ must not be switched from 5 volts to 21 volts or vise-versa.

### AC CHARACTERISTICS

($T_A$ = 25 ±3°C, $V_{CC}$ = 5V ±5%, $V_{PP}$ = 21V ±0.5V)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Address Setup Time | $t_{AS}$ | 2 | — | — | μs |
| $\overline{CE}$ Setup Time | $t_{CES}$ | 2 | — | — | μs |
| Data Setup Time | $t_{DS}$ | 2 | — | — | μs |
| Address Hold Time | $t_{AH}$ | 0 | — | — | μs |
| Data Hold Time | $t_{DH}$ | 2 | — | — | μs |
| Chip Enable to Output Float Delay | $t_{DF}$ | 0 | — | 130 | ns |
| $V_{PP}$ Setup Time | $t_{VS}$ | 2 | — | — | μs |
| $\overline{PGM}$ Pulse Width | $t_{PW}$ | 25 | 50 | 55 | ms |
| $\overline{OE}$ Setup Time | $t_{OES}$ | 2 | — | — | μs |
| Data Valid from $\overline{OE}$ | $t_{OE}$ | — | — | 150 | ns |

### PROGRAMMING WAVEFORM