ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

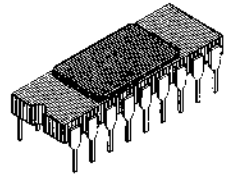
The Fujitsu MBM100470 is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. The device is organized ad 4096 words by one bit, and it features on-chip voltage/temperature compensation for improved noise margin.

The MBM100470 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon) as well as IOP (Isolation by Oxide and Polysilicon), processing.

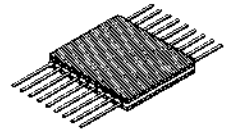
Operation for the MBM100470 is specified over a temperature range of from 0° to 85°C (T_A for DIP, T_C for Flat Package). It also features 18-pin Ceramic DIP and Flat Package, and is fully compatible with industry-standard 100K-series ECL families.

FEATURES

- **4096 words x 1-bit organization**
- **On-chip voltage/temperature compensation for improved noise margin**
- **Address access time:**
  20ns Max.
  14ns Typ.
- **Chip select access time:**
  15ns Max.
  5ns Typ.
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of 0.16mW/bit**
- **DOPOS and IOP processing**
- **Pin compatible with the F100470**



CERAMIC PACKAGE
DIP-18C-F02



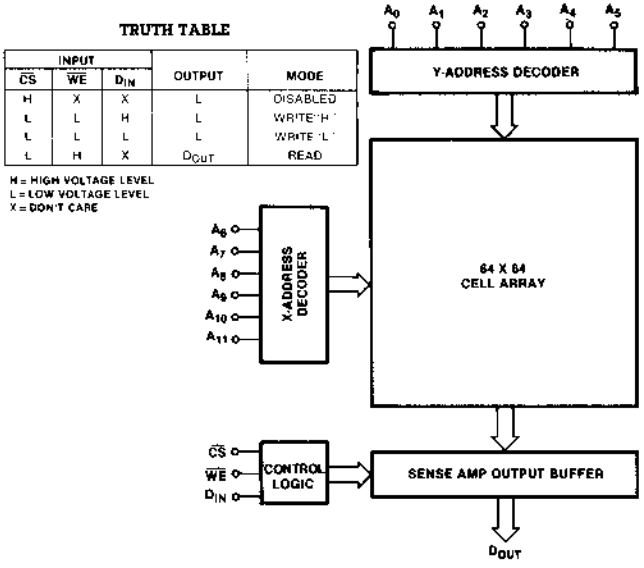
CERAMIC PACKAGE
FPT-18C-C01

MBM100470 BLOCK DIAGRAM

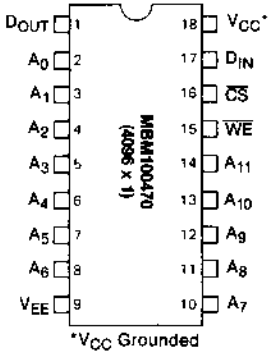
TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE



PIN ASSIGNMENT



*V_{CC} Grounded

NOTE: DIP and Flatpack Styles conform to the same pin assignment

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUNCTIONAL DESCRIPTION

The Fujitsu 100470 is fully decoded 4096-bit read/write random access memory organized as 4096 words by one bit. Memory cell selection is achieved by means of 12-bit address designated $A_0 - A_{11}$. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A for DIP	−55 to +125	°C
	T_C for Flat Package	−55 to +125	
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in operational sections of this data sheet.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package
Supply Voltage	V_{EE}	−5.7	−4.5	−4.2	V	0°C to 85°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	7	—	pF

DC CHARACTERISTICS

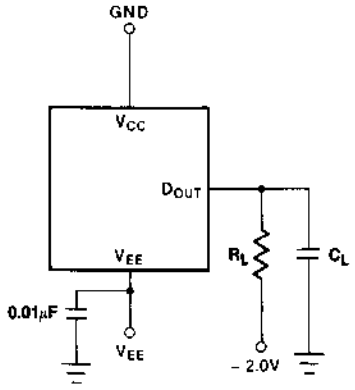
(V_{CC} = 0V, V_{EE} = −4.5V, Output Load = 50Ω and 30pF to −2.0V, T_A = 0°C to 85°C for DIP, T_C = 0°C to 85°C for Flat Package, Airflow ≧ 2.5 m/s, unless otherwise noted.)

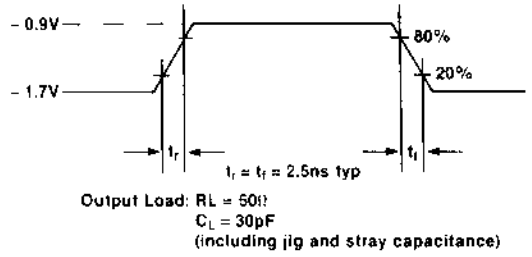
Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\,max.}$ or $V_{IL\,min.}$)	V_{OH}	−1025	—	−880	mV
Output Low Voltage (V_{IN} = $V_{IH\,max.}$ or $V_{IL\,min.}$)	V_{OL}	−1810	—	−1620	mV
Output High Voltage (V_{IN} = $V_{IH\,min.}$ or $V_{IL\,max.}$)	V_{OHC}	−1035	—	—	mV
Output Low Voltage (V_{IN} = $V_{IH\,min.}$ or $V_{IL\,max.}$)	V_{OLC}	—	—	−1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1165	—	−880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1810	—	−1475	mV
Input High Current (V_{IN} = $V_{IH\,max.}$)	I_{IH}	—	—	220	μA
Input Low Current (V_{IN} = $V_{IL\,min.}$)	I_{IL}	−50	—	—	μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\,min.}$)	I_{IL}	0.5	—	170	μA
Power Supply Current (All Inputs and Output Open)	I_{EE}	−195	—	—	mA

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −4.5V ±5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 85°C for DIP, T_C = 0°C to 85°C for Flat Package, Airflow ≧ 2.5 m/s, unless otherwise noted.)

AC TEST CONDITIONS





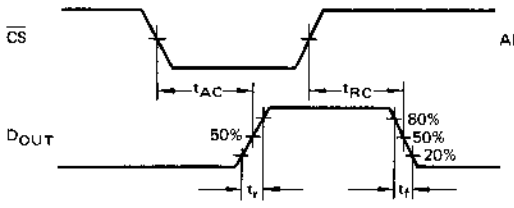
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

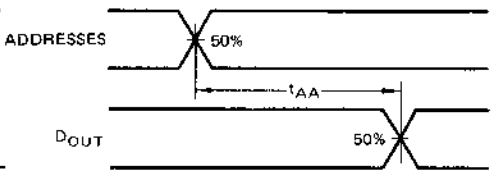
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	14	20	ns
Chip Select Access Time	t_{AC}	—	5	15	ns
Chip Select Recovery Time	t_{RC}	—	5	15	ns

READ CYCLE

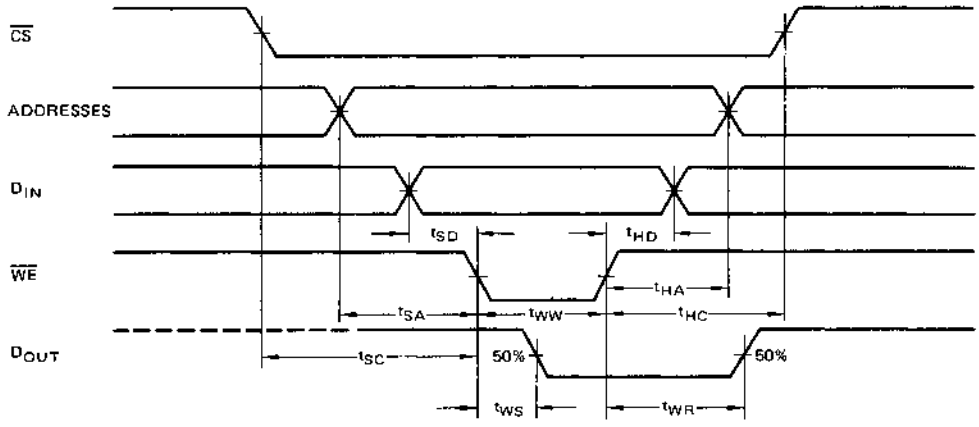




WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	15	6	—	ns
Write Disable Time	t_{WS}	—	—	15	ns
Write Recovery Time	t_{WR}	—	—	15	ns
Address Set Up Time	t_{SA}	3	0	—	ns
Chip Select Set Up Time	t_{SC}	2	0	—	ns
Data Set Up Time	t_{SD}	2	0	—	ns
Address Hold Time	t_{HA}	2	0	—	ns
Chip Select Set Up Time	t_{HC}	2	0	—	ns
Data Hold Time	t_{HD}	2	0	—	ns

WRITE CYCLE

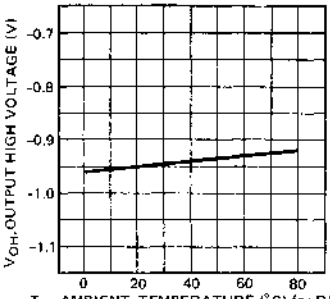


RISE TIME AND FALL TIME

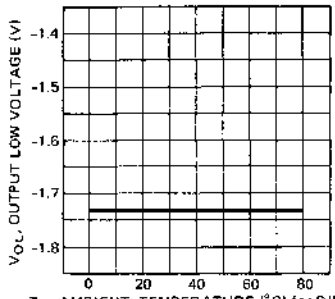
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	—	3	—	ns
Output Fall Time	t_f	—	3	—	ns

TYPICAL CHARACTERISTICS CURVES

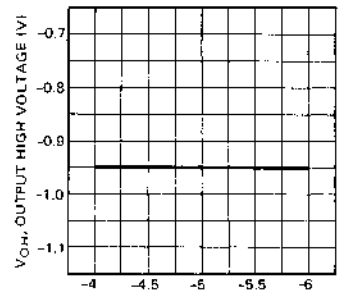
OUTPUT HIGH VOLTAGE vs TEMPERATURE



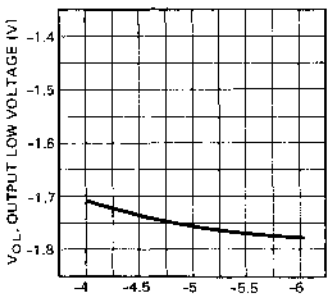
OUTPUT LOW VOLTAGE vs TEMPERATURE



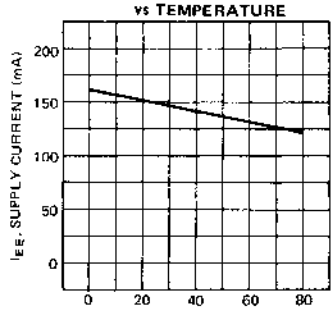
OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE



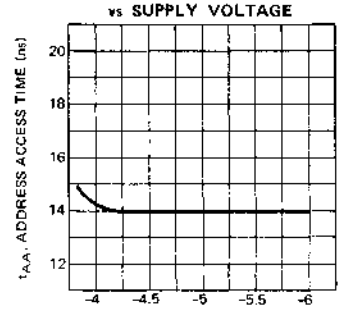
OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE



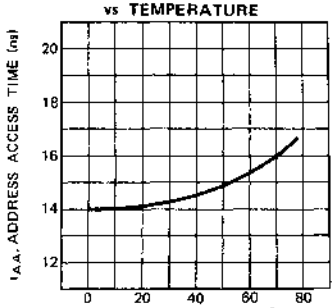
SUPPLY CURRENT vs TEMPERATURE



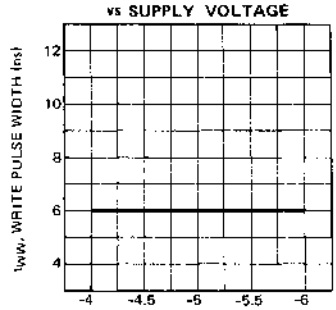
ADDRESS ACCESS TIME vs SUPPLY VOLTAGE



ADDRESS ACCESS TIME vs TEMPERATURE



WRITE PULSE WIDTH vs SUPPLY VOLTAGE



WRITE PULSE WIDTH vs TEMPERATURE