MP5516

2.65V to 16V, 6A, Power Loss Protection Management IC with E-Fuse

DESCRIPTION

The MP5516 is a monolithic power management solution designed to manage energy storage and release in enterprise solid-state drives (SSDs). It integrates an input current limit (I_{LIMIT_E-FUSE}) switch and a bidirectional buck-boost converter for energy management. The e-fuse features a low on-resistance, current limiting, and reverse current blocking.

The configurable I_{LIMIT_E-FUSE} prevents inrush current during start-up. Reverse-current blocking prevents backup energy from flowing to the failing input voltage (V_{IN}) port to fully utilize the backup energy during a power outage.

Backup energy is stored in the storage capacitors. MPS's patented energy storage and release management control circuit minimizes the storage capacitor requirement. The IC provides a high storage voltage (V_{STRG}) to store energy in capacitance. If an input outage occurs, this energy is released to the system during a hold time (t_{HOLD}). V_{STRG} and the buck release voltage (V_{BUCK_RLS}) are both configurable for different system applications.

The configurable charge current (I_{CHARGE}) is provided to ramp up V_{STRG} in a controllable manner. Constant-on-time (COT) control reduces the voltage dip during the transition between boost charge mode and buck release mode. Only one inductor is required, which minimizes the total solution size.

The device also features an I^2C interface and an internal analog-to-digital converter (ADC). I_{LIMIT_E-FUSE} can be configured via the I^2C. The I^2C can also perform capacitor health tests. The internal ADC monitors the input voltage, input current, and input power.

The MP5516 requires a minimal number of readily available, standard external components, and is available in a QFN-25 (4mmx4mm) package.

FEATURES

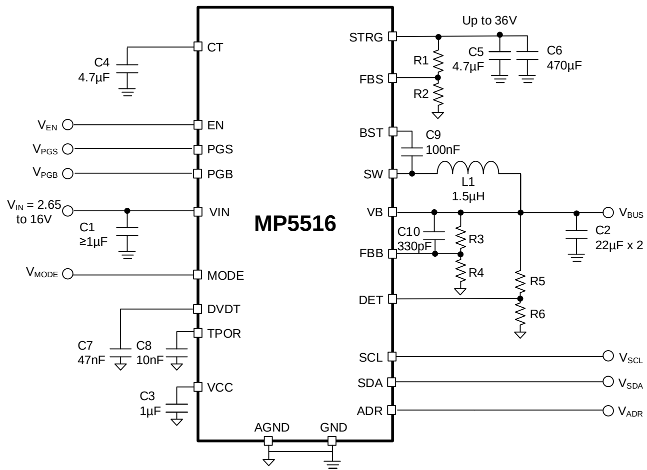
- Input Current Limit (I_{LIMIT_E-FUSE}) Switch:
  - Wide 2.65V to 16V Input Voltage (V_{IN}) Range
  - 20mΩ $R_{DS(ON)}$ MOSFET for E-Fuse
  - 1.2A to 6A Configurable I_{LIMIT_E-FUSE}
  - 3.3V, 5V, or 12V Selectable Over-Voltage Protection (OVP)
  - Reverse-Current Blocking at Input to Prevent Current Leakage
  - Configurable Soft-Start Time (t_{SS})
  - Configurable Start-Up Delay Time (t_{TPOR})
- 36V Charge and Backup Converter:
  - Up to 36V Configurable Storage Voltage
  - 60mΩ/37mΩ $R_{DS(ON)}$ MOSFETs
  - Configurable Boost Charge Current
  - Boost Charge Mode and Buck Release Mode Auto-Alternating via System Voltage Regulation
  - Constant On-Time (COT) Control for Steady-State Operation in Buck Release Mode with Configurable Switching Frequency (f_{SW})
  - Short-Circuit Protection (SCP) for Both Load Side and Energy Storage Side
  - Storage Capacitance Detection
- System:
  - Multiple-Time Programmable (MTP) Memory Up to 1000 Times
  - Digital I^2C Interface for Status Monitoring, Parameter Configuration, and Operation Control
  - Enable (EN) Control
  - Available in a Compact QFN-25 (4mmx4mm) Package

MPL Optimized Performance with MPS Inductor MPL-AL6050 Series

APPLICATIONS

- Enterprise Solid-State Drives (SSDs)
- Power Backup Solutions

TYPICAL APPLICATION



Storage Voltage Release

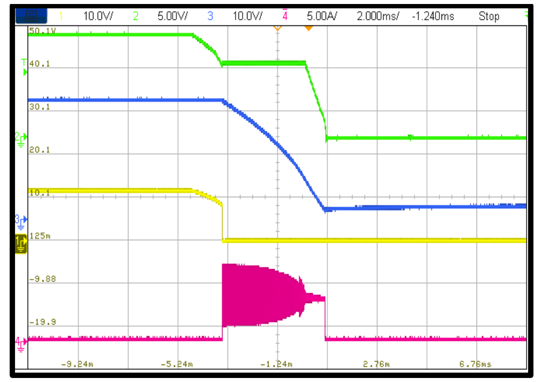
V_{IN} = 12V, V_{DET} = 8.4V, V_{BUS_RLS} = 8.6V,
V_{STRG} = 28V, L = 1.5µH, f_{SW} = 600kHz,
I_{BUS_LOAD} = 5A

CH2: V_{BUS} 5V/div.

CH3: V_{STRG} 10V/div.

CH1: V_{PGB} 10V/div.

CH4: I_L 5A/div.



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5516GR-xxxx**	QFN-25 (4mmx4mm)	*See Below*	1
MP5516GR-0000	QFN-25 (4mmx4mm)	*See Below*	1
EVKT-MP5516	Evaluation Kit		

* For Tape & Reel, add suffix -Z (e.g. MP5516GR-xxxx-Z).

** "xxxx" is the configuration code identifier for the register setting stored in the MTP.

The default number is "0000". Each "x" can be hexadecimal value between 0 and F. Contact an MPS FAE to create this unique number, even if ordering the "0000" code. "MP5516GR-0000" is the default version.

TOP MARKING

MPSYWW
MP5516
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP5516: Part number
LLLLLL: Lot number

EVALUATION KIT EVKT-MP5516

EVKT-MP5516 Kit contents: (Items below can be ordered separately).

#	Part Number	Item	Quantity
1	EV5516-R-00B	MP5516 evaluation board	1
2	EVKT-USBI2C-02-BAG	Includes one USB to I^2C communication interface, one USB cable, and one ribbon cable	1
3	MP5516GR-0000	MP5516 PMIC (can be used for MTP configuration)	2
4	Online resources	Includes datasheet, user guide, product brief, and GUI	1

Order direct from MonolithicPower.com or our distributors.

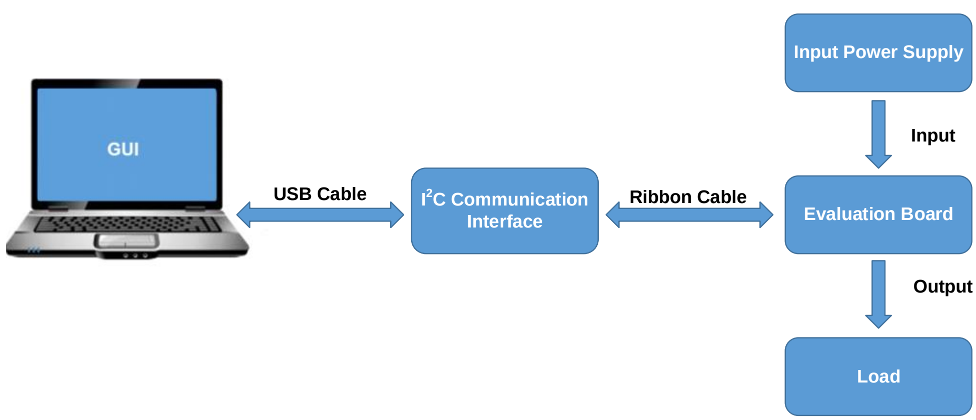
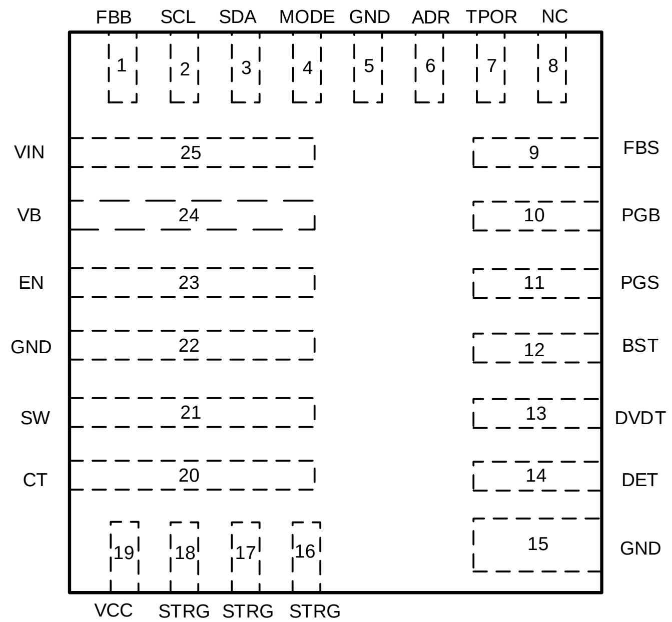


Figure 1: EVKT-MP5516 Evaluation Kit Set-Up

PACKAGE REFERENCE

TOP VIEW



QFN-25 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	FBB	**Bus voltage feedback sense.** Use an external resistor divider to set the buck mode regulation threshold. The internal voltage reference (V_{REF}) is 0.6V.
2	SCL	**I^2C interface clock pin.** The SCL pin can support an up to 3.4MHz I^2C clock.
3	SDA	**I^2C interface data pin.**
4	MODE	**Output clamp voltage selection.** Pull the MODE pin to logic high to set the clamp voltage (V_{CLAMP}) to 5.6V. Pull MODE to logic low to set V_{CLAMP} to 3.7V. Float MODE to set V_{CLAMP} to 13V.
5	AGND	**PMIC signal ground.** Connect a ⩾1µF between the AGND and VCC pins to provide a clean internal control power supply.
6	ADR	**I^2C address.** The I^2C address can be configured via the ADR pin. There are three I^2C address options. Pull ADR high to set the I^2C address to 59h. Pull ADR low to set the I^2C address to 5Ah. Float ADR to set the I^2C address to 5Bh.
7	TPOR	**E-fuse start-up delay time.** Connect a ⩾1nF capacitor between the TPOR and AGND pins to set the e-fuse start-up delay time (t_{TPOR}).
8	NC	**Not connected.** Float the NC pin.
9	FBS	**Storage voltage feedback sense.** A voltage divider connected to the FBS pin sets the storage voltage (V_{STRG}) during boost charging mode. The internal V_{REF} is 1.2V.
10	PGB	**Bus voltage power good indicator.** The PGB pin is an open drain output. If the DET pin voltage (V_{DET}) drops below 0.6V, then PGB is pulled low. If both the FBB pin voltage (V_{FBB}) and the DET pin voltage (V_{DET}) exceed 0.63V, then PGB is pulled high.
11	PGS	**Storage voltage power good indication.** The PGS pin is an open drain output. If the FBS pin voltage (V_{FBS}) drops below 1.08V, then PGS is pulled low. If V_{FBS} exceeds 1.17V, then PGS is pulled high.
12	BST	**Bootstrap.** Connect a 0.1µF bootstrap (BST) capacitor (C_{BST}) between the BST and SW pins to supply the high-side MOSFET (HS-FET) driver.
13	DVDT	**Bus voltage start-up slew rate control.** Connect a capacitor between the DVDT and AGND pins to set the bus voltage (V_{BUS}) start-up slew rate.
14	DET	**Bus voltage detection.** The DET pin sets V_{BUS} so that the part enters buck release mode once V_{FBB} drops below the boost to buck transition threshold (V_{BOOST_BUCK}). The buck mode detection point can be configured via an external resistor divider. The internal V_{REF} is 0.6V.
15, 22	GND	**Power ground**.
16, 17, 18	STRG	**Backup energy storage.** Connect the backup capacitors to the STRG pin for the energy storage and release functions.
19	VCC	**Internal LDO output.** The VCC pin voltage (V_{CC}) is supplied internally. Connect a ⩾1µF ceramic capacitor between the VCC and AGND pins to provide a clean internal power supply.
20	CT	**Internal disconnect MOSFET drain.** Connect a ⩾2.2µF capacitor to the CT pin for stable operation. The voltage rating of the CT capacitor (C_{CT}) should to be equal to the storage capacitor (C_{STRG}).
21	SW	**Switching node.** The SW pin is used for the energy storage and release circuitry. Connect an inductor between the SW and VB pins.
23	EN	**Enable.** The EN pin controls the input load switch. Pull EN logic high to turn the load switch on; pull EN to GND to turn it off.
24	VB	**Bus voltage.** Place a 22µF to 47µF ceramic capacitor as close to the VB pin as possible.
25	VIN	**Input power supply.** Place a ⩾1µF ceramic capacitor as close to the VIN pin as possible. If the VIN power line is long and the system has a high input voltage (V_{IN}) spike, then place a TVS diode at the input.

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) 18V
V_{BUS}, V_{PGS}, V_{PGB}, V_{MODE}, V_{TPOR}, V_{ADR}, V_{FBB}, V_{DET},
V_{EN}, V_{CT} - V_{STRG} ....-0.3V to +18V
V_{STRG}, V_{CT}, V_{BST}, V_{FBS} ....-0.3V to +40V
V_{SW}..... -0.3V (-2V < 40ns) to +40V (41V < 40ns)
V_{DVDT}, V_{SCL}, V_{SDA} ....-0.3V to 5.5V
V_{CC}, V_{BST} - V_{SW} ....-0.3V to 5.5V
Continuous power dissipation (T_A = 25°C) (2)
Junction temperature ....150°C
Lead temperature ....260°C
EVL5516-R-00A (3) 5.66W

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM)....................750V

Recommended Operating Conditions (4)

Input voltage (V_{IN}), V_{BUS} ....2.65V to 13.5V
V_{PGS}, V_{PGB}, V_{MODE}, V_{TPOR}, V_{ADR}, V_{FBB}, V_{DET}, V_{EN},
V_{CT} - V_{STRG} ....2.65V to 16V
V_{STRG}, V_{CT}, V_{BST}, V_{FBS} .... V_{IN_MAX} to 36V
V_{SW}..... -0.3V (-2V < 40ns) to +40V (41V < 40ns)
V_{DVDT}, V_{SCL}, V_{SDA} ....-0.3V to +5V
V_{CC}, V_{BST} - V_{SW} ....-0.3V to +5V
Internal junction temp (T_J)........ -40°C to +125°C
Ambient temperature .... -40°C to +85°C

Thermal Resistance (3)

Thermal Resistance (3)	θ_{JA}	θ_{JC}	
EVL5516-R-00A (3)	22.1	8.9	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on EVL5516-R-00A, 6-layer PCB.
4) The device is not guaranteed to function outside of its operating conditions.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to 125°C (5), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
E-Fuse						
Input voltage	V_{IN}		2.65		16	V
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$	MODE is pulled logic low	2.4	2.5	2.6	V
		MODE is pulled logic high	3.35	3.5	3.65	V
		MODE is floating	7.8	8.25	8.7	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$	MODE is pulled logic low	2.1	2.2	2.3	V
		MODE is pulled logic high	3.15	3.3	3.45	V
		MODE is floating	7.2	7.75	8.2	V
E-fuse on resistance	$R_{DS(ON)\_E-FUSE}$			20		mΩ
Reverse blocking current	I_{RB}	V_{IN} = 0V, V_{BUS} = 16V, V_{EN} = 0V		2		µA
Bias current	I_{BIAS}	V_{IN} = 5V, V_{EN} = 0V		1.6		mA
Bus voltage (V_{BUS}) trigger threshold	$V_{TRIGGER}$	MODE is pulled logic low		3.9	4.15	V
		MODE is pulled logic high		6	6.3	V
		MODE is floating		13.8	15	V
Output clamp voltage	V_{CLAMP}	MODE is pulled logic low		3.7	3.95	V
		MODE is pulled logic high		5.6	5.9	V
		MODE is floating		13	13.5	V
V_{BUS} soft-start time via DVDT	t_{DVDT}	C_{DVDT} = 10nF, MODE is pulled high, from 10% of V_{BUS} to 90% of V_{BUS}		1.2		ms
E-fuse start-up reset delay	t_{TPOR}	C_{TPOR} = 10nF		3.4		ms
E-fuse current limit	I_{LIMIT_E-FUSE}	I^2C-configurable, EFUSE[5:3] = 111	5.4	6	6.6	A
PGB rising threshold	V_{PGB_RISING}	V_{FBB} rising	0.621	0.63	0.639	V
PGB falling threshold	$V_{PGB\_FALLING}$	V_{DET} falling	0.591	0.6	0.609	V
VCC regulation voltage	V_{CC}	$V_{IN} \geqslant$ 5V		5		V
		V_{IN} < 5V		V_{IN}		V
Enable (EN) logic high	V_{EN_HIGH}		1.5			V
EN logic low	V_{EN_LOW}				0.4	V
36V Charge and Backup Converter						
Boost mode operating input voltage	V_{BOOST}		2.8		16	V
Boost mode input UVLO rising threshold	$V_{BOOST\_UVLO\_RISING}$			2.6	2.8	V
Boost mode input UVLO hysteresis	$V_{BOOST\_UVLO\_HYS}$			0.22		V
Storage voltage	V_{STRG}				36	V
Switching frequency	f_{SW}	I^2C-configurable, STRG[1:0] = 01		600		kHz

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to 125°C (5), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
HS-FET minimum on time (6)	$t_{ON\_MIN\_HS}$			80		ns
LS-FET minimum on time (6)	t_{ON,MIN_LS}			80		ns
Boost over-voltage protection (OVP) threshold	V_{BOOST_OVP}	V_{FBS} rising	1.18	1.2	1.22	V
Boost OVP release threshold	$V_{BOOST\_OVP\_RLS}$	V_{FBS} falling	1.15	1.17	1.19	V
Boost charge peak current	I_{CHARGE_PEAK}	I^2C-configurable, PLP[3:1] = 001, V_{IN} = 5V, L = 2.2µH		850		mA
Mode transition threshold	V_{BUCK_BOOST}	V_{FBB} rising	0.621	0.63	0.639	V
	V_{BOOST_BUCK}	V_{DET} falling	0.591	0.6	0.609	V
Buck detection reference voltage (V_{REF})	V_{BUCK_DET}		0.591	0.6	0.609	V
Buck regulation V_{REF}	V_{BUCK_REF}		0.591	0.6	0.609	V
Buck regulation V_{REF} accuracy		T_J = 25°C	-1%		+1%	
			-1.5%		+1.5%	
Buck valley current limit	I_{LIMIT_VALLEY}			4		A
PGS rising threshold	V_{PGS_RISING}	V_{FBS} rising	1.145	1.17	1.195	V
PGS falling threshold	$V_{PGS\_FALLING}$	V_{FBS} falling	1.05	1.075	1.1	V
Pre-charge current	$I_{PRE\text{-}CHARGE}$			150		mA
High-side MOSEFT (HS-FET) on resistance	$R_{DS(ON)\_HS}$			60		mΩ
Low-side MOSEFT (LS-FET) on resistance	$R_{DS(ON)\_LS}$			37		mΩ
Disconnect MOSFET on resistance	$R_{DS(ON)\_DIS}$			16		mΩ
Capacitor Health Detection						
Capacitor health detection discharge current	$I_{DISCHARGE}$	I^2C-configurable, PLP[7:6] = 11		20		mA
Thermal shutdown (6)	T_{SD}			150		°C
Thermal hysteresis (6)	T_{HYS}			25		°C
I^2C Interface						
High-level V_{IN}	V_{IH}		1.2			V
Low-level V_{IN}	V_{IL}				0.4	V
Input leakage current	I_{LKG_IN}			1		nA
Output leakage current	I_{LKG_OUT}			10		nA
Low-level output voltage	V_{OL}	10mA sink			0.3	V

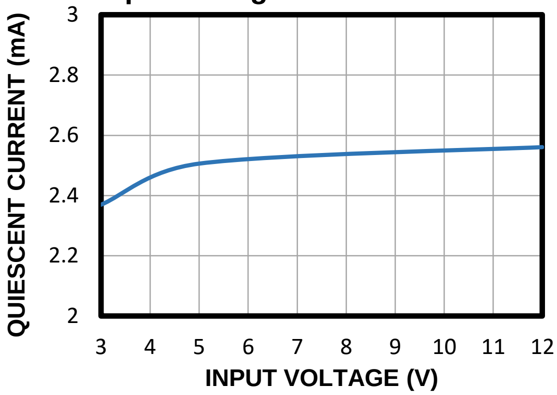
Note:

5) Guaranteed by over-temperature (OT) correlation. Not tested in production.
6) Guaranteed by engineering sample characterization. Not tested in production.

TYPICAL CHARACTERISTICS

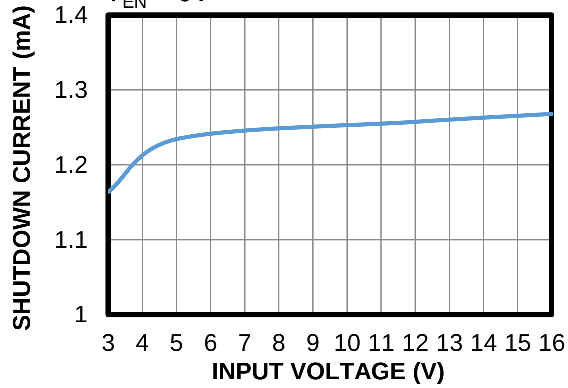
V_{IN} = 12V, V_{STRG} = 28V, V_{DET} = 8.4V, V_{BUS_RLS} = 8.6V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Quiescent Current vs. Input Voltage

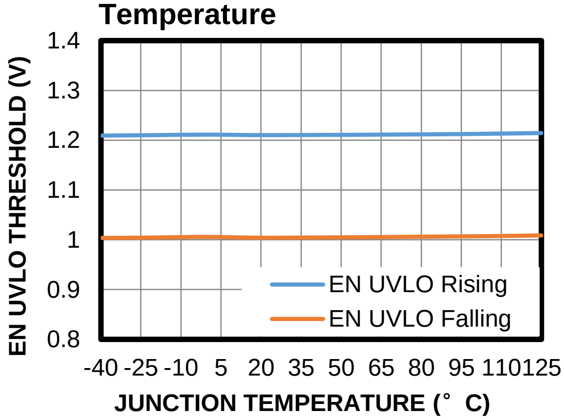


Shutdown Current vs. Input Voltage

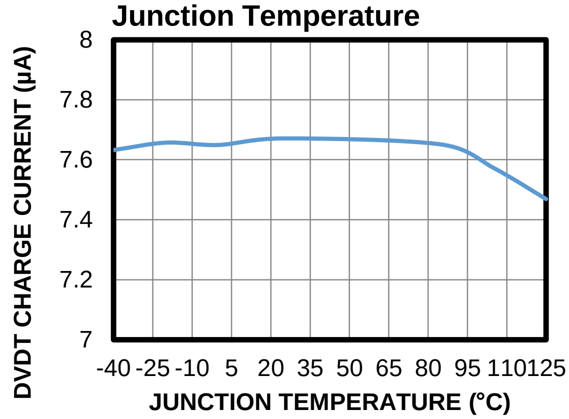
V_{EN} = 0V



EN UVLO Threshold vs. Junction Temperature

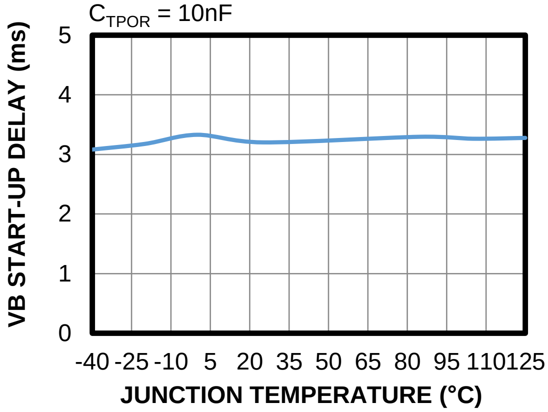


DVDT Charge Current vs. Junction Temperature

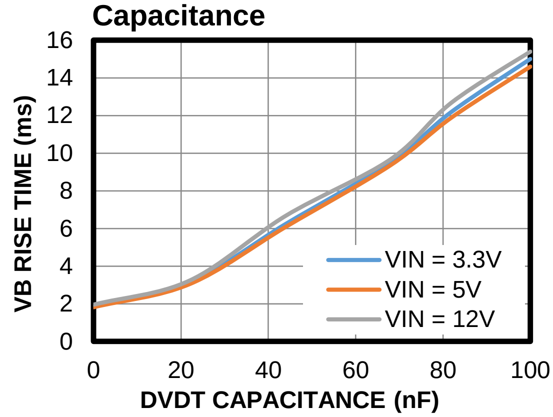


VB Start-Up Delay vs. Junction Temperature

C_{TPOR} = 10nF

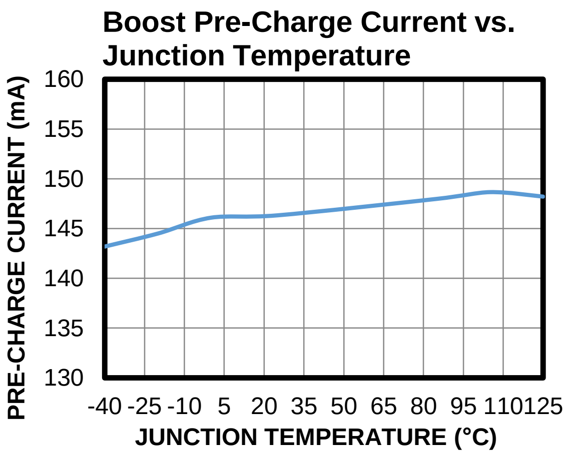


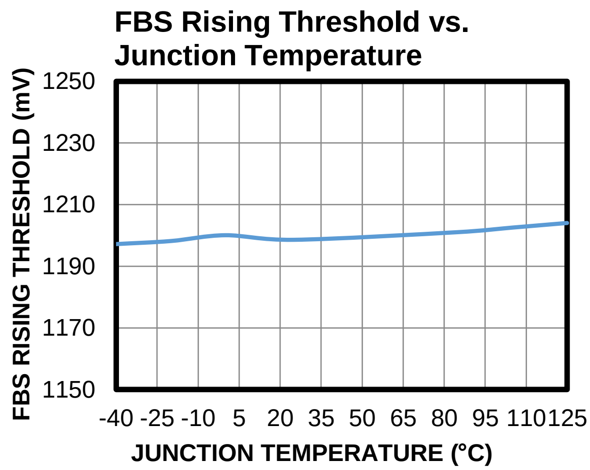
VB Rise Time vs. DVDT Capacitance

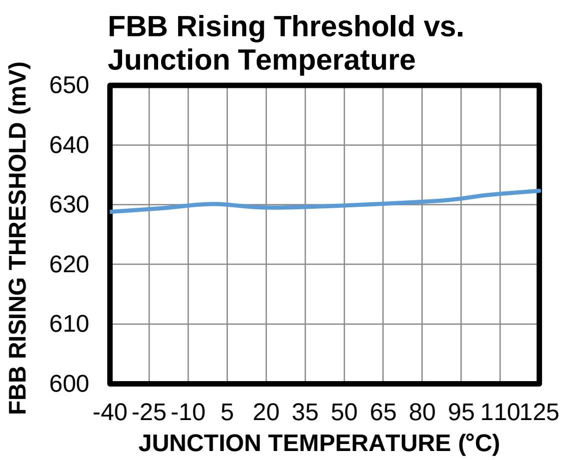


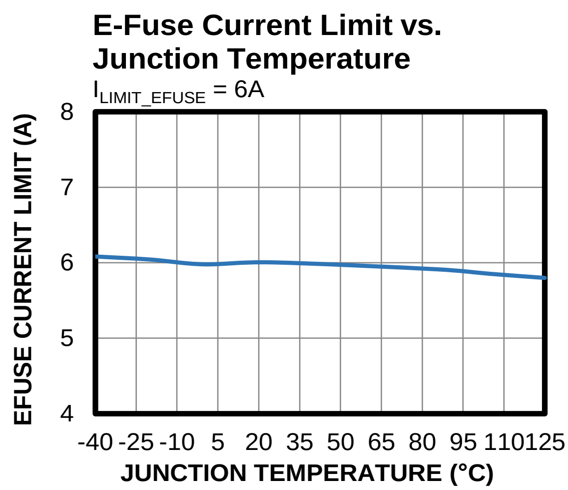
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{STRG} = 28V, V_{DET} = 8.4V, V_{BUS_RLS} = 8.6V, L = 1.5µH, T_A = 25°C, unless otherwise noted.





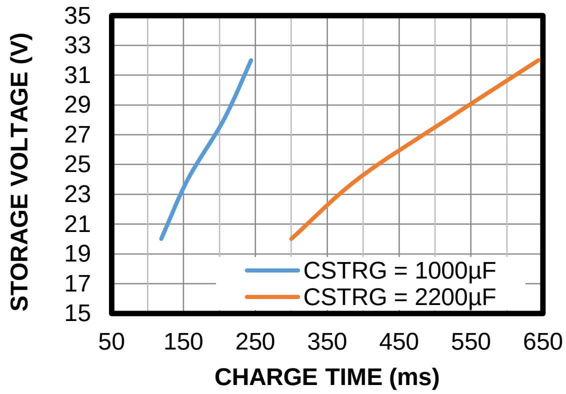




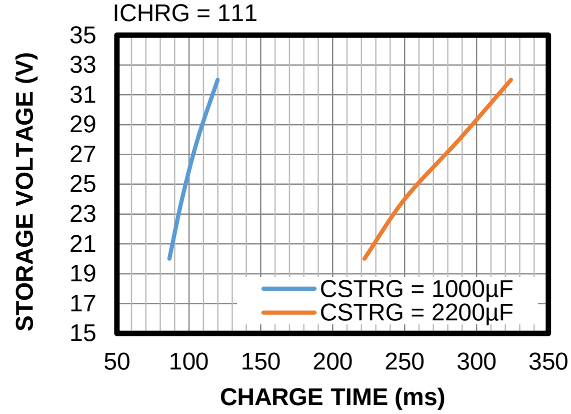
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{STRG} = 28V, V_{DET} = 8.4V, V_{BUS_RLS} = 8.6V, L = 1.5μH, T_A = 25°C, unless otherwise noted.

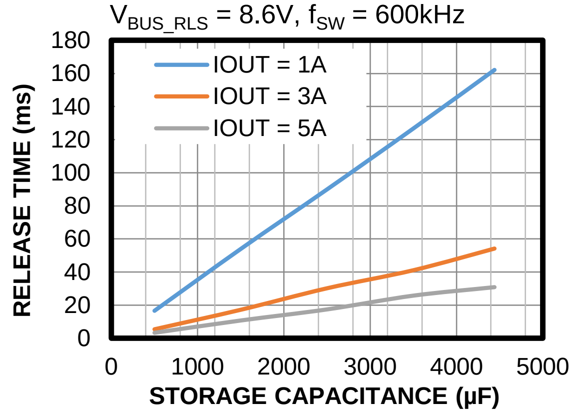
Storage Voltage vs. Charge Time
ICHRG = 001



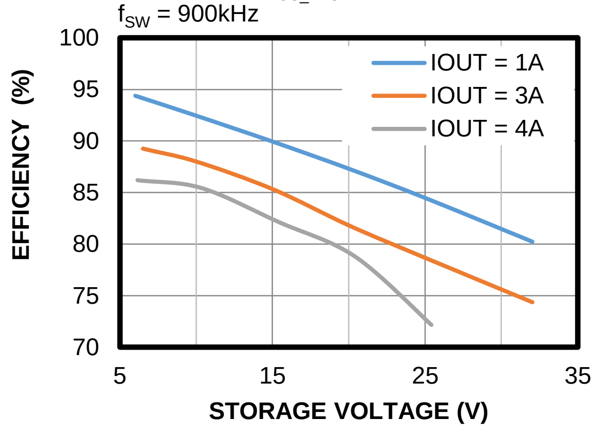
Storage Voltage vs. Charge Time
ICHRG = 111



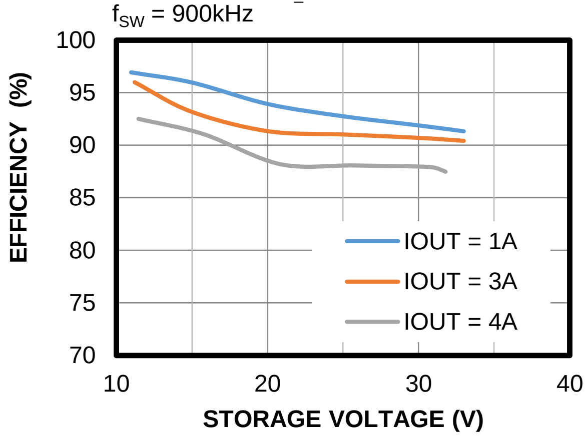
Release Time vs. Storage Capacitance
V_{BUS_RLS} = 8.6V, f_{SW} = 600kHz



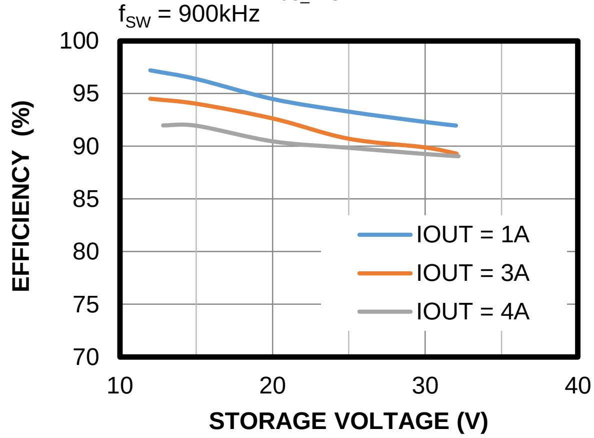
Efficiency vs. Storage Voltage
Buck mode, V_{BUS_RLS} = 3.3V, f_{SW} = 900kHz



Efficiency vs. Storage Voltage
Buck mode, V_{BUS_RLS} = 8.6V, f_{SW} = 900kHz



Efficiency vs. Storage Voltage
Buck mode, V_{BUS_RLS} = 10V, f_{SW} = 900kHz

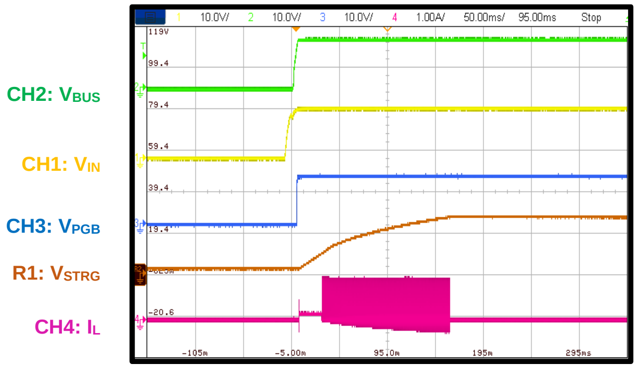


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{STRG} = 28V, V_{DET} = 8.4V, V_{BUS_RLS} = 8.6V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

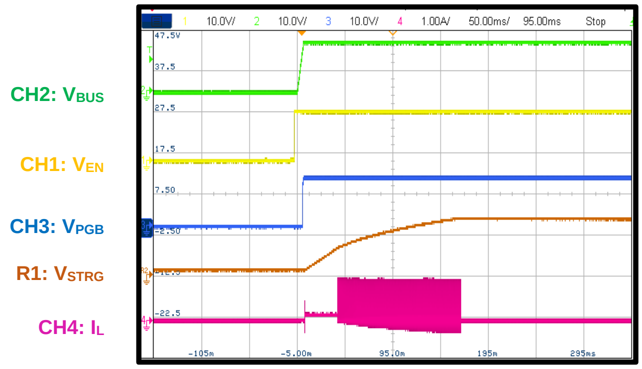
Start-Up through VIN

I_{BUS_LOAD} = 5A



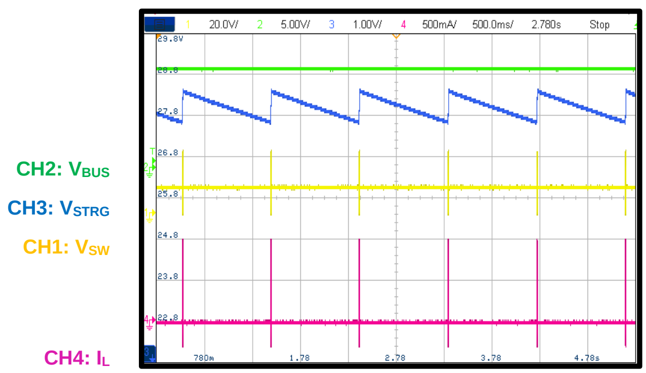
Start-Up through EN

I_{BUS_LOAD} = 5A



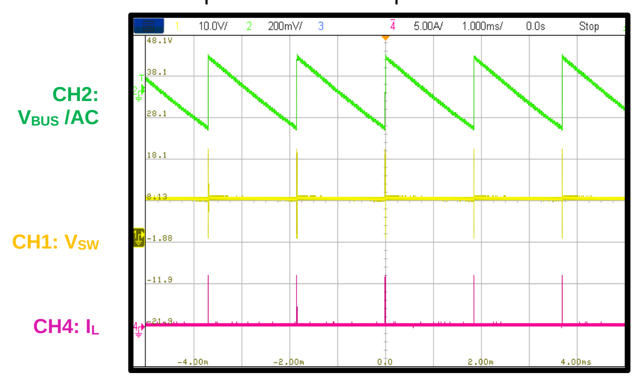
Boost Steady State

ICHRG = 001



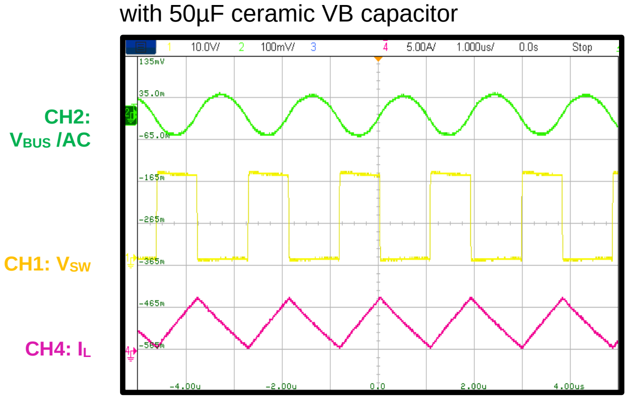
Buck Steady State

V_{STRG} = 20V, I_{BUS_LOAD} = 0A, f_{SW} = 600kHz, with 50µF ceramic VB capacitor



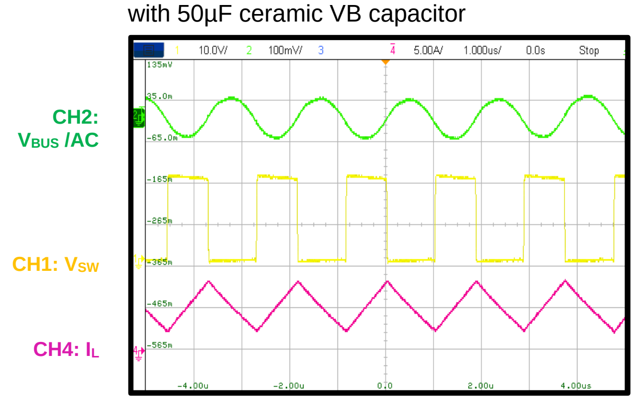
Buck Steady State

V_{STRG} = 20V, I_{BUS_LOAD} = 3A, f_{SW} = 600kHz, with 50µF ceramic VB capacitor



Buck Steady State

V_{STRG} = 20V, I_{BUS_LOAD} = 5A, f_{SW} = 600kHz, with 50µF ceramic VB capacitor

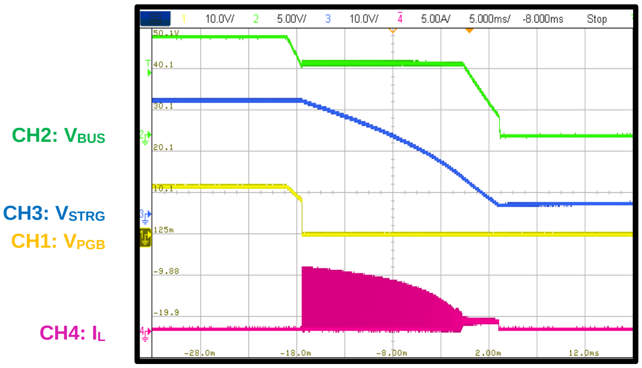


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{STRG} = 28V, V_{DET} = 8.4V, V_{BUS_RLS} = 8.6V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

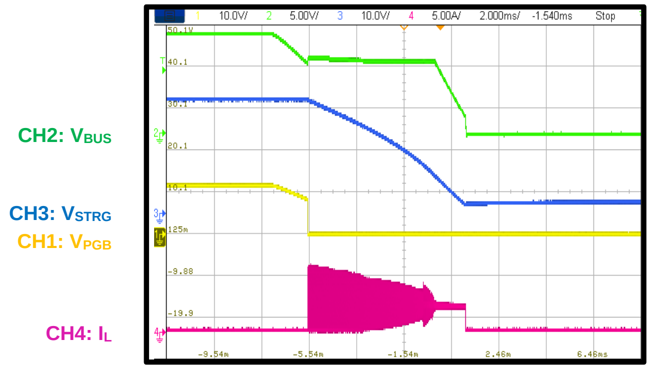
V_{STRG} Release

I_{BUS_LOAD} = 1A



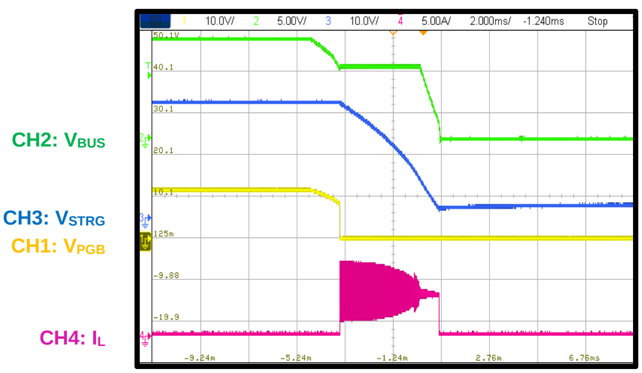
V_{STRG} Release

I_{BUS_LOAD} = 3A



V_{STRG} Release

I_{BUS_LOAD} = 5A



FUNCTIONAL BLOCK DIAGRAM

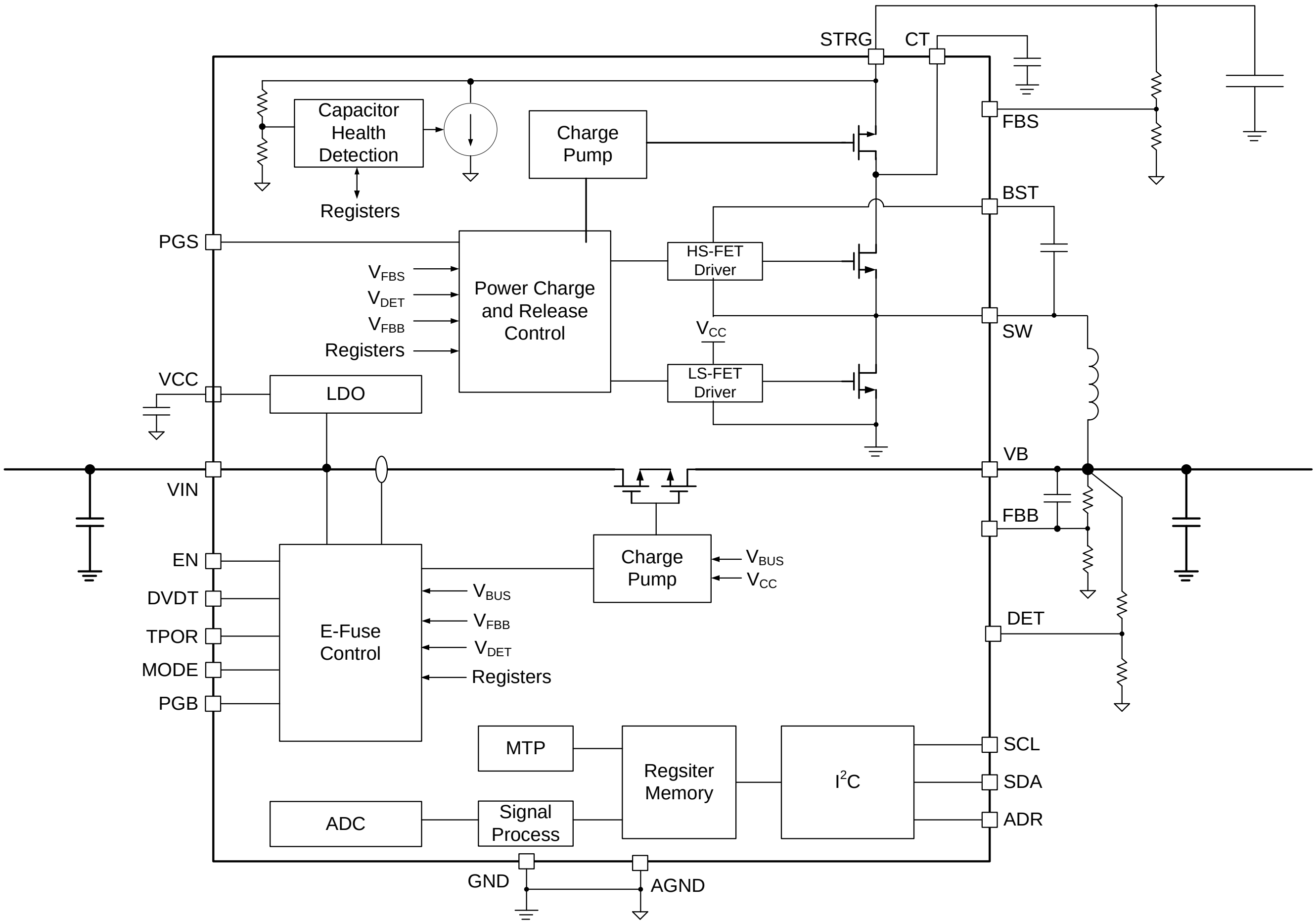


Figure 2: Functional Block Diagram

OPERATION

The MP5516 is a power loss protection power management IC (PMIC) that manages energy storage and release to back up data in solid state drives (SSDs) and other backup power supply applications. The integrated bi-directional DC/DC converter transfers energy between the system and the energy storage side with high efficiency. Constant-on-time (COT) control provides stable operation and fast dynamic response. The integrated reverse-blocking MOSEFT at the input prevents energy leakage while the input power source is removed or inserted with inverse polarity. The configurable input current limit (I_{LIMIT_E-FUSE}) and the bi-directional DC/DC converter achieve power path management for improved system dynamic load response. Three selectable over-voltage protection (OVP) thresholds are provided for applications with different input power sources.

The device features an internal I²C interface. The switching frequency (f_{SW}), I_{LIMIT_E-FUSE}, boost charge current (I_{CHARGE}), and other control parameters can be configured via the I²C. This reduces the number of external components required.

The MP5516 integrates a capacitor health detection. The capacitor health detection results are stored in the data registers for microcontroller unit (MCU) reading via the I²C interface.

I²C Address

The ADR pin sets the I²C slave address. Table 1 shows the ADR configurations for different I²C address settings.

Table 1: ADR Configurations for Different I²C Address Settings

ADR	High	Low	Floating
I²C Address	59h	5Ah	5Bh

MODE

The MODE pin sets the e-fuse under-voltage lockout (UVLO) protection threshold and the clamp voltage (V_{CLAMP}). Table 2 shows the MODE configurations for different UVLO and OVP thresholds.

Table 2: MODE Configurations for Different UVLO and OVP Thresholds

MODE	UVLO	OVP
High	3.5V	5.6V
Low	2.5V	3.7V
Floating	8.25V	13V

Enable (EN) Control

The enable (EN) pin and the EN bit start up the e-fuse and the bidirectional circuit. If both the EN pin and the EN bit are high, then the PMIC starts up.

Pull EN low to turn the e-fuse off and the buck release circuit on to support the downstream load.

E-Fuse Start-Up Reset Delay

The e-fuse features a start-up reset delay time. This delay time (t_{TPOR}) can be set via an external capacitor (C_{TPOR}) connected to the TPOR pin.

If C_{TPOR} is connected to TPOR, then C_{TPOR} is charged via an internal current source. t_{TPOR} can be estimated with Equation (1):

$$t_{TPOR}\ (ms) = 0.34 \times C_{TPOR}\ (nF) \qquad (1)$$

If there is not an external capacitor connected to the TPOR pin, then t_{TPOR} is set to the internal default value (1.4ms). If t_{TPOR} is below 1.4ms with an external capacitor connected to TPOR, then t_{TPOR} remains 1.4ms.

Bus Voltage (V_{BUS}) Rising Slew Rate Control

The e-fuse employs V_{BUS} soft start (SS) to prevent input inrush current from flowing between the VIN and VB pins. This soft-start time (t_{DVDT}) can be set via an external capacitor (C_{DVDT}) connected to the DVDT pin.

If C_{DVDT} is connected to DVDT, then C_{DVDT} is charged via an internal current source (7.2µA).

t_{DVDT} can be estimated with Equation (2):

$$t_{DVDT}(ms) = 0.14 \times C_{DVDT}(nF) \qquad (2)$$

If there is not an external capacitor connected to DVDT, then t_{DVDT} is set to the internal default value (2ms).

Internal Blocking MOSFET

There is an internal blocking MOSFET between the bidirectional converter's high side MOSFET (HS-FET) and the STRG pin. The blocking MOSFET limits the current flowing between the VB and STRG pins during the pre-charge period. The CT pin connects the blocking MOSFET and the HS-FET. Connect a capacitor to CT to stabilize the pre-charge loop. The voltage rating of this capacitor should exceed the storage voltage (V_{STRG}).

Internal LDO Output (VCC)

The VCC pin powers the PMIC's internal circuitry. VCC is supplied by an internal 5V LDO from V_{IN} or V_{STRG}. Use a ⩾1µF decoupling capacitor to decouple VCC.

Buck Release Mode Detection

If the DET pin voltage (V_{DET}) drops below 0.6V, then the bidirectional converter operates in buck release mode. The resistor divider connected to DET sets the V_{BUS} detection threshold. See the Application Information section on page 27 for more details.

Buck Release Mode Regulation

If the PMIC is operating in buck release mode, then the regulation voltage (V_{BUCK_RLS}) is set by the resistor divider connected to the FBB pin. If both the FBB pin voltage (V_{FBB}) and the DET pin voltage (V_{DET}) exceed 0.63V, then the PMIC enters boost charge mode. See the Application Information section on page 27 for more details.

Boost Charge Mode Regulation

If the PMIC is operating in boost charge mode, then V_{STRG} is set by the resistor divider connected to the FBS pin. See the Application Information section on page 27 for more details.

V_{BUS} Power Good Indication (PGB)

If V_{DET} drops below 0.6V, then the PGB pin is pulled low to indicate a power failure. The MP5516 exists boost charge mode, and enters buck release mode. If both V_{DET} and V_{FBB} exceed 0.63V, then PGB is pulled high via an external pull-up resistor.

Storage Voltage (V_{STRG}) Power Good Indication (PGS)

The PGS pin indicates the PG indicator for V_{STRG}. If the FBS pin voltage (V_{FBS}) exceeds 1.17V, then PGS is pulled high. If V_{FBS} drops below 1.08V, then PGS is pulled low.

Start-Up Sequence

Once V_{IN} exceeds its UVLO rising threshold, the EN bit in register 01h (EFUSE) is set to 1, and the EN pin is pulled high. The e-fuse turns on once t_{TPOR} has elapsed. Once t_{TPOR} is complete, the e-fuse initiates a V_{BUS} SS. The CT capacitor (C_{CT}) is also charged during t_{DVDT}.

If the ENCH bit in register 02h (PLP) is set to 1, and V_{BUS} exceeds the pre-charge threshold, then the pre-charge period starts after the charge delay time. The STRG capacitor (C_{STRG}) is charged by the pre-charge current via the disconnect MOSET.

Pre-charging ends once the disconnect MOSET voltage exceeds its internal threshold. Then the start-up through the disconnect MOSFET is complete, and C_{STRG} is charged in boost mode. Figure 3 shows the start-up sequence.

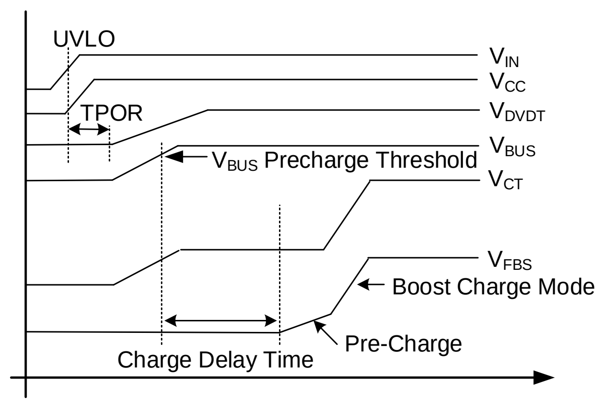


Figure 3: Start-Up Sequence

If any of the following occur, then the e-fuse turns off:

- V_{IN} drops below its UVLO threshold
- The EN bit is 0
- The EN pin is pulled to ground
- The PMIC is operating in buck release mode

Boost Charge Mode

The bidirectional converter starts up once the pre-charge period is complete and both V_{DET} and V_{FBB} have exceeded 0.63V. Then the PMIC enters boost charge mode to charge C_{STRG}.

The MP5516 operates in burst mode to minimize the converter's power loss. If V_{FBS} drops below 1.17V, then the PMIC enters burst charge mode to charge C_{STRG}. Once C_{STRG} is charged and V_{FBS} is 1.2V, then the converter stops switching and V_{STRG} is released slowly.

During boost charge mode, the converter's peak charge current (I_{CHARGE_PEAK}) can be controlled via the I^2C. I_{CHARGE_PEAK} can be configured via the ICHRG bits in register 02h.

Constant-on-time (COT) control is employed in boost charge mode. f_{SW} can be configured via the FSW bits in register 06h (STRG).

Figure 4 shows boost charge mode.

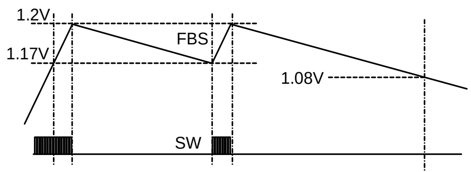


Figure 4: Boost Charge Mode

The MP5516 provides OVP for V_{STRG}. If V_{FBS} exceeds 114% of the reference voltage (V_{REF}), then the boost converter shuts down until the storage voltage V_{STRG} drops to a set value.

Buck Release Mode

If the power fails, then the PMIC enters buck release mode to support the system power via the storage energy.

V_{DET} determines the power failure threshold. If V_{DET} drops below 0.6V, then a power failure has occurred and PGB is pulled low. The e-fuse turns off and the bidirectional converter transitions from boost charge mode to buck release mode.

COT control is employed in buck release mode. f_{SW} can be configured via the FSW bits in register 06h. The regulated V_{BUCK_RLS} can be configured via the FBB resistor divider.

Output Clamp Voltage (V_{CLAMP}) and Over-Voltage Protection (OVP)

The MODE pin sets the clamp voltage (V_{CLAMP}) threshold. Table 3 shows the clamp voltages for different V_{IN} applications.

Table 3: V_{CLAMP} for Different Input Voltages

V_{IN}	V_{CLAMP}
3.3V	3.7V
5V	5.6V
12V	13V

The output OVP thresholds (V_{OUT_OVP}) slightly exceed the V_{CLAMP} thresholds. Table 4 shows the OVP thresholds for different input voltages.

Table 4: V_{OUT_OVP} for Different Input Voltages

V_{IN}	V_{OUT_OVP}
3.3V	3.9V
5V	6V
12V	13.8V

If V_{BUS} exceeds V_{OUT_OVP}, then the clamping circuit pulls V_{BUS} to V_{CLAMP}. The clamping circuit releases once V_{IN} drops below V_{CLAMP}. Figure 5 shows the output V_{CLAMP} function.

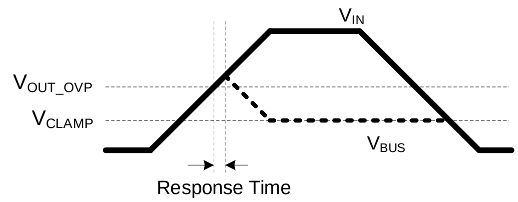


Figure 5: Output Voltage Clamping

Input Current Limit (I_{LIMIT_E-FUSE})

The e-fuse input current (I_{IN}) is sensed internally. The input current limit (I_{LIMIT_E-FUSE}) is set by the ILIM_EFUSE bits in register 01h.

Reverse Current Blocking

The e-fuse employs reverse current blocking to prevent reverse current flow. If the reverse current flowing between the VB and VIN pins is triggered, then the input switch turns off.

Current-Limit Buck

If V_{FBB} drops below V_{REF} once I_{LIMIT_E-FUSE} is triggered, then the PMIC enters buck release mode to support the extra load current (I_{LOAD}). If triggering I_{LIMIT_E-FUSE} enables buck release mode, then the PMIC exits buck release mode once the release time reaches the value set by the MAX_RLS_TIMER_CLBK bits in register 14h (PLP_CTRL4) or once V_{FBS} drops below V_{REF} x VS_TH_CLBK.

Over-Current Protection (OCP) during Buck Release Mode

If COT control is used for the buck converter, then the HS-FET on-time (t_{ON_HS}) is fixed. This prevents current runaway while the HS-FET is on. The MP5516 employs valley current limiting for the low-side MOSFET (LS-FET) during buck release mode.

The LS-FET current (I_{LS}) is sensed during the LS-FET on time (t_{ON_LS}). The HS-FET does not turn on unless I_{LS} is below the valley current limit (I_{LIMIT_VALLEY}). This function can be used to limit I_{LOAD} in the case of a change in the load or an output short. Valley current limiting prevents current runaway, and protects the system from over-current (OC) stress.

Figure 6 shows the valley current limiting function.

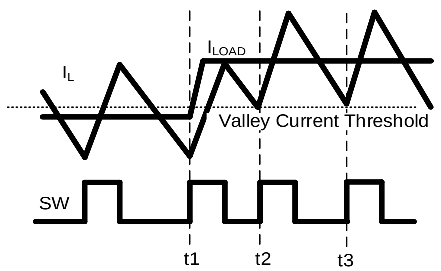


Figure 6: Valley Current Limiting

I_{LOAD} increases at t1. To support the additional current, the inductor current (I_L) ramps up according to the shorter HS-FET off time (t_{OFF_HS}) after a fixed t_{ON}. The HS-FET does not turn on again until I_{LS} reaches the I_{LIMIT_VALLEY}.

VB Short Circuit Protection (SCP)

If short circuit on VB occurs, then buck release mode is triggered to discharge the storage capacitors. C_{STRG} discharges with a maximum current until V_{STRG} is not sufficient for the PMIC to operate in buck release mode. The e-fuse limits I_{IN} at a set level. If the internal junction temperature (T_J) exceeds 150°C, then the part shuts down.

STRG SCP

The MP5516 provides SCP for STRG. If V_{STRG} does not exceed 0.7V in pre-charge mode after a set time, then the disconnect MOSFET turns off and the bidirectional converter latches off. The MP5516 also features a fast-off function. If the current flowing from the CT to STRG exceeds 6A, then the fast-off function is triggered. This function protects the bidirectional converter from shorts on the STRG pin.

STRG Open-Circuit Protection

The MP5516 provides open-circuit protection for STRG. If V_{STRG} reaches the set value before the configured timer is complete, then C_{STRG} is considered “open.” The STRG_OPEN bit in register 09h (STATUS) is set to 1 to indicate that the storage capacitor is open.

Capacitor Health Detection

The capacitor health detection function is active once the rising edge of the CAP_EN bit in register 06h is detected. Figure 7 shows a capacitor health test.

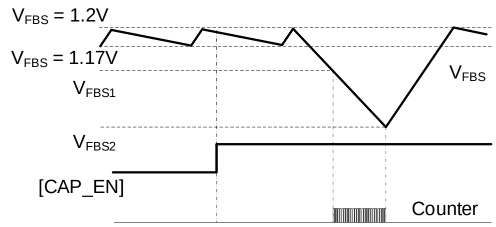


Figure 7: Capacitor Health Test

The internal discharge current ($I_{DISCHARGE}$) discharges C_{STRG}. An internal 500Hz discharge timer calculates the discharge time ($t_{DISCHARGE}$). As shown in Figure 7, the timer starts once V_{STRG} = V_{STRG1}, and ends once V_{STRG} reaches V_{STRG2}; therefore, C_{STRG} stops discharging once V_{STRG} = V_{STRG2}. Then C_{STRG} is charged back to the set value.

$t_{DISCHARGE}$ is stored in register 07h (TIMER1) and register 08h (TIMER2). TIMER1 stores the higher 8 bits, and TIMER2 stores the lower 8 bits.

Ensure that V_{STRG1} and V_{STRG2} are set properly. If the initial storage voltage is V_{STRG1}, then its corresponding V_{FBS} should be below 1.17V. Set V_{STRG2} below V_{STRG1}, but high enough to prevent excessive C_{STRG} discharge during a capacitor health test.

C_{STRG} can be calculated with Equation (3):

$$C_{STRG} = I_{DISCHARGE} \times t_{DISCHARGE} / (V_{STRG1} - V_{STRG2}) \quad (3)$$

Set the CAP_EN bit to 0 in register 06 (STRG) before the next capacitor health detection.

Thermal Shutdown

The MP5516 monitors the die temperature internally to prevent the PMIC from operating at exceedingly high temperatures. If the die temperature exceeds the thermal shutdown threshold (typically 150°C), then the PMIC shuts down. The thermal warning threshold is about 120°C. Once the temperature drops below about 125°C, the PMIC starts up and resumes normal operation.

I²C INTERFACE

I²C Serial Interface

The I²C is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. A master device connected to the line generates the SCL signal and device address to arrange the communication sequence.

The MP5516 interface is an I²C slave, which supports both fast mode (400kHz) and high-speed mode (3.4MHz). The I²C interface adds flexibility to the power supply solution. The output voltage (V_{OUT}), transition slew rate, and other parameters can be controlled instantaneously via the I²C interface. If the master sends an 8-bit value, then the 7-bit address should be followed by a 0 or 1 to indicate a write or read operation, respectively.

Start and Stop Conditions

Start (S) and stop (P) conditions are signaled by the master device, which signifies the beginning and end of the I²C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 8).

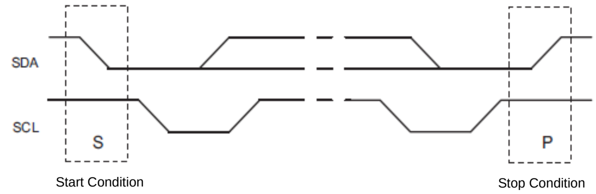


Figure 8: Start and Stop Conditions

The master generates the SCL clocks, then transmits the device address and the read/write direction bit (R/W) on the SDA line.

Transfer Data

Data is transferred in 8-bit bytes by the SDA line. Each byte of data must be followed by an acknowledge (ACK) bit.

I²C Update Sequence

The MP5516 requires a start condition, valid I²C address, register address byte, and data byte for a single data update. The MP5516 acknowledges each byte that has been received by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP5516. The MP5516 performs an update on the falling edge of the LSB byte. Figure 9, Figure 10, and Figure 11 show examples of I²C write and read sequences.

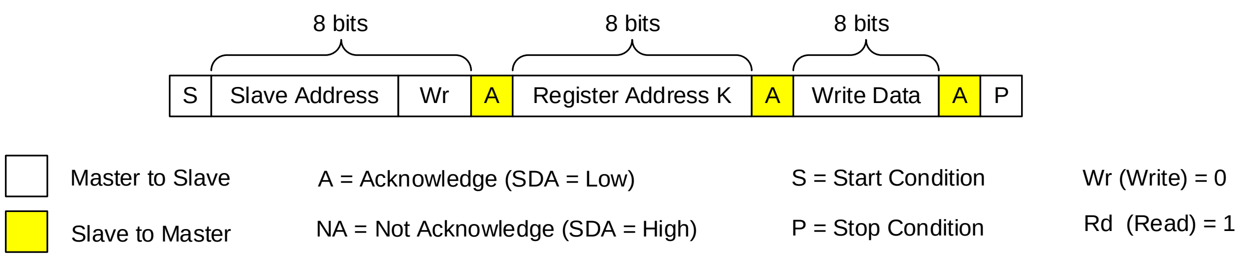


Figure 9: I²C Write Example (Write Single Register)

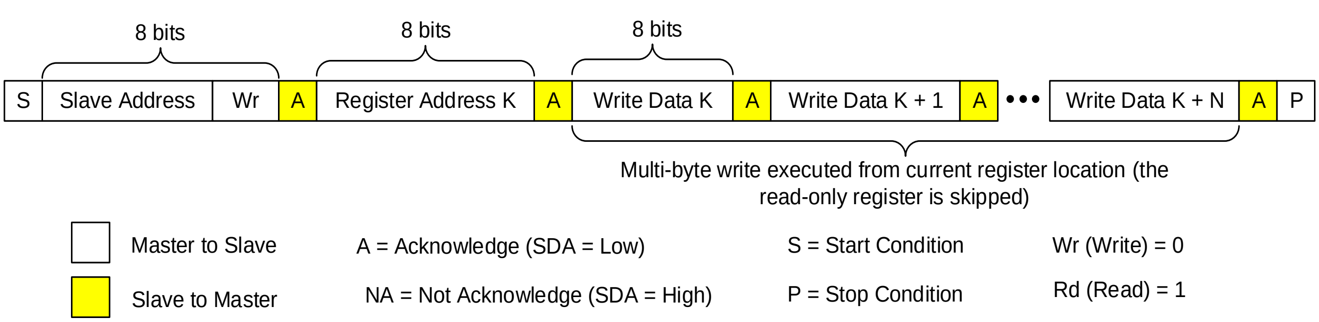


Figure 10: I²C Write Example (Write Multi-Register)

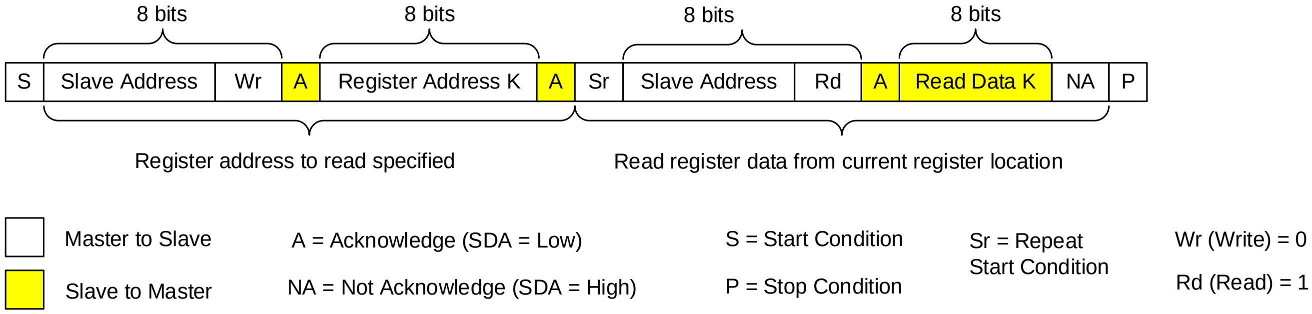


Figure 11: I²C Read Example (Read Single Register)

MTP E-FUSE DESCRIPTIONS AND DEFAULT VALUES (MP5516-0000)

Table 5: MTP E-Fuse Default Values

Function	Bit #	Description	Default
ILIM_E-FUSE	3	E-fuse current limit	111 (6A)
EN	1	Enable e-fuse	1 (e-fuse is enabled)
IDIS_CAP_TEST	2	Discharge current during capacitor health detection	11 (20mA)
ICHRG	3	Peak inductor current (I_{CHARGE_PEAK}) during boost charge mode	001 (0.85A)
ENCH	1	Enable boost charge mode	1 (boost charge mode is enabled)
VSTRG1	8	The initial storage to start capacitor test	01000110 (10.5V)
VSTRG2	8	The final storage to stop capacitor test	00101111 (7.05V)
PGS_MODE	1	Storage voltage power good (PG) indication	0 (PGS is pulled low if V_{FBS} drops below 1.08V)
CAP_EN	1	Enable capacitor health detection	0 (capacitor health detection is disabled)
FSW	2	PLP converter switching frequency (f_{SW})	01 (600kHz)
ADC_EN	1	Enable analog-to-digital converter (ADC)	1 (ADC is enabled)
CLBK_EN	1	Enable current-limit buck	0 (current-limit buck is enabled)
CAP_OPEN_TH	4	Storage voltage capacitor (C_{STRG}) open timer threshold	1111 (12ms max)

I^2C REGISTER MAP

Register Map

Address	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00h	MTP	R/W	Reserved (7)					MTP Write Status	Reserved (7)	MTP Write Control
01h	EFUSE	R/W	Reserved (7)		ILIM_EFUSE			Reserved (7)		EN
02h	PLP	R/W	IDIS_CAP_TEST		Reserved (7)		ICHRG			ENCH
04h	VSTRG1	R/W	VSTRG1							
05h	VSTRG2	R/W	VSTRG2							
06h	STRG	R/W	PGS_MODE	Reserved (7)	CAP_EN	Reserved (7)	Reserved (7)		FSW	
07h	TIMER1	R	TIMER1							
08h	TIMER2	R	TIMER2							
09h	STATUS	R/W	ILIM	OV	CAP_TEST_SET_ERR	OT	PGB	PGS	STRG_OPEN	Reserved (7)
0DH	VIN_ADC	R	VIN_ADC							
0EH	IIN_ADC	R	IIN_ADC							
0FH	EFUSE_CTRL1	R/W	Reserved (7)			ADC_EN	Reserved (7)			
13H	PLP_CTRL3	R/W	Reserved (7)							CLBK_EN
14H	PLP_CTRL4	R/W	MAX_RLS_TIMER_CLBK						VS_TH_CLBK	
16H	CAP_CTRL2	R/W	Reserved (7)				CAP_OPEN_TH			

Notes:

7) Reserved bits. Do not write different values to these bits.

Register 00h (MTP)

Name	Bits	Description	Default Value
MTP write status	D[2]	This bit should be set to 0 before writing data to the MTP. 0: MTP write is free 1: MTP write is busy	Read only
MTP write control	D[0]	If this bit is set to 1, then all I^2C register data is written to the MTP. Reserved data in the MTP is loaded to the I^2C registers during start-up. 0: MTP write is disabled (default) 1: MTP write is enabled	0

Register 01h (E-FUSE)

Name	Bits	Description	Default Value
ILIM_EFUSE	D[5:3]	These bits set the e-fuse current limit (I_{LIMIT_E-FUSE}). 000: 1.2A 001: 2A 010: 2.5A 011: 3A 100: 3.5A 101: 4A 110: 4.5A 111: 6A (default)	111
EN	D[0]	This bit enables the e-fuse. 0: E-fuse is disabled 1: E-fuse is enabled (default)	1

Register 02h (PLP)

Name	Bits	Description	Default Value
IDIS_CAP_TEST	D[7:6]	These bits set the discharge current ($I_{DISCHARGE}$) during capacitor health detection. 00: 2mA 01: 5mA 10: 10mA 11: 20mA (default)	11
ICHRG	D[3:1]	These bits set the peak inductor current (I_{CHARGE_PEAK}) during boost charge mode. 000: 0.6A 001: 0.85A (default) 010: 1.1A 011: 1.35A 100: 1.6A 101: 1.85A 110: 2.1A 111: 2.35A	001
ENCH	D[0]	This bit enables boost charge mode. 0: Boost charge mode is disabled 1: Boost charge mode is enabled (default)	1

Register 04h (VSTRG1)

Name	Bits	Description	Default Value
VSTRG1	D[7:0]	These bits set the initial storage voltage (V_{STRG}) to start the capacitor test. If the capacitor test is enabled, then the 500Hz timer starts counting once V_{STRG} drops to V_{STRG1}. 00001010: 1.5V (minimum) 01000110: 10.5V (default) 11110000: 36V (maximum) … 0.15V per step	01000110

Register 05h (VSTRG2)

Name	Bits	Description	Default Value
VSTRG2	D[7:0]	These bits set the final V_{STRG} to stop the capacitor test. If the capacitor test is enabled, then the 500Hz timer stops counting once V_{STRG} drops to V_{STRG2}. (May have variation when the counter stops.) 00001010 = 1.5V (minimum) 00101111: 7.05V (default) 11110000 = 36V (maximum) … 0.15V per step	00101111

Register 06h (STRG)

Name	Bits	Description	Default Value
PGS_MODE	D[7]	This bit sets the PGS trigger mode threshold. 0: If the FBS voltage (V_{FBS}) drops below 1.08V, then PGS is pulled low (default) 1: If either V_{FBS} drops below 1.08V or C_{STRG} open is detected, then PGS is pulled low	0
CAP_EN	D[5]	Capacitor health detection starts once the CAP_EN rising edge is detected. The microcontroller unit (MCU) can start capacitor health detection by setting this bit to 1. 0: Capacitor health detection is disabled (default) 1: Capacitor health detection is enabled	0
FSW	D[1:0]	These bits set the switching frequency (f_{SW}) in both boost charge mode and buck release mode. 00: 300kHz 01: 600kHz (default) 10: 900kHz 11: 1.2MHz	01

Register 07h (TIMER1)

Name	Bits	Description	Default Value
TIMER1	D[7:0]	These are the first 8 bits of the capacitor health detection discharge timer (500Hz).	00000000

Register 08h (TIMER2)

Name	Bits	Description	Default Value
TIMER2	D[7:0]	These are the last 8 bits of the capacitor health detection discharge timer (500Hz).	00000000

Register 09h (STATUS)

Name	Bits	Description	Default Value
ILIM	D[7]	0: I_{LIMIT_E-FUSE} has not been triggered (default) 1: I_{LIMIT_E-FUSE} has been triggered	0
OV	D[6]	0: Over-voltage protection (OVP) has not been triggered (default) 1: OVP has been triggered	0
CAP_TEST_SET_ERR	D[5]	0: V_{STRG1} and V_{STRG2} are set at the correct values (e.g. V_{STRG1} is below the V_{STRG} regulation voltage, and exceeds V_{STRG2}) (default) 1: V_{STRG1} and V_{STRG2} are set at incorrect values (e.g. V_{STRG1} exceeds the V_{STRG} regulation voltage, or V_{STRG2} exceeds V_{STRG1})	0
OT	D[4]	0: Die temperature < 150°C (default) 1: Die temperature > 150°C	0
PGB	D[3]	0: PGB is pulled logic high (default) 1: PGB is pulled logic low	0
PGS	D[2]	0: PGS is pulled logic high (default) 1: PGS is pulled logic low	0
STRG_OPEN	D[1]	0: C_{STRG} is not open (default) 1: C_{STRG} is open	0

Register 0Dh (VIN)

Name	Bits	Description	Default Value
VIN_ADC	D[7:0]	These bits monitor the ADC input voltage (V_{IN}). If CAP_EN is enabled, then VIN_ADC is disabled. V_{IN}(mV) = VIN_ADC x LSB, LSB = 50mV	00000000

Register 0Eh (IIN)

Name	Bits	Description	Default Value
IIN_ADC	D[7:0]	These bits monitor the ADC input current (I_{IN}). If CAP_EN is enabled, then IIN_ADC is disabled. I_{IN}(mA) = IIN_ADC x LSB The ILIM_EFUSE bits (D[5:3]) in register 01h determine the LSB value. The ILIM_EFUSE settings and their corresponding LSB values are listed below: • If ILIM_EFUSE is 000, then LSB is 8mA • If ILIM_EFUSE is 001, then LSB is 13.33mA • If ILIM_EFUSE is 010, then LSB is 16.67mA • If ILIM_EFUSE is 011, then LSB is 20mA • If ILIM_EFUSE is 100, then LSB is 23.33mA • If ILIM_EFUSE is 101, then LSB is 26.67mA • If ILIM_EFUSE is 110, then LSB is 30mA • If ILIM_EFUSE is 111, then LSB is 40mA	00000000

Register 0Fh (EFUSE_CTRL1)

Name	Bits	Description	Default Value
ADC_EN	D[4]	This bit enables the ADC. The ADC V_{STRG} is not controlled by this bit. 0: The ADC is disabled 1: The ADC is enabled (default) A password is required to activate the ADC_EN function. Write the following to register F0h: 0x56, 0xE3, 0x5A, and 0xAC. Then read register F0h. If register F0h is 0x13, then ADC_EN can be configured.	1

Register 13h (PLP_CTRL3)

Name	Bits	Description	Default Value
CLBK_EN	D[0]	This bit enables CLBK once I_{LIMIT_E-FUSE} has been triggered. 0: If I_{LIMIT_E-FUSE} is triggered and the FBB pin voltage (V_{FBB}) drops to the reference voltage (V_{REF}), then CLBK is disabled (default) 1: If I_{LIMIT_E-FUSE} is triggered and the FBB pin voltage (V_{FBB}) drops to the reference voltage (V_{REF}), then CLBK is enabled A password is required to activate the CLBK_EN function. Write the following to register F0h: 0x56, 0xE3, 0x5A, and 0xAC. Then read register F0h. If register F0h is 0x13, then CLBK_EN can be configured.	0

Register 14h (PLP_CTRL4)

Name	Bits	Description	Default Value
MAX_RLS_ TIMER_CLBK	D[7:2]	These bits set the release timer. If triggering I_{LIMIT_E-FUSE} enables CLBK, then the PMIC exits CLBK once the release timer reaches its configured value. 000000: 0.1ms (minimum) 010000: 1.6ms (default) 111111: 6.4ms (maximum) A password is required to activate the MAX_RLS_TIMER_CLBK function. Write the following to register F0h: 0x56, 0xE3, 0x5A, and 0xAC. Then read register F0h. If register F0h is 0x13, then MAX_RLS_TIMER_CLBK can be configured.	010000
VS_TH_CLBK	D[1:0]	If triggering I_{LIMIT_E-FUSE} enables CLBK, then the PMIC exits buck release mode once V_{FBS} drops below V_{REF} x VS_TH_CLBK. 00: 95% (default) 01: 92.5% 10: 90% 11: 87.5% A password is required to activate the MAX_RLS_TIMER_CLBK function. Write the following to register F0h: 0x56, 0xE3, 0x5A, and 0xAC. Then read register F0h. If register F0h is 0x13, then VS_TH_CLBK can be configured.	00

Register 16h (CAP_CTRL2)

Name	Bits	Description	Default Value
CAP_OPEN_TH	D[3:0]	These bits set the C_{STRG} open timer threshold. If V_{STRG} reaches its set value before the timer is complete, then C_{STRG} is considered “open”. 0000 = 0ms (minimum) … 1111 = 12ms (maximum) (default) 0.8ms per step A password is required to activate the MAX_RLS_TIMER_CLBK function. Write the following to register F0h: 0x56, 0xE3, 0x5A, and 0xAC. Then read register F0h. If register F0h is 0x13, then CAP_OPEN_TH can be configured.	1111

APPLICATION INFORMATION

Setting the Storage Voltage (V_{STRG})

V_{STRG} can be set by the FBS resistor divider (see Figure 12).

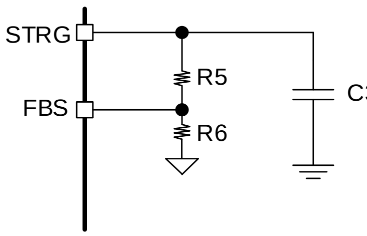


Figure 12: V_{STRG} Feedback Circuit

V_{STRG} can be calculated with Equation (4):

$$V_{STRG} = (1 + \frac{R_5}{R_6}) \times V_{REF} \quad (4)$$

Where V_{REF} is 1.2V.

The R5 and R6 values are selected based on the application requirement. Typically, a larger R5 and R6 provide a lower leakage current, which is desired in most designs.

Setting the Buck Release Mode Regulation Voltage

In buck release mode, the release voltage (V_{BUS_RLS}) is regulated by the FBB resistor divider (see Figure 13).

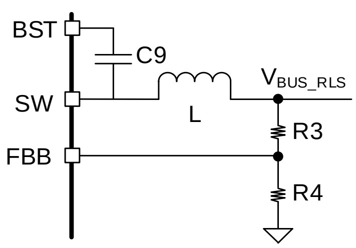


Figure 13: Release Feedback Circuit

V_{BUS_RLS} can be calculated with Equation (5):

$$V_{BUS\_RLS} = (1 + \frac{R_3}{R_4}) \times V_{REF} \quad (5)$$

Where V_{REF} is 0.6V.

It is recommended that the sum of R3 and R4 be between 10kΩ and 200kΩ.

Setting the Power Failure Threshold

The VB thresholds to trigger buck release mode are set by the DET resistor divider (see Figure 14).

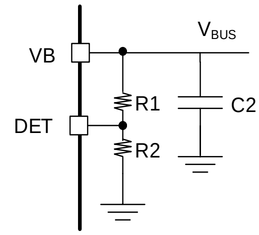


Figure 14: Power Failure Threshold Feedback Circuit

The power failure threshold (V_{BUS_PFI}) can be calculated with Equation (6):

$$V_{BUS\_PFI} = (1 + \frac{R_1}{R_2}) \times V_{REF} \quad (6)$$

Where V_{REF} is 0.6V.

It is recommended that the sum of R1 and R2 be between 10kΩ and 200kΩ.

Setting the E-Fuse Input Current Limit

The input current limit of the e-fuse is set via I^2C interface. See the Register 01h (E-FUSE) section on page 23 for more details.

Setting the Bus Voltage Rise Time

Connect a capacitor to the DVDT pin to control the V_{BUS} rising slew rate during start-up. See Equation 2 on page 15 to calculate the rise time during soft start (SS).

Selecting the Storage Capacitor (C_{STRG})

C_{STRG} stores energy during normal operation, and releases this energy to VB during an input power loss. General-purpose electrolytic capacitors or low-profile POS capacitors are used for most applications. The voltage rating of C_{STRG} should exceed 20% of the target V_{STRG}.

The capacitance reduction with the DC voltage offset should also be considered. Different capacitors have different voltage derating performances. Choose a capacitor with a high enough voltage rating to guarantee the capacitance.

The required capacitance is determined by the length of the dying gasp (t_{DASP}) of the application. The required storage capacitance (C_{STRG}) can be calculated with Equation (7):

$$C_{STRG} = \frac{2 \times V_{BUS\_RLS} \times I_{RLS} \times \tau_{DASP}}{(V_{STRG}^2 - V_{BUS\_RLS}^2) \times Eff} \quad (7)$$

Where I_{RLS} is the bus release current while V_{BUS} is regulated at V_{BUS_RLS} in buck release mode, t_{DASP} is the dying gasp, and Eff is the energy-release efficiency in buck release mode.

Consider the efficiency during buck release mode when selecting C_{STRG}. For example, if I_{RLS} is 3A, t_{DASP} is 20ms, V_{STRG} is 28V, V_{BUS_RLS} is 7.5V, and the efficiency is 90%, then the required C_{STRG} is 1374µF.

Selecting the Bootstrap Capacitor (C_{BST})

The BST capacitor (C_{BST}) supplies power to the buck converter's HS-FET. It is recommended to use a 0.1µF to 1µF ceramic decoupling capacitor for C_{BST}.

Selecting the Input Capacitor (C_{IN})

Voltage spikes at the input may occur during start up or fast-off mode. Add an input capacitor (C_{IN}) to reduce any V_{IN} spikes. Choose a capacitance that satisfies the application requirement. Typically, a larger C_{IN} is more effective at reducing voltage spikes; however, a larger C_{IN} results in a higher input inrush current (especially during hot-plug conditions). Choose C_{IN} to be ≥1µF.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 15 and follow the guidelines below:

1. Connect the high-current paths (VIN, VB, SW, STRG, and PGND) using short, wide, and direct traces.
2. Keep the SW trace as short as possible, and away from the feedback network.
3. Connect the decoupling capacitor between the VB and PGND pins, placed as close to these pins as possible.
4. Connect the decoupling capacitor between the VCC and AGND pins, placed as close to theses pins as possible.
5. Place the feedback resistors next to FBB, FBS, and DET.
6. Keep the BST voltage paths (BST, C_{BST}, and SW) as short as possible.
7. Connect the signal grounds together, then connect them to PGND using a one-point connection.

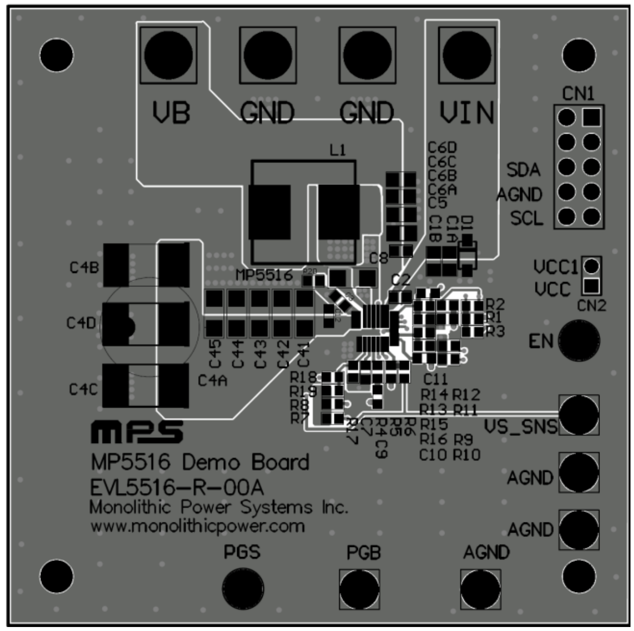


Figure 15: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

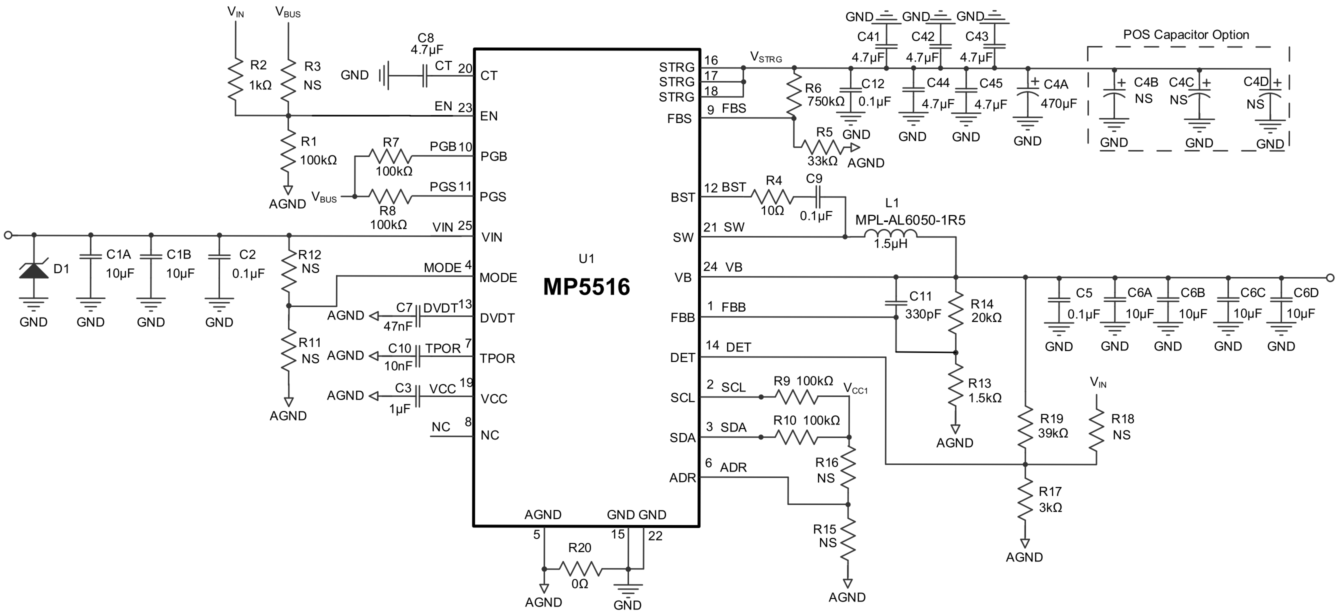
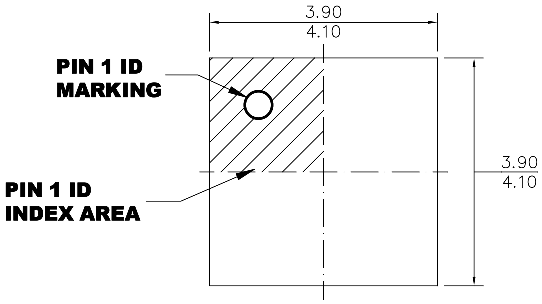


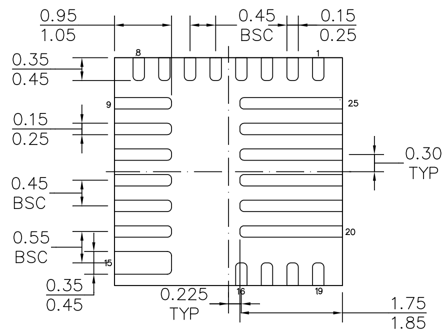
Figure 16: Typical Application Circuit (V_{IN} = 12V, V_{STRG} = 28V)

PACKAGE INFORMATION

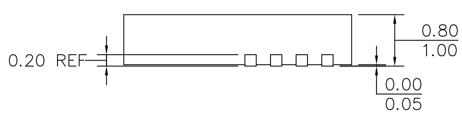
QFN-25 (4mmx4mm)



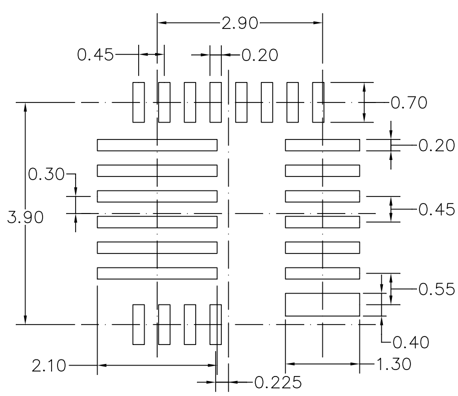
TOP VIEW



BOTTOM VIEW



SIDE VIEW

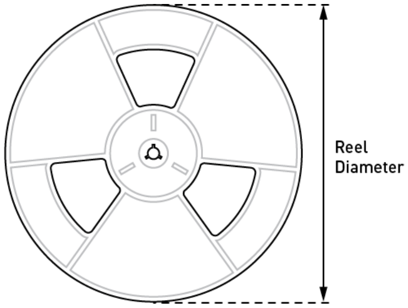


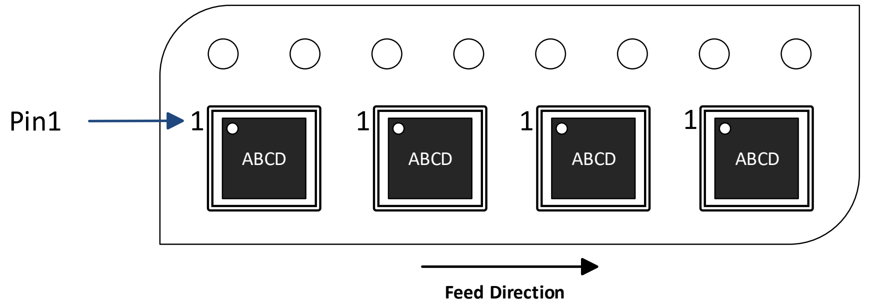
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITIES SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5516GR-Z	QFN-25 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/28/2022	Initial Release	-
1.1	7/7/2023	Updated “70mΩ/42mΩ $R_{DS(ON)}$ MOSFETS” to “60mΩ/37mΩ $R_{DS(ON)}$ MOSFETS” in the Features section	1
		Deleted “Use a 0.1µF decoupling capacitor to decouple MODE” in the MODE description	5
		Deleted “The reverse blocking feature can be disabled by the RVS_BLK_EN bit in register 01h” in the Reverse Current Blocking section	17
		Updated the PCB Layout Guidelines section: • Updated “3. Place the VB decoupling capacitor as close to PGND as possible.” to “3. Connect the decoupling capacitor between the VB and PGND pins, placed as close to these pins as possible.” • Updated “4. Place the VCC decoupling capacitor as close to AGND as possible.” to “4. Connect the decoupling capacitor between the VCC and AGND pins, placed as close to theses pins as possible.”	28