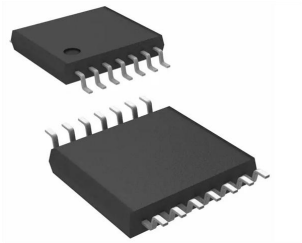
96 kHz, 24 Bit Δ-∑ ADC

PRODUCT DESCRIPTION

The MS1808 is a stereo A/D converter, which is suitable for audio system. Its sample rate ranges from 8kHz to 96kHz.

The MS1808 has high-accuracy feature achieved by using enhanced dual-bit delta-sigma technology. The MS1808 is single-ended input without external devices. The audio interface has two modes (MSB Justified, I^2S) and is proper for DTV, DVR and AV applications.



TSSOP14

FEATURES

- Linear Phase Anti-alias Digital Filter
- Single-ended Input
- Digital HPF with Offset Voltage Cancellation
- High Performance:
  S/(N+D): 85dB
  DR: 95dB
  S/N: 95dB
- Sample Rate: 8kHz ~ 96kHz
- Master Clock:
  256fs/384fs/512fs/768fs (8kHz~48kHz)
  256fs/384fs (48kHz~96kHz)
- Master or Slave Mode
- Audio Interface: 24bit MSB Left-justified or I^2S
- Analog Power Supply：4.5V~5.5V
- Digital Power Supply：2.7V~5.5V
- Operating Temperature Range: -40°C~105°C
- TSSOP14 Package

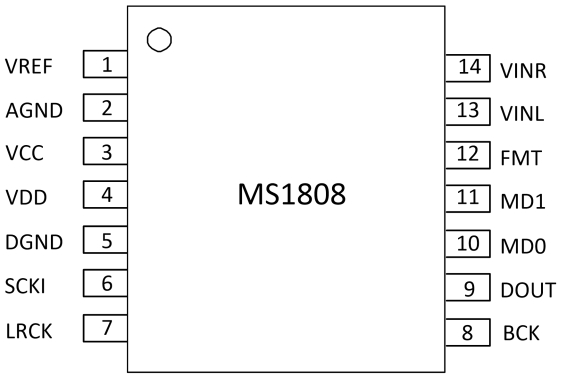
APPLICATIONS

- DVD Recorder
- DTV
- CD Recorder

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS1808	TSSOP14	MS1808

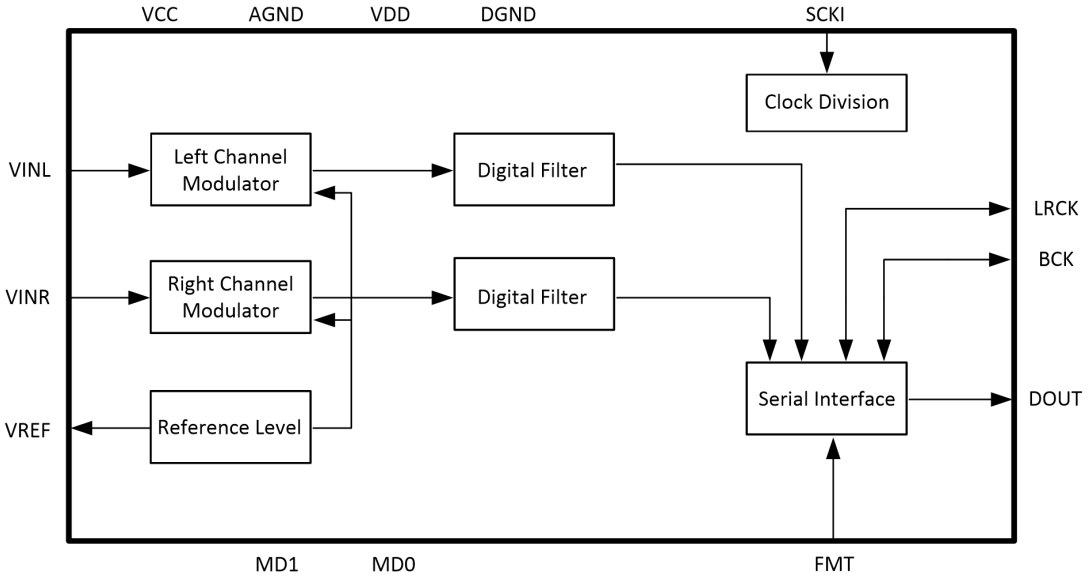
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	VREF	O	Common-mode Voltage Output Pin,VCC/2 Bias Voltage of ADC Input
2	AGND	-	Analog Ground Pin
3	VCC	-	Analog Power Supply Pin, 4.5V~5.5V
4	VDD	-	Digital Power Supply：2.7V~5.5V
5	DGND	-	Digital Ground Pin
6	SCKI	I	Master Clock Input Pin
7	LRCK	I/O	Output Channel Clock Pin
8	BCK	I/O	Audio Serial Data Clock Pin
9	DOUT	O	Audio Serial Data Output Pin
10	MD0	I	Mode 0 Select Pin
11	MD1	I	Mode 1 Select Pin
12	FMT	I	Audio Interface Type Select Pin ”L”: 24bit I^2S Compatible, “H”: 24bit MSB Justified
13	VINL	I	Lch Analog Input Pin
14	VINR	I	Rch Analog Input Pin

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter		Symbol	Range	Unit
Power Supply	Analog	VCC	-0.3 ~ 6.0	V
	Digital	VDD	-0.3 ~ 6.0	V
	|AGND – DGND| (1)	ΔGND	0.3	V
Input Current of All Pins Except Power Supply		IIN	±10	mA
Analog Input Voltage(VINL, VINR pin)		VINA	-0.3 ~ VCC+0.3	V
Digital Input Voltage (2)		VIND	-0.3 ~ VDD+0.3	V
Operating Temperature		Ta	-40 ~ 105	°C
Storage Temperature		Tstg	-65 ~ 150	°C

Note: (1) AGND and DGND must be connected to the same analog ground plane.

(2) FMT, SCKI, BCK, LRCK, MD1, MD0 pin.

RECOMMENDED OPERATING CONDITIONS

AGND, DGND = 0V

Parameter		Symbol	Range	Unit
Power Supply (1)	Analog	VCC	4.5 ~ 5.5	V
	Digital	VDD	2.7 ~ VCC	V

Note (1): No specific demands for VCC, VDD power-up sequences.

Unused Pin

Classification	Pin Name	Setting
Analog	VINR	The pin should be open
	VINL	The pin should be open

ELECTRICAL CHARACTERISTICS

Analog Characteristics

Ta=25°C; VCC=5.0V, VDD=3.3V; AGND=DGND=0V; fs=48kHz, 96kHz; BCK = 64fs; Signal Frequency = 1kHz; 24bit Data; Measurement Frequency=20Hz~20kHz at fs=48kHz, 40Hz~40kHz at fs=96kHz. Unless otherwise specified.

Parameter			Min	Typ	Max	Unit
ADC Analog Input Characteristics						
Resolution					24	Bits
Input Voltage (1)			2.7	0.6VCC	3.3	Vpp
S/(N+D)	fs = 48kHz	-1dBFS	75	85		dB
	BW = 20kHz	-60dBFS		39		dB
	fs = 96kHz	-1dBFS		90		dB
	BW = 40kHz	-60dBFS		38		dB
DR (-60dBFS, A-weighted)			85	95		dB
S/N (A-weighted)			85	95		dB
Input Resistance	fs = 48kHz		13	20		kΩ
	fs = 96kHz		9	14		kΩ
Interchannel Isolation			80	85		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift				100		ppm/°C
Power Supply Rejection (2)				50		dB
Power Supply						
Power Supply Current						
Normal Operation						
VCC				10	16	mA
VDD (fs = 48kHz)				2	5	mA
VDD (fs = 96kHz)				4	9	mA

Note:

(1) The value is full scale (0dB) of input voltage. Input voltage is in proportional to VCC,Vin=0.6×VCC (Vpp).

(2) PSRR is applied to VCC and VDD with 1kHz, 50mVpp.

Filter Characteristics (fs=48kHz)

Ta = -40°C~105°C; VCC = 4.5V~5.5V; VDD = 2.7V~5.5V.

Parameter		Symbol	Min	Typ	Max	Unit
ADC Digital Filter (Decimation LPF)						
Passband (1)	±0.1dB	PB	0		18.9	kHz
	-0.2dB			20.0		kHz
	-3.0dB			23.0		kHz
Stopband		SB	28			kHz
Passband Ripple		PR			±0.04	dB
Stopband Attenuation		SA	68			dB
Group Delay Distortion		ΔGD		0		us
Group Delay		GD		16		1/fs
ADC Digital Filter (HPF)						
Frequency Response (2)	-3dB	FR		1.0		Hz
	-0.1dB			6.5		Hz

Filter Characteristics (fs=96kHz)

Ta = -40°C~105°C; VCC = 4.5V~5.5V; VDD = 2.7V~5.5V.

Parameter		Symbol	Min	Typ	Max	Unit
ADC Digital Filter (Decimation LPF)						
Passband (1)	±0.1dB	PB	0		37.8	kHz
	-0.2dB			40.0		kHz
	-3.0dB			46.0		kHz
Stopband		SB	56			kHz
Passband Ripple		PR			±0.04	dB
Stopband Attenuation		SA	68			dB
Group Delay Distortion		ΔGD		0		us
Group Delay		GD		16		1/fs
ADC Digital Filter (HPF)						
Frequency Response (2)	-3dB	FR		2.0		Hz
	-0.1dB			13.0		Hz

Note:

(1) The passband and stopband frequencies change with fs. For example, PB=18.9kHz@±0.1dB is 0.39375×fs.

(2) The calculated delay time induced by digital filtering.

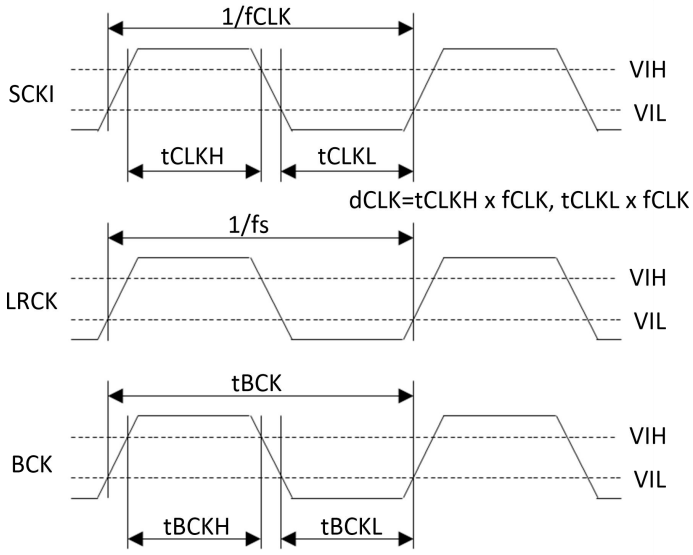
Switching Characteristics

Ta = -40°C~105 °C; VCC = 4.5V~5.5V; VDD = 2.7V~5.5V; CL=20pF.

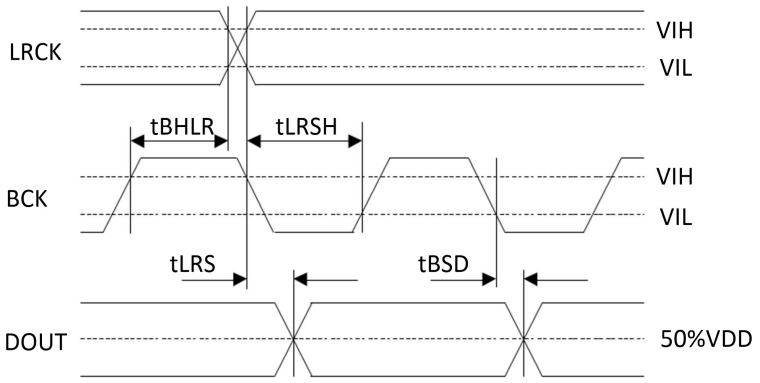
Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Timing					
512fs,256fs Frequency	fCLK	2.048		24.576	MHz
Duty Cycle	dCLK	40		60	%
768fs,384fs Frequency	fCLK	3.072		36.864	MHz
Duty Cycle	dCLK	40		60	%
LRCK Frequency		8		96	kHz
Duty Cycle Slave Mode	fs	45		55	%
Master Mode			50		%
Audio Interface Timing					
Slave Mode					
BCK Period	tBCK	160			ns
BCK Pulse Width Low	tBCKL	65			ns
Pulse Width High	tBCKH	65			ns
LRCK Edge to BCK "↑" (1)	tLRSH	30			ns
BCK "↑" to LRCK Edge (1)	tBHLR	30			ns
LRCK to DOUT(MSB) (Except I^2S Mode)	tLRS			35	ns
BCK "↓" to DOUT	tBSD			35	ns
Master Mode					
BCK Frequency	fBCK		64fs		Hz
BCK Duty	dBCK		50		%
BCK "↓" to LRCK	tMBLR	-20		20	ns
BCK "↓" to DOUT	tBSD	-20		35	ns

Note (1): BCK rising edge must not occur on the LRCK rising and falling edges.

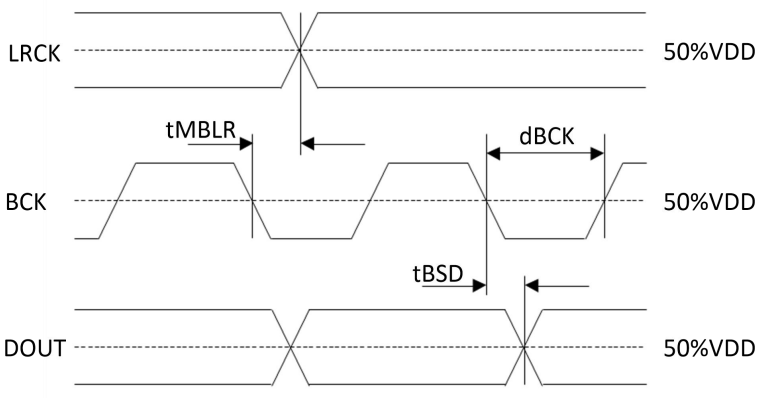
TIMING DIAGRAMS



Clock Timing



Audio Interface Timing (Slave Mode)



Audio Interface Timing (Master Mode)

FUNCTIONAL DESCRIPTION

Hardware Control

Pull-up and pull-down resistance and GPIO control FMT, MD0 and MD1 pins to choose output code format and operation mode.

System Clock

The MS1808 supports 256fs, 384fs and 512fs as system clock. fs is audio sample rate. SCLKI is input pin of system clock. Table 1 shows the relationship between typical sample rate and system clock frequency.

Table 1. System Clock Example

fs	SCKI		
	256fs	384fs	512fs
32kHz	8.192MHz	12.288 MHz	16.384 MHz
44.1kHz	11.2896 MHz	16.9344 MHz	22.5792 MHz
48 kHz	12.288 MHz	18.432 MHz	24.576 MHz
96 kHz	24.576 MHz	36.864 MHz	N/A

Interface Mode

MD1 and MD0 choose master mode or slave mode as mode select pins. Table 2 shows interface mode options. In master mode, BCK and LRCK act as output pins, and BCK frequency is 64fs.While In slave mode, BCK and LRCK act as input pins, and BCK frequency is 48fs or 64fs.

Table 2. Interface Mode

MD1	MD0	Interface Mode
0	0	Slave Mode (256fs, 384fs, 512fs Automatic detection)
0	1	Master Mode (512fs)
1	0	Master Mode (384fs)
1	1	Master Mode (256fs)

Data Format

Table 3. Data Format

Format	FMT	Data Format
Format 0	L	24bit, I^2S Compatible
Format 1	H	24bit, Left Justified

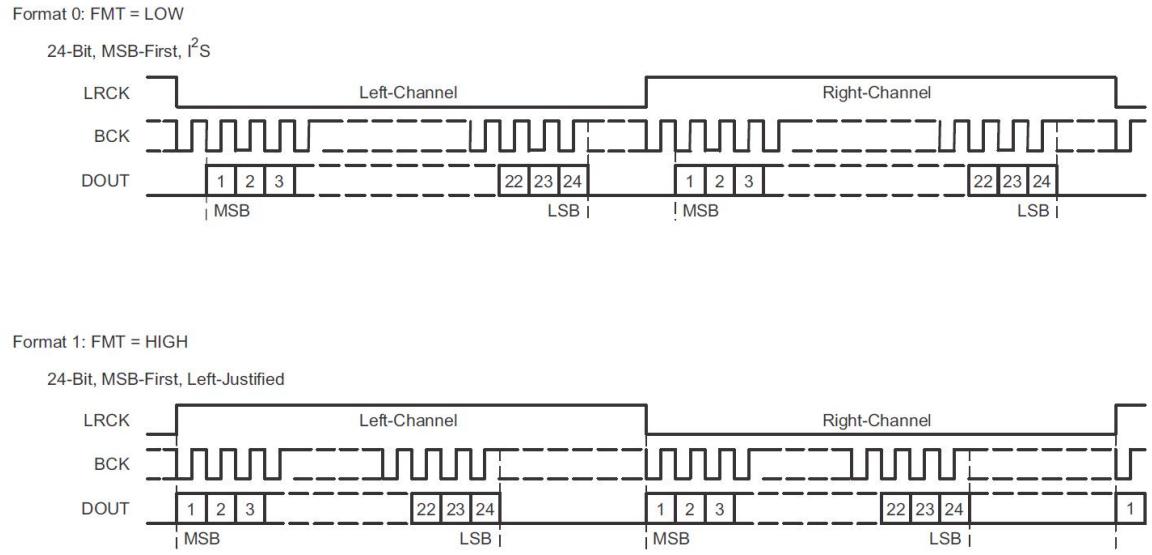


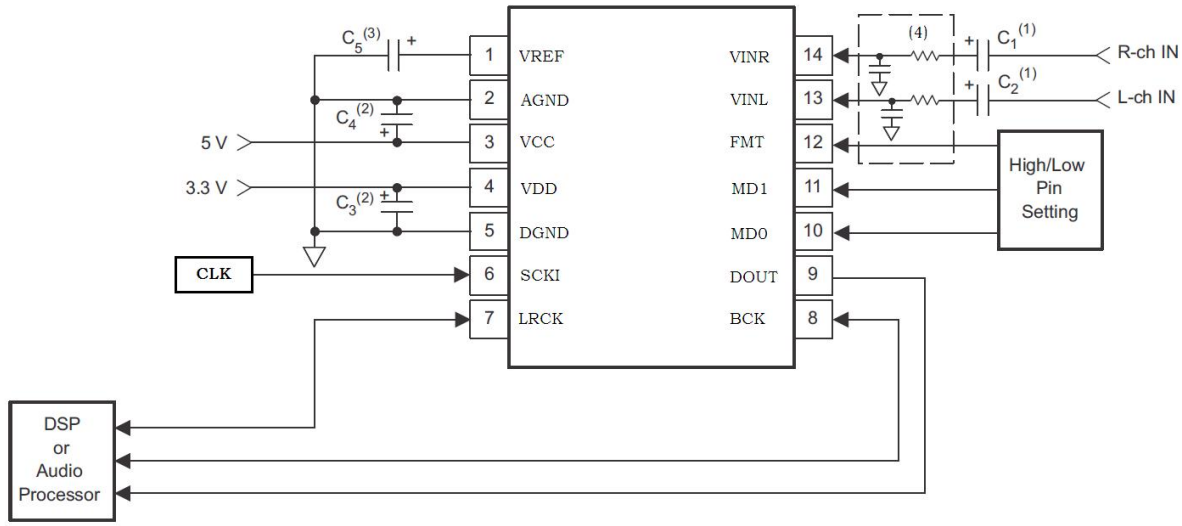
Figure 1. Audio Data Format

Digital High-Pass Filter

The MS1808 has a high-pass filter to eliminate DC offset. The HPF cut-off frequency is 1.0Hz(@fs = 48kHz), and changes with sample rate (fs).

During initiation period, the ADC data outputs of two channels are set as two's complements. At the end of initiation, ADC output gradually corresponds to input signal (Settling requires about group delay time).

TYPICAL APPLICATION DIAGRAM



1. C1, C2: 10uF AC Coupling Capacitor
2. C3, C4: 10uF Electrolytic Capacitor, 0.1uF Ceramic Capacitor
3. C5: 2.2uF Capacitor
4. Optional External Anti-alias Filter

Ground and Power Supply Decouple

The MS1808 requires special careful power and ground arrangements. And if VCC and VDD are separated, the power-up sequence is not the key. AGND and DGND must be connected on the same ground plane. The system analog ground and digital ground should be connected together and close to PCB ground. The decoupling capacitor should be placed as close to the MS1808 as possible , and small ceramic capacitor should be the nearest.

Voltage Reference

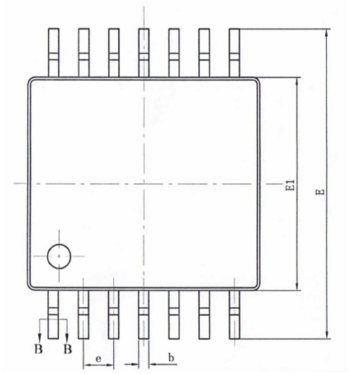
The analog voltage input range is set by VCC and VREF is 50% VCC. A 2.2uF capacitor is attached to VREF pin. In order to avoid needless coupling into the MS1808, all signals especially clock signals should be separate from VREF pin.

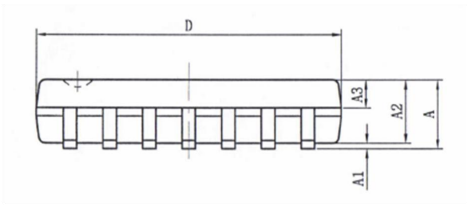
Analog Input

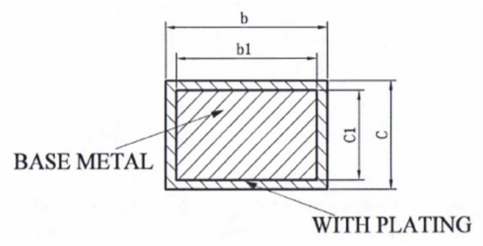
The ADC input is single-ended and biased to common-mode voltage (50% VCC) via 20kΩ (typ@fs=48kHz). The input signal range scales with VCC, normally 0.6×VCC Vpp(typ). The ADC output data format is two's complement. The internal high-pass filter eliminates DC offset voltage.

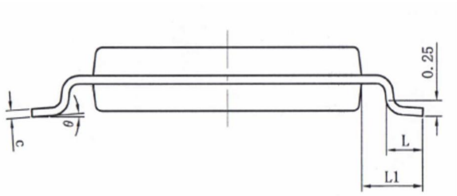
PACKAGE OUTLINE DIMENSIONS

TSSOP14





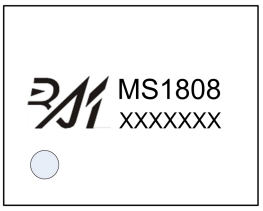




Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A			1.20
A1	0.05		0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20		0.30
b1	0.19	0.22	0.25
c	0.13		0.19
c1	0.12	0.13	0.14
D	4.86	4.96	5.06
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45		0.75
L1	1.00BSC		
θ	0		8°
L/F Carrier Size(mil)	79×79		90×110
	118×153		

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description



Product Name : MS1808

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS1808	TSSOP14	3000	1	3000	8	24000

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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