Rockchip RV1126B Datasheet

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Chapter 1 Introduction

1.1 Overview

RV1126B is a high-performance vision processor SoC for machine vision application, especially for AI related application.

It is based on quad-core ARM Cortex-A53 64-bit core which integrates NEON and FPU. There is a 32KB I-cache and 32KB D-cache for each core and 512KB unified L2 cache. The build-in NPU Support INT8/INT16 hybrid operation and computing power is up to 3.0TOPs. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RV1126B introduces a new generation totally hardware-based maximum 12-Megapixel ISP (image signal processor) and post processor. It implements a lot of algorithm accelerators, such as HDR, 3A, LSC, 3DNR, 2DNR, sharpening, dehaze, fisheye correction, gamma correction, feature points detection and so on. A maximum 8-Megapixel AI-ISP is also introduced as a complement to traditional ISP, which offers superior spatial denoising performance and enhanced image enhancement effects. Cooperating with two MIPI CSI(or LVDS/SubLVDS) and one DVP(BT.601/BT.656/BT.1120) interface, users can build a system that receives video data from four camera sensors simultaneously.

The video encoder embedded in RV1126B support H.265/H.264 video encoding and the multi-stream encoding is supported also. With the help of this feature, the video from camera can be encoded with higher resolution and stored in local memory and transferred another lower resolution video to cloud storage at the same time.

The H.264/H.265 video decoder in RV1126B support 4Kp30 for H.264 and H.265.
In addition to the previous high-performance multimedia block, RV1126B also contains rich audio, memory and other peripheral interfaces such as I2C, SPI, PWM and so on. These can help users add more sensors or other peripherals into whole system to improve flexibility and expansibility.

RV1126B has high-performance external DRAM(DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/4X) capable of sustaining demanding memory bandwidths.

Also the RTC, POR, RMII Ethernet PHY and Audio Codec are integrated in RV1126B.

1.2 Features

1.2.1 Application Processor

- Quad core ARM Cortex-A53
- Full implementation of the ARM architecture v8-A instruction set, ARM Neon Advanced SIMD
- Separately Integrated Neon and FPU
- 32KB L1 I-Cache and 32KB L1 D-Cache
- Unified 512KB L2 Cache for Cortex-A53
- TrustZone technology support
- Separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
  - PD_CPU2: 3rd Cortex-A53 + Neon + FPU + L1 I/D Cache
  - PD_CPU3: 4th Cortex-A53 + Neon + FPU + L1 I/D Cache
- One isolated voltage domain to support DVFS

1.2.2 Memory Organization

- Internal on-chip memory
  - Bootrom
    - Support system boot from the following device:
      - SPI interface

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        - eMMC interface
        - SD/MMC interface
      - Support system code download by the following interface:
        - USB2.0 interface
        - UART interface
  - 64KB system SRAM
  - 8KB PMU SRAM

- External off-chip memory
  - Dynamic Memory Interface (DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X)
    - Compatible with JEDEC standards
    - Compatible with DDR3/DDR3L/ DDR4 /LPDDR3/LPDDR4/LPDDR4X
    - Support 32-bit data width, 2 ranks (chip selects), max 4GB addressing space per rank, total addressing space is 4GB (max)
    - Low power modes, such as power-down and self-refresh for SDRAM
  - eMMC Interface
    - Fully compliant with JEDEC eMMC 4.51 specification
    - Support HS200, but not support CMD Queue
    - Support three data bus width mode: 1bit, 4bits and 8bits
  - SD/MMC Interface
    - Compatible with SD3.0, MMC ver4.51
    - Support 1bit, 4bits data bus width
  - Flexible Serial Flash Interface (FSPI0)
    - Support transfer data from/to serial flash device
    - Support 1bit, 2bits or 4bits data bus width
    - Support 2 chips select

1.2.3 System Component

- HPMCU
  - Integrated 16KB Cache
  - Integrated Programmable Interrupt Controller, all IRQ lines connected to GIC for CPU also connect to MCU
  - Integrated Debug Controller with JTAG interface

- LPMCU
  - Integrated Programmable Interrupt Controller, all IRQ lines in VD_PMU domain are connected to MCU
  - Integrated Debug Controller with JTAG interface
  - Used for low power application

- CRU (clock & reset unit)
  - Support total 4 PLLs to generate all clocks
  - One oscillator with 24MHz clock input
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component

- PMU (power management unit)
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - Support 4 separate voltage domains，CPU_DVDD,NPU_DVDD,VDD_LOGIC,VDD_PMU
  - Support 3 separate power domains, which can be power up/down by software based on different application scenes

- Timer
  - Support 2 secure timers with 64bits counter and interrupt-based operation

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- Support 6 non-secure timers with 64bits counter and interrupt-based operation
- Support 1 non-secure timers with 64bits counter for low power mode application
- Support two operation modes: free-running and user-defined count for each timer
- Support timer work state checkable

- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Three Watchdog for non-secure application
  - One Watchdog for secure application

- Interrupt Controller
  - Support 256 SPI interrupt sources input from different components inside SoC
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed, high-level sensitive or rising edge sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Support 2 physical channels
  - Support 39 groups of peripheral request interfaces
  - Support 48 logic channels, each logic channel support the following feature
    - Support the data transfer of memory-to-memory, memory-to-peripherals, peripherals-to-memory
    - Support Linked list DMA function to complete scatter-gather transfer
    - Support three kinds of multi-block transfer: contiguous address, auto reload, link list

- Secure System
  - Support one cipher engine
    - Support Symmetrical algorithms
      - AES-128, AES-192, AES-256, SM4
      - ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode for AES and SM4
    - Hash algorithm
      - SHA-1, SHA-256/224, MD5, SM3 with hardware padding
      - HMAC of SHA-1, SHA-256, MD5, SM3 with hardware padding
    - Asymmetrical algorithms
      - RSA (up to 4096 bits), ECC (up to 256 bits), SM2
    - Key-ladder(KL)
      - Support obtaining the root key from OTP or RKRNG and deriving it
      - Support write out root key or derived key to some specific modules
      - Number of stages can be configured
  - Support secure OTP
  - Support secure debug
  - Support secure OS
  - Except CPU, the other masters in the SoC can also support security and non-security mode by software-programmable
  - Some slave components in SoC can only be addressed by security master and the other slave components can be addressed by security master or non-security master by software-programmable
  - System SRAM, part of space is addressed only in security mode
  - External DDR space can be divided into 16 parts, each part can be software-

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programmable to be enabled by each master

- Mailbox
  - One Mailbox with 4 channels in SoC used to service Cortex-A53 and HPMCU communication
  - One Mailbox in VD_PMU used for Cortex-A53 and LPMCU communication.
  - Support independent interrupt in each Mailbox channel

- Decompression
  - Support for decompressing GZIP files
  - Support for decompressing data in DEFLATE format
  - Support for decompressing data in ZLIB format
  - Support the limit size function of the decompressed data to prevent the memory from being maliciously destroyed during the decompression process

- Real Time Clock (RTC)
  - Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz crystal oscillator
  - Support compensation for the second and hour count
  - BCD representation of time, calendar and alarm
  - 12- or 24-hour clock with AM and PM in 12-hour mode
  - Interrupts are separately software maskable
    - Alarm interrupt
    - Periodic interrupt
    - Chip power off interrupt
    - Battery power atypical interrupt

1.2.4 AOV(Always On Video) subsystem

- One SPI slave interface for receiving data from camera
- Dedicated SPI master for external flash device access
- Low power control unit for power saving
- LPMCU is used for system control

1.2.5 AOA(Always On Audio) subsystem

- One Audio ADC and one Low power SAI controller for receiving data from sensor
- Dedicated SPI master for external flash device access
- Low power control unit for power saving
- One AOA_Controller for system control to detect sound and wake up SoC
  - Support Audio Time Detect
  - Support Audio Feature Extract
  - Support Audio AI Detect

1.2.6 Video CODEC

- Video Decoder
  - Real-time decoding of H.264 and H.265
  - Support MMU
  - H.265 HEVC/MVC Main Profile yuv420@L5.0 up to 3840x2160@30fps
  - H.264 AVC/MVC Main Profile yuv400/yuv420/yuv422@L5.1 up to 3840x2160@30fps
- Video Encoder
  - HEVC Main Profile, Level 5.0 High Tier
  - H.264 High Profile, Level 5.0
  - JPEG Baseline
  - Parallel encoding (HEVC+JPEG or H264+JPEG)
  - Support up to 12M@30fps
  - Support common primary stream such as 3840x2160@30fps, 1920x1080@30fps
  - Bitrate up to 200Mbps with CBR/VBR/FixQP/QPMAP bitrate control
  - YUV420 and YUV400 stream format

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- Slice split
- Area and block mapping ROI
- 8-area OSD
- Link table configuration mode
- YUV/RGB video source with crop, rotation and mirror
- Ultra low delay encoding
- Motion and Occlusion Detection
- Dual reference frame search(HEVC)

- JPEG Decoder
  - Support Baseline(DCT sequential)
  - Support JPEG file interchange format (JFIF) 1.02
  - Support image size is from 48x48 to 65520x65520
  - Support YUV400/YUV420/YUV422/YUV440/YUV411/YUV444

1.2.7 Neural Process Unit

- Rockchip NPU engine:
  - 3 TOPS* for INT8
  - Support INT4, INT8, INT16, FP16 operation
  - Support deep learning frameworks: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, Android NN, etc.

  * Sparsity
- One isolated voltage domain to support DVFS

1.2.8 2D Graphics Engine

- 2D Graphics Engine(RGA)
- Data format
  - SRC0 Input data format:
    - ARGB8888/RGBA8888/RGBA4444/RGBA5551
    - RGB888P/RGB565
    - YUV422-P/YUV422-SP-8bit/10bit(clip to 8bit after input)
    - YUV420-P/YUV420-SP-8bit/10bit(clip to 8bit after input)
    - YUV444I/YUV444SP-8bit
    - YVYU422-8bit
    - YUV400-8bit
    - TILE4X4 YUV420/422/444-8bit
    - TILE4X4 YUV420/422/444-10bit(clip to 8bit after input)
    - BPP1/2/4/8
  - SRC1 Input data format:
    - ARGB8888/RGBA8888/RGBA4444/RGBA5551/A8
    - RGB888P/RGB565
  - Output data format(all YUV format is 8bit):
    - ARGB8888/RGBA8888/ARGB4444/RGBA4444/ARGB5551/RGBA5551
    - RGB888/RGB565
    - YUV420/YUV422 P/SP
    - YUV400/Y4
    - YUV444SP/444I
  - Pixel Format conversion, BT.601/BT.709
  - Dither operation
  - Max resolution: 8192x8192 source, 4096x4096 destination
- Scaling
  - Down-scaling: Average/Bilinear filter
  - Up-scaling: Bi-cubic filter(source>1992 would use Bi-linear)
  - Arbitrary non-integer scaling ratio, from 1/16 to 16
- Rotation
  - 0, 90, 180, 270 degree rotation
  - x-mirror, y-mirror operation
  - Mirroring and rotation co-operation
- BitBLT

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- Block transfer
- Color palette/Color fill, support with alpha
- Transparency mode (color keying/stencil test, specified value/value range)
- Two source BitBLT
- A+B=B only BitBLT, A support rotate & scale when B fixed
- A+B=C second source (B) has same attribute with (C) plus rotation function

- Alpha Blending
  - Comprehensive per-pixel alpha(color/alpha channel separately)
  - Fading
  - Support SRC1(R2Y)+SRC0(YUV) -> DST(YUV)
  - Support DST Full CSC convert for YUV2YUV
- OSD Automatic Inversion
  - Support OSD sources in ARGB8888/ARGB1555/ARGB444/ARGB2BPP format
  - Support SRC0 and OSD overlay

1.2.9 Display Interface

- Support MCU/RGB LCD Interface up to 24-bits
- Support BT.656/BT.1120 Interface
- Support 4lane MIPI interface, 1.5Gbps/lane
- Max output resolution is 1920x1080@60fps

1.2.10 Video Output Processor (VOP)

- Up to 1920x1080 @60fps
- Multiple layer
  - Background layer
    - programmable 24-bit color
  - Win0 layer
    - YUV444,YUV422,YUV420,RGB888, ARGB888, RGB565
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - RGB2YUV(BT601_l/BT709_l)
    - YUV2RGB(BT601_l/BT709_l/BT601_f)
  - Win2 layer
    - RGB888, ARGB888, RGB565
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - RGB2YUV(BT601/BT709)
    - Support multi-region
- Support RGB or YUV domain overlay
- BCSH (Brightness, Contrast, Saturation, Hue adjustment)
- BCSH: RGB2YUV (BT601/BT709)
- Support Gamma adjust for PAD
- Support dither down allegro RGB888to666 RGB888to565 and dither down FRC (Frame Rate Control) (configurable) RGB888to666
- Blank and black display
- Standby mode

1.2.11 Video Input Interface

- MIPI Interface
  - Support Two MIPI CSI/LVDS/SubLVDS DPHY
    - Each MIPI DPHY V1.2, 4lanes, 2.5Gbps per lane
    - Each interface may be configured as 2x2 data lanes port
    - Support virtual channel
- DVP interface
  - 8/10/12/14/16-bit, up to 150MHz I/O frequency
  - BT.601/BT.656 and BT.1120 VI interface

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- Support the polarity of pixel_clk, hsync, vsync configurable

1.2.12 Image Signal Processor

- Video Capture (VICAP)
  - Support BT.601 RAW8/10/12/14 YCbCr 422 8-bit input
  - Support BT.656 YCbCr 422 8-bit progressive/interlaced input
  - Support 16-pins BT.1120 YCbCr 422 8-bit progressive/interlaced input
  - Support 2/4 mixed BT.656/BT.1120 YCbCr 422 input
  - Support dual-edge sampling for BT.656/BT.1120
  - Support receiving four groups of MIPI CSI/LVDS interfaces, up to four IDs for each group
  - Support VC/DT configurable for each ID
  - Support ten MIPI CSI data formats: RAW8/10/12/14/16, RGB888, YUV422 8bit, YUV422 8bit interlaced, YUV420 8bit, Legacy YUV420 8bit
  - Support three modes of MIPI CSI HDR: virtual channel mode, identification code mode, line counter mode
  - Support four LVDS data formats: RAW8/10/12, YUV422 8bit
  - Support RAW rounding
  - Support window cropping
  - Support reducing frame rate
  - Support 4/8/16/32 times down-sampling for RAW data
  - Support RAW 2x2 binning
  - Support pixel extraction from 2x2 pattern
  - Support UV mean down-sampling for YUV422
  - Support compact/non-compact output format for RAW data
  - Support NV16/NV12/YUV400/YUYV output format for YUV data
  - Support virtual stride when write to DDR
  - Support DMA wrap mode
  - Support DMA burst gather 2/4/8
  - Support MMU
  - Support QOS(hurry/press)
  - Support sending RAW data directly to ISP

- Image Signal Process (ISP)
  - VICAP input: RX raw8/raw10/raw12/raw14/raw16
  - Maximum input: 12M@30fps
  - Minimum input: 264x264
  - RGBIR: Remosaic RGB-IR pattern to RGB pattern
  - Auto Enhance (AE)/Histogram, Auto Focus (AF) and Auto White Balance (AWB) statistics output
  - BLC: Black Level Correction
  - DPCC: Static/Dynamic Defect Pixel Cluster Correction
  - PDAF: Phase Detection Auto Focus
  - LSC: Lens Shading Correction
  - Bayer-3DNR: Temporal Bayer-raw Noise Reduction
  - CAC: Chromatic Aberration Correction
  - HDR-MGE: 2-Frame Merge into High-Dynamic Range
  - EXPANDER: Sensor expander
  - GIC: Green Imbalance Correction
  - HDR-DRC: HDR Dynamic Range Compression, tone mapping in RGB filed
  - DeBayer: Advanced Adaptive Demosaic
  - CCM/CSM: Color Correction Matrix, RGB2YUV
  - Gamma: Gamma out correction
  - Dehaze/Enhance: Automatic dehaze and effect enhancement
  - LocalHist: local histogram to enhance local contrast
  - HSV: Hue, Saturation,Value color palette for customer
  - LDCH: Lens Distortion Correction in the Horizontal direction
  - YNR: Spatial luma (Y) Noise Reduction in YUV domain

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- CNR: Spatial chroma(C) Noise Reduction in YUV domain
- Sharp: Image sharpening and boundary filtering
- Gain: Image local gain
- Multi-sensor reuse ISP, 2 sensors for maximum
- Bus interface: 32bit AHB configuration, 128bit AXI R/W
- Low power, auto-gating for each block
- MI R/W burst group to improve memory utilization
- MI 2 paths output, MP stepless scaling, SP 1080p (width no more than 1920) scaling
- tile4x4 output
- Online mode: support data from VICAP and data to Encoder, data from ISP to VPSS, ISP to VPSL
- Support ISP2NPU with AI-ISP path, BAY3D output IIR data and gain data to DDR which used by NPU

- AI-ISP
  - Operator modes
    - Mode0: 18x18 convolution
    - Mode1: 24x24 convolution
  - Network Depth
    - Single mode Support up to 8 layers
    - Combo mode Support up to 16 layers
  - Processing Modes
    - Single mode Support up to 6 input channels (commonly 4 channels)
    - Combo mode Support up to 7 input channels
  - Channel Control
    - Each input channel has an independent enable control
    - some input channels support up-sampling and S2D operations
  - Maximum Resolution: Support up to 4096x4096
  - Support maximum 8M@30fps performance

- FishEye Correction(FEC)
  - Input mode and data format
    - RASTER: YUV420SP
    - TILE: YUV420
  - Output mode and data format
    - RASTER: YUV420SP
    - TILE: YUV420
    - FBCE: YUV420
    - QUAD(To AVSP): YUV420
  - Support 32x16,16x8, 4x4(only support 4096x4096 resolution below) density
  - Support up to 4 times reduction factor
  - Input resolution 64x64~8160x8160
  - Output resolution 64x64~8160x8160
  - Performance will be almost 3840x2160 30fps, which different meshgrid will affedct it

- Any View Stitching Processor(AVSP)
  - DCP Input mode and data format
    - RASTER: YUV420SP
    - QUAD: YUV420
  - DCP Output mode and data format
    - RASTER: YUV420SP
    - QUAD: YUV420
  - RCS Input mode and data format
    - QUAD:YUV420
  - RCS Output mode and data format
    - RASTER: YUV420SP

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- TILE: YUV420
- FBCE:YUV420

- Support resolution 64x64~1024x4096
- Support band number 1~6
- Support decomposition output directly

1.2.13 Video Processing Sub-System(VPSS)

- VPSS
  - Offline DMA input:
    - Line RGB888/ARGB888/RGB565/UYVY/YUV422/YUV420 SP 8bits
    - Tile4x4 YUV422/YUV420 8bits (Rotate 0/90/180/270)
    - RKFBCD64x4 YUV444/YUV422/YUV420 8bits
    - Line-Rot90 UYVY/YUV422/YUV420 8bits (Rotate 90)
  - Online ISP input
  - Both DMA and ISP input
  - Six output channels
  - Maximum image resolution: 4096x3072 (width no more than 4096)
  - Minimum image resolution: 32x32
  - YUV422 processing
  - MIRROR: Horizontal Mirror
  - CMSC: Cover or Mosaic in 8 areas
  - CROP: Cropping on 6 channels
  - Channel0 output:
    - Scale: Bilinear or average filter
    - ASPT_RATIO: Aspect Ratio for image boundary extension
    - Output scan order:
      - Line YUV422/YUV420 SP 8bits
      - Tile4x4 YUV422/YUV420 8bits
      - RKFBCE64x4 YUV422/YUV420 8bits
    - Flip: Vertical Flip for line mode
  - Channel1 output:
    - Scale: Bilinear filter
    - ASPT_RATIO: Aspect Ratio for image boundary extension
    - Output scan order:
      - Line RGB888/ARGB888/RGB565/YUV422/YUV420 SP 8bits
      - Tile4x4 YUV422/YUV420 8bits
      - RKFBCE64x4 YUV422/YUV420 8bits
    - Flip: Vertical Flip for line YUV mode
    - Resolution up to 12M@30fps
  - Channel2 output:
    - Scale: Bilinear or average filter (output width no more than 1920)
    - ASPT_RATIO: Aspect Ratio for image boundary extension
    - Output scan order: Line YUV422/YUV420 SP 8bits
    - Flip: Vertical Flip for line mode
    - Resolution up to 12M@30fps
  - Channel3 output:
    - Scale: Bilinear filter (output width no more than 1920)
    - ASPT_RATIO: Aspect Ratio for image boundary extension
    - Output scan order: Line YUV422/YUV420 SP 8bits
    - Flip: Vertical Flip
    - Resolution up to 1920x1080@30fps
  - Channel4 output:
    - Scale: Bilinear filter (output width no more than 1920)
    - ASPT_RATIO: Aspect Ratio for image boundary extension
    - Output scan order: Line YUV422/YUV420 SP 8bits
    - Flip: Vertical Flip
    - Resolution up to 1920x1080@30fps
  - Channel5 output:

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- Scale: Bilinear filter (output width no more than 1920)
- ASPT_RATIO: Aspect Ratio for image boundary extension
- Output scan order: Line YUV422/YUV420 SP 8bits
- Flip: Vertical Flip
- Resolution up to 1920x1080@30fps

- Tile4x4 or RKFBCE64x4 of channel0 and channel1 are mutually exclusive

- VPSS_Lite(VPSL)
  - Online or offline input in Luma Pyramid path
  - Online input in Sigma Pyramid path
  - Raw or Y image input format
  - Luma Pyramid multi-band output: Raw mode has 3 channels, Y mode has 6 channels
  - Sigma Pyramid multi-band output: Raw mode has 4 channels, Y mode has 5 channels
  - Maximum image resolution: 4096x3072 (width no more than 4096)
  - Minimum image resolution: 64x64

1.2.14 On-Chip Offset Calibration(OOC) of infrared detector

- OOC Interface
  - Support full and data Mode.
- WIN1
  - Data Format：Raw8(Valid Data 6-bits)
  - Support virtual width(max 4096 word)
  - Support active offset
  - Support display offset
  - Support line key
  - Support frame key and frame offset set
  - Support bit valid cycle num
  - Support valid data aligned adjust
  - Line/Frame key num set
  - Support Frame/Line key parameter user define
- PDAF
  - Data Format：Raw8
  - Support virtual width(max 4096 word)
  - Support active offset
  - Support display offset
  - Support bit valid cycle num
  - Support valid data aligned adjust
  - Support last line pixel num set

1.2.15 Serial Audio Interface(SAI)

- Support 3 SAI interfaces
  - SAI 0 support 4 TX lanes and 4 RX lanes
  - SAI 1 support 1 TX lane and 1 RX lane
  - SAI 2 support 1 TX lane and 3 RX lanes
  - One Low-power SAI used for AOA sub-system
  - Support audio protocol: I2S, PCM, TDM
  - Support up to 128 slots available with configurable size
  - Support slot length 8 to 32 bits configurable
  - Support slot valid data length 8 to 32 bits configurable

- PDM
  - Support up to 8 channels
  - Support resolution is from 16bits to 24bits
  - Support sample rate is up to 192KHz
  - Support PDM master receive mode
  - Support gain control

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- ASRC
  - Support dual 2-channel ASRC
  - Support sample rate and resample rate range from 8 to 384KHz
  - Support real-time transmission mode
  - Support memory fetch mode

- Digital Audio Codec
  - Support 2-channels digital DAC
  - Support I2S/PCM interface, master and slave mode
  - Support 16-bit sample resolution
  - Support three modes of mixing for every digital DAC channel
  - Support volume control

- Audio Codec
  - Integrated 2 Audio ADC
  - Support Analog gain between 0~48dB with 3db/step
  - Support 1-channel Differential-mode/Single-mode/Pseudo-differential mode ADC
  - Support I2S/PCM master and slave mode
  - Support 16 ~32bit sample resolution
  - Support sample rate up to 192kHz
  - Support passband ripple within +/-0.1dB
  - Support stopband attenuation at least 60dB
  - Support volume control
  - Support programmable negative volume gain and positive volume gain.

1.2.16 Connectivity

- SDIO interface
  - Compatible with SDIO3.0 protocol
  - 4-bit data bus widths

- MAC 10/100/1000M Ethernet
  - Support one Ethernet controllers
  - Support Integrated IEEE 802.3/802.3u compliant 10/100Mbps Ethernet PHY
  - Support 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Support 10/100-Mbps data transfer rates with the RMII interfaces
  - Support 10/100-Mbps data transfer rates with embedded Ethernet PHY
  - Support both full-duplex and half-duplex operation
  - Support for TCP Segmentation Offload (TSO) and UDP Segmentation Offload (USO) network acceleration
  - Support Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008

- USB 2.0 Host
  - Support one USB2.0 Host
  - Compatible with USB 2.0 specification
  - Support high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a

- USB 3.0
  - Support DRD (dual role device)
  - Compliant with USB 3.0 Specification, Revision 1.0
  - Compliant with USB Specification, Revision 2.0
  - Compliant with eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
  - Support xHCI Host with up to 64 devices
  - Support Control/Bulk (including stream)/Interrupt/Isochronous Transfer

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- SPI interface
  - Support 2 SPI Controllers
  - Support two chip-select output
  - Support serial-master and serial-slave mode, software-configurable

- I2C Master controller
  - Support 6 I2C ports in Master mode
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100k bits/s in the Standard-mode, up to 400K bits/s in the Fast-mode and up to 1M bit/s in high speed mode

- UART interface
  - Support 8 UART ports
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode for UART1~UART7
  - Support RS485 function for UART1~UART7

- PWM
  - Support 4 PWM interface(PWM0-PWM3), total 28 channels
  - Support input capture mode
  - Support continuous mode and one-shot output mode
  - Support two-stage frequency division of working clock
  - PWM0,PWM2~3 support 8 channel (CH0~CH7) with interrupt-based operation
  - PWM0,PWM2~3 support biphasic counter
  - Only PWM2 support generates waveform through lookup table
  - PWM1 support 4 channel (CH0~CH3) with interrupt-based operation
  - PWM1 support power key capture mode
  - PWM1 support clock frequency meter
  - PWM1 support clock counter

- CAN interface
  - 2 CAN ports
  - Compliance to CAN and CAN FD specification
  - Support CAN standard and extended frame
  - Support data frame, remote frame, overload frame, error frame and frame interval
  - Support Internal Storage Mode
  - Support protocol exception event

- DSMC master interface
  - Support up to select 4 chips, and the selecting signals could be configured to be valid simultaneously in the write transaction
  - Support 8-wire and 16-wire serial transfer mode
  - Support configurable write/read contiguous address merging transaction
  - Support configurable write/read boundary address splitting transaction
  - Support to transform WRAP transfer to INCR transfer
  - Support byte access
  - Support configurable serial address width: 16 bits or 32 bits in different region
  - Support 3 clock mode: normal mode, always-on mode, no-edge-clk mode

1.2.17 Others

- Multiple groups of GPIO
  - All of GPIOs can be used to generate interrupt

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- Support level trigger and edge trigger interrupt
- Support configurable polarity of level trigger interrupt
- Support configurable rising edge, falling edge and both edge trigger interrupt
- Support configurable pull direction (a weak pull-up and a weak pull-down)
- Support configurable drive strength

- Temperature Sensor (TS-ADC)
  - Support User-Defined Mode and Automatic Mode
  - In User-Defined Mode, start_of_conversion can be controlled completely by software, and also can be generated by hardware.
  - In Automatic Mode, the temperature of alarm (high/low temperature) interrupt can be configurable
  - In Automatic Mode, the temperature of system reset can be configurable
  - Support 2 channel TS-ADC (used for CPU and NPU respectively)
  - -40~125°C temperature range and +/-3.5°C temperature accuracy
  - Resolution: 0.01°C

- Successive approximation ADC (SARADC)
  - Support 3 SARADC, each support 8 single-ended input channels
  - 13-bit resolution
  - Up to 2MS/s sampling rate
  - Support single mode and series conversion mode

- OTP
  - Support 8K bits size, 6.5K bits for secure application
  - Support Program/Read/Idle mode

- Package Type
  - FCCSP 491-pin (body: 14mm x 14mm; ball size: 0.25mm; ball pitch: 0.42mm&0.5mm&0.65mm mixed)

1.3 Block Diagram

The following figure shows the basic block diagram.

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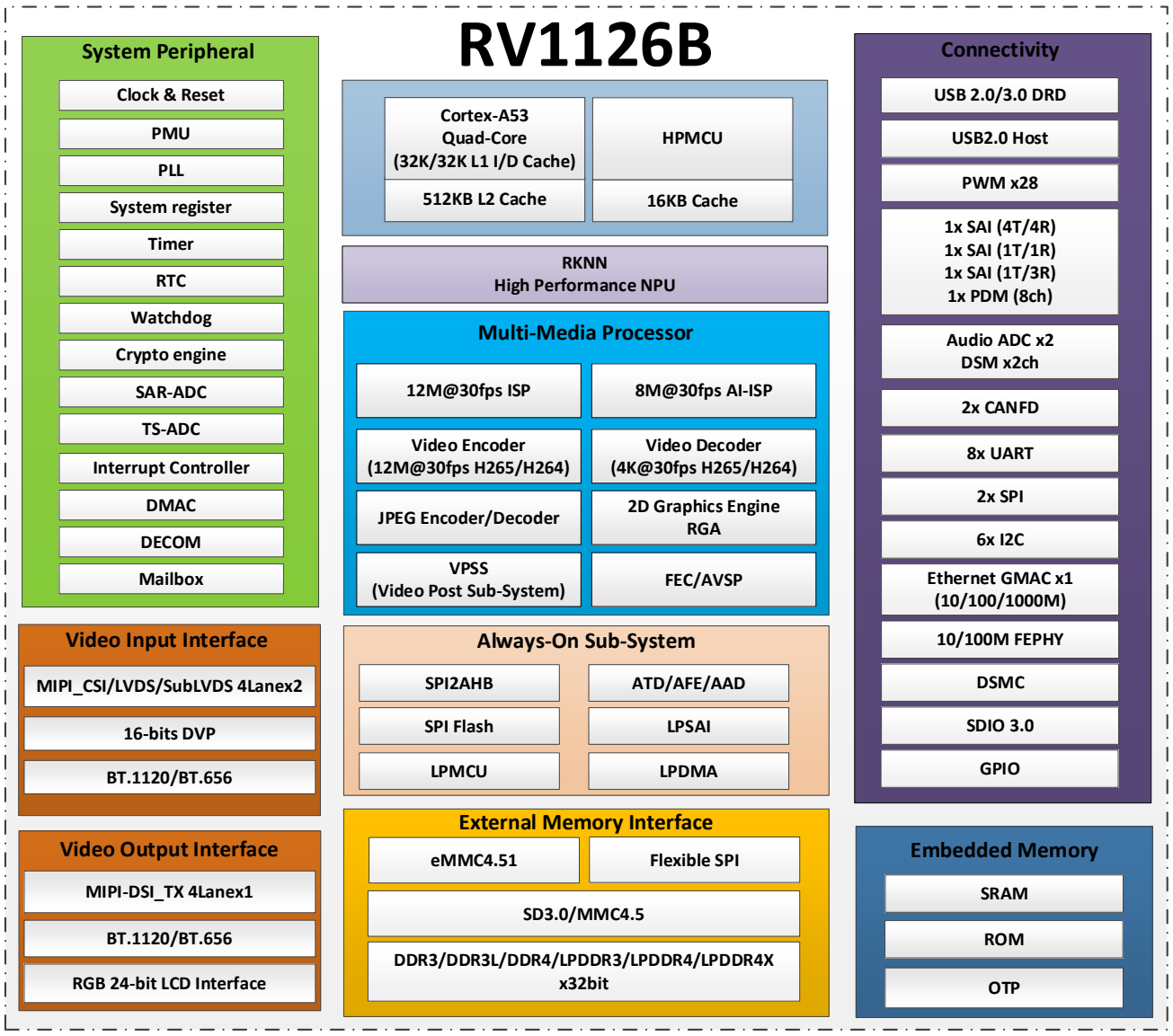

Fig. 1-1 Block Diagram

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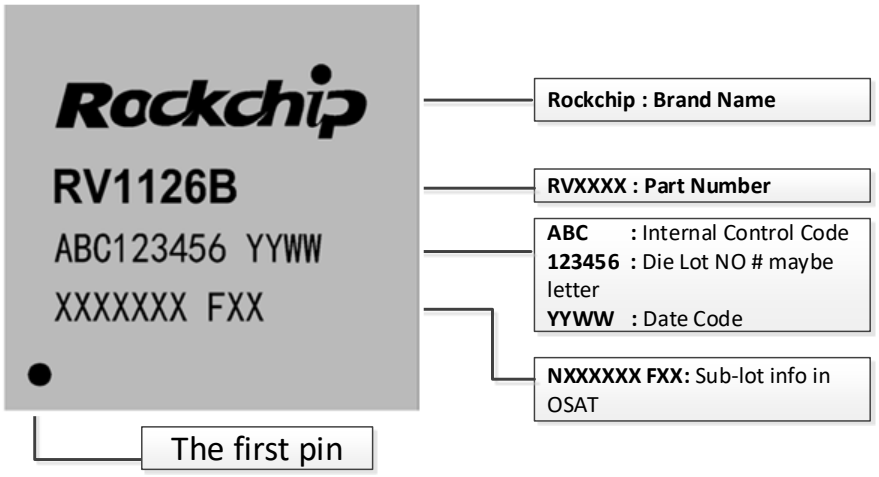
Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Q'ty	Device Feature
RV1126B	RoHS	FCCSP491	1190pcs	Quad-core application processor

2.2 Top Marking



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2.3 Package Dimension

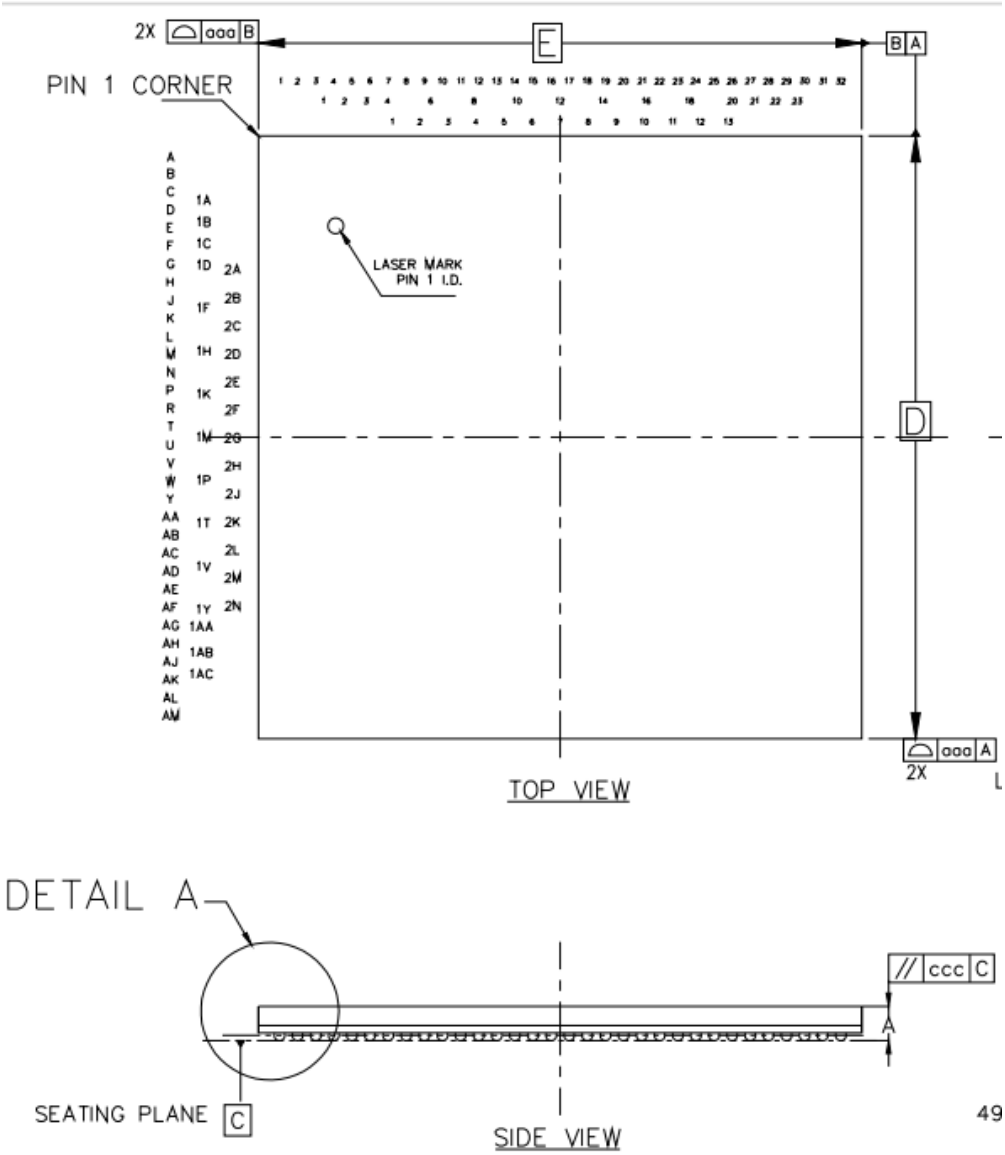

Fig. 2-1 RV1126B Package Top View and Side View

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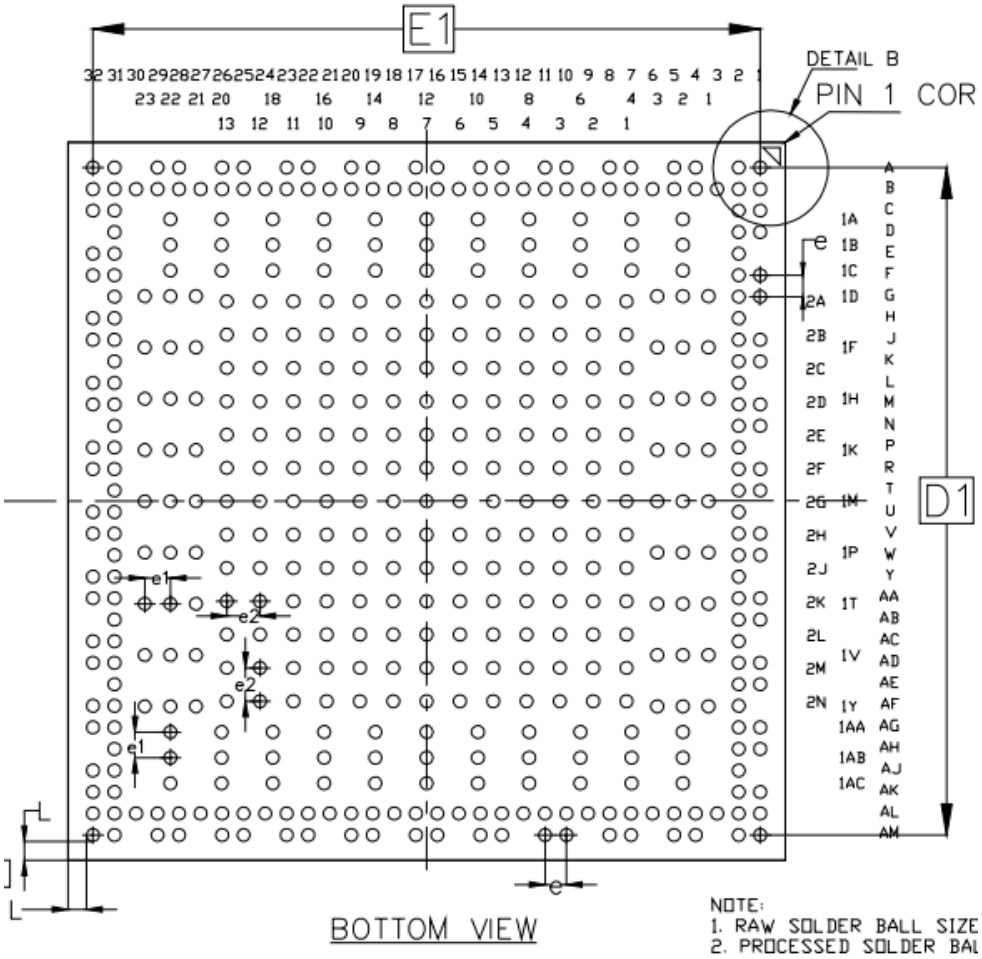

Fig. 2-2 RV1126B Package Bottom View

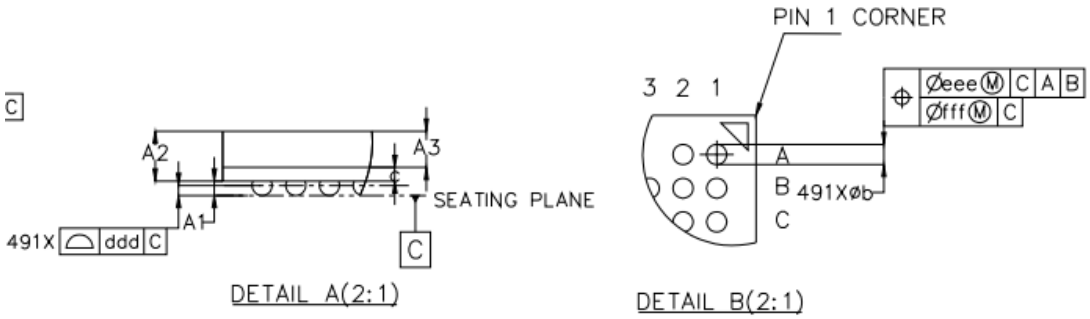

Fig. 2-3 RV1126B PKG Detail A&B

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SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.720	0.800	0.880
A1	0.130	0.180	0.230
A2	0.570	0.620	0.670
A3	0.450 BASIC		
c	0.140	0.170	0.200
D	13.900	14.000	14.100
D1	13.020 BASIC		
E	13.900	14.000	14.100
E1	13.020 BASIC		
e	0.420 BASIC		
e1	0.500 BASIC		
e2	0.650 BASIC		
b	0.200	0.250	0.300
b1	0.210	0.260	0.310
L	0.365 REF		
aaa	0.150		
ccc	0.200		
ddd	0.080		
eee	0.150		
fff	0.050		

Fig. 2-4 RV1126B Package Dimension

2.4 MSL Information

Moisture sensitivity Level ： MSL3

2.5 Lead Finish/Ball material Information

Lead Finish/Ball material ： SnAgCu

2.6 Pin Number List

Table 2-1 RV1126B Pin Number Order Information

Pin Name	Pin#	Pin Name	Pin#
VSS_0	A1	VO_LCDC_D18/ETH_TXCTL_M1/VI_CIF_D14_M1/DSMC_D5/IR_FPA_SDA6/PWM3_CH2_M1/GPIO5_C2	1F23
DDR3_DQ26/DDR4_DQU2_B/LPDDR3_DQ28/LPDDR4_DQ10_B	A2	DDR3_DQ3/DDR4_DQL3_A/LPDDR3_DQ0/LPDDR4_DQ11_A	1H1
DDR3_ODT0/DDR4_CSN0/LPDDR3_ODT0/LPDDR4_A2_B	A4	VSS_40	1H2
DDR3_CKE/DDR4_ACTN/LPDDR3_CKE/LPDDR4_A3_B	A5	DDR3_DQ6/DDR4_DQL6_A/LPDDR3_DQ5/LPDDR4_DQ14_A	1H3
DDR3_ODT1/DDR4_BG0/LPDDR3_ODT1/LPDDR4_CSN1_A	A7	VO_LCDC_D13/ETH_MDIO_M1/VI_CIF_D9_M1/DSMC_DQS0/UART7_RX_M0/GPIO5_B5	1H21
DDR3_A12/DDR4_A5/LPDDR4_ODT0_B	A8	VO_LCDC_D12/VI_CIF_D8_M1/DSMC_CSN0/UART7_TX_M0/GPIO5_B4	1H22
DDR3_A1/DDR4_A8/LPDDR3_A1/LPDDR4_CKE0_A	A10	VO_LCDC_D10/ETH_RXD1_M1/VI_CIF_D6_M1/DSMC_RESETN/DSMC_INT1/PWM2_CH0_M1/UART6_RTSN_M0/GPIO5_B2	1H23
DDR3_A5/DDR4_A9/LPDDR3_A5/LPDDR4_A5_A	A11	DDR3_DQS0P/DDR4_DQSL_P_A/LPDDR3_DQS0P/LPDDR4_DQS1P_A	1K1

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Pin Name	Pin#	Pin Name	Pin#
DDR3_A0/DDR4_ODT1/LPDDR3_A0/LPDDR4_ODT1_B	A13	DDR3_DQS0N/DDR4_DQSL_N_A/LPDDR3_DQS0N/LPDDR4_DQS1N_A	1K2
DDR3_A14/DDR4_A14_WEN/LPDDR4_CSN1_B	A14	VSS_41	1K3
SAI2_SDI1_M0/UART1_RX_M1/I2C5_SDA_M1/GPIO3_B7	A16	SARADC2_IN3/VI_CIF_D15_M0/ETH_MDIO_M0/PDM_CLK1_M1/UART7_CTSN_M1/GPIO6_B7	1K21
SAI2_SDI2_M0/UART2_TX_M0/GPIO3_B1	A17	VSS_42	1K22
VSS_1	A19	VO_LCDC_D9/ETH_RXD0_M1/VI_CIF_D5_M1/DSMC_D8/IR_FPA_SDA3/UART6_RX_M0/GPIO5_B1	1K23
SDMMC1_D2/GPIO3_A4	A20	DDR3_DM0/DDR4_DML_A/LPDDR3_DM0/LPDDR4_DM1_A	1M1
SDMMC1_D0/I2C1_SCL_M1/GPIO3_A2	A22	VSS_43	1M2
SDMMC1_D1/I2C1_SDA_M1/GPIO3_A3	A23	DDR3_DQ1/DDR4_DQL1_A/LPDDR3_DQ6/LPDDR4_DQ9_A	1M3
FEPHY_TXN	A25	VI_CIF_D12_M0/ETH_MCLK_M0/SPI1_CLK_M0/PDM_CLK0_M1/UART7_TX_M1/GPIO6_B4	1M21
FEPHY_TXP	A26	SARADC2_IN1/VI_CIF_D13_M0/ETH_RXCTL_M0/PDM_SDI0_M1/UART7_RX_M1/GPIO6_B5	1M22
MIPI_DPHY_DSI_TX_D1N	A28	SARADC2_IN2/VI_CIF_D14_M0/PDM_SDI1_M1/UART7_RTSN_M1/GPIO6_B6	1M23
MIPI_DPHY_DSI_TX_D1P	A29	DDR3_DQ7/DDR4_DQL7_A/LPDDR3_DQ1/LPDDR4_DQ15_A	1P1
MIPI_DPHY_DSI_TX_D2P	A31	VSS_44	1P2
AVSS1_0	A32	FSPI0_D1/SAI1_SCLK_M0/GPIO1_B5	1P3
DDR3_DQ25/DDR4_DQU1_B/LPDDR3_DQ31/LPDDR4_DQ9_B	B1	VI_CIF_D9_M0/ETH_TXCTL_M0/SPI1_CSN0_M0/SAI0_SDI1_M1/SAI0_SDO3_M1/UART6_RX_M1/GPIO6_B1	1P21
DDR3_DQ27/DDR4_DQU3_B/LPDDR3_DQ29/LPDDR4_DQ11_B	B2	VI_CIF_D10_M0/ETH_RXD0_M0/SPI1_MOSI_M0/PDM_SDI2_M1/UART6_RTSN_M1/GPIO6_B2	1P22
VSS_2	B3	VI_CIF_D11_M0/ETH_RXD1_M0/SPI1_MISO_M0/PDM_SDI3_M1/UART6_CTSN_M1/GPIO6_B3	1P23
DDR3_CASN/DDR4_CKE/LPDDR4_A1_B	B4	FSPI0_D3/SAI1_SDI_M0/GPIO1_B6	1T1
DDR3_CSN0/DDR4_ODT0/LPDDR3_CSN0/LPDDR4_A4_B	B5	FSPI0_D0/SAI1_LRCK_M0/GPIO1_B4	1T2
VSS_3	B6	FSPI0_D2/SAI1_SDO_M0/GPIO1_B2	1T3
DDR3_A11/DDR4_A16_RASN/LPDDR4_CSN0_B	B7	SPI0_CSN0_M1/SAI1_SDI_M1/PWM0_CH6_M1/UART5_TX_M0/I2C4_SDA_M2/GPIO4_A6	1T21
DDR3_BA2/DDR4_A6/LPDDR4_A0_A	B8	SPI0_CLK_M1/SAI1_SDO_M1/PWM0_CH7_M1/UART5_RX_M0/I2C4_SCL_M2/GPIO4_A7	1T22
VSS_4	B9	SARADC1_IN0/VI_CIF_D0_M0/ETH_PPSTRIG_M0/CAN0_RXD_M1/SAI0_SCLK_M1/PWM1_CH0_M2/UART4_TX_M2/I2C3_SCL_M3/GPIO6_A0	1T23
DDR3_BA0/DDR4_CSN1	B10	FSPI0_CSN0/SAI1_MCLK_M0/GPIO1_B0	1V1
DDR3_CSN1/DDR4_BA0/LPDDR3_CSN1/LPDDR4_CSN0_A	B11	EMMC_D2/FSPI1_D2_M1/PWM3_CH2_M0/GPIO1_A2	1V2
VSS_5	B12	EMMC_D1/FSPI1_D1_M1/PWM3_CH1_M0/GPIO1_A1	1V3
DDR3_A3/DDR4_A0/LPDDR3_A3/LPDDR4_CKE1_A	B13	SPI0_CSN1_M1/SAI1_MCLK_M1/PWM0_CH5_M1/UART4_TX_M0/GPIO4_A3	1V21
DDR3_A13/DDR4_A13/LPDDR4_A3_A	B14	SPI0_MOSI_M1/SAI1_SCLK_M1/I2C3_SCL_M1/GPIO4_A4	1V22
VSS_6	B15	VSS_45	1V23
SPI1_CSN1_M1/SAI2_MCLK_M0/SDMMC1_D	B16	VSS_46	1Y1

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Pin Name	Pin#	Pin Name	Pin#
ETN/UART1_TX_M1/I2C5_SCL_M1/GPIO3_B6			
UART2_RX_M0/GPIO3_B0	B17	VSS_47	1Y2
UART2_CTSN_M0/GPIO3_A7	B18	VSS_48	1Y3
UART2_RTSN_M0/GPIO3_A6	B19	SAI0_SCLK_M0/PWM2_CH4_M1/GPIO7_A0	1Y21
SDMMC1_D3/GPIO3_A5	B20	VSS_49	1Y22
SDMMC1_CMD/GPIO3_A1	B21	PWM0_CH4_M1/UART4_RX_M0/GPIO4_A2	1Y23
SDMMC1_CLK/GPIO3_A0	B22	USB_DRD_VBUSDET	1AA2
VSS_7	B23	FSPI1_D1_M0/SPI0_MISO_M0/GPIO0_B1	1AA4
FEPHY_RXN	B24	FSPI1_D2_M0/SPI0_CSN1_M0/GPIO0_A6	1AA6
FEPHY_RXP	B25	I2C2_SCL_M0/PWM0_CH4_M0/GPIO0_D0	1AA8
AVSS1_1	B26	SPI2AHB_D2/PWM0_CH1_M0/UART1_RX_M0/I2C5_SDA_M0/GPIO0_C5	1AA10
MIPI_DPHY_DSI_TX_D0N	B27	SPI2AHB_CSN0/I2C0_SCL_M0/GPIO0_C2	1AA12
MIPI_DPHY_DSI_TX_D0P	B28	SAI0_SDI3_M0/SAI0_SDO1_M0/PDM_SDI3_M0/UART2_RTSN_M1/GPIO7_A7	1AA14
MIPI_DPHY_DSI_TX_CLKN	B29	SAI0_MCLK_M0/PWM2_CH6_M1/GPIO7_A2	1AA16
MIPI_DPHY_DSI_TX_CLKP	B30	SDMMC0_D3/UART3_TX_M0/UART4_CTSN_M3/JTAG_TMS_M1/GPIO2_A3	1AA18
MIPI_DPHY_DSI_TX_D2N	B31	SDMMC0_D1/UART0_TX_M0/I2C0_SCL_M1/GPIO2_A1	1AA20
MIPI_DPHY_DSI_TX_D3N	B32	I2C4_SCL_M3/PDM_CLK1_M0/PWM2_CH5_M1/GPIO7_A1	1AA22
DDR3_DQ24/DDR4_DQU0_B/LPDDR3_DQ30/LPDDR4_DQ8_B	C1	USB_DRD_ID	1AB2
VSS_8	C2	FSPI1_D0_M0/SPI0_MOSI_M0/GPIO0_B0	1AB4
AVSS1_2	C31	PWR_CTRL1/GPIO0_A4	1AB6
MIPI_DPHY_DSI_TX_D3P	C32	SPI2AHB_D0/PWM0_CH3_M0/UART1_CTSN_M0/GPIO0_C7	1AB8
VSS_9	D1	SPI2AHB_D1/PWM0_CH2_M0/UART1_RTSN_M0/GPIO0_C6	1AB10
DDR3_DM3/DDR4_DMU_B/LPDDR3_DM3/LPDDR4_DM1_B	D2	SPI2AHB_CLK/I2C0_SDA_M0/GPIO0_C3	1AB12
VO_LCDC_CLK/SPI1_MISO_M2/DSMC_INT2/PWM1_CH0_M1/UART3_CTSN_M1/GPIO5_D3	D31	SAI0_SDI2_M0/SAI0_SDO2_M0/PDM_SDI2_M0/DSM_AUD_RN/I2C1_SCL_M3/UART2_RX_M1/GPIO7_B0	1AB14
DDR3_DQ31/DDR4_DQU7_B/LPDDR3_DQ27/LPDDR4_DQ15_B	E2	SAI0_SDI0_M0/PDM_SDI0_M0/GPIO7_A6	1AB16
VO_LCDC_HSYNC/SPI1_CLK_M2/ETH_PPSTRIG_M1/DSMC_CSN2/I2C3_SDA_M2/PWM1_CH2_M1/GPIO5_D1	E31	SDMMC0_D2/UART3_RX_M0/UART4_RTSN_M3/JTAG_TCK_M1/TEST_CLK1_OUT/GPIO2_A2	1AB18
VO_LCDC_VSYNC/SPI1_MOSI_M2/DSMC_INT3/PWM1_CH1_M1/UART3_RTSN_M1/GPIO5_D2	E32	SDMMC0_D0/UART0_RX_M0/I2C0_SDA_M1/GPIO2_A0	1AB20
DDR3_DQ29/DDR4_DQU5_B/LPDDR3_DQ25/LPDDR4_DQ13_B	F1	SAI0_LRCK_M0/DSM_AUD_LN/PWM2_CH7_M1/GPIO7_A3	1AB22
DDR3_DQ30/DDR4_DQU6_B/LPDDR3_DQ26/LPDDR4_DQ14_B	F2	FSPI1_CLK_M0/SPI0_CLK_M0/GPIO0_B2	1AC2
VO_LCDC_D20/ETH_RXD3_M1/VI_CIF_VSYNC_M1/DSMC_D3/SAI1_SDO_M2/PWM3_CH4_M1/GPIO5_C4	F31	FSPI1_CSN0_M0/SPI0_CSN0_M0/GPIO0_A7	1AC4
VO_LCDC_DEN/SPI1_CSN0_M2/ETH_PTP_REFCLK_M1/DSMC_CSN3/I2C3_SCL_M2/PWM0_CH6_M2/GPIO5_D0	F32	I2C2_SDA_M0/PWM0_CH5_M0/GPIO0_D1	1AC6
DDR3_DQ28/DDR4_DQU4_B/LPDDR3_DQ24/LPDDR4_DQ12_B	G1	SPI2AHB_D3/PWM0_CH0_M0/UART1_TX_M0/I2C5_SCL_M0/GPIO0_C4	1AC8

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Pin Name	Pin#	Pin Name	Pin#
VSS_10	G2	I2C3_SDA_M0/PWM0_CH6_M0/PWR_CTRL2/GPIO0_C1	1AC10
VO_LCDC_D19/ETH_RXD2_M1/VI_CIF_D15_M1/DSMC_D4/SAI1_MCLK_M2/PWM3_CH3_M1/GPIO5_C3	G31	I2C3_SCL_M0/PWM0_CH7_M0/GPIO0_C0	1AC12
DDR3_DQ12/DDR4_DQU4_A/LPDDR3_DQ12/LPDDR4_DQ4_B	H2	SAI0_SDI1_M0/SAI0_SDO3_M0/PDM_SDI1_M0/DSM_AUD_RP/I2C1_SDA_M3/UART2_TX_M1/GPIO7_B1	1AC14
VSS_11	H31	I2C4_SDA_M3/PDM_CLK0_M0/UART2_CTSN_M1/GPIO7_A4	1AC16
VO_LCDC_D15/ETH_TXD0_M1/VI_CIF_D11_M1/DSMC_CLKP/PWM2_CH3_M1/UART7_CTSN_M0/GPIO5_B7	H32	SDMMC0_CMD/UART3_CTSN_M0/UART4_TX_M3/GPIO2_A5	1AC18
DDR3_DQ14/DDR4_DQU6_A/LPDDR3_DQ14/LPDDR4_DQ6_B	J1	SDMMC0_CLK/UART3_RTSN_M0/UART4_RX_M3/GPIO2_A4	1AC20
DDR3_DQ13/DDR4_DQU5_A/LPDDR3_DQ13/LPDDR4_DQ5_B	J2	SAI0_SDO0_M0/DSM_AUD_LP/GPIO7_A5	1AC22
VO_LCDC_D14/ETH_MDC_M1/VI_CIF_D10_M1/DSMC_CLKN/DSMC_INT0/PWM2_CH2_M1/UART7_RTSN_M0/GPIO5_B6	J31	DDR3_RESETN/DDR4_RESETN/LPDDR4_RESETN	2A1
VO_LCDC_D16/ETH_TXD1_M1/VI_CIF_D12_M1/DSMC_D7/IR_FPA_SDA4/PWM3_CH0_M1/GPIO5_C0	J32	DDR_RZQ	2A2
DDR3_DQ15/DDR4_DQU7_A/LPDDR3_DQ15/LPDDR4_DQ7_B	K1	VSS_50	2A3
DDR3_DM1/DDR4_DMU_A/LPDDR3_DM1/LPDDR4_DM0_B	K2	VSS_51	2A4
VO_LCDC_D8/ETH_RXCTL_M1/VI_CIF_D4_M1/DSMC_D9/IR_FPA_SDA2/UART6_TX_M0/GPIO5_B0	K31	VSS_52	2A5
VSS_12	L2	VSS_53	2A6
VO_LCDC_D7/SPI0_CSN1_M2/VI_CIF_D3_M1/DSMC_D10/SAI2_LRCK_M1/I2C5_SDA_M2/PWM0_CH0_M1/UART5_CTSN_M1/GPIO5_A7	L31	VSS_54	2A7
VO_LCDC_D6/SPI0_CLK_M2/DSMC_D11/SAI2_SDI0_M1/PWM0_CH1_M1/UART5_RTSN_M1/GPIO5_A6	L32	VSS_55	2A8
DDR3_DQ9/DDR4_DQU1_A/LPDDR3_DQ11/LPDDR4_DQ1_B	M1	VSS_56	2A9
DDR3_DQ8/DDR4_DQU0_A/LPDDR3_DQ10/LPDDR4_DQ0_B	M2	SARADC0_IN6	2A10
VSS_13	M31	FEPHY_REXT	2A11
VO_LCDC_D5/SPI0_MISO_M2/DSMC_D12/SAI2_SCLK_M1/PWM0_CH2_M1/UART5_RX_M1/GPIO5_A5	M32	FEPHY_AVDD_0V9	2A12
DDR3_DQ10/DDR4_DQU2_A/LPDDR3_DQ8/LPDDR4_DQ2_B	N1	AVSS1_4	2A13
DDR3_DQ11/DDR4_DQU3_A/LPDDR3_DQ9/LPDDR4_DQ3_B	N2	VSS_57	2B1
VO_LCDC_D4/SPI0_MOSI_M2/DSMC_D13/SAI2_SDO_M1/PWM0_CH3_M1/UART5_TX_M1/GPIO5_A4	N31	VSS_58	2B2
VSS_14	P2	VSS_59	2B3
VO_LCDC_D3/SPI0_CSN0_M2/DSMC_D14/SAI2_MCLK_M1/PWM0_CH4_M2/UART4_RX_M1/GPIO5_A3	P31	VSS_60	2B4
VO_LCDC_D2/ETH_PPSCLK_M1/VI_CIF_D2_M1/DSMC_D15/SAI2_SDI1_M1/PWM0_CH5_M2/UART4_TX_M1/GPIO5_A2	P32	VSS_61	2B5
DDR3_DQ0/DDR4_DQL0_A/LPDDR3_DQ2/LPDDR4_DQ8_A	R1	VSS_62	2B6
DDR3_DQ2/DDR4_DQL2_A/LPDDR3_DQ4/LPDDR4_DQ10_A	R2	VSS_63	2B7
VO_LCDC_D0/ETH_TXD3_M1/VI_CIF_D0_M1/DSMC_CSN1/IR_FPA_SDA0/PWM2_CH4_M0/	R31	VCCIO3_VCC	2B8

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Pin Name	Pin#	Pin Name	Pin#
UART4_RTSN_M1/GPIO5_A0			
VO_LCDC_D1/I2C5_SCL_M2/VI_CIF_D1_M1/DSMC_DQS1/SAI2_SDI2_M1/IR_FPA_SDA1/PWM2_CH5_M0/UART4_CTSN_M1/GPIO5_A1	R32	SARADC0_AVDD_1V8	2B9
DDR3_DQ5/DDR4_DQL5_A/LPDDR3_DQ7/LPDDR4_DQ13_A	T1	FEPHY_AVDD_3V3	2B10
DDR3_DQ4/DDR4_DQL4_A/LPDDR3_DQ3/LPDDR4_DQ12_A	T2	SARADC0_IN4	2B11
VSS_15	T31	MIPI_DSI_TX0_AVDD_0V9	2B12
VSS_16	U2	AVSS1_5	2B13
SARADC2_IN6/VI_CIF_CLKOUT_M0/ETH_TXCLK_M0/FEPHY_LEDLINK_M2/PWM0_CH2_M2/UART3_TX_M2/GPIO6_C2	U31	VSS_64	2C1
SARADC2_IN5/VI_CIF_CLKIN_M0/ETH_CLK_25M_OUT_M0/PWM0_CH1_M2/UART3_CTSN_M2/GPIO6_C1	U32	VSS_65	2C2
DDR3_DQ18/DDR4_DQL2_B/LPDDR3_DQ23/LPDDR4_DQ2_A	V1	DDR_VDDQ_0	2C3
DDR3_DQ19/DDR4_DQL3_B/LPDDR3_DQ22/LPDDR4_DQ3_A	V2	DDR_VDDQ_1	2C4
SARADC2_IN7/VI_CIF_HSYNC_M0/ETH_RXCLK_M0/FEPHY_LEDSPD_M2/PWM0_CH3_M2/UART3_RX_M2/I2C2_SDA_M2/GPIO6_C3	V31	DDR_VDDQ_2	2C5
SARADC2_IN4/VI_CIF_VSYNC_M0/ETH_MDC_M0/PWM0_CH0_M2/UART3_RTSN_M2/I2C2_SCL_M2/GPIO6_C0	V32	VSS_66	2C6
DDR3_DQ17/DDR4_DQL1_B/LPDDR3_DQ18/LPDDR4_DQ1_A	W1	VSS_67	2C7
DDR3_DM2/DDR4_DML_B/LPDDR3_DM2/LPDDR4_DM0_A	W2	VSS_68	2C8
SARADC2_IN0/VI_CIF_D8_M0/ETH_TXD1_M0/SPI1_CSN1_M0/SAI0_SDI2_M1/SAI0_SDO2_M1/UART6_TX_M1/GPIO6_B0	W31	VSS_69	2C9
DDR3_DQ16/DDR4_DQL0_B/LPDDR3_DQ19/LPDDR4_DQ0_A	Y2	VSS_70	2C10
VSS_17	Y31	FEPHY_AVDD_1V8	2C11
SARADC1_IN7/VI_CIF_D7_M0/ETH_TXD0_M0/PWM2_CH3_M2/SAI0_SDI3_M1/SAI0_SDO1_M1/UART4_CTSN_M2/GPIO6_A7	Y32	MIPI_DSI_TX0_AVDD_1V8	2C12
DDR3_DQS2N/DDR4_DQSL_N_B/LPDDR3_DQS2N/LPDDR4_DQS0N_A	AA1	OTP_VCC_1V8	2C13
VSS_18	AA2	VSS_71	2D1
SARADC1_IN5/VI_CIF_D5_M0/ETH_TXD2_M0/PWM2_CH1_M2/UART5_CTSN_M2/I2C5_SDA_M3/GPIO6_A5	AA31	VSS_72	2D2
SARADC1_IN6/VI_CIF_D6_M0/ETH_TXD3_M0/PWM2_CH2_M2/UART4_RTSN_M2/GPIO6_A6	AA32	DDR_VDDQ_3	2D3
DDR3_DQS2P/DDR4_DQSL_P_B/LPDDR3_DQS2P/LPDDR4_DQS0P_A	AB1	VSS_73	2D4
VSS_19	AB2	VSS_74	2D5
SARADC1_IN4/VI_CIF_D4_M0/ETH_RXD3_M0/SAI0_MCLK_M1/PWM2_CH0_M2/UART5_RTSN_M2/I2C5_SCL_M3/GPIO6_A4	AB31	NPU_DVDD_0	2D6
DDR3_DQ23/DDR4_DQL7_B/LPDDR3_DQ20/LPDDR4_DQ7_A	AC2	NPU_DVDD_1	2D7
SARADC1_IN3/VI_CIF_D3_M0/ETH_RXD2_M0/CAN1_TXD_M1/SAI0_SDI0_M1/PWM1_CH3_M2/UART5_RX_M2/I2C4_SDA_M1/GPIO6_A3	AC31	NPU_DVDD_2	2D8
SARADC1_IN2/VI_CIF_D2_M0/ETH_PPSCLK_M0/CAN1_RXD_M1/SAI0_SDO0_M1/PWM1_CH2_M2/UART5_TX_M2/I2C4_SCL_M1/GPIO6_A2	AC32	VSS_75	2D9

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Pin Name	Pin#	Pin Name	Pin#
DDR3_DQ21/DDR4_DQL5_B/LPDDR3_DQ16/ LPDDR4_DQ5_A	AD1	VSS_76	2D10
DDR3_DQ22/DDR4_DQL6_B/LPDDR3_DQ17/ LPDDR4_DQ6_A	AD2	VSS_77	2D11
VSS_20	AD31	VSS_78	2D12
SARADC1_IN1/VI_CIF_D1_M0/ETH_PTP_REF CLK_M0/CAN0_TXD_M1/SAI0_LRCK_M1/PW M1_CH1_M2/UART4_RX_M2/I2C3_SDA_M3/G PIO6_A1	AD32	FEPHY_LEDLINK_M1/SPI1_CSN1_M2/C AN0_RXD_M0/IR_FPA_FSYNC/I2C2_SC L_M1/PWM0_CH7_M2/UART3_TX_M1/ GPIO5_D4	2D13
DDR3_DQ20/DDR4_DQL4_B/LPDDR3_DQ21/ LPDDR4_DQ4_A	AE1	VSS_79	2E1
VSS_21	AE2	VSS_80	2E2
CAM_CLK0_OUT/UART5_CTSN_M0/GPIO4_B1	AE31	DDR_VDDQ_4	2E3
EMMC_CLK/FSPI1_CLK_M1/GPIO1_B3	AF2	DDR_VDDQL_0	2E4
CAM_CLK1_OUT/UART5_RTSN_M0/GPIO4_B0	AF31	LOGIC_DVDD_0	2E5
SPI0_MISO_M1/SAI1_LRCK_M1/I2C3_SDA_M 1/GPIO4_A5	AF32	NPU_DVDD_3	2E6
EMMC_CMD/FSPI1_CSN0_M1/GPIO1_B1	AG1	NPU_DVDD_4	2E7
FSPI0_CLK/GPIO1_B7	AG2	NPU_DVDD_5	2E8
CAM_CLK3_OUT/UART4_RTSN_M0/I2C1_SDA _M2/GPIO4_A0	AG31	VSS_81	2E9
CAM_CLK2_OUT/UART4_CTSN_M0/I2C1_SCL _M2/GPIO4_A1	AG32	LOGIC_DVDD_3	2E10
EMMC_D7/PWM3_CH7_M0/GPIO1_A7	AH1	VSS_82	2E11
EMMC_D6/PWM3_CH6_M0/GPIO1_A6	AH2	VCCIO5_VCC_0	2E12
VSS_22	AH31	VO_LCDC_D11/ETH_MCLK_M1/VI_CIF_ D7_M1/DSMC_RDYN/PWM2_CH1_M1/U ART6_CTSN_M0/GPIO5_B3	2E13
EMMC_D5/FSPI0_CSN1/PWM3_CH5_M0/GPI O1_A5	AJ2	VSS_83	2F1
MIPI_DPHY_CSI_RX1_D0N	AJ31	VSS_84	2F2
MIPI_DPHY_CSI_RX1_D0P	AJ32	DDR_VDDQ_5	2F3
EMMC_D4/PWM3_CH4_M0/GPIO1_A4	AK1	DDR_VDDQL_1	2F4
EMMC_D3/FSPI1_D3_M1/PWM3_CH3_M0/GPI O1_A3	AK2	LOGIC_DVDD_1	2F5
VSS_23	AK31	VSS_85	2F6
MIPI_DPHY_CSI_RX1_D1N	AK32	VSS_86	2F7
EMMC_D0/FSPI1_D0_M1/PWM3_CH0_M0/GPI O1_A0	AL1	VSS_87	2F8
USB_DRD_DP	AL2	VSS_88	2F9
USB_HOST_DM	AL3	LOGIC_DVDD_4	2F10
USB_HOST_DP	AL4	VSS_89	2F11
VSS_24	AL5	VCCIO5_VCC_1	2F12
USB_DRD_SSRXP	AL6	VSS_90	2F13
USB_DRD_SSRXN	AL7	VSS_91	2G1
VSS_25	AL8	VSS_92	2G2
UART0_RX_M2/PWM1_CH3_M0/I2C1_SDA_M 0/JTAG_TMS_M0/GPIO0_B4	AL9	VSS_93	2G3
SDMMC0_DETN/PWM1_CH0_M0/GPIO0_A5	AL10	VSS_94	2G4
FSPI1_D3_M0/PWM1_CH1_M0/TSADC_SHUT/ TSADC_SHUTORG/GPIO0_A1	AL11	LOGIC_DVDD_2	2G5
RTC_32K_OUT/CLK_32K/GPIO0_A2	AL12	VSS_95	2G6
NPOR_DET	AL13	VSS_96	2G7
OSC_XOUT	AL14	VSS_97	2G8
OSC_XIN	AL15	VSS_98	2G9
AVSS3_0	AL16	LOGIC_DVDD_5	2G10
AUDIO_ADC1_MICP	AL17	VSS_99	2G11

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Pin Name	Pin#	Pin Name	Pin#
AUDIO_ADC1_MICN	AL18	VCCIO6_VCC	2G12
VSS_26	AL19	VSS_100	2G13
MIPI_DPHY_CSI_RX0_D3P	AL20	VSS_101	2H1
MIPI_DPHY_CSI_RX0_D3N	AL21	VSS_102	2H2
MIPI_DPHY_CSI_RX0_CLK1P	AL22	VSS_103	2H3
MIPI_DPHY_CSI_RX0_CLK0N	AL23	LOGIC_DVDD_6	2H4
MIPI_DPHY_CSI_RX0_D1P	AL24	VSS_104	2H5
MIPI_DPHY_CSI_RX0_D1N	AL25	CPU_DVDD_1	2H6
VSS_27	AL26	CPU_DVDD_2	2H7
MIPI_DPHY_CSI_RX1_D2P	AL27	CPU_DVDD_3	2H8
MIPI_DPHY_CSI_RX1_D2N	AL28	VSS_105	2H9
MIPI_DPHY_CSI_RX1_CLK1P	AL29	VSS_106	2H10
MIPI_DPHY_CSI_RX1_CLK1N	AL30	VSS_107	2H11
MIPI_DPHY_CSI_RX1_CLK0P	AL31	TSADC_AVDD_1V8/SARADC1&2_AVDD_1V8	2H12
MIPI_DPHY_CSI_RX1_D1P	AL32	VSS_108	2H13
VSS_28	AM1	DDR_VREFOUT	2J1
USB_DRD_DM	AM2	VCCIO1_VCC	2J2
USB_DRD_SSTXP	AM4	VSS_109	2J3
USB_DRD_SSTXN	AM5	PLL_AVDD_1V8	2J4
OSC_RTC_XOUT	AM7	VSS_110	2J5
OSC_RTC_XIN	AM8	CPU_DVDD_4	2J6
UART0_TX_M2/PWM1_CH2_M0/I2C1_SCL_M0/JTAG_TCK_M0/GPIO0_B3	AM10	CPU_DVDD_5	2J7
PWR_CTRL0/GPIO0_A3	AM11	CPU_DVDD_6	2J8
REF_CLK0_OUT/TEST_CLK0_OUT/GPIO0_A0	AM13	CPU_DVDD_0	2J9
VSS_29	AM14	VSS_111	2J10
AUDIO_ADC0_MICP	AM16	VSS_112	2J11
AUDIO_ADC0_MICN	AM17	VCCIO4_VCC	2J12
MIPI_DPHY_CSI_RX0_D2P	AM19	VSS_113	2J13
MIPI_DPHY_CSI_RX0_D2N	AM20	VSS_114	2K1
MIPI_DPHY_CSI_RX0_CLK1N	AM22	USB_AVDD_3V3	2K2
MIPI_DPHY_CSI_RX0_CLK0P	AM23	VSS_115	2K3
MIPI_DPHY_CSI_RX0_D0P	AM25	PLL_AVDD_0V9	2K4
MIPI_DPHY_CSI_RX0_D0N	AM26	PMUIO_VDD0V9/OSC_VDD_0V9	2K5
MIPI_DPHY_CSI_RX1_D3P	AM28	VSS_116	2K6
MIPI_DPHY_CSI_RX1_D3N	AM29	VSS_117	2K7
MIPI_DPHY_CSI_RX1_CLK0N	AM31	VSS_118	2K8
VSS_30	AM32	VSS_119	2K9
DDR3_CLKN/DDR4_CLKN/LPDDR3_CLKN/LPDDR4_CLKN_B	1A2	VSS_120	2K10
DDR3_A10/DDR4_A15_CASN/LPDDR4_A0_B	1A4	MIPI_DPHY_CSI_RX1_AVDD_1V8	2K11
DDR3_A15/DDR4_A3/LPDDR4_A5_B	1A6	MIPI_DPHY_CSI_RX1_AVDD_0V9	2K12
DDR3_A4/DDR4_A7/LPDDR3_A4/LPDDR4_ODT0_A	1A8	VSS_121	2K13
VSS_31	1A10	VSS_122	2L1
DDR3_A7/DDR4_A11/LPDDR3_A7/LPDDR4_A2_A	1A12	USB_AVDD_1V8_0	2L2
SPI1_CLK_M1/SAI2_SCLK_M0/PWM2_CH2_M0/UART1_RTSN_M1/I2C4_SCL_M0/FEPHY_LEDLINK_M0/GPIO3_B4	1A14	USB_AVDD_1V8_1	2L3
SPI1_CSN0_M1/SAI2_LRCK_M0/PWM2_CH3_M0/UART1_CTSN_M1/I2C4_SDA_M0/FEPHY_	1A16	PMUIO0_VCC3V3	2L4

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Pin Name	Pin#	Pin Name	Pin#
LEDSPD_M0/GPIO3_B5			
SARADC0_IN2	1A18	PMUIO0_LDO3V3	2L5
SARADC0_IN7_BOOT	1A20	AUDIO_ADC1_VCM	2L6
UART0_TX_M1/JTAG_TCK_M2/CAN1_RXD_M0 /PWM2_CH6_M0/GPIO5_D6	1A22	AVSS3_1	2L7
DDR3_CLKP/DDR4_CLKP/LPDDR3_CLKP/LPD DR4_CLKP_B	1B2	VSS_123	2L8
VSS_32	1B4	VCCIO7_VCC	2L9
VSS_33	1B6	VCCIO2_VCC	2L10
VSS_34	1B8	MIPI_DPHY_CSI_RX0_AVDD_1V8	2L11
DDR3_A6/DDR4_A4/LPDDR3_A6/LPDDR4_CL KP_A	1B10	MIPI_DPHY_CSI_RX0_AVDD_0V9	2L12
DDR3_A9/DDR4_A2/LPDDR3_A9/LPDDR4_A4 _A	1B12	VSS_124	2L13
SPI1_MISO_M1/SAI2_SDI0_M0/PWM2_CH1_ M0/PRELIGHT_TRIG_OUT/GPIO3_B3	1B14	USB_AVDD_0V9_0	2M1
SPI1_MOSI_M1/SAI2_SDO_M0/PWM2_CH0_ M0/FLASH_TRIG_OUT/GPIO3_B2	1B16	USB_AVDD_0V9_1	2M2
SARADC0_IN3	1B18	RTC_AVDD	2M3
SARADC0_IN0	1B20	VSS_125	2M4
UART0_RX_M1/JTAG_TMS_M2/CAN1_TXD_M 0/PWM2_CH7_M0/GPIO5_D7	1B22	PMUIO1_VCC	2M5
VSS_35	1C2	AUDIO_ADC0_VCM	2M6
DDR3_RASN/DDR4_A12/LPDDR4_A1_A	1C4	AUDIO_ADC0_VREF	2M7
DDR3_WEN/DDR4_BA1/LPDDR4_CKE1_B	1C6	VSS_126	2M8
DDR3_BA1/DDR4_A1/LPDDR4_CKE0_B	1C8	VSS_127	2M9
DDR3_A8/DDR4_A10/LPDDR3_A8/LPDDR4_C LKN_A	1C10	VSS_128	2M10
DDR3_A2/DDR4_BG1/LPDDR3_A2/LPDDR4_ ODT1_A	1C12	VSS_129	2M11
VSS_36	1C14	VSS_130	2M12
SARADC0_IN5	1C16	VSS_131	2M13
SARADC0_IN1	1C18	VSS_132	2N1
AVSS1_3	1C20	VSS_133	2N2
FEPHY_LEDSPD_M1/CAN0_TXD_M0/IR_FPA_ MCLK/I2C2_SDA_M1/PWM1_CH3_M1/UART3 _RX_M1/GPIO5_D5	1C22	VSS_134	2N3
DDR3_DQS3P/DDR4_DQSU_P_B/LPDDR3_DQ S3P/LPDDR4_DQS1P_B	1D1	VSS_135	2N4
DDR3_DQS3N/DDR4_DQSU_N_B/LPDDR3_D QS3N/LPDDR4_DQS1N_B	1D2	VSS_136	2N5
VSS_37	1D3	VSS_137	2N6
VO_LCDC_D23/ETH_RXCLK_M1/VI_CIF_HSY NC_M1/DSMC_D0/SAI1_SDI_M2/PWM3_CH7 _M1/GPIO5_C7	1D21	AUDIO_ADC_AVDD1V8	2N7
VO_LCDC_D22/ETH_TXCLK_M1/VI_CIF_CLKI N_M1/DSMC_D1/SAI1_LRCK_M2/PWM3_CH6 _M1/GPIO5_C6	1D22	AUDIO_ADC1_VREF	2N8
VO_LCDC_D21/ETH_TXD2_M1/VI_CIF_CLKO UT_M1/DSMC_D2/SAI1_SCLK_M2/PWM3_CH 5_M1/GPIO5_C5	1D23	VSS_138	2N9
DDR3_DQS1P/DDR4_DQSU_P_A/LPDDR3_DQ S1P/LPDDR4_DQS0P_B	1F1	VSS_139	2N10
DDR3_DQS1N/DDR4_DQSU_N_A/LPDDR3_D QS1N/LPDDR4_DQS0N_B	1F2	VSS_140	2N11
VSS_38	1F3	VSS_141	2N12
VSS_39	1F21	VSS_142	2N13
VO_LCDC_D17/ETH_CLK_25M_OUT_M1/VI_C IF_D13_M1/DSMC_D6/IR_FPA_SDA5/PWM3_	1F22		

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Pin Name	Pin#	Pin Name	Pin#
CH1_M1/GPIO5_C1			

2.7 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-2 IO function description list

Interface	Pin Name	Direction	Description
Misc	OSC_ XIN	I	Clock input of 24M crystal XO
	OSC_ XOUT	O	Clock output of 24M crystal XO
	OSC_RTC_XIN	I	Clock input of 32K crystal XO
	OSC_RTC_XOUT	O	Clock output of 32K crystal XO
	REF_CLK0_OUT	O	24M Clock out
	CAM_CLK*i*_OUT (*i*=0~3)	O	Reference Clock Output for external Sensor chip
	CLK_32K	I/O	32K clock If configured as input，clock is provided from external circuit； If configured as output，clock is provided from internal circuit of chip；
	RTC_32K_OUT	O	32K clock out from RTC
	PWR_CTRL*i* (*i*=0~2)	O	Chip low power mode output indication signal
	FEPHY_LEDLINK	O	FEPHY link status indication
	FEPHY_LEDSPD	O	FEPHY speed indication
	FLASH_TRIG_OUT	O	Hold signal for flash light
	PRELIGHT_TRIG_OUT	O	Hold signal for prelight

Interface	Pin Name	Direction	Description
SW-DP	JTAG_TCK_M*i* (*i*=0~2)	I	SWD interface clock input
	JTAG_TMS_M*i* (*i*=0~2)	I/O	SWD interface data input/output

Interface	Pin Name	Direction	Description
eMMC Interface	EMMC_CLK	O	eMMC card clock
	EMMC_CMD	I/O	eMMC card command output and response input
	EMMC_D[*i*] (*i*=0~7)	I/O	eMMC card data input and output

Interface	Pin Name	Direction	Description
SPI	SPI*i*_CLK_M*j* (i=0,1)(*j*=0~2)	I/O	SPI serial clock
	SPI*i*_CSN0_M*j* (i=0,1)(*j*=0~2)	I/O	SPI chip select signal, low active
	SPI*i*_CSN1_M*j* (i=0,1)(*j*=0~2)	O	SPI chip select signal, low active
	SPI*i*_MOSI_M*j* (i=0,1)(*j*=0~2)	I/O	SPI serial data input
	SPI*i*_MISO_M*j* (i=0,1)(*j*=0~2)	I/O	SPI serial data output

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Interface	Pin Name	Direction	Description
FSPI0 Controller	FSPI0_CLK	O	FSPI0 serial clock
	FSPI0_CSN0_M*j* (j=0,1)	O	FSPI0 chip select0 signal, low active
	FSPI0_Di(i=0~3)	I/O	FSPI0 serial data input/output signal

Interface	Pin Name	Direction	Description
FSPI1 Controller	FSPI1_CLK_M*j* (j=0,1)	O	FSPI1 serial clock
	FSPI1_CSN0_M*j* (j=0,1)	O	FSPI1 chip select signal, low active
	FSPI1_D*i*_M*j* (i=0~3) (j=0,1)	I/O	FSPI1 serial data input/output signal

Interface	Pin Name	Direction	Description
SPI2AHB Controller	SPI2AHB_CLK	I	SPI2AHB serial clock
	SPI2AHB_CSN	I	SPI2AHB chip select signal, low active
	SPI2AHB_Di(i=0~3)	I/O	SPI2AHB serial data input/output signal

Interface	Pin Name	Direction	Description
SD/MMC/ SDIO Host Controller	SDMMCi_CLK	O	SDMMC card clock
	SDMMCi_CMD	I/O	SDMMC card command output and response input
	SDMMCi_D[*j*] (*i*=0~1)(j=0~3)	I/O	SDMMC card data input and output

Interface	Pin Name	Direction	Description
SAI0 Controller	SAI0_MCLK_M*j* (j=0~1)	I/O	I2S/PCM/TDM reference clock
	SAI0_SCLK_M*j* (j=0~1)	I/O	I2S/PCM/TDM serial clock
	SAI0_LRCK_M*j* (j=0~1)	I/O	I2S/PCM/TDM channel indication signal
	SAI0_SDO*i*_M*j* (*i*=0~3)(j=0~1)	O	I2S/PCM/TDM serial data output
	SAI0_SDI*i*_M*j* (*i*=0~3)(j=0~1)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
SAI1 Controller	SAI1_MCLK_M*j* (j=0~2)	I/O	I2S/PCM/TDM reference clock
	SAI1_SCLK_M*j* (j=0~2)	I/O	I2S/PCM/TDM serial clock
	SAI1_LRCK_M*j* (j=0~2)	I/O	I2S/PCM/TDM channel indication signal
	SAI1_SDO_M*j* (j=0~2)	O	I2S/PCM/TDM serial data output
	SAI1_SDI_M*j* (j=0~2)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
SAI2 Controller	SAI2_MCLK_M*j* (j=0~1)	I/O	I2S/PCM/TDM reference clock
	SAI2_SCLK_M*j* (j=0~1)	I/O	I2S/PCM/TDM serial clock
	SAI2_LRCK_M*j*	I/O	I2S/PCM/TDM channel indication signal

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Interface	Pin Name	Direction	Description
	(j=0~1)		
	SAI2_SDO_M*j* (j=0~1)	O	I2S/PCM/TDM serial data output
	SAI2_SDI*i*_M*j* (*i*=0~2)(j=0~1)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
PWM	PWM0_CH*i*_Mj(*i*=0~7)(j=0,1,2)	I/O	Pulse Width Modulation input and output
	PWM1_CH*i*_Mj(*i*=0~3) (j=0,1,2)	I/O	Pulse Width Modulation input and output
	PWM2_CH*i*_Mj(*i*=0~7) (j=0,1,2)	I/O	Pulse Width Modulation input and output
	PWM3_CH*i*_Mj(*i*=0~7) (j=0,1)	I/O	Pulse Width Modulation input and output

Interface	Pin Name	Direction	Description
I2C	I2C*0*_SDA_Mj (j=0,1)	I/O	I2C0 data
	I2C*0*_SCL_Mj (j=0,1)	O	I2C0 clock
	I2C*2*_SDA_Mj (j=0,1,2)	I/O	I2C2 data
	I2C*2*_SCL_Mj (j=0,1,2)	O	I2C2 clock
	I2C*i*_SDA_Mj (*i*=1,3,4,5)(j=0~3)	I/O	I2C data
	I2C*i*_SCL_Mj (*i*=1,3,4,5)(j=0~3)	O	I2C clock

Interface	Pin Name	Direction	Description
UART	UART*i*_RX_Mj (*i*=0,3,5) (j=0,1,2)	I	UART serial data input
	UART*i*_TX_Mj (*i*=0,3,5) (j=0,1,2)	O	UART serial data output
	UART*i*_CTSN_Mj (*i*=0,3,5) (j=0,1,2)	I	UART clear to send modem status input
	UART*i*_RTSN_Mj (*i*=0,3,5) (j=0,1,2)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
UART	UART*i*_RX_Mj (*i*=1,2,6,7) (j=0,1)	I	UART serial data input
	UART*i*_TX_Mj (*i*=1,2,6,7) (j=0,1)	O	UART serial data output
	UART*i*_CTSN_Mj (*i*=1,2,6,7) (j=0,1)	I	UART clear to send modem status input
	UART*i*_RTSN_Mj (*i*=1,2,6,7) (j=0,1)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
UART	UART*4*_RX_Mj (j=0,1,2,3)	I	UART serial data input

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Interface	Pin Name	Direction	Description
	UART*4*_TX_Mj (j=0,1,2,3)	O	UART serial data output
	UART*4*_CTSN_Mj (j=0,1,2,3)	I	UART clear to send modem status input
	UART*4*_RTSN_Mj (j=0,1,2,3)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
FEPHY	FEPHY_REXT	O	External 6K-Ohm resistor to ground
	FEPHY_RXN	I	FEPHY transceiver negative input
	FEPHY_RXP	I	FEPHY transceiver positive input
	FEPHY_TXN	O	FEPHY transceiver negative output
	FEPHY_TXP	O	FEPHY transceiver positive output

Interface	Pin Name	Direction	Description
ACODEC	AUDIO_ADCi_MICN(i=0,1)	I	ADC channel negative input
	AUDIO_ADCi_MICP (i=0,1)	I	ADC channel positive input
	AUDIO_ADCi_VREF (i=0,1)	O	Microphone bias output
	AUDIO_ADCi_VCM (i=0,1)	O	Reference voltage output

Interface	Pin Name	Direction	Description
MIPI_RX	MIPI_DPHY_CSI_RX*i*_CK0N (i=0,1)	I	MIPI_RX PHY negative clock input
	MIPI_DPHY_CSI_RX*i*_CK0P (i=0,1)	I	MIPI_RX PHY positive clock input
	MIPI_DPHY_CSI_RX*i*_CK1N (i=0,1)	I	MIPI_RX PHY negative clock input
	MIPI_DPHY_CSI_RX*i*_CK1P (i=0,1)	I	MIPI_RX PHY positive clock input
	MIPI_DPHY_CSI_RX*i*_D*j*N (i=0,1)(j=0~3)	I	MIPI_RX PHY negative data input
	MIPI_DPHY_CSI_RX*i*_D*j*P (i=0,1)(j=0~3)	I	MIPI_RX PHY positive data input

Interface	Pin Name	Direction	Description
MIPI_TX	MIPI_DPHY_DSI_TX_CKN	O	MIPI_TX PHY negative clock output
	MIPI_DPHY_DSI_TX_CKP	O	MIPI_TX PHY positive clock output
	MIPI_DPHY_DSI_TX_D*j*N (j=0~3)	O	MIPI_TX PHY negative data output
	MIPI_DPHY_DSI_TX_D*j*P (j=0~3)	O	MIPI_TX PHY positive data output

Interface	Pin Name	Direction	Description
USB 2.0	USB_HOST_DP	I/O	USB 2.0 Data signal DP

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	USB_HOST_DM	I/O	USB 2.0 Data signal DM
	USB_DRD_DP	I/O	USB 2.0 Data signal DP
	USB_DRD_DM	I/O	USB 2.0 Data signal DM

Interface	Pin Name	Direction	Description
USB 3.0	USB_DRD_SSRXN	I	USB 3.0 Data signal RXN
	USB_DRD_SSRXP	I	USB 3.0 Data signal RXP
	USB_DRD_SSTXN	O	USB 3.0 Data signal RXN
	USB_DRD_SSTXP	O	USB 3.0 Data signal RXP

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Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for CPU	CPU_ DVDD	-0.3	1.25	V
Supply voltage for NPU	NPU_DVDD	-0.3	1.1	V
Supply voltage for LOGIC	LOGIC_DVDD	-0.3	1.1	V
Supply voltage for PMUIO0	PMUIO0_VCC3V3 PMUIO0_LDO3V3	-0.3	3.8	V
Supply voltage for PMUIO1	PMUIO1_VCC	-0.3	3.8	V
Supply voltage for VCCIO1	VCCIO1_VCC	-0.3	3.8	V
Supply voltage for VCCIO2	VCCIO2_VCC	-0.3	3.8	V
Supply voltage for VCCIO3	VCCIO3_VCC	-0.3	3.8	V
Supply voltage for VCCIO4	VCCIO4_VCC	-0.3	3.8	V
Supply voltage for VCCIO5	VCCIO5_VCC	-0.3	3.8	V
Supply voltage for VCCIO6	VCCIO6_VCC	-0.3	3.8	V
Supply voltage for VCCIO7	VCCIO7_VCC	-0.3	3.8	V
Supply voltage for FEPHY	FEPHY_AVDD1V8	-0.3	2	V
Supply voltage for FEPHY	FEPHY_AVDD3V3	-0.3	3.8	V
Supply voltage for RTC	RTC_AVDD	-0.3	3.8	V
0.9V supply voltage	FEPHY_AVDD_0V9 PLL_AVDD_0V9 MIPI_DPHY_CSI_RX0_AVDD_0V9 MIPI_DPHY_CSI_RX1_AVDD_0V9 MIPI_DPHY_DSI_TX_AVDD_0V9 USB_AVDD_0V9 USB3_AVDD_0V9 PMUIO_VDD0V9	-0.3	1.1	V
1.8V supply voltage	AUDIO_ADC_AVDD_1V8 SARADC0_AVDD_1V8 SARADC1_AVDD_1V8 PLL_AVDD_1V8 USB_AVDD_1V8/USB3_AVDD_1V8 MIPI_DPHY_CSI_RX0_AVDD_1V8 MIPI_DPHY_CSI_RX1_AVDD_1V8 MIPI_DPHY_DSI_TX_AVDD_1V8	-0.3	2.0	V
3.3V supply voltage	USB_AVDD_3V3	-0.3	3.8	V
Supply voltage for DDR IO	DDR_VDDQ	-0.3	1.65	V
Storage Temperature	Tstg	-40	125	℃
Max Conjunction Temperature	Tj	NA	125	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Related Power Group	Min	Typ	Max	Unit
Supply voltage for CPU	CPU_ DVDD	0.81	0.95	1.21	V
Supply voltage for NPU	NPU_DVDD	0.81	0.95	1.05	V
Supply voltage for LOGIC	LOGIC_DVDD	0.81	0.9	1.00	V
Supply voltage for PMUIO0	PMUIO0_VCC3V3 PMUIO0_LDO3V3	2.97	3.3	3.63	V
Supply voltage for PMUIO1	PMUIO1_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO1	VCCIO1_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V

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Parameters	Related Power Group	Min	Typ	Max	Unit
Supply voltage for VCCIO2	VCCIO2_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO3	VCCIO3_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO4	VCCIO4_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO5	VCCIO5_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO6	VCCIO6_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO7	VCCIO7_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for RTC	RTC_AVDD	1.6	3.3	3.63	V
DDR3 IO VDDQ power	DDR_VDDQ	1.425	1.5	1.575	V
DDR3L IO VDDQ Power	DDR_VDDQ	1.283	1.35	1.417	V
LPDDR3 IO VDDQ Power	DDR_VDDQ	0.994	1.2	1.3	V
DDR4 IO VDDQ Power	DDR_VDDQ	0.994	1.2	1.3	V
LPDDR4 IO VDDQ Power	DDR_VDDQ	1.0	1.1	1.21	V
LPDDR4X IO VDDQ Power	DDR_VDDQL	0.54	0.6	0.66	V
0.9V supply voltage	FEPHY_AVDD_0V9 PLL_AVDD_0V9 MIPI_DPHY_CSI_RX0_AVDD_0V9 MIPI_DPHY_CSI_RX1_AVDD_0V9 MIPI_DPHY_DSI_TX_AVDD_0V9 USB_AVDD_0V9 USB3_AVDD_0V9 PMUIO_VDD0V9	0.81	0.9	0.99	V
1.8V supply voltage	AUDIO_ADC_AVDD_1V8 SARADC0_AVDD_1V8 SARADC1_AVDD_1V8 PLL_AVDD_1V8 USB_AVDD_1V8/USB3_AVDD_1V8 MIPI_DPHY_CSI_RX0_AVDD_1V8 MIPI_DPHY_CSI_RX1_AVDD_1V8 MIPI_DPHY_DSI_TX_AVDD_1V8 FEPHY_AVDD1V8	1.62	1.8	1.98	V
3.3V supply voltage	USB_AVDD3V3 FEPHY_AVDD_3V3	2.97	3.3	3.63	V
Ambient Operating Temperature	Ta	-20	25	85	℃

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	NA	43	Kohm
	Pulldown Resistor	Rpd	16	NA	43	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	NA	0.35*VDDO	V
	Input High Voltage	Vih	0.65*VDDO	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	1.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	NA	43	Kohm
	Pulldown Resistor	Rpd	16	NA	43	Kohm

Parameters		Symbol	Min	Typ	Max	Unit
DDR IO @DDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.10	V

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Parameters		Symbol	Min	Typ	Max	Unit
	Output High Voltage	Voh_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.10	V
DDR IO @DDR3L mode	Input High Voltage	Vih_ddr	VREF + 0.09	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.09	V
	Output High Voltage	Voh_ddr	VREF + 0.09	NA	DDR_VDDQ	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.09	V
DDR IO @DDR4 mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.10	V
DDR IO @ LPDDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.10	V
DDR IO @LPDDR4 mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.10	V
DDR IO @LPDDR4X mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDDQL	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	VREF + 0.10	NA	DDR_VDDQL	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.10	V

Parameters		Symbol	Min	Typ	Max	Unit
MIPI IO@ MIPI HS receiver mode	Common-mod voltage HS receive mode	VCMRX(DC)	70	NA	300	mV
	Differential input high threshold	VIDTH	NA	NA	70	mV
	Differential input low threshold	VIDTL	-70	NA	NA	mV
	Single-ended input high voltage	VIHHS	NA	NA	460	mV
	Single-ended input low voltage	VILHS	-40	NA	NA	mV
	Single-ended threshold for HS termination enable	VTERM-EN	NA	NA	450	mV
	Differential input impedance	ZID	80	100	125	ohm
MIPI IO@ MIPI LP receiver mode	Logic 1 input voltage	VIH	880	NA	NA	mV
	Logic 0 input voltage, not in ULP State	VIL	NA	NA	550	mV
	Logic 0 input voltage, ULP State	VIL-ULPS	NA	NA	300	mV
	Input hysteresis	VHYST	25	NA	NA	mV
MIPI IO@ 1.8V TTL RX mode	Logic 1 input voltage	VIH	1.2	NA	1.58	V
	Logic 0 input voltage, not in ULP State	VIL	NA	NA	0.6	V
	Input hysteresis	VHYST	25	NA	NA	mV

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	10	uA

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Parameters		Symbol	Test condition	Min	Typ	Max	Unit
			Vin = 3.3V, pulldown enabled	NA	NA	10	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	10	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10	uA
			Vin = 1.8V, pulldown enabled	NA	NA	10	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	10	uA

Note: VDDO and DVDD are both IO power Supply

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for INT PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Int PLL	Input clock frequency(Frac)	F_{in}	Fin = FREF @1.8V/0.99V	10	NA	800	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @3.3V/0.99V	475	NA	1900	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @3.3V/0.99V	9	NA	1900	MHz
	Lock time	T_{lt}	@ 3.3V/0.99V, FREF=24M,REFDIV=1	NA	1000	1500	Input clock cycles

Table 3-6 Electrical Characteristics for FRAC PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Frac PLL	Input clock frequency(Frac)	F_{in}	Fin = FREF @1.8V/0.99V	1	NA	1200	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @3.3V/0.99V	950	NA	3800	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @3.3V/0.99V	19	NA	3800	MHz
	Lock time	T_{lt}	@ 3.3V/0.99V, FREF=24M,REFDIV=1	NA	250	500	Input clock cycles

Notes:

① *REFDIV is the input divider value;*
② *FBDIV is the feedback divider value;*
③ *POSTDIV is the output divider value*

3.6 Electrical Characteristics for USB2.0 Interface

Table 3-7 Electrical Characteristics for USB2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
Output resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	2.7	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V

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Parameters	Symbol	Test condition	Min	Typ	Max	Unit
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode	NA	+-250	NA	mV
		HS mode	NA	+-25	NA	mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	NA	150	mV
Disconnect threshold			570	600	664	mV

3.7 Electrical Characteristics for USB3.0

Table 3-8 Electrical Characteristics for USB3PHY

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Transmitter						
Differential p-pTx voltage swing	VTX-DIFF-PP		0.8	NA	1.2	V
Low power differential p-p Tx voltage swing	VTX-DIFF-PP-LOW		0.4	NA	1.2	V
Tx de-emphasis level ratio	RTX-DIFF-DC		80	NA	120	ohm
Single Ended Output Resistance Matching	RTX-DC-OFFSET		NA	NA	5	%
The amount of voltage change allowed during Receiver Detection	$V_{TX-RCV-DETECT}$		NA	NA	600	mV
Output rising time for 20% to 80%	Tr		25	NA	NA	ps
Output falling time for 20% to 80%	Tf		25	NA	NA	ps
AC Coupling Capacitor	C_{TX}		75	NA	200	nF
Unit Interval	UI		399.88	NA	400.12	ps
Input Voltage Swing	$V_{rxdpp-c}$		250	NA	1200	mV
Input differential impedance	R_{rxd-c}		80	NA	120	ohm
Single Ended input Resistance Matching	$T_{rxd-c-ms}$		NA	NA	5	%

3.8 Electrical Characteristics for DDR IO

Table 3-9 Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
DDR IO @DDR3 mode	Input leakage current		@ 1.5V , 125℃	-80		6	uA
DDR IO @DDR3L mode	Input leakage current		@ 1.35V , 125℃	-65		5	uA
DDR IO @DDR4 mode	Input leakage current		@ 1.2V , 125℃	-50		4	uA
DDR IO @LPDDR3 mode	Input leakage current		@ 1.2V , 125℃	-50		4	uA
DDR IO @LPDDR4 mode	Input leakage current		@ 1.1V , 125℃	-45		3.5	uA
DDR IO @LPDDR4X mode	Input leakage current		@ 0.6V , 125℃	-20		1.5	uA

3.9 Electrical Characteristics for MIPI DSI

Table 3-10 Electrical Characteristics for MIPI DSI

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Parameters	Symbol	Min	Typ	Max	Units
Common-mode variations above 450 MHz	ΔVcmtx(HF)	NA	NA	15	mVrms
Common-mode variations between 50MHz – 450MHz	ΔVcmtx(LF)	NA	NA	25	mVpeak
20%-80% rise time and fall time	Tr and Tf	NA	NA	0.3	UI
		100	NA	NA	ps

3.10 Electrical Characteristics for MIPI CSI interface

Table 3-11 HS Receiver AC specifications (for MIPI mode)

Parameters	Symbol	Min	Typ	Max	Unit
Common-mode interference beyond 450 MHz	ΔVCMRX(HF)	NA	NA	100	mV
Common-mode interference 50MHz – 450MHz	ΔVCMRX(LF)	-50	NA	50	mV
Common-mode termination	CCM	NA	NA	60	pF

Table 3-12 LP Receiver AC specifications (for MIPI mode)

Parameters	Symbol	Min	Typ	Max	Unit
Input pulse rejection	eSPIKE	NA	NA	300	V.ps
Minimum pulse width response	TMIN-RX	20	NA	NA	ns
Peak interference amplitude	VINT	NA	NA	200	mv
Interference frequency	fINT	450	NA	NA	MHz

Table 3-13 HS Receiver AC specifications (for LVDS mode)

Parameters	Symbol	Min	Typ	Max	Unit
Common-mode interference beyond 450 MHz	ΔVCMRX(HF)	NA	NA	100	mV
Common-mode interference 50MHz – 450MHz	ΔVCMRX(LF)	-50	NA	50	mV
Common-mode termination	CCM	NA	NA	50	pF

3.11 Electrical Characteristics for Audio CODEC interface

Table 3-14 Electrical Characteristics for Audio CODEC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Resolution				24		℃
Full Scale Input Range		0dB Gain in PGA state		+/- 1.0		Vrms
Input Resistance	RIN			20		Kohm
Input Capacitance	CIN			10		pF
Negative Gain Range	G(negative)		-9		0	dB
Negative Gain Step				3		dB/Step
Positive Gain Range	G(positive)		0		48	dB
Positive Gain Step				12		dB/Step
Signal to Noise Ratio	SNR	fs=48kHz -60dBFS, A-weighted		94		dB
Total Harmonic Distortion	THD	fs=48kHz -3dBFS, A-weighted		98		dB
Power Supply Rejection	PSRR			90		dB

3.12 Electrical Characteristics for SARADC

Table 3-15 Electrical Characteristics for SARADC

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Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Resolution	ENOB	f_S=1MS/s fclk=24MHz	NA	11.2	13	bit
Analog Input Channel			NA	NA	8	
Analog Input Range	VIN		0	NA	1.8	V
Analog Input maximum voltage					3.3	V
Differential Non-Linearity	DNL		NA	±1	±3	LSB
Integral Non-Linearity	INL		NA	±2	±6	LSB
Conversion Rage	f_S		NA	1	NA	MS/s
Signal to Noise and Distortion Ratio	SINAD	f_S=1MS/s f_{OUT}=1.17KHz	NA	69.2	NA	dB
Total Harmonic Distortion	THD		NA	77.3	NA	dB

3.13 Electrical Characteristics for TSADC

Table 3-16 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Accuracy from -40℃ to 125℃	T_{JACC}		NA	NA	±3.5	℃
Sensing Temperature Range	T_{RANGE}		-40	NA	125	℃
Resolution	T_{LSB}		NA	0.01	NA	℃

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Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Value	Unit	Note
Junction-to-ambient thermal resistance	θ_{JA}	28.1958	(℃/W)	(1)
Junction-to-board thermal resistance	θ_{JB}	6.06026	(℃/W)	(2)
Junction-to-case thermal resistance	θ_{JC}	1.4992	(℃/W)	(3)
Thermal characterization parameter	ψ_{JT}	0.1221	(℃/W)	(4)

*Note (1): The package-board system is placed in the natural convection (JEDEC JESD51-2 standard), and the 2S2P test-board is designed in accordance with JESD 51-7/JESD 51-9. The actual system design and environment may be different.（The PCB is 4 layers, 114.5 mm*101.5 mm）*

Note (2): ϑ_{JB} is measured in the special environment (JEDEC JESD51-8 standard), and the printed circuit board used to mount the devices is specified in JESD51-7.

Note (3): The thermal resistance ϑ_{JC} is provided in compliance with the JEDEC JESD51-14.

Note (4): ψ_{JT} - The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package, ψ_{JT} is measured in the test environment of ϑ_{JA} (JEDEC JESD51-2 standard).

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