Rockchip RV1103B Datasheet

Revision 1.1
October 2024

Chapter 1 Introduction

1.1 Overview

RV1103B is a highly integrated vision processor SoC for IPC, especially for AI related application.

It is based on single-core ARM Cortex-A7 32-bit core which integrates NEON and FPU. The build-in NPU supports INT8 operation. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RV1103B introduces a new generation totally hardware-based maximum 8-Megapixel ISP (image signal processor). It implements a lot of algorithm accelerators, such as HDR, 3A, LSC, 3DNR, 2DNR, sharpening, dehaze, gamma correction and so on. Cooperating with two MIPI CSI interface, users can build a system that receives video data from two camera sensors simultaneously.

The video encoder embedded in RV1103B supports H.265/H.264 video encoding and the multi-stream encoding is supported also. With the help of this feature, the video from camera can be encoded with higher resolution and stored in local memory and transferred another lower resolution video to cloud storage at the same time.

RV1103B has a build-in 16-bit DRAM DDR2/DDR3L capable of sustaining demanding memory bandwidths. Also the RTC, POR and Audio Codec are integrated in RV1103B.

1.2 Features

1.2.1 Application Processor

- Single core ARM Cortex-A7
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD
- Separately Integrated Neon and FPU
- 32KB L1 I-Cache and 32KB L1 D-Cache
- Unified 128KB L2 Cache for Cortex-A7
- TrustZone technology support

1.2.2 Memory Organization

- Internal on-chip memory
  - Bootrom
    - Support system boot from the following device:
      - SPI interface
      - eMMC interface
      - SD/MMC interface
    - Support system code download by the following interface:
      - USB2.0 interface
      - UART interface
  - 32KB system SRAM
  - 8KB PMU SRAM
  - RV1103BG1 SIP 512Mb DDR2
  - RV1103BG2 SIP 1Gb DDR3L
  - RV1103BG3 SIP 2Gb DDR3L

- External off-chip memory
  - eMMC Interface
    - Fully compliant with JEDEC eMMC 4.51 specification
    - Support HS200, but not support CMD Queue
    - Support two data bus width mode: 1bit and 4bits
  - SD/MMC Interface

- Compatible with SD3.0, MMC ver4.51
- Support 1bit, 4bits data bus width

- Flexible Serial Flash Interface (FSPI0)
  - Support transfer data from/to serial flash device
  - Support 1bit, 2bits or 4bits data bus width

1.2.3 System Component

- HPMCU
  - MCU in integrate 16KB Cache
  - Integrated Programmable Interrupt Controller, all IRQ lines connected to GIC for CPU also connect to MCU
  - Integrated Debug Controller with JTAG interface

- CRU (clock & reset unit)
  - Support total 2 PLLs to generate all clocks
  - One oscillator with 24MHz clock input
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component

- PMU (power management unit)
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - Support 3 separate voltage domains，CPU_NPU_DVDD,VDD_LOGIC,VDD_PMU.

- Timer
  - Support 2 secure timers with 64bits counter and interrupt-based operation
  - Support 6 non-secure timers with 64bits counter and interrupt-based operation
  - Support 1 non-secure timers with 64bits counter for low power mode application
  - Support two operation modes: free-running and user-defined count for each timer
  - Support timer work state checkable

- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - One Watchdog for non-secure application
  - One Watchdog for secure application

- Interrupt Controller
  - Support 128 SPI interrupt sources input from different components inside RV1103B
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed, high-level sensitive or rising edge sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Support 2 physical channels
  - Support 12 hardware requests from peripherals
  - Support 16 logic channels, each logic channel support the following feature
    - Support the data transfer of memory-to-memory, memory-to-peripherals, peripherals-to-memory
    - Support Linked list DMA function to complete scatter-gather transfer

- Supports three kinds of multi-block transfer: contiguous address, auto reload, link list

- Secure System
  - Embedded cipher engines
    - Support SHA-1, SHA-256/224 with hardware padding
    - Support HMAC, AEC CBC MAC, AES CMAC
    - Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
    - Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/GCM/CBC-MAC/CMAC mode
    - Support up to 4096 bits PKA mathematical operations for RSA/ECC/SM2
    - Support generating random numbers
  - Support secure OTP
  - Support secure debug
  - Support secure OS
  - Except CPU, the other masters in the SoC can also support security and non-security mode by software-programmable
  - Some slave components in SoC can only be addressed by security master and the other slave components can be addressed by security master or non-security master by software-programmable
  - System SRAM, part of space is addressed only in security mode
  - External DDR space can be divided into 8 parts, each part can be software-programmable to be enabled by each master

- Mailbox
  - One Mailbox in SoC used to service Cortex-A7 and HPMCU communication
  - Support four mailbox elements, each element includes one data word, one command word register and one flag bit that can represent one interrupt
  - Provide 32 lock registers for software to use to indicate whether mailbox is occupied

- Decompression
  - Support for decompressing GZIP files
  - Support the limit size function of the decompressed data to prevent the memory from being maliciously destroyed during the decompression process

- Real Time Clock (RTC)
  - Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz crystal oscillator
  - Support compensation for the second and hour count
  - BCD representation of time, calendar and alarm
  - 12- or 24-hour clock with AM and PM in 12-hour mode
  - Interrupts are separately software maskable
    - Alarm interrupt
    - Periodic interrupt
    - Chip power off interrupt
    - Battery power atypical interrupt

1.2.4 Video CODEC

- Video Encoder
  - HEVC Main Profile, Level 5.0 High Tier
  - H.264 High Profile, level 5.0
  - JPEG Baseline
  - Support up to 3840x2160@25fps
  - Bitrate up to 200Mbps with CBR/VBR/FixQP/QPMAP bitrate control
  - YUV444, YUV420 and YUV400 format
  - Slice split
  - Area and block mapping ROI
  - 8-area OSD

- Link table configuration mode
- YUV/RGB video source with crop, rotation and mirror
- Ultra-low delay encoding
- Motion and Occlusion Detection

1.2.5 Neural Process Unit

- Neural network acceleration engine
- Support integer 8 operation
- Support creating simple custom operators
- Support deep learning frameworks: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, Android NN, etc.

1.2.6 2D Graphics Engine

- 2D Graphics Engine
- Input data:
  - RGB888/RGB565
  - YUV422-P/YUV422-SP-8bit
  - YUV420-P/YUV420-SP-8bit
  - YUV444I/YUV444SP-8bit
  - YVYU422-8bit
  - YUV400-8bit
- Output data:
  - RGB888/RGB565
  - YUV420/YUV422 P/SP
  - YUV400
  - YUV444SP/444I
- Pixel Format conversion, BT.601/BT.709
- Max resolution: 2880x1620 source, 2880x1620 destination
- Scaling
  - Down-scaling: Average filter/Bilinear filter
  - Up-scaling: Bi-cubic filter(Horizontal), Bilinear filter(Vertical)
  - Arbitrary non-integer scaling ratio, from 1/16 to 16
- Rotation
  - 0, 90, 180, 270-degree rotation
  - x-mirror, y-mirror
  - Mirroring and rotation co-operation
- BitBLT
  - Block transfer
  - Color fill
  - Transparency mode (color keying/stencil test, specified value/value range)

1.2.7 Video Input Interface

- MIPI Interface
  - Two MIPI CSI DPHY
    - Each MIPI DPHY V1.2, 2lanes, 1.5Gbps per lane
    - Support to combine 2 DPHY together to one 4lanes
- Video Capture (VICAP)
  - Support receiving two groups of MIPI CSI interfaces, up to four IDs for each group
  - Support VC/DT configurable for each ID
  - Support ten MIPI CSI data formats: RAW8/10/12/14/16, RGB888, YUV422 8bit, YUV422 8bit interlaced, YUV420 8bit, Legacy YUV420 8bit
  - Support three modes of MIPI CSI HDR: virtual channel mode, identification code mode, line counter mode
  - Support RAW rounding
  - Support window cropping
  - Support reducing frame rate
  - Support compact/non-compact output format for RAW data
  - Support NV16/NV12/YUV400/YUYV output format for YUV data

- Support virtual stride when write to DDR
- Support DMA wrap mode
- Support DMA burst gather 2/4/8
- Support QOS(hurry/press)
- Support sending RAW data directly to ISP

- Image Signal Process (ISP)
  - Maximum input: 3840x2160@20fps
  - Minimum input: 264x264
  - Auto Enhance (AE)/Histogram and Auto White Balance (AWB)
  - BLC: Black Level Correction
  - DPCC: Static/Dynamic Defect Pixel Cluster Correction
  - LSC: Lens Shading Correction
  - Bayer-2DNR: Spatial Bayer-raw Noise Reduction
  - Bayer-3DNR: Temporal Bayer-raw Noise Reduction
  - CAC: Chromatic Aberration Correction
  - HDR-Merge: 2-Frame Merge into High-Dynamic Range
  - HDR-DRC: HDR Dynamic Range Compression, Tone mapping
  - GIC: Green Imbalance Correction
  - DeBayer: Advanced Adaptive Demosaic
  - CCM/CSM: Color Correction Matrix, RGB2YUV, etc.
  - Gamma: Gamma out correction
  - HSV: Hue, Saturation,Value Color Palette for Customer
  - LDCH: Lens Distortion Correction only in the Horizontal direction
  - YNR: Spatial luma Noise Reduction in YUV domain
  - CNR: Spatial chroma Noise Reduction in YUV domain
  - Dehaze/Enhance: Automatic Dehaze and effect enhancement
  - localHist：local Histogram to Enhance local contrast
  - Sharp: Image sharpening and boundary filtering
  - CMSK: Privacy cover and mask
  - Gain: Image local gain
  - Multi-sensor reuse ISP, 2 sensors for maximum
  - Bus interface: 32bit AHB configuration, 128bit AXI R/W
  - Low power, auto-gating for each block
  - MI R/W burst group to improve memory utilization
  - MI 3 path output, MP stepless scaling, SP/BP scaling under 1080p

1.2.8 Audio Interface

- SAI
  - Support audio protocol: I2S, PCM, TDM
  - Support up to 128 slots available with configurable size
  - Support slot length 8 to 32 bits configurable
  - Support slot valid data length 8 to 32 bits configurable
  - Support 2 channel TX and 2 channel RX for I2S

- Audio Codec
  - Support one 24-bits ADC channels with 90dB SNR for stereo recording from microphone
  - Support one 24-bits DAC channels with 90dB SNR for stereo playback
  - Support differential and single-ended microphone or line input
  - Sampling rate of 8KHz/12KHz/16KHz/24KHz/32KHz/44.1kHz/48KHz/96KHz

1.2.9 Connectivity

- SDIO interface
  - Compatible with SDIO3.0 protocol
  - 4-bit data bus widths

- MAC 10/100M Ethernet controller and embedded PHY

- Support one Ethernet controllers
- Support 10/100-Mbps data transfer rates with the RMII interfaces
- Support both full-duplex and half-duplex operation

- USB 2.0
  - Compatible with USB 2.0 specification
  - Support one USB 2.0 Host/Device
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a

- SPI interface
  - Support one SPI Controllers
  - Support two chip-select output
  - Support serial-master and serial-slave mode, software-configurable

- I2C Master controller
  - Support five I2C Master(I2C0-I2C4)
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100k bits/s in the Standard-mode, up to 400K bits/s in the Fast-mode and up to 1M bit/s in high speed mode

- UART interface
  - Support three UART interfaces (UART0-UART2)
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode for all UART

- PWM
  - Support three PWM interface(PWM0-PWM2)
  - Support 4 channel (CH0~CH3) with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provides reference mode and output various duty-cycle waveform
  - Only PWM0 support one clock frequency calculation engine and one clock free running counter

1.2.10 Others

- Multiple groups of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction (a weak pull-up and a weak pull-down)
  - Support configurable drive strength

- Temperature Sensor (TS-ADC)
  - Support User-Defined Mode and Automatic Mode
  - In User-Defined Mode, start_of_conversion can be controlled completely by software, and also can be generated by hardware.
  - In Automatic Mode, the temperature of alarm (high/low temperature) interrupt can be configurable

- In Automatic Mode, the temperature of system reset can be configurable
- -40~125°C temperature range and +/-5°C temperature accuracy

- Successive approximation ADC (SARADC)
  - 10-bit resolution
  - Up to 1MS/s sampling rate
  - one single-ended input channels

- OTP
  - Support 8K bits size, 7K bits for secure application
  - Support Program/Read/Idle mode

- Package Type
  - RoHS QFN88 (body: 9mm x 9mm pitch 0.35mm)

1.3 Block Diagram

The following diagram shows the basic block diagram.

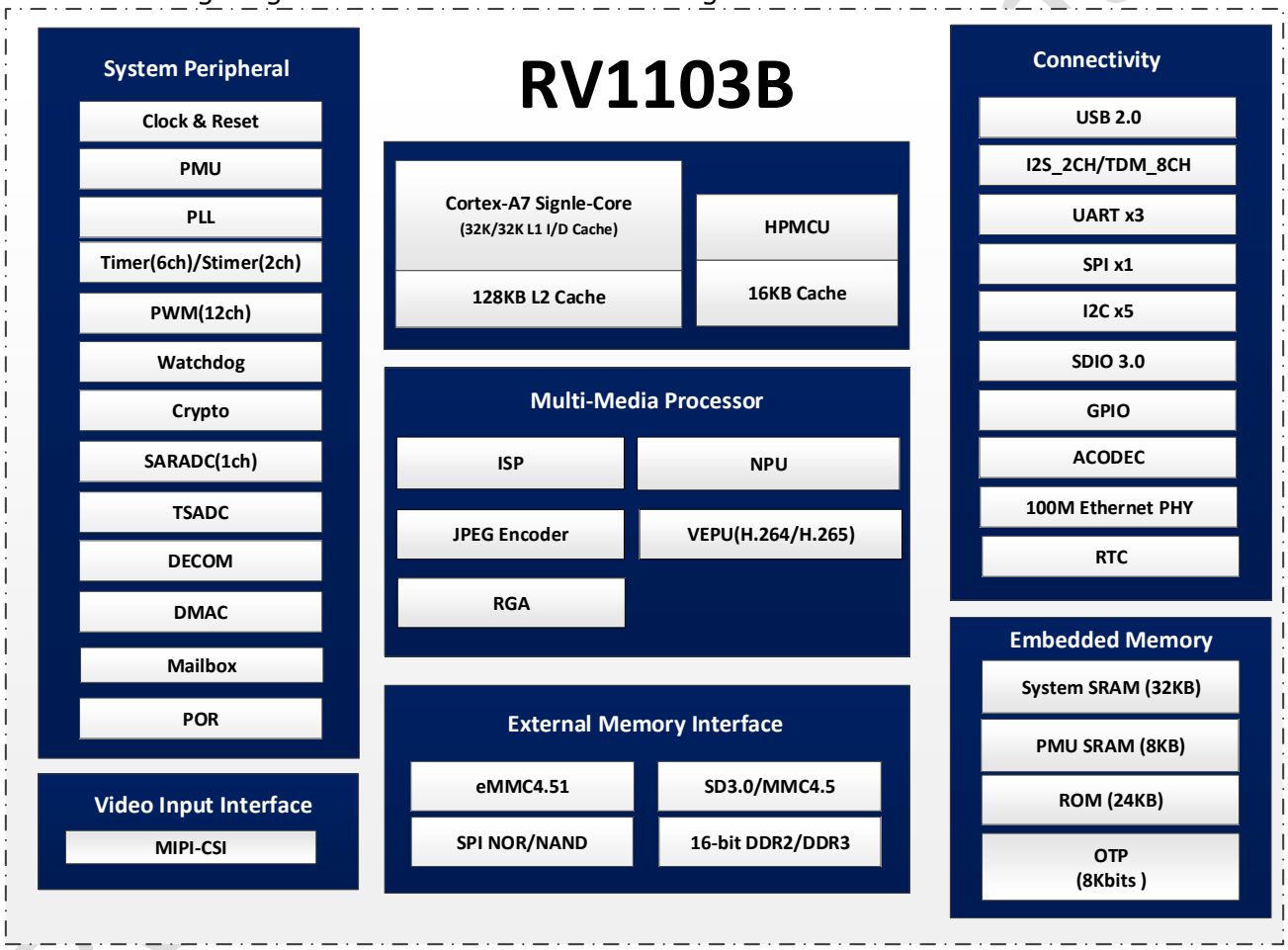

Fig. 1-1 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Q'ty	Device Feature
RV1103BG1	RoHS	QFN88	2600ea/tray	Cortex A7 + MCU +512Mb DDR2
RV1103BG2	RoHS	QFN88	2600ea/tray	Cortex A7 + MCU + 1Gb DDR3L
RV1103BG3	RoHS	QFN88	2600ea/tray	Cortex A7 + MCU + 2Gb DDR3L

2.2 Top Marking

Rockchip : Brand Name

RVXXXXX : Chip Name Prefix

ABC : Subcontractor Code
XXXXXXX : Die Lot NO #
DEFG : Date Code

NXXXXXX: Sub-lot Info in OSAT
GX: Chip Name Suffix

2.3 Package Dimension

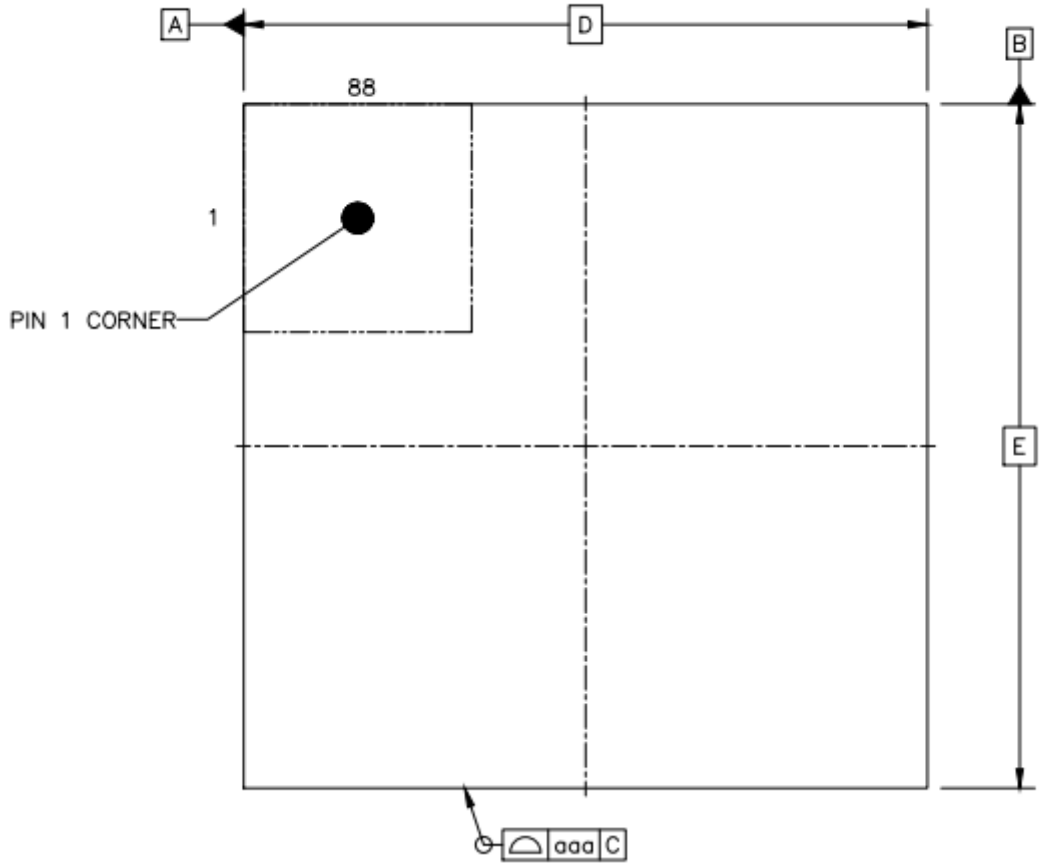

Fig. 2-1 Package Top View

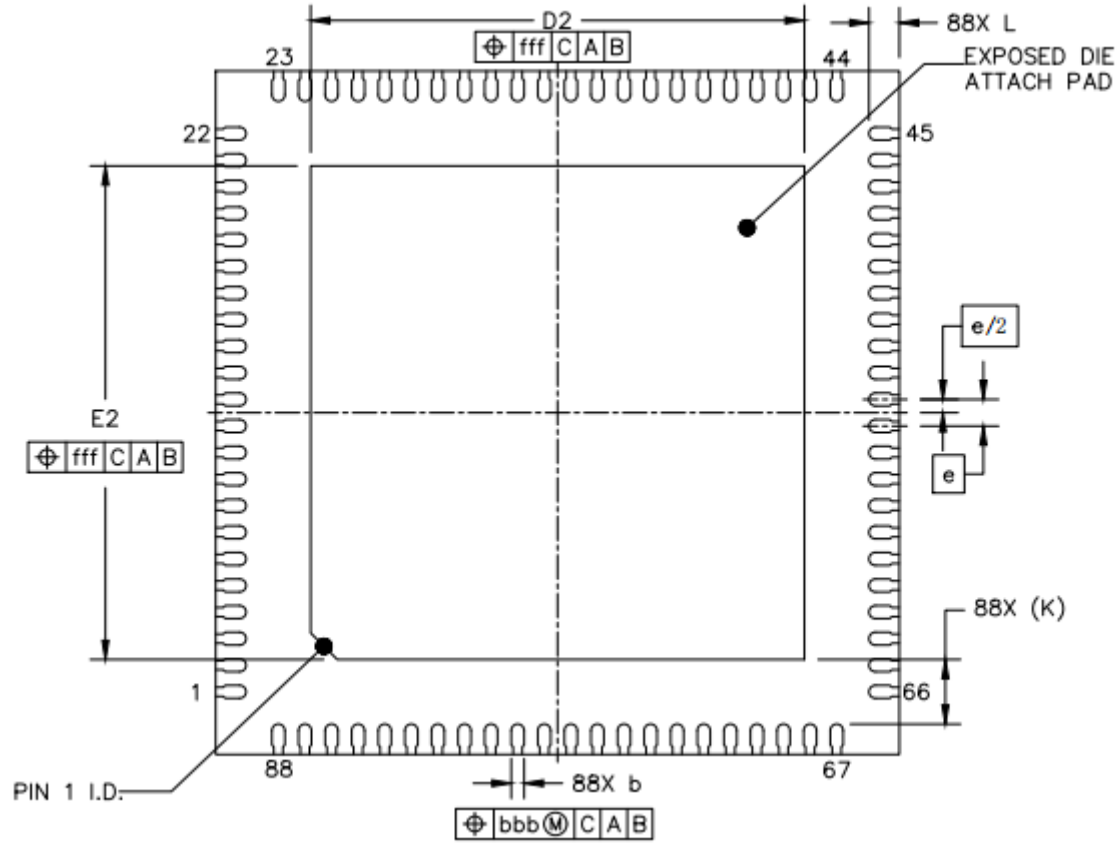

Fig. 2-2 Package Bottom View

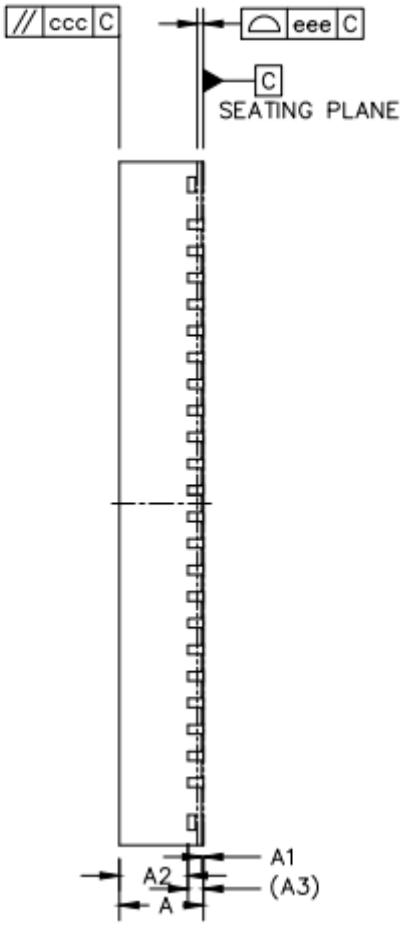

Fig. 2-3 Package Side View

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	1.05	1.1	1.15
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.9	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.10	0.16	0.22
BODY SIZE	X	D		9 BSC	
	Y	E		9 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	6.4	6.5	6.6
	Y	E2	6.4	6.5	6.6
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.85 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

Fig. 2-4 Package Dimension

2.4 MSL Information

Moisture sensitivity Level ： MSL3

2.5 Lead Finish/Ball material Information

Lead Finish/Ball material ： Sn

2.6 Pin Number List

Table 2-1 Pin Number Order Information

Pin	Pin Name	Pin	Pin Name
1	PWR_CTRL1/FSPI1_CS0n/GPIO0_A4_d	45	MIPI_AVDD1V8/VCCIO7_VCC1V8
2	UART0_TX_M0/PWM0_CH1_M0/I2C0_SCL_M0/FSPI1_D2/JTAG_TCK_M0/GPIO0_A5_d	46	CAM_CLK0_OUT/I2C0_SCL_M2/UART2_TX_M2/GPIO1_B5_d
3	UART0_RX_M0/PWM0_CH2_M0/I2C0_SDA_M0/FSPI1_D3/JTAG_TMS_M0/GPIO0_A6_u	47	CAM_CLK1_OUT/I2C0_SDA_M2/UART2_RX_M2/GPIO1_B6_d
4	PMUIO0_DVDD33	48	PWM0_CH1_M2/I2C4_SCL_M1/UART2_RTSN_M2/GPIO1_B7_d
5	RTC_AVDD	49	PWM0_CH2_M2/I2C4_SDA_M1/UART2_CTSN_M2/GPIO1_C0_d
6	OSC_RTC_XOUT	50	DVDD_LOGIC
7	OSC_RTC_XIN	51	VCCIO4_DVDD1833
8	DVDD_LOGIC	52	SDMMC0_DETN/GPIO1_A6_u
9	SDMMC1_D1/UART1_RTSN_M3/PWM0_CH0_M1/SPI0_CS1n_M1/GPIO2_A0_d	53	SDMMC0_D1/UART1_RX_M1/PWM2_CH1_M0/GPIO1_A7_d
10	SDMMC1_D0/UART1_CTSN_M3/PWM0_CH1_M1/SPI0_MOSI_M1/GPIO2_A1_d	54	SDMMC0_D0/UART1_TX_M1/PWM2_CH0_M0/GPIO1_B0_d
11	SDMMC1_CLK/UART1_TX_M3/PWM0_CH2_M1/SPI0_CLK_M1/GPIO2_A2_d	55	SDMMC0_CLK/UART1_RTSN_M1/GPIO1_B1_d
12	SDMMC1_CMD/UART1_RX_M3/PWM1_CH0_M1/SPI0_CS0n_M1/GPIO2_A3_d	56	SDMMC0_CMD/UART1_CTSN_M1/GPIO1_B2_d
13	SDMMC1_D3/UART1_RTSN_M2/PWM1_CH1_M1/I2C1_SCL_M1/SPI0_MISO_M1/ETH_LED_DPX/GPIO2_A4_d	57	SDMMC0_D3/UART0_RX_M2/JTAG_TMS_M2/PWM2_CH3_M0/I2C0_SDA_M1/GPIO1_B3_d
14	SDMMC1_D2/UART1_CTSN_M2/PWM1_CH2_M1/I2C1_SDA_M1/GPIO2_A5_d	58	SDMMC0_D2/UART0_TX_M2/JTAG_TCK_M2/PWM2_CH2_M0/I2C0_SCL_M1/GPIO1_B4_d
15	VCCIO6_DVDD1833	59	USB_AVDD3V3
16	UART1_TX_M2/PWM2_CH0_M1/I2C2_SCL_M1/SAI_SDI/ETH_LED_LINK/GPIO2_A6_d	60	USB_DM
17	UART1_RX_M2/SPI0_CS1n_M0/PWM2_CH1_M1/I2C2_SDA_M1/SAI_SCLK/ETH_LED_SPD/GPIO2_A7_d	61	USB_DP
18	UART2_TX_M1/SPI0_CLK_M0/PWM0_CH3_M1/I2C4_SCL_M0/SAI_MCLK/FLASH_TRIG_OUT/GPIO2_B0_d	62	USB_AVDD1V8
19	UART2_RX_M1/SPI0_MOSI_M0/PWM1_CH3_M1/I2C4_SDA_M0/SAI_LRCK/PRELIGHT_TRIG_OUT/GPIO2_B1_d	63	ACODEC_AVSS
20	UART2_RTSN_M1/SPI0_CS0n_M0/PWM2_CH2_M1/I2C3_SDA_M1/SAI_SDO/GPIO2_B2_d	64	ACODEC_LINEOUT
21	UART2_CTSN_M1/SPI0_MISO_M0/PWM2_CH3_M1/I2C3_SCL_M1/GPIO2_B3_d	65	ACODEC_VCM
22	OTP_AVDD1V8/SARADC_AVDD1V8/TSADC_AVDD1V8	66	ACODEC_AVDD1V8
23	SARADC_IN0/GPIO2_B4_z	67	ACODEC_MIC_N
24	CPU_NPU_DVDD	68	ACODEC_MIC_P
25	FEPHY_AVDD1V8	69	ACODEC_MICBIAS
26	FEPHY_REXT	70	VCCIO3_DVDD1833
27	FEPHY_AVDD3V3	71	EMMC_D3/FSPI0_D3/GPIO1_A0_u
28	FEPHY_TXP	72	EMMC_D0/FSPI0_D0/GPIO1_A1_u
29	FEPHY_TXN	73	EMMC_D1/FSPI0_D1/GPIO1_A2_u
30	FEPHY_RXP	74	EMMC_D2/FSPI0_D2/GPIO1_A3_u
31	FEPHY_RXN	75	EMMC_CLK/FSPI0_CLK/GPIO1_A4_d
32	DVDD_LOGIC	76	EMMC_CMD/FSPI0_CSN/GPIO1_A5_u

Pin	Pin Name	Pin	Pin Name
33	MIPICSI_D3N/GPIO1_C1_u	77	DDR_VDDQ
34	MIPICSI_D3P/GPIO1_C2_u	78	VSS
35	MIPICSI_CK1N/GPIO1_C3_u	79	DDR_VDDQ
36	MIPICSI_CK1P/GPIO1_C4_u	80	VSS
37	MIPICSI_D2N/GPIO1_C5_u	81	DDR_VDDQ
38	MIPICSI_D2P/GPIO1_C6_u	82	OSC_AVDD1V8/PLL_AVDD1V8
39	MIPICSI_D1N/GPIO1_D0_u	83	OSC_SOC_XIN
40	MIPICSI_D1P/GPIO1_D1_u	84	OSC_SOC_XOUT
41	MIPICSI_CK0N/GPIO1_D2_u	85	RTC_32K_OUT/CLK_32K/CLK_24M_OUT/FSPI1_CLK/GPIO0_A0_z
42	MIPICSI_CK0P/GPIO1_D3_u	86	PWM0_CH0_M0/CPU_AVS/FSPI1_D1/GPIO0_A1_d
43	MIPICSI_D0N/GPIO1_D4_u	87	PWM0_CH3_M0/FSPI1_D0/GPIO0_A2_d
44	MIPICSI_D0P/GPIO1_D5_u	88	PWR_CTRL0/GPIO0_A3_u
		EPAD	VSS

2.7 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-2 IO function description list

Interface	Pin Name	Direction	Description
Misc	OSC_SOC_XIN	I	Clock input of 24M crystal XO
	OSC_SOC_XOUT	O	Clock output of 24M crystal XO
	OSC_RTC_XIN	I	Clock input of 32K crystal XO
	OSC_RTC_XOUT	O	Clock output of 32K crystal XO
	CPU_AVS	O	Voltage control for CPU and NPU voltage domain
	CLK_24M_OUT	O	24M Clock out
	CAM_CLK0_OUT	O	Reference Clock Output for external Sensor chip
	CAM_CLK1_OUT	O	Reference Clock Output for external Sensor chip
	CLK_32K	I/O	32K clock If configured as input，clock is provided from external circuit； If configured as output，clock is provided from internal circuit of chip；
	RTC_32K_OUT	O	32K clock out from RTC
	PWR_CTRL0	O	Chip low power mode output indication signal
	PWR_CTRL1	O	Chip low power mode output indication signal
	ETH_LED_DPX	O	FEPHY duplex mode indication
	ETH_LED_LINK	O	FEPHY link status indication
	ETH_LED_SPD	O	FEPHY speed indication
	FLASH_TRIG_OUT	O	Hold signal for flash light
	PRELIGHT_TRIG_OUT	O	Hold signal for prelight

Interface	Pin Name	Direction	Description
SW-DP	JTAG_TCK_M*i* (*i*=0~2)	I	SWD interface clock input
	JTAG_TMS_M*i* (*i*=0~2)	I/O	SWD interface data input/output

Interface	Pin Name	Direction	Description
eMMC Interface	EMMC_CLK	O	eMMC card clock
	EMMC_CMD	I/O	eMMC card command output and response input
	EMMC_D[*i*] (*i*=0~3)	I/O	eMMC card data input and output

Interface	Pin Name	Direction	Description
SPI0	SPI0_CLK_M*i*(*i*=0~1)	I	SPI serial clock
	SPI0_CSN0_M*i*(*i*=0~1)	I/O	SPI chip select signal, low active
	SPI0_CSN1_M*i*(*i*=0~1)	O	SPI chip select signal, low active
	SPI0_MOSI_M*i*(*i*=0~1)	I	SPI serial data input
	SPI0_MISO_M*i*(*i*=0~1)	O	SPI serial data output

Interface	Pin Name	Direction	Description
FSPI0 Controller	FSPI0_CLK	O	FSPI0 serial clock
	FSPI0_CSN	O	FSPI0 chip select signal, low active
	FSPI0_Di(i=0~3)	I/O	FSPI0 serial data input/output signal

Interface	Pin Name	Direction	Description
FSPI1 Controller	FSPI1_CLK	O	FSPI1 serial clock
	FSPI1_CSN	O	FSPI1 chip select signal, low active
	FSPI1_Di(i=0~3)	I/O	FSPI1 serial data input/output signal

Interface	Pin Name	Direction	Description
SPI2AHB Controller	SPI2AHB_CLK	I	SPI2AHB serial clock
	SPI2AHB_CSN	I	SPI2AHB chip select signal, low active
	SPI2AHB_Di(i=0~3)	I/O	SPI2AHB serial data input/output signal

Interface	Pin Name	Direction	Description
SD/MMC/ SDIO Host Controller	SDMMCi_CLK	O	SDMMC card clock
	SDMMCi_CMD	I/O	SDMMC card command output and response input
	SDMMCi_D[*j*] (*i*=0~1)(j=0~3)	I/O	SDMMC card data input and output

Interface	Pin Name	Direction	Description
SAI Controller	SAI_MCLK	I/O	I2S/PCM/TDM reference clock
	SAI_SCLK	I/O	I2S/PCM/TDM serial clock
	SAI_LRCK	I/O	I2S/PCM/TDM channel indication signal

Interface	Pin Name	Direction	Description
	SAI_SDO	O	I2S/PCM/TDM serial data output
	SAI_SDI	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
PWM	PWM0_CH*i*_Mj(*i*=0 ~3)(j=0,1)	I/O	Pulse Width Modulation input and output
	PWM1_CH*i*_Mj(*i*=0 ~3) (j=0,1)	I/O	Pulse Width Modulation input and output
	PWM2_CH*i*_Mj(*i*=0 ~3) (j=0,1)	I/O	Pulse Width Modulation input and output

Interface	Pin Name	Direction	Description
I2C	I2C*i*_SDA_Mj (*i*=0,1,2,3,4)(j=0, 1)	I/O	I2C data
	I2C*i*_SCL_Mj (*i*=0,1,2,3,4)(j=0, 1)	I/O	I2C clock

Interface	Pin Name	Direction	Description
UART	UART*i*_RX_Mj (*i*=0,1,2) (j=0,1,2)	I	UART serial data input
	UART*i*_TX_Mj (*i*=0,1,2) (j=0,1,2)	O	UART serial data output
	UART*i*_CTSN_Mj (*i*=0,1,2) (j=0,1,2)	I	UART clear to send modem status input
	UART*i*_RTSN_Mj (*i*=0,1,2) (j=0,1,2)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
FEPHY	FEPHY_REXT	O	External 6K-Ohm resistor to ground
	FEPHY_RXN	I/O	FEPHY transceiver negative output/input
	FEPHY_RXP	I/O	FEPHY transceiver positive output/input
	FEPHY_TXN	I/O	FEPHY transceiver negative output/input
	FEPHY_TXP	I/O	FEPHY transceiver positive output/input

Interface	Pin Name	Direction	Description
ACODEC	ACODEC_LINEOUT	O	DAC channel out
	ACODEC_MIC_N	I	ADC channel negative input
	ACODEC_MIC_P	I	ADC channel positive input
	ACODEC_MICBIAS	O	Microphone bias output
	ACODEC_VCM	O	Reference voltage output

Interface	Pin Name	Direction	Description
MIPI_RX	MIPICSI_CK0N	I	MIPI_RX PHY negative clock input
	MIPICSI_CK0P	I	MIPI_RX PHY positive clock input
	MIPICSI_CK1N	I	MIPI_RX PHY negative clock input
	MIPICSI_CK1P	I	MIPI_RX PHY positive clock input
	MIPICSI_D0N	I	MIPI_RX PHY negative data input

Interface	Pin Name	Direction	Description
	MIPICSI_D0P	I	MIPI_RX PHY positive data input
	MIPICSI_D1N	I	MIPI_RX PHY negative data input
	MIPICSI_D1P	I	MIPI_RX PHY positive data input
	MIPICSI_D2N	I	MIPI_RX PHY negative data input
	MIPICSI_D2P	I	MIPI_RX PHY positive data input
	MIPICSI_D3N	I	MIPI_RX PHY negative data input
	MIPICSI_D3P	I	MIPI_RX PHY positive data input

Interface	Pin Name	Direction	Description
USB 2.0	USB_DP	I/O	USB 2.0 Data signal DP
	USB_DM	I/O	USB 2.0 Data signal DM

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for CPU and NPU	CPU_NPU_DVDD	0	1.1	V
Supply voltage for LOGIC	LOGIC_DVDD_i(i=1~3)	0	1.1	V
Supply voltage for PMUIO0	PMUIO0_DVDD33	0	3.8	V
Supply voltage for VCCIO3	VCCIO3_DVDD1833	0	3.8	V
Supply voltage for VCCIO4	VCCIO4_DVDD1833	0	3.8	V
Supply voltage for VCCIO6	VCCIO6_DVDD1833	0	3.8	V
Supply voltage for FEPHY	FEPHY_AVDD1V8	0	2	V
Supply voltage for FEPHY	FEPHY_AVDD3V3	0	3.8	V
Supply voltage for RTC	RTC_AVDD	0	3.8	V
1.8V supply voltage	ACODEC_AVDD1V8 OTP_AVDD1V8/SARADC_AVDD1V8/TSADC_AVDD1V8 OSC_AVDD1V8/PLL_AVDD1V8 USB_AVDD1V8 MIPI_AVDD1V8/VCCIO7_VCC1V8	0	2.0	V
3.3V supply voltage	USB_AVDD3V3	0	3.8	V
Supply voltage for DDR IO (DDR2 1.8V; DDR3L 1.35V)	DDR_VDDQ_i（i=1~3）	0	TBD	V
Storage Temperature	Tstg	-40	125	℃
Max Conjunction Temperature	Tj	NA	125	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Related Power Group	Min	Typ	Max	Unit
Supply voltage for CPU and NPU	CPU_NPU_DVDD	0.81	0.9	TBD	V
Supply voltage for LOGIC	LOGIC_DVDD_i(i=1~3)	0.81	0.9	0.99	V
Supply voltage for PMUIO0	PMUIO0_DVDD33	2.97	3.3	3.63	V
Supply voltage for VCCIO3	VCCIO3_DVDD1833	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO4	VCCIO4_DVDD1833	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO6	VCCIO6_DVDD1833	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for RTC	RTC_AVDD	1.6	3.3	3.63	V
1.8V supply voltage	ACODEC_AVDD1V8 OTP_AVDD1V8/SARADC_AVDD1V8/TSADC_AVDD1V8 OSC_AVDD1V8/PLL_AVDD1V8 USB_AVDD1V8 MIPI_AVDD1V8/VCCIO7_VCC1V8 FEPHY_AVDD1V8	1.62	1.8	1.98	V
3.3V supply voltage	USB_AVDD3V3 FEPHY_AVDD3V3	2.97	3.3	3.63	V
Supply voltage for DDR IO (DDR2 1.8V; DDR3L 1.35V)	DDR_VDDQ_i（i=1~3）	1.62 1.22	1.8 1.35	1.98 1.48	V
Ambient Operating Temperature	Ta	-20	25	85	℃

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	NA	43	Kohm
	Pulldown Resistor	Rpd	16	NA	43	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	NA	0.35*VDDO	V
	Input High Voltage	Vih	0.65*VDDO	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	1.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	NA	43	Kohm
	Pulldown Resistor	Rpd	16	NA	43	Kohm

Parameters		Symbol	Min	Typ	Max	Unit
MIPI IO@ MIPI HS receiver mode	Common-mod voltage HS receive mode	VCMRX(DC)	70	NA	300	mV
	Differential input high threshold	VIDTH	NA	NA	70	mV
	Differential input low threshold	VIDTL	-70	NA	NA	mV
	Single-ended input high voltage	VIHHS	NA	NA	460	mV
	Single-ended input low voltage	VILHS	-40	NA	NA	mV
	Single-ended threshold for HS termination enable	VTERM-EN	NA	NA	450	mV
	Differential input impedance	ZID	80	100	125	ohm
MIPI IO@ MIPI LP receiver mode	Logic 1 input voltage	VIH	880	NA	NA	mV
	Logic 0 input voltage, not in ULP State	VIL	NA	NA	550	mV
	Logic 0 input voltage, ULP State	VIL-ULPS	NA	NA	300	mV
	Input hysteresis	VHYST	25	NA	NA	mV
MIPI IO@ 1.8V TTL RX mode	Logic 1 input voltage	VIH	1.2	NA	1.58	V
	Logic 0 input voltage, not in ULP State	VIL	NA	NA	0.6	V
	Input hysteresis	VHYST	25	NA	NA	mV

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	10	uA
			Vin = 3.3V, pulldown enabled	NA	NA	10	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	10	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10	uA

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
			Vin = 1.8V, pulldown enabled	NA	NA	10	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	10	uA

Note: VDDO and DVDD are both IO power Supply

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for INT PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
	Input clock frequency(Frac)	F_{in}	Fin = FREF @1.8V/0.99V	10	NA	800	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @3.3V/0.99V	475	NA	1900	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @3.3V/0.99V	9	NA	1900	MHz
	Lock time	T_{lt}	@ 3.3V/0.99V, FREF=24M,REFDIV=1	NA	1000	1500	Input clock cycles

Table 3-6 Electrical Characteristics for FRAC PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
	Input clock frequency(Frac)	F_{in}	Fin = FREF @1.8V/0.99V	1	NA	1200	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @3.3V/0.99V	950	NA	3800	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @3.3V/0.99V	19	NA	3800	MHz
	Lock time	T_{lt}	@ 3.3V/0.99V, FREF=24M,REFDIV=1	NA	250	500	Input clock cycles

Notes:

① *REFDIV is the input divider value;*
② *FBDIV is the feedback divider value;*
③ *POSTDIV is the output divider value*

3.6 Electrical Characteristics for USB2.0 Interface

Table 3-7 Electrical Characteristics for USB2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
Output resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	2.7	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode	NA	+-250	NA	mV
		HS mode	NA	+-25	NA	mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	NA	150	mV
Disconnect threshold			570	600	664	mV

3.7 Electrical Characteristics for MIPI CSI interface

Table 3-8 HS Receiver AC specifications (for MIPI mode)

Parameters	Symbol	Min	Typ	Max	Unit
Common-mode interference beyond 450 MHz	ΔVCMRX(HF)	NA	NA	100	mV
Common-mode interference 50MHz – 450MHz	ΔVCMRX(LF)	-50	NA	50	mV
Common-mode termination	CCM	NA	NA	60	pF

Table 3-9 LP Receiver AC specifications (for MIPI mode)

Parameters	Symbol	Min	Typ	Max	Unit
Input pulse rejection	eSPIKE	NA	NA	300	V.ps
Minimum pulse width response	TMIN-RX	20	NA	NA	ns
Peak interference amplitude	VINT	NA	NA	200	mv
Interference frequency	fINT	450	NA	NA	MHz

3.8 Electrical Characteristics for Audio CODEC interface

Table 3-10 Electrical Characteristics for Audio CODEC

Test conditions: AVDD = 1.8V, DVDD = 0.8V, TA = 25°C, 1KHz Sine Input, Fs = 48KHz

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Operating Condition						
Analog Supply	AVDD		1.62	1.8	1.98	V
Microphone Bias						
Bias Voltage	V_{MICB}		0.8*AVDD	NA	0.975*AVDD	V
Bias Current	I_{MICB}		NA	NA	3	mA
Microphone Gain Boost PGA						
Programmable Gain	G_{BST}		0	NA	20	dB
Gain Step Size			NA	1.5	NA	dB
Input Resistance	R_{IN}	G_{BST}=0dB	NA	44	NA	KΩ
		G_{BST}=20dB	NA	8	NA	KΩ
Input Capacitance	C_{IN}		NA	10	NA	pF
ALC PGA						
Programmable Gain	G_{ALC}		-9	NA	37.5	dB
Gain Step Size			NA	1.5	NA	dB
ADC						
Signal to Noise Ratio	SNR	A-weighted	NA	92	NA	dB
Total Harmonic Distortion	THD	-3dBFS input	NA	-80	NA	dB
Channel Separation			NA	80	NA	dB
Power Supply Rejection	PSRR	1KHz	NA	80	NA	dB
Digital Filter Pass Band Ripple			0.1	0.125	0.125	
DAC Line Output						
Programmable Gain	G_{DRV}		-39	NA	6	dB
Gain Step Size			NA	1.5	NA	dB
Signal to Noise Ratio	SNR	A-weighted	NA	93	NA	dB
Total Harmonic Distortion	THD	-3dBFS output 600Ω load	NA	-84	NA	dB

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Power Supply Rejection	PSRR	1KHz	NA	55	NA	dB
Power Consumption						
Standby			NA	0.01	NA	mA
Mono Recording			NA	2.5	NA	mA
Mono Playback		Quiescent output	NA	2.5	NA	mA

3.9 Electrical Characteristics for SARADC

Table 3-11 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Resolution			NA	10	NA	bit
Effective Number of Bit	ENOB		NA	9	NA	bit
Differential Non-Linearity	DNL		-1	NA	+1	LSB
Integral Non-Linearity	INL		-2	NA	+2	LSB
Reference voltage	VREFP		NA	1.8	NA	V
Input Capacitance	C_{IN}		NA	8	NA	pF
Sampling Rate	f_S		NA	NA	1	MS/s
Spurious Free Dynamic Range	SFDR	f_S=1MS/s f_{OUT}=1.17KHz	NA	61	NA	dB
Signal to Noise and Harmonic Ratio	SNDR		NA	56	NA	dB

3.10 Electrical Characteristics for TSADC

Table 3-12 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Accuracy from -40℃ to 125℃	T_{JACC}		NA	NA	±5	℃
Sensing Temperature Range	T_{RANGE}		-40	NA	125	℃
Resolution	T_{LSB}		NA	0.6	NA	℃

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Value	Unit	Note
Junction-to-ambient thermal resistance	θ_{JA}	TBD	(℃/W)	(1)
Junction-to-board thermal resistance	θ_{JB}	TBD	(℃/W)	(2)
Junction-to-case thermal resistance	θ_{JC}	TBD	(℃/W)	(3)
Thermal characterization parameter	ψ_{JT}	TBD	(℃/W)	(4)

*Note (1): The package-board system is placed in the natural convection (JEDEC JESD51-2 standard), and the 2S2P test-board is designed in accordance with JESD 51-7/JESD 51-9. The actual system design and environment may be different.（The PCB is 4 layers, 114.5 mm*101.5 mm）*

Note (2): ϑ_{JB} is measured in the special environment (JEDEC JESD51-8 standard), and the printed circuit board used to mount the devices is specified in JESD51-7.

Note (3): The thermal resistance ϑ_{JC} is provided in compliance with the JEDEC JESD51-14.

Note (4): ψ_{JT} - The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package, ψ_{JT} is measured in the test environment of ϑ_{JA} (JEDEC JESD51-2 standard).

