



Features

- ESD Protect for 6 high-speed I/O channels
- Provide ESD protection for each channel to IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air)
IEC 61000-4-2 (ESD) $\pm 10\text{kV}$ (contact)
- **For low operating voltage of 1.5V and below**
- **Ultra low capacitance: 0.35pF typical**
- Fast turn-on and low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS (Transient Voltage Suppression) diode
- Solid-state silicon-avalanche and active circuit triggering technology
- Simplified layout for high-speed differential signaling channels
- **Green part**

Applications

- Thunderbolt interface
- Consumer Electronics
- Mobile Devices

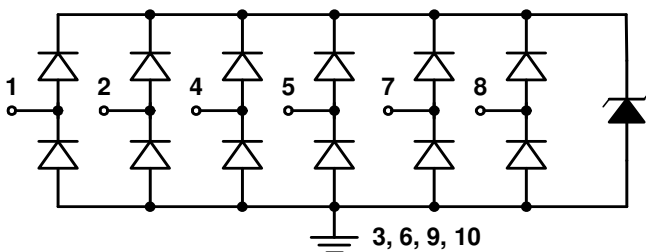
Description

AZ108S-06F is a design which includes ESD rated clamping cell arrays to protect high speed data interfaces. The AZ108S-06F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage damage caused by Electrostatic Discharging (ESD).

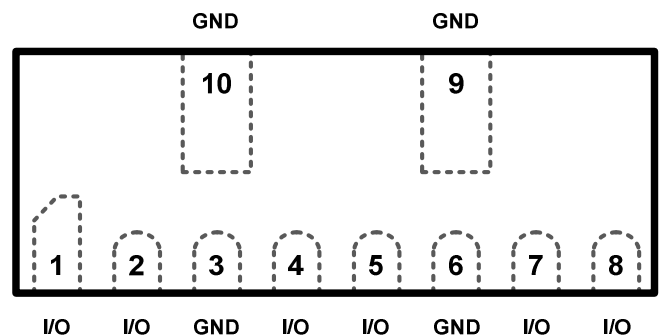
AZ108S-06F is a unique design which includes ESD rated, ultra low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the internal ESD line or ground line. The internal unique design of clamping cell prevents over-voltage on the internal ESD line and on the I/O line, which is protecting any downstream components.

AZ108S-06F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram



Pin Configuration



DFN3310P10E
(Top View)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	SYMBOL	RATING	UNITS
Operating Supply Voltage (I/O pin to GND)	V_{DC}	1.65	V
ESD per IEC 61000-4-2 (Air)	V_{ESD-1}	± 15	kV
ESD per IEC 61000-4-2 (Contact)	V_{ESD-2}	± 10	
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	$^{\circ}C$
Operating Temperature	T_{OP}	-55 to +85	$^{\circ}C$
Storage Temperature	T_{STO}	-55 to +150	$^{\circ}C$

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V_{RWM}	I/O pin to Ground, $T = 25^{\circ}C$.			1.5	V
Reverse Leakage Current	$I_{CH-Leak}$	$V_{RWM} = 1.5V$, $V_{GND} = 0V$, I/O pin to Ground, $T = 25^{\circ}C$.			0.5	μA
Reverse DC Breakdown Voltage	V_{BV}	$I_{BV} = 1mA$, I/O pin to Ground, $T = 25^{\circ}C$.	4.5		7.5	V
Forward Voltage	V_F	$I_F = 15mA$, Ground to I/O pin, $T = 25^{\circ}C$.	0.6		1.2	V
ESD Clamping Voltage (Note 1)	V_{clamp}	IEC 61000-4-2 +8kV ($I_{TLP} = 16A$), Contact mode, I/O pin to Ground, $T = 25^{\circ}C$.		7.0		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, $T = 25^{\circ}C$, Contact mode, I/O pin to Ground.		0.3		Ω
Channel Input Capacitance	C_{IN}	$V_{GND} = 0V$, $V_{IN} = 1.0V$, $f = 1MHz$, $T = 25^{\circ}C$, any I/O pin to Ground.		0.35	0.5	pF
Channel to Channel Input Capacitance	C_{CROSS}	$V_{GND} = 0V$, $V_{IN} = 1.0V$, $f = 1MHz$, $T = 25^{\circ}C$, between I/O pins.		0.03	0.08	pF

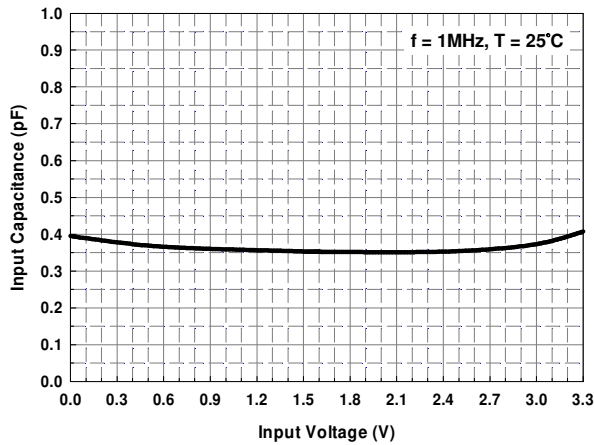
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: $Z_0 = 50\Omega$, $t_p = 100ns$, $t_r = 1ns$.

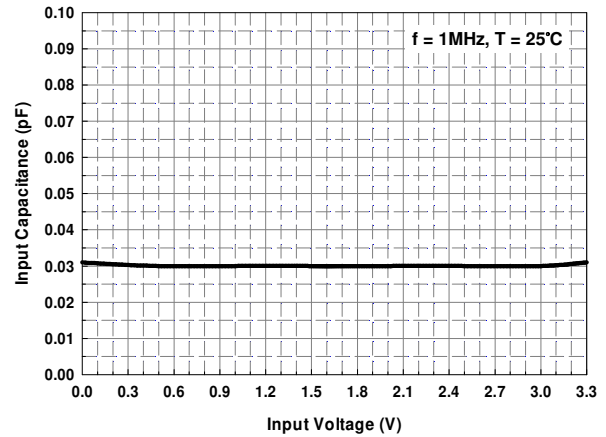


Typical Characteristics

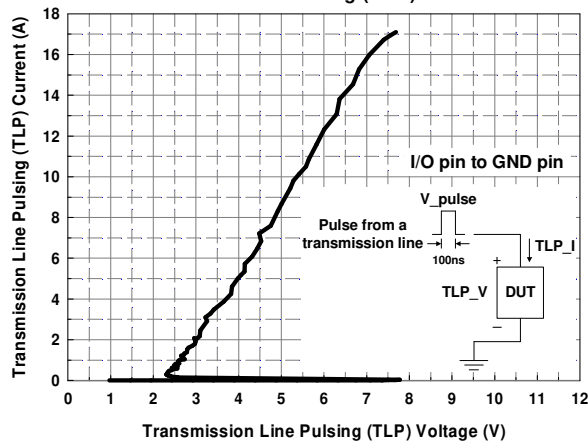
Typical Variation of C_{IN} vs. V_{IN}



Typical Variation of $C_{IO-to-IO}$ vs. V_{IN}



Transmission Line Pulsing (TLP) Measurement



Applications Information

A. Device Connection

The AZ108S-06F is designed to protect 6 high-speed data lines from transient over-voltage (such as ESD stress pulse). The device connection of AZ108S-06F is shown in the Fig. 1. In Fig. 1, the 6 protected high-speed data lines are connected to the ESD protection pins (pin1, pin2, pin4, pin5, pin7 and pin8) of AZ108S-06F. The AZ108S-06F is designed for allowing the

traces to run straight through the device to simplify the PCB layout. The ground pin (pin3, pin6, pin9 and pin10) of AZ108S-06F is a negative reference pin. This pin should be directly connected to the GND rail of PCB. To get minimum parasitic inductance, the path length should keep as short as possible.

AZ108S-06F can provide ESD protection for 6 I/O signal lines simultaneously. If the number of I/O signal lines is less than 6, the unused I/O pins can be simply left as NC pins.

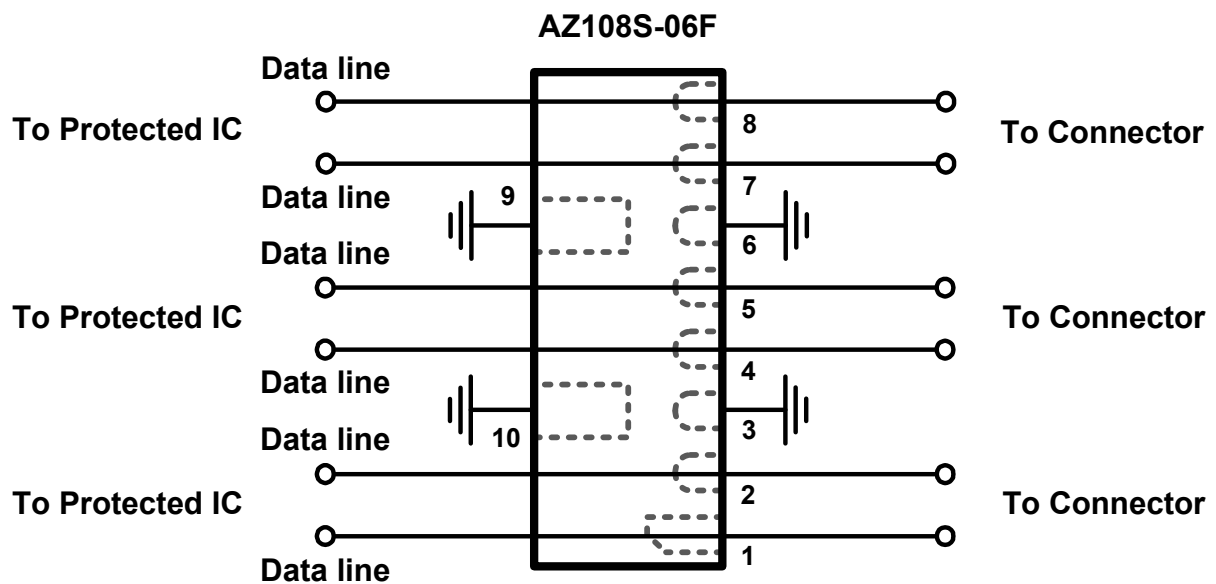
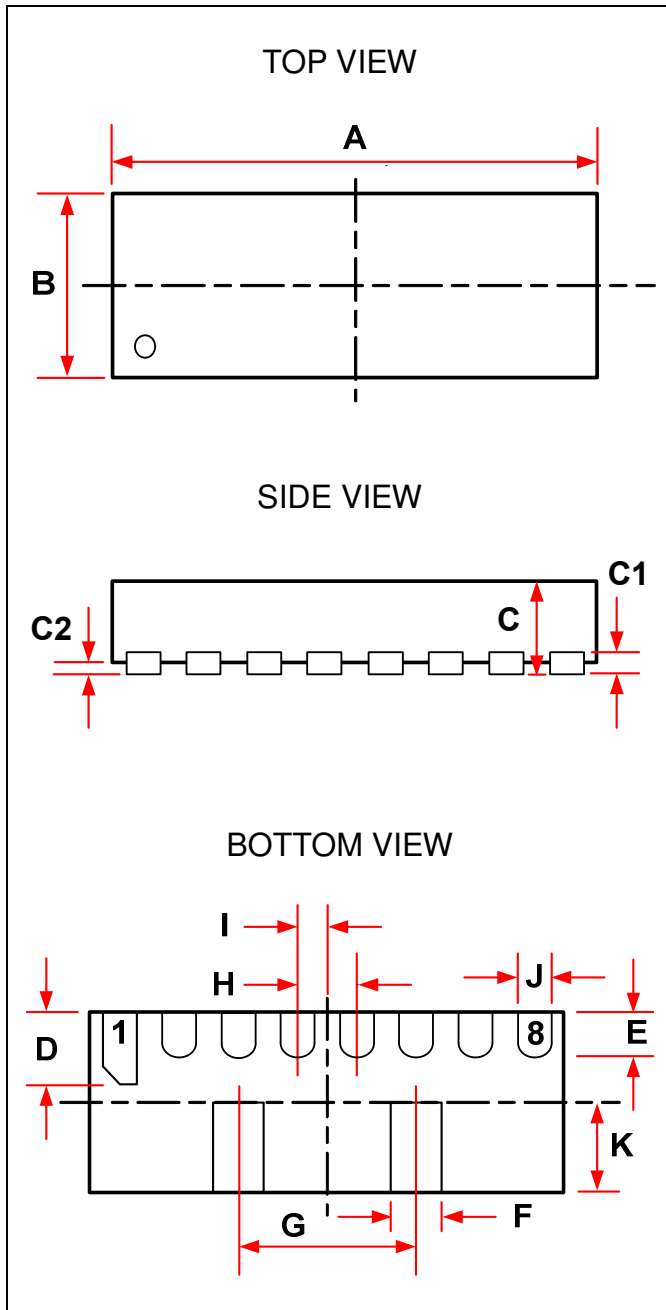


Fig. 1 Data lines connection of AZ108S-06F.

Mechanical Details

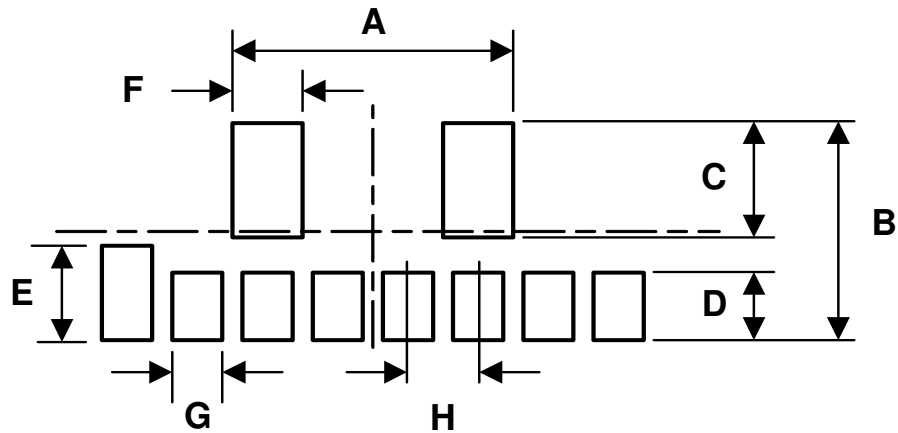
DFN3310P10E
PACKAGE DIAGRAMS



PACKAGE DIMENSIONS

SYMBOL	Millimeters		
	MIN.	NOM.	MAX.
A	3.250	3.300	3.350
B	0.950	1.000	1.050
C	0.450	0.500	0.550
C1	0.152 REF		
C2	0.000	0.020	0.050
D	0.300	0.350	0.400
E	0.200	0.250	0.300
F	0.300	0.350	0.400
G	1.190 BSC		
H	0.400 BSC		
I	0.200 BSC		
J	0.150	0.200	0.250
K	0.450	0.500	0.550

LAND LAYOUT

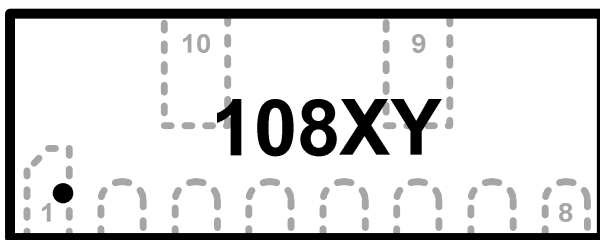


Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Dimensions	
Index	Millimeters
A	1.66
B	1.20
C	0.65
D	0.40
E	0.50
F	0.50
G	0.25
H	0.40

MARKING CODE



108=Device Code

X=Date Code

Y=Control Code

Part Number	Marking Code
AZ108S-06F.R7G (Green Part)	108XY

Note. Green means Pb-free, RoHS, and Halogen free compliant.



Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ108S-06F.R7G	Green	T/R	7 inch	3,000/reel	3 reels = 9,000/box	6 boxes = 54,000/carton

Revision History

Revision	Modification Description
Revision 2014/07/30	Preliminary Release.
Revision 2016/06/16	1. Add the max. value of Reverse DC Breakdown Voltage. 2. Update the ESD Clamping Voltage and add the ESD Dynamic Turn-on Resistance. 3. Update the Package Dimensions. 4. Formal Release.
Revision 2017/05/22	Update Ordering Information.