Features

- ESD Protect for Transition Minimized Differential Signaling (TMDS) channels
- Protects four I/O lines
- Provide ESD protection for each line to
  IEC 61000-4-2 (ESD) ±15kV (air), ±11kV (contact)
  IEC 61000-4-5 (Lightning) 4A (8/20μs)
- **For operating voltage of 3.3V and below**
- **Ultra low capacitance : 0.4pF typical**
- Fast turn-on and Low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS (Transient Voltage Suppression) diode
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- High Definition Multi-Media Interface (HDMI) 1.3 & 1.4 and 2.0 version
- DisplayPort interface
- SATA and eSATA interface
- USB3.0 and USB3.1
- V-By-One
- MIPI interface
- LVDS interface
- Desktop and Notebooks PCs
- Consumer Electronics
- Set Top Box

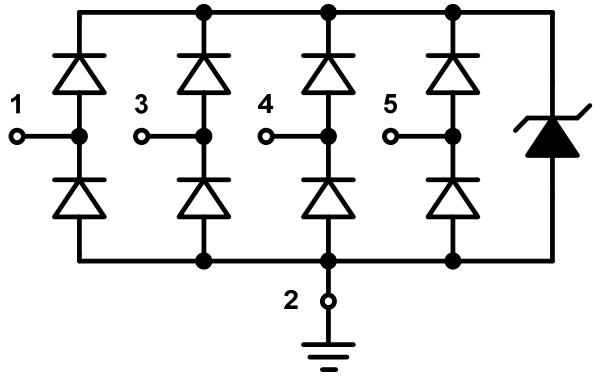
Description

AZ1743-04F is a design which includes ESD rated diode arrays to protect high speed data interfaces. The AZ1743-04F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD), Lightning, and Cable Discharge Event (CDE).

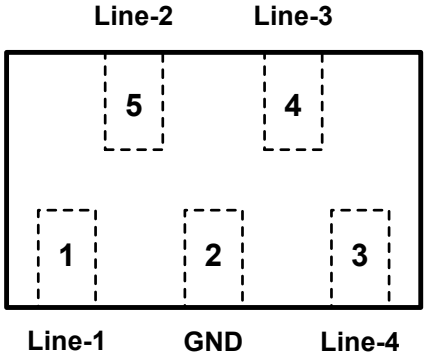
AZ1743-04F is a unique design which includes ESD rated, ultra low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the internal ESD line or to ground line. The internal unique design of clamping cell prevents over-voltage on the internal ESD line and on the I/O line, which is protecting any downstream components.

AZ1743-04F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



DFN1308P5Z (Top View)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp= 8/20μs)	I_{PP}	4	A
Operating Voltage (I/O pin-GND)	V_{DC}	3.6	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	15 11	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

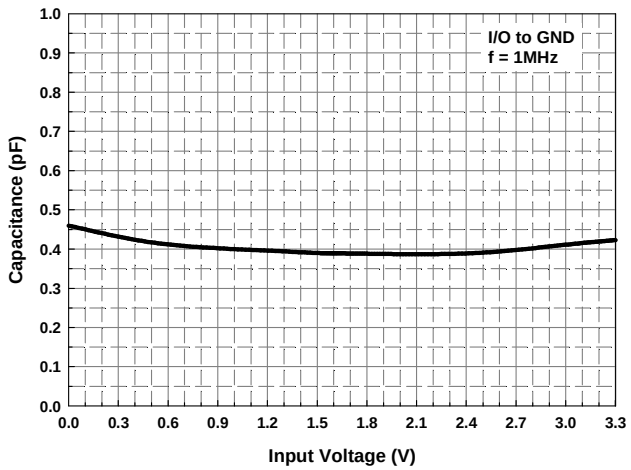
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1,-3,-4,-5 to pin-2, T = 25°C.			3.3	V
Channel Leakage Current	$I_{CH-Leak}$	$V_{Pin-1,-3,-4,-5}$ = 3.3V, V_{Pin-2} = 0V, T = 25°C.			1.0	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T = 25°C, pin-1,-3,-4,-5 to pin-2.	4.5		7.5	V
Forward Voltage	V_F	I_F = 15mA, pin-2 to pin-1,-3,-4,-5, T = 25°C.	0.6		1.2	V
ESD Clamping Voltage (Note 1)	V_{clamp}	IEC 61000-4-2 +8kV (I_{TLP}=16A), T = 25°C, Contact mode, any I/O pin to Ground.		9.5		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+8kV, T = 25°C, Contact mode, any I/O pin to Ground.		0.28		Ω
Channel Input Capacitance	C_{IN}	V_{pin-2} = 0V, V_{IN} = 1.65V, f = 1MHz, T = 25°C, any I/O pin to Ground.		0.4	0.55	pF
Channel to Channel Input Capacitance	C_{CROSS}	V_{pin-2} = 0V, V_{IN} = 1.65V, f = 1MHz, T = 25°C, between I/O pins.		0.02	0.05	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

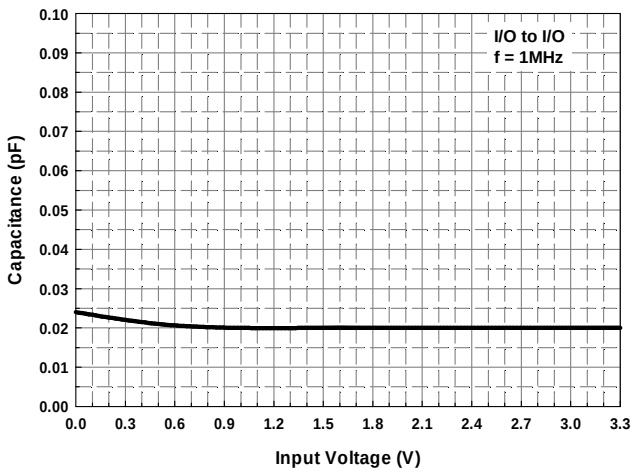
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

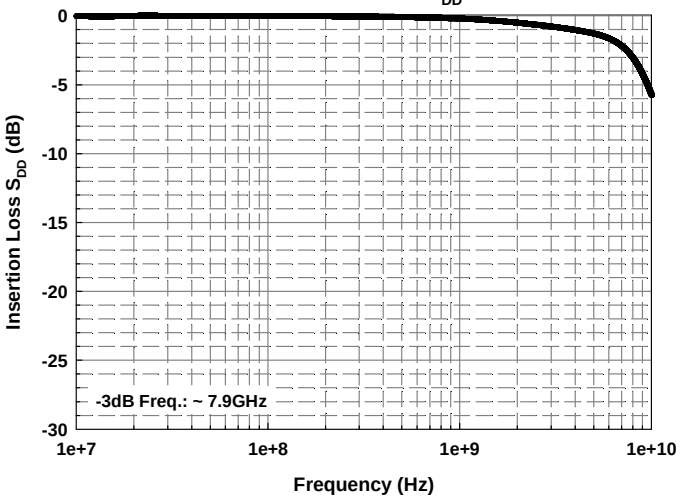
Typical Variation of C_{IN} vs. V_{IN}



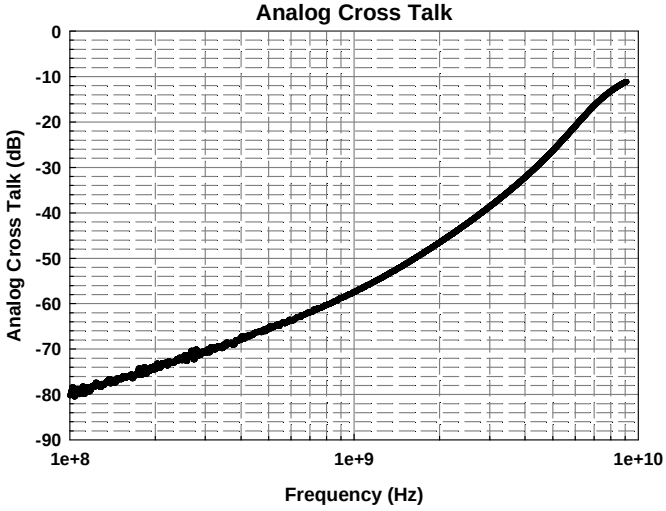
Typical Variation of $C_{IO\text{-}to\text{-}IO}$ vs. V_{IN}



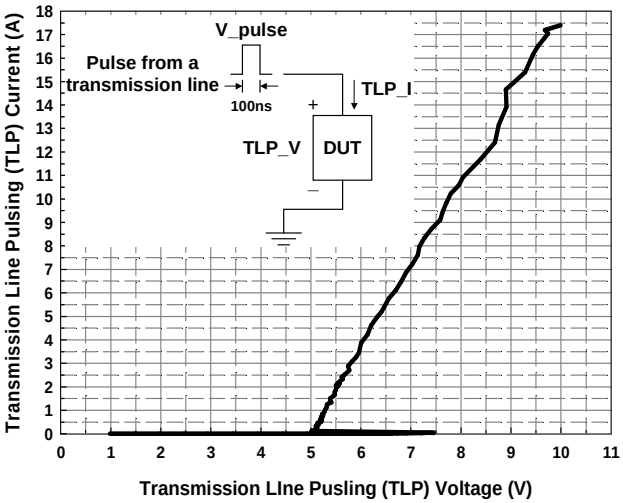
Insertion Loss S_{DD}



Analog Cross Talk



Transmission Line Pulsing (TLP) Measurement



Applications Information

The AZ1743-04F is designed to protect four data lines from transient over-voltage (such as ESD stress pulse). The device connection of AZ1743-04F is shown in the Fig. 1. In Fig. 1, the four protected data lines are connected to the ESD protection pins (pin1, pin3, pin4, and pin5) of AZ1743-04F. The ground pin (pin2) of AZ1743-04F is the negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible.

AZ1743-04F can provide ESD protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

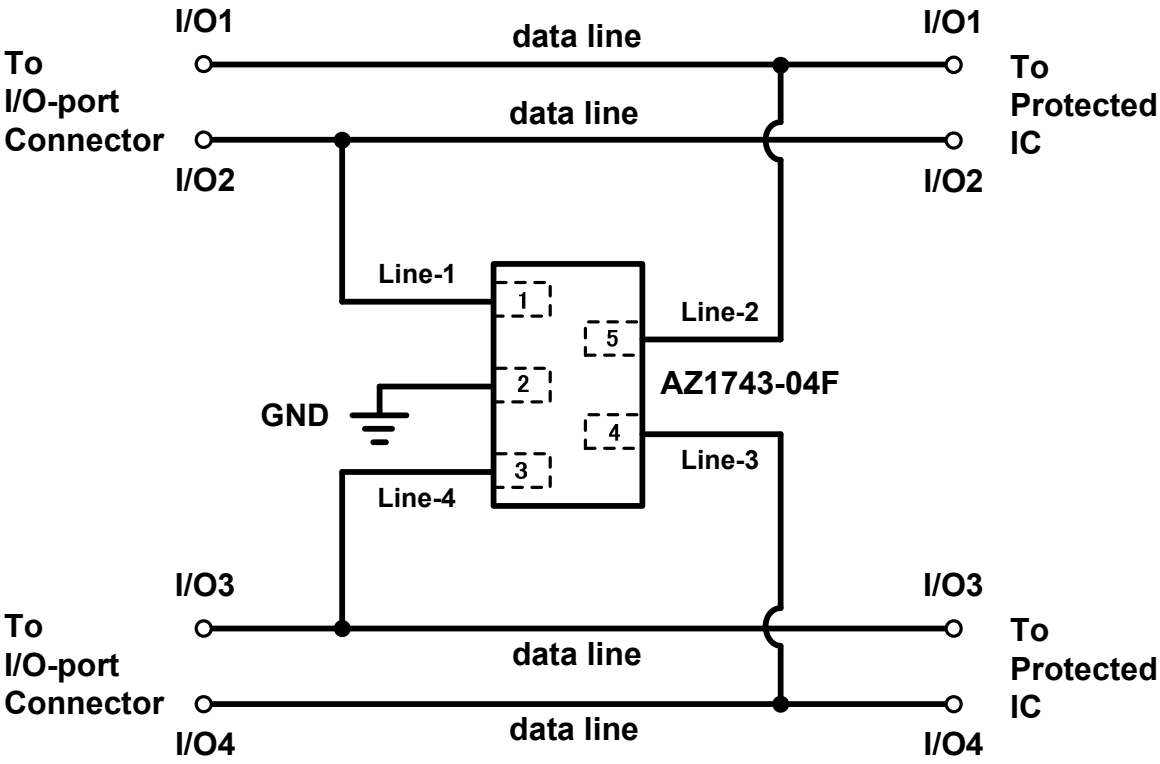
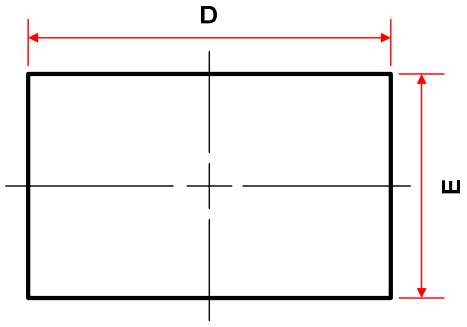
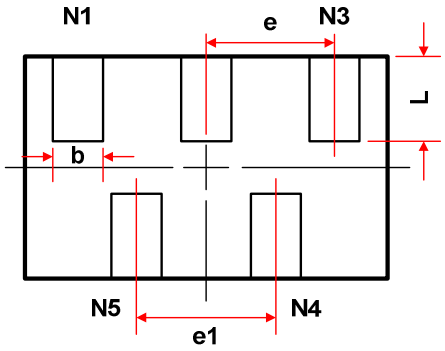


Fig. 1 Data lines connection of AZ1743-04F.

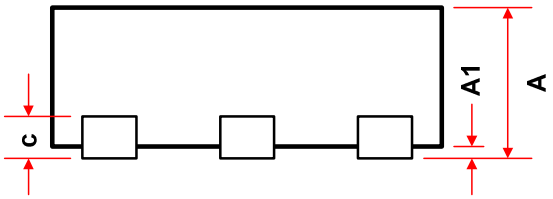
PACKAGE OUTLINE (DFN1308P5Z)



TOP VIEW



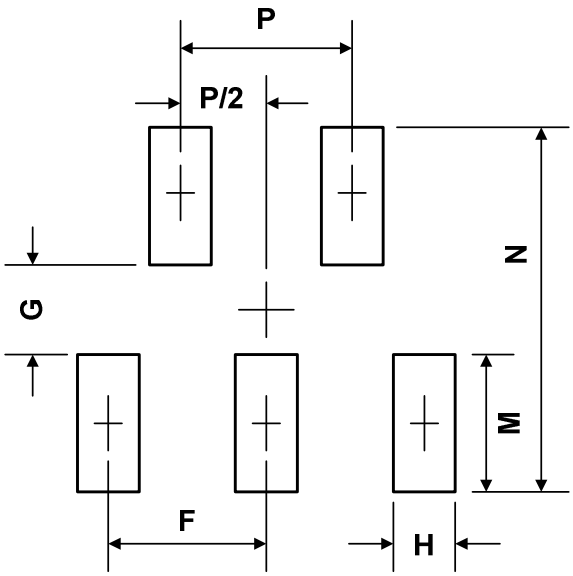
BOTTOM VIEW



SIDE VIEW

Symbol	Millimeters		
	MIN	NOM	MAX
A	0.37	0.40	0.43
A1	0.00	0.02	0.05
b	0.13	0.18	0.23
c	0.08	0.13	0.18
D	1.20	1.30	1.40
e	0.45 BSC		
e1	0.50 BSC		
E	0.70	0.80	0.90
L	0.20	0.25	0.30

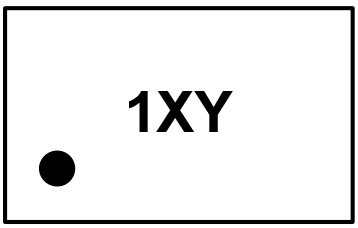
LAND LAYOUT



Dimensions	
Index	**Millimeter**
F	0.45
G	0.25
H	0.18
M	0.40
N	1.05
P	0.50

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



1 = Device Code
X = Date Code
Y= Control Code

Part Number	Marking Code
AZ1743-04F.R7G (Green part)	1XY

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ1743-04F.R7G	Green	T/R	7 inch	3,000/reel	4 reels = 12,000/box	6 boxes = 72,000/carton

Revision History

Revision	Modification Description
Revision 2016/06/20	Preliminary Release.
Revision 2017/04/27	Formal Release.