Automotive System Basis Chip Integrated LDO and CAN-Transceivers

Features

- Integrated 5 V or 3.3 V up to 250 mA, ±2% Accuracy, Main Low-dropout Voltage Regulator
- Integrated 5 V up to 150 mA, ±2% Accuracy, Auxiliary Regulator with Off-board Usage Protection
- Voltage Regulator with External PNP Transistor Configurable for Off-board Usage or for Load Sharing
- Very Low Quiescent Current Consumption in Low Power Mode
- Integrated CAN Transceiver Meets the ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5 Physical Layer Standards (Meet ISO 11898-2:2024 and CiA601-4 for Signal Improvement Capability (SIC) Option Available)
- Support Classical CAN and Optimized CAN FD SIC up to 8 Mbps Data Rates
- Support Partial Networking by Means of Selective Wake Up/Wake-Up Frame
- Local Wake-up via the WAKE Pin and Wake-up Source Recognition
- Integrated Configurable Timeout and Window Watchdog, Reset Outputs for Fail-safe and Supervision Functions
- 16-, 24- and 32- Bit SPI for Diagnostics and Configuration
- Configuration of Selected Functions via Non-volatile Memory
- Protection Feature:
  - Bus Pin IEC 61000-4-2 ESD Protection up to ±8 kV
  - Bus Fault Protection: ±45 V
  - Undervoltage and Overvoltage Protection
  - Short Circuit Protection
  - Overtemperature Warning and Shutdown Protection
- Available in DFN3.5X5.5-20 Package with Improved Automated Optical Inspection (AOI) Capability
- AEC-Q100 Qualified for Automotive Applications , Grade 1

Applications

- Heating, Ventilation and Air Conditioning (HVAC)
- Body Control Modules (BCM), Tailgate, Seat, Roof, Door, Trailer Modules
- Passive Keyless Entry and Start Modules, Remote Keyless Entry Modules
- Lighting Control Modules
- Gear Shifters and Steering Column Control Module

Description

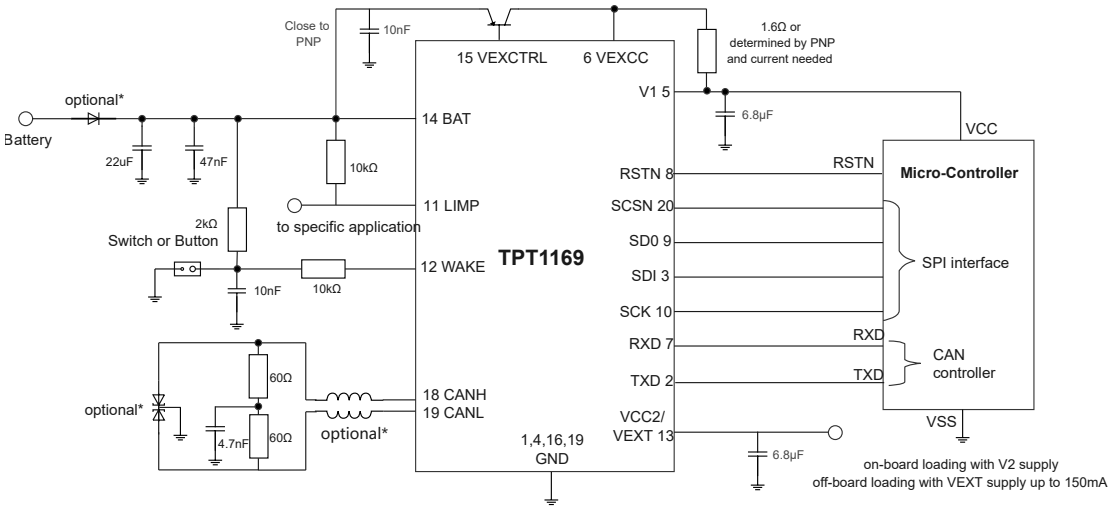
The TPT1169xQ is a system basis chip (SBC) designed for automotive applications. The device functions as a main power supply for the microcontroller and as a transceiver for the CAN bus networks.

The SBC integrates 250-mA main low drop-out voltage regulator for the microcontroller as a power supply with 5-V and 3.3-V output options. Additionally, it includes another 5-V 150-mA low drop-out voltage regulator for other on-board device power supply. The X version features a voltage regulator with off-board protection, designed for off-board devices power supply. Furthermore, the SBC integrates CAN transceiver that supports partial networking and enables data rates of up to 8 Mbps. This transceiver meets the ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5 Physical Layer Standards. Variants with signal improvement capability (SIC) also meets CiA601-4 standards. Moreover, the system integrates a configurable timeout/window watchdog with a reset feature, limp home outputs, and an undervoltage reset feature. It also includes an integrated Serial Peripheral Interface (SPI) for configuration and monitoring purposes.

The SBC offers low-power modes for low-power consumption applications. The device can be woken up from low-power mode locally via wake-pin or cyclic wake-up, and remote wake-up via bus is also possible.

The TPT1169xQ is available in the exposed pad DFN3.5X5.5-20L package, featuring enhanced automated optical inspection (AOI) capabilities. Additionally, it is AEC-Q100 qualified for automotive applications.

Typical Application Circuit



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Product Family Table

Order Number	V1 Output	V2/VEXT Output	CAN Transceiver	CAN FD Passive and Partial Networking	Device ID
TPT11695Q-DFUR-S	5 V for MCU only	V2 5 V for on-board loads	8Mbps CAN FD SIC	Disable	CFh
TPT11695XQ-DFUR-S	5 V for MCU and CAN	VEXT 5 V for off-board loads	8Mbps CAN FD SIC	Disable	CEh
TPT11695FQ-DFUR-S	5 V for MCU only	V2 5 V for on-board loads	8Mbps CAN FD SIC	Supported	EFh
TPT11695XFQ-DFUR-S	5 V for MCU and CAN	VEXT 5 V for off-board loads	8Mbps CAN FD SIC	Supported	EEh
TPT11693Q-DFUR-S	3.3 V for MCU only	V2 5 V for CAN and on-board loads	8Mbps CAN FD SIC	Disable	C9h
TPT11693FQ-DFUR-S	3.3 V for MCU only	V2 5 V for CAN and on-board loads	8Mbps CAN FD SIC	Supported	E9h

Revision History

Date	Revision	Notes
2025-05-15	Rev.Pre.0	Initial version
2025-07-15	Rev.A.0	Released version

Pin Configuration and Functions

TPT1169xQ
DFN3.5x5.5-20L Package
Top View

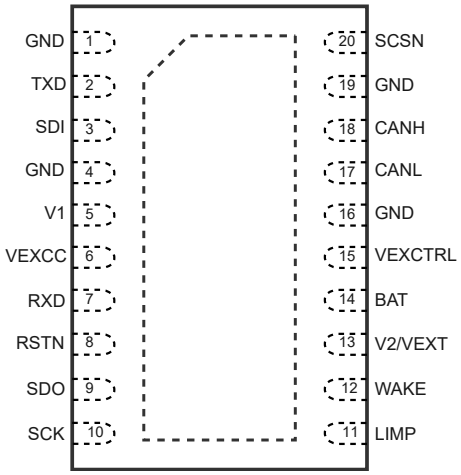


Table 1. Pin Functions: TPT1169xQ

Pin		Description
No.	Name	
1	GND	Ground
2	TXD	CAN transceiver transmit input
3	SDI	SPI Data input
4	GND	Ground
5	V1	LDO1 output
6	VEXCC	External PNP transistor current measurement; connected to the collector of external PNP transistor
7	RXD	CAN transceiver receive output
8	RSTN	Reset input/output; active low
9	SDO	SPI Data output
10	SCK	SPI clock input
11	LIMP	Limp home output; open-drain; active low
12	WAKE	Local wake-up input
13	V2/VEXT	LDO2 output (without X suffix) / LDO for off-board device (with X suffix)
14	BAT	Battery supply voltage
15	VEXCTRL	External PNP transistor control pin; connected to the base of the external PNP transistor
16	GND	Ground
17	CANL	CAN transceiver Low-level BUS line

Pin		Description
No.	Name	
18	CANH	CAN transceiver High-level BUS line
19	GND	Ground
20	SCSN	SPI chip select, active low

(1) DFN package die is connected to both the GND pin and the exposed pad. The GND pin must be soldered to board ground and for enhanced thermal and electrical performance, the exposed pad is also recommended be soldered to board ground.

Specifications

Absolute Maximum Ratings (1)

Parameter		Conditions	Min	Typ	Max	Unit
V_{BAT}	Supply Voltage Range	Pin VBAT	−0.3		45.0	V
V_{HV}	High Voltage Pin Voltage Range	Pin LIMP, VEXCTRL	−0.3		45.0	V
V_{OUT}	Power Output Voltage Range	Pin VOUT1, VOUT2	−0.3		6.0	V
V_{LOGIC}	Logic Terminal Voltage Range	Pin TXD, RXD, SDI, SCK, SCSN, RSTN	−0.3		V_{VOUT1}+0.3	V
V_{EXCC}	Pin VEXCC Voltage Range	Pin VEXCC	−0.3		6.0	V
V_{EXT}	Pin VEXT Voltage Range	Pin VEXT	−0.3		45.0	V
V_{WAKE}	Pin WAKE Voltage Range	Pin WAKE	−18		45.0	V
V_{BUS}	CAN Bus Voltage Range	Pin CANH, CANL	−45		45.0	V
V_{BUS_DIFF}	Differential Output Voltage of Can Bus	CANH - CANL	−45		45.0	V
I_{LIMP_IN}	LIMP Pin Input Current				20.0	mA
T_J	Junction Temperature		−55		150.0	°C
T_{STG}	Storage Temperature		−55		150.0	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD and Transient Ratings

Parameter		Condition	Min	Max	Unit
V_{ESD}	Electrostatics Discharge	Contact discharge on bus pins (CANH,CANL),IEC61000−4−2(150 pF, 330Ω discharge circuit)	−8	8	kV
		Human Body Model (HBM) on bus pins (CANH,CANL),AEC Q100-002 (1)	−15	15	kV
		Human Body Model (HBM) on any pins,AEC Q100-002 (1)	−8	8	kV
		Charged Device Model (CDM) on all pins,AEC Q100-011	−1.5	1.5	kV
V_{TRAN}	Transient Immunity ISO 7637-2 on Bus Pins	Pulse1	−100		V
		Pulse2a		75	V
		Pulse3a	−150		V
		Pulse3b		100	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDAJEDEC JS-001 specification.

Recommended Operating Conditions

	Parameter	Min	Max	Unit
V_S	Battery Power Supply Voltage	6.5	40	V
f_{SPI}	SPI Frequency		4	MHz
T_A	Operating Temperature	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
DFN3.5x5.5-20L	29	24.74	°C/W

Electrical Characteristics

All test conditions: V_{BAT} = 12 V, R_L = 60 Ω, T_A = −40°C to 125°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Pin V_{BAT}; Battery Supply						
V_{BAT}	Supply Voltage		2.8		40	V
$V_{TH\_DET\_PON}$	Power-on Detection Threshold on V_{BAT}	V_{BAT} rising	4.2		4.55	V
$V_{TH\_DET\_POFF}$	Power-off Detection Threshold on V_{BAT}	V_{BAT} falling	2.8		3	V
I_{BAT}	Sleep-Mode Supply Current	MC = 001; CAN offline mode; V_{OUT2}/V_{EXT} off; 7 V ≤ V_{BAT} ≤ 40 V		41	65	μA
	Standby-Mode Supply Current	MC = 100; CAN offline mode; V_{OUT2}/V_{EXT} off; I_{OUT1} = 0 μA; 7 V ≤ V_{BAT} ≤ 40 V		63	91	μA
	Additional Supply Current	Additional current with V_{OUT2} on (V_{2C} = 01/10/11); V_{OUT2}/V_{EXT} off; I_{OUT1} = 0 μA; 7 V ≤ V_{BAT} ≤ 40 V (1)		8	32	μA
		Additional current with V_{EXT} on (V_{EXTC} = 01/10/11); V_{OUT2}/V_{EXT} off; I_{OUT1} = 0 μA; 7 V ≤ V_{BAT} ≤ 40 V (1)		8	32	μA
		Additional current in CAN offline bias mode		52	65	μA
		Additional current when partial networking enabled; bus active; CPNC = 1; PNCOK = 1 (1)		900	1,200	μA
		Additional current from WAKE input; WPRE = 1; WPFE = 1		2	3	μA
	Normal-Mode Supply Current	MC = 111; CAN active mode; recessive; V_{TXD} = V_{OUT1}		4	7.5	mA
		MC = 111; CAN active mode; dominant; V_{TXD} = 0 V		46	67	mA
Pin V1; Voltage Output 1						
$R_{ON\_BAT-VOUT1}$	On Resistance between V_{BAT} Pin and V_{OUT1} Pin	2.8 V ≤ V_{BAT} ≤ 3.25 V; I_{OUT1} = 250 mA			3.2	Ω
V_O	Output Voltage	V_{OUT1_NORM} = 5 V; 5.5 V ≤ V_{BAT} ≤ 40 V; I_{OUT1} ≤ 200 mA (1)	4.9	5	5.1	V
		V_{OUT1_NORM} = 5 V; 5.65 V ≤ V_{BAT} ≤ 40 V; I_{OUT1} ≤ 250 mA	4.9	5	5.1	V
		V_{OUT1_NORM} = 5 V; V_{BAT} ≤ V_{UVBAT} and rising; t ≤ $t_{STARTUP}$			5.5	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		V_{OUT1_NORM} = 3.3 V; 3.834 V ≤ V_{BAT} ≤ 40 V; I_{OUT1} ≤ 200 mA	3.234	3.3	3.366	V
		V_{OUT1_NORM} = 3.3 V; 3.984 V ≤ V_{BAT} ≤ 40 V; I_{OUT1} ≤ 250 mA	3.234	3.3	3.366	V
Δ V_{RET_RAM}	RAM Retention Voltage Difference between V_{BAT} and V_{OUT1}; 5-V Variants Only	2.4 V ≤ V_{BAT} ≤ 3 V; I_{OUT1} = 2 mA			100	mV
		2.4V ≤ V_{BAT} ≤ 3 V; I_{OUT1} = 200 µA (1)			10	mV
$R_{ON\_BAT-VOUT1}$	On Resistance between V_{BAT} Pin and V_{OUT1} Pin	3.25 V ≤ V_{BAT} ≤ 5.65 V; I_{OUT1} = 250 mA			3	Ω
V_{UVD_OUT1}	V_{OUT1} Under-Voltage Detection Voltage; 5-V Variants	$V_{UV\_OUT1\_NORM}$ = 90%	4.5		4.75	V
		$V_{UV\_OUT1\_NORM}$ = 80%	4		4.25	V
		$V_{UV\_OUT1\_NORM}$ = 70%	3.5		3.75	V
		$V_{UV\_OUT1\_NORM}$ = 60%	3		3.25	V
	V_{OUT1} Under-Voltage Detection Voltage; 3.3-V Variants	$V_{UV\_OUT1\_NORM}$ = 90%	2.97		3.135	V
V_{UVR_OUT1}	V_{OUT1} Under-Voltage Recovery Voltage; 5-V Variants	$V_{UV\_OUT1\_NORM}$ = 90%	4.5		4.75	V
	V_{OUT1} Under-Voltage Recovery Voltage; 3.3-V Variants	$V_{UV\_OUT1\_NORM}$ = 90%	2.97		3.135	V
I_{SINK}	Sink Current	5.65 V ≤ V_{BAT} ≤ 18 V	214			mA
I_{O_SC}	Short-Circuit Output Current		−500		−250	mA
$I_{DD\_CAN\_INTV1}$	Internal CAN Supply Current from V1 (1)	Normal mode; MC = 111; CAN active mode; CAN dominant; V_{TXD} = 0 V; short-circuit on bus lines; −3 V ≤ V_{CANH} = V_{CANL} ≤ +18 V			85	
Pin V_{EXCTRL}; PNP Base						
I_{O_SC}	Short-Circuit Output Current	V_{EXCTRL} ≥ 4.5 V; 7 V ≤ V_{BAT} ≤ 40 V	3.4	5.8	7.5	mA
$I_{TH\_ACT\_PNP}$	PNP Activation Threshold Current; Load Current Increasing	PDC = 0	40	83	130	mA
		PDC = 1	18	50	70	mA
$I_{TH\_DEACT\_PNP}$	PNP Deactivation Threshold Current; Load Current Falling	PDC = 0	16	44	60	mA
		PDC = 1	1	11	22	mA
$V_{TH\_ICTRL\_PNP}$	PNP Current Control Threshold Voltage	Rising edge on V_{BAT} pin	5.9		7.5	V
Pin V_{EXCC}; PNP Collector						
$V_{TH\_ACT\_ILIM}$	Current Limiting Activation Threshold Voltage	Measured across resistor connected between V_{EXB} pin and V_{OUT1} pin; 2 V ≤ V_{OUT1} ≤ 5.5 V; 7.5 V ≤ V_{BAT} ≤ 40 V	240		360	mV
Pin V2; Voltage Output 2						
V_O	Output Voltage	6.2 V ≤ V_{BAT} ≤ 40 V; I_{OUT2} ≤ 150 mA	4.9	5	5.1	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$R_{ON\_BAT-VOUT2}$	On Resistance between V_{BAT} Pin and V_{OUT2} Pin	4.5 V ≤ V_{BAT} ≤ 6.2 V; 5 mA ≤ I_{OUT2} ≤ 150 mA			8.7	Ω
V_{UVD_OUT2}	V_{OUT2} Under-Voltage Detection Voltage		4.45			V
V_{UVR_OUT2}	V_{OUT2} Under-Voltage Recovery Voltage				4.8	V
V_{OVD_OUT2}	V_{OUT2} Over-Voltage Detection Voltage		5.2		5.5	V
V_{OVR_OUT2}	V_{OUT2} Over-Voltage Recovery Voltage		5.2		5.5	V
I_{O_SC}	Short-Circuit Output Current		−300		−180	mA
$I_{DD\_CAN\_INTV2}$	Internal CAN Supply Current from V2 (1)	Normal mode; MC = 111; CAN active mode; CAN dominant; V_{TXD} = 0 V; short-circuit on bus lines; −3 V ≤ V_{CANH} = V_{CANL} ≤ +18 V			85	mA
Pin V_{EXT}; Voltage Output External						
V_O	Output Voltage	6.2 V ≤ V_{BAT} ≤ 40 V; I_{EXT} ≤ 150 mA	4.9	5	5.1	V
$R_{ON\_BAT-VEXT}$	On Resistance between V_{BAT} Pin and V_{EXT} Pin	4.5 V ≤ V_{BAT} ≤ 6.2 V; 5 mA ≤ I_{EXT} ≤ 150 mA			11	Ω
V_{UVD_OUT2}	V_{EXT} Under-Voltage Detection Voltage		4.45			V
V_{UVR_OUT2}	V_{EXT} Under-Voltage Recovery Voltage				4.8	V
V_{OVD_OUT2}	V_{EXT} Over-Voltage Detection Voltage		5.2			V
V_{OVR_OUT2}	V_{EXT} Over-Voltage Recovery Voltage				5.5	V
I_{O_SC}	Short-Circuit Output Current		−300		−150	mA
Pin LIMP; Limp-Home Output						
V_O	Output Voltage	I_{LIMP} = 0.8 mA; LHC = 1			0.4	V
I_{LO}	Output Leakage Current	0 V ≤ V_{LIMP} ≤ 28 V; LHC = 0	−5		5	μA
Pin SDI, SCK and SCSN; Serial Peripheral Inputs						
V_{TH_SW}	Switching Threshold Voltage		0.25 × V_{OUT1}		0.75 × V_{OUT1}	V
$V_{TH\_SW\_HYS}$	Switching Threshold Voltage Hysteresis		0.05 × V_{OUT1}			V
R_{PD_SCK}	Pull-down Resistance on SCK Pin		40	60	80	kΩ
R_{PU_SCSN}	Pull-up Resistance on SCSN Pin		40	60	80	kΩ

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{PD_SDI}	Pull-down Resistance on SDI Pin		40	60	80	kΩ
R_{PU_SDI}	Pull-up Resistance on SDI Pin		40	60	80	kΩ
C_I	Input Capacitance (1)	$V_I = V_{OUT1}$		3	6	pF
Pin SDO; Serial Peripheral Output						
V_{OH}	High-Level Output Voltage	I_{OH} = −4 mA	V_{OUT1} − 0.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 4 mA			0.4	V
I_{LO_OFF}	Off-State Output Leakage Current	$V_{SCS\_N} = V_{OUT1}$; V_{SDO} = 0 V or V_{OUT1}	−5		5	μA
C_{O_SDO}	Output Capacitance (1)	$V_{SCS\_N} = V_{OUT1}$		3	6	pF
Pin TXD; CAN Transmit Data Input						
V_{TH_TXD}	Switching Threshold Voltage		0.25 × V_{OUT1}		0.75 × V_{OUT1}	V
V_{HYS_TXD}	Hysteresis Voltage on Pin TXD		0.05 × V_{OUT1}			V
R_{PU_TXD}	Pull-up Resistance		40	60	80	kΩ
Pin RXD; CAN Receive Data Output						
V_{OH}	High-Level Output Voltage	I_{OH} = −4 mA	V_{OUT1} − 0.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 4 mA			0.4	V
R_{PU_RXD}	Pull-up Resistance on RXD Pin		40	60	80	Ω
Pin WAKE; Local Wake Input						
$V_{TH\_WAKE\_R}$	Rising Switching Threshold Voltage		2.8		4.1	V
$V_{TH\_WAKE\_F}$	Falling Switching Threshold Voltage		2.4		3.75	V
V_{HYS_WAKE}	Hysteresis Voltage on WAKE Pin		250		800	mV
I_{I_WAKE}	Input Current				1.5	μA
Pin RSTN; Reset Output						
V_{OL}	Low-Level Output Voltage	1.0 V ≤ V_{OUT1} ≤ 5.5 V; pull-up resistor to V_{OUT1} ≥ 900 Ω	0		0.2 × V_{OUT1}	V
R_{PU_RSTN}	Pull-up Resistance		40	60	80	kΩ
V_{TH_RSTN}	Switching Threshold Voltage		0.25 × V_{OUT1}		0.75 × V_{OUT1}	V
V_{HYS_RSTN}	Hysteresis Voltage on Pin RSTN		0.05 × V_{OUT1}			V
Pin CANH, CANL; CAN-Bus Lines						

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{O_DOM}	Dominant Output Voltage, CANH	Dominant; V_{TXD} = 0 V; t < t_{TXD_DTO}; 4.75 V ≤ V_{CC} ≤ 5.25 V; 50 Ω ≤ R_L ≤ 65 Ω	2.75	3.5	4.5	V
	Dominant Output Voltage, CANL	Dominant; V_{TXD} = 0 V; t < t_{TXD_DTO}; 4.75 V ≤ V_{CC} ≤ 5.25 V; 50 Ω ≤ R_L ≤ 65 Ω	0.5	1.5	2.25	V
$V_{TX\_SYM\_DOM}$	Transmitter Dominant Voltage Symmetry	$V_{TX\_SYM\_DOM}$ = V_{CAN} − V_{CANH} − V_{CANL}; V_{CAN} = 5 V	−400		400	mV
V_{TX_SYM}	Transmitter Symmetry (Dominant or Recessive), V_{CANH} + V_{CANL} / V_{CC} (1)	4.75 V ≤ V_{CAN} ≤ 5.25 V; C_{SPLIT} = 4.7 nF;R_L = 60 Ω; f_{TXD} = 250 kHz, 1 MHz, 2.5 MHz	0.9		1.1	
V_{OD_DOM}	Dominant Differential Output Voltage	Normal mode; V_{TXD} = 0 V; t < t_{TXD_DTO}; 4.75 V ≤ V_{CAN} ≤ 5.25 V; 50 Ω ≤ R_L ≤ 65 Ω	1.5		3	V
		Normal mode; V_{TXD} = 0 V; t < t_{TXD_DTO}; 4.75 V ≤ V_{CAN} ≤ 5.25 V; 45 Ω ≤ R_L ≤ 70 Ω	1.4		3.3	V
		Normal mode; V_{TXD} = 0 V; t < t_{TXD_DTO}; 4.75 V ≤ V_{CAN} ≤ 5.25 V; R_L = 2240 Ω (1)	1.5		5	V
V_{OD_REC}	Recessive Differential Output Voltage	Active/listen-only/offline bias mode; V_{TXD} = V_{IO}	−50		50	mV
		Offline mode	−0.2		0.2	V
V_{O_REC}	Recessive Output Voltage	Active mode; V_{TXD} = V_{IO}; no load	2	0.5 × V_{CAN}	3	V
		Offline bias/listen-only mode; V_{TXD} = V_{IO}; no load	2	2.5	3	V
		Offline mode; no load	−0.1		0.1	V
$I_{O\_SC\_DOM}$	Dominant Short-Circuit Output Current	−40 V ≤ V_{CANH} / V_{CANL} ≤ +40 V	−75		75	mA
$I_{O\_SC\_REC}$	Recessive Short-Circuit Output Current	−40 V ≤ V_{CANH} / V_{CANL} ≤ +40 V	−3		3	mA
$V_{TH\_RX\_DIF}$	Differential Receiver Threshold Voltage	Active/listen-only mode; t < t_{TXD_DTO}; −30 V ≤ V_{CANH} / V_{CANL} ≤ +30 V	0.5		0.9	V
		Offline mode; t < t_{TXD_DTO}; −30 V ≤ V_{CANH} / V_{CANL} ≤ +30 V	0.4		1.15	V
V_{REC_RX}	Receiver Recessive Voltage (1)	Normal mode; t < t_{TXD_DTO}; −30 V ≤ V_{CANH} / V_{CANL} ≤ +30 V	−4		0.5	V
		Standby mode; t < t_{TXD_DTO}; −30 V ≤ V_{CANH} / V_{CANL} ≤ +30 V	−4		0.4	V
V_{DOM_RX}	Receiver Dominant Voltage (1)	Normal mode; t < t_{TXD_DTO}; −30 V ≤ V_{CANH} / V_{CANL} ≤ +30 V	0.9		9	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Standby mode; $t < t_{TXD\_DTO}$; $-30\ V \le V_{CANH} / V_{CANL} \le +30\ V$	1.15		9	V
$V_{HYS\_RX\_DIF}$	Differential Receiver Hysteretic Threshold	Normal mode; $t < t_{TXD\_DTO}$; $-30\ V \le V_{CANH} / V_{CANL} \le +30\ V$	50	100	300	mV
R_{IN}	CANH or CANL Input Resistance	$-2\ V \le V_{CANH} / V_{CANL} \le +7\ V$	25	40	50	kΩ
ΔR_{IN}	Input Resistance Deviation	$0\ V \le V_{CANH} / V_{CANL} \le +5\ V$	−3		3	%
R_{IN_DIF}	Differential Input Resistance	$-2\ V \le V_{CANH} / V_{CANL} \le +7\ V$	50	80	100	kΩ
C_{IN}	Common-Mode Input Capacitance (1)				30	pF
C_{IN_DIF}	Differential Input Capacitance (1)				15	pF
I_L	Unpowered Bus Input Leakage Current	$V_{BAT} = V_{CAN} = 0\ V$ or pins shorted to GND via 47 kΩ; $V_{CANH} = V_{CANL} = 5\ V$	−10		10	μA
V_{UVD_CAN}	CAN Under-Voltage Detection Voltage	On pin BAT; V_{BAT} falling	4.2		4.55	V
		V_{CAN} falling (1)	4.45		4.8	V
V_{UVR_CAN}	CAN Under-Voltage Recovery Voltage	On pin BAT; V_{BAT} rising	4.5		5	V
		V_{CAN} rising (1)	4.45		4.8	V
I_{DD_CAN}	CAN Supply Current	CAN active mode; CAN recessive; $V_{TXD} = V_{V1}$	1	3.3	6	mA
			3	7.5	15	mA
Pin CANH; CANL; SIC						
$R_{IN\_DIF\_ACT\_REC}$	Active Recessive Phase Differential Input Resistance (1)	Recessive; $V_{TXD} = 0\ V$; $t < t_{TXD\_DTO}$; $4.75\ V \le V_{CC} \le 5.25\ V$; $1.5\ V \le V_{CANH} \le V_{CC} - 1.5\ V$; $1.5\ V \le V_{CANL} \le V_{CC} - 1.5\ V$; $R_{IN\_DIF\_ACT\_REC} = R_{IN\_ACT\_REC\_CANH} + R_{IN\_ACT\_REC\_CANL}$	75		133	Ω
Temperature Detection						
T_{J_OTP}	Over-Temperature Protection Junction Temperature		167	177	187	°C
$T_{J\_OTP\_R}$	Over-Temperature Protection Recover Junction Temperature		125	137	147	°C
$T_{J\_OTP\_WARN}$	Over-Temperature Protection Warning Junction Temperature		127	137	147	°C
MTP Non-Volatile Memory						
$N_{CY\_W\_MTP}$	Number of MTP Write Cycles (1)	$6\ V \le V_{BAT} \le 40\ V$; $0\ ℃ \le T_J \le 125\ ℃$			1,000	

(1) The data is based on bench test and design simulation

AC Timing Requirements

All test conditions: V_{BAT} = 12 V, R_L = 60 Ω, T_A = −40°C to 125°C, unless otherwise noted.

Symbol	Parameter	Condition	Max	Typ	Min	Unit
V_{OUT1} Timing Characteristics						
t_{START_UP}	Start-up Time	Time from V_{BAT} > $V_{TH\_DET\_PON}$ until V_{OUT1} > $V_{UV\_OUT1\_NORM}$ (90%); C_{VOUT1} = 4.7 µF		2.8	4.7	ms
t_{D_UVD}	Under-Voltage Detection Delay Time (1)	V_{OUT1} falling	6		54	µs
$t_{D\_UVD-RSTN}$	Delay Time from Under-Voltage Detection to RSTN Low (1)	Undervoltage on V_{OUT1}			63	µs
V_{OUT2} Timing Characteristics						
t_{D_UVD}	Under-Voltage Detection Delay Time (1)	V_{OUT2}/V_{EXT} falling	6		32	µs
		At start-up V_{OUT2}/V_{EXT}	2.2	2.5	2.8	ms
t_{D_OVD}	Over-Voltage Detection Delay Time (1)	V_{OUT2}/V_{EXT} rising	6		32	µs
SPI Timing Characteristics (1)						
t_{CY_CLK}	Clock Cycle Time		250			ns
t_{SPI_LEAD}	SPI Enable Lead Time		50			ns
t_{SPI_LAG}	SPI Enable Lag Time		50			ns
t_{CLK_H}	Clock High Time		100			ns
t_{CLK_L}	Clock Low Time		100			ns
t_{SU_D}	Data Input Set-up Time		50			ns
t_{H_D}	Data Input Hold Time		50			ns
t_{V_Q}	Data Output Valid Time	SDO pin; C_L = 20 pF			50	ns
$t_{D\_SDI\_SDO}$	SDI to SDO Delay Time	SPI address bits and read-only bit; C_L = 20 pF			50	ns
t_{WH_S}	Chip Select Pulse Width High	SCSN pin	250			ns
$t_{D\_SCK-SCSN}$	Delay Time from SCK Low to SCSN Low		50			ns
CAN Timing Characteristics						
$t_{D\_TXDL\_RXDL}$	Loop Delay Time from TXD Low to RXD Low	Normal mode; V_{TXD} = 30% V_{OUT1} to V_{RXD} = 30% V_{OUT1}; C_{RXD} = 15 pF; f_{TXD} = 250 kHz; R_L = 60 Ω; C_L = 100 pF			190	ns
$t_{D\_TXDH\_RXDH}$	Loop Delay Time from TXD High to RXD High	Normal mode; V_{TXD} = 70% V_{OUT1} to V_{RXD} = 70% V_{OUT1}; C_{RXD} = 15 pF; f_{TXD} = 250 kHz; R_L = 60 Ω; C_L = 100 pF			190	ns

Symbol	Parameter	Condition	Max	Typ	Min	Unit
$t_{D\_TXD\_BUS\_DOM}$	Delay Time from TXD to Bus Dominant	Normal mode; R_L = 60 Ω; C_L = 100 pF; $V_{CANH} - V_{CANL}$ = 900 mV		60	80	ns
$t_{D\_TXD\_BUS\_REC}$	Delay Time from TXD to Bus Recessive	Normal mode; R_L = 60 Ω; C_L = 100 pF; $V_{CANH} - V_{CANL}$ = 900 mV		60	80	ns
$t_{D\_BUSDOM\_RXD}$	Delay Time from Bus Dominant to RXD	C_{RXD} = 15 pF; V_{RXD} = 30% V_{OUT1}		105	110	ns
$t_{D\_BUSREC\_RXD}$	Delay Time from Bus Recessive to RXD	C_{RXD} = 15 pF; V_{RXD} = 70% V_{OUT1}		105	110	ns
$t_{D\_PAS\_REC\_START}$	Signal improvement start time of passive recessive phase (1)	Normal mode; 4.75 V ≤ V_{CC} ≤ 5.25 V R_L = 60 Ω; C_L = 100 pF; C_{RXD} = 15 pF;			530	ns
$t_{D\_ACT\_REC\_START}$	Start time of active signal improvement phase Start time of active signal improvement phase (1)	Normal mode; 4.75 V ≤ V_{CC} ≤ 5.25 V R_L = 60 Ω; C_L = 100 pF; C_{RXD} = 15 pF			120	ns
$t_{D\_ACT\_REC\_END}$	End time of active signal improvement phase (1)	Normal mode; 4.75 V ≤ V_{CC} ≤ 5.25 V R_L = 60 Ω; C_L = 100 pF; C_{RXD} = 15 pF	355			ns
$t_{WAKE\_BUS\_DOM}$	Bus Dominant Wake-up Time	Pulse for wake-up on CANH and CANL pins; CAN offline mode	0.5		1.8	μs
$t_{WAKE\_BUS\_REC}$	Bus Recessive Wake-up Time	Pulse for wake-up on CANH and CANL pins; CAN offline mode	0.5		1.8	μs
t_{WAKE_TO}	Wake-up Time-out Time	Between first and second dominant pulses; CAN offline modes	0.8		10	ms
t_{TXD_DTO}	TXD Dominant Time-out Time	CAN active mode; TXD = 0 V	2.7		3.3	ms
$t_{TO\_SILENCE}$	Bus Silence Time-out Time (1)	Recessive time measurement started in all CAN modes	0.95		1.17	s
$t_{D\_BUSACT-BIAS}$	Delay Time from Bus Active to Bias				200	μs
$t_{STARTUP\_CAN}$	CAN Start-up Time	To CTS = 1; when switching to active mode			220	μs
CAN FD Timing Characteristics						
Δt_{BIT_BUS}	Transmitted Recessive Bit Width Deviation	$\Delta t_{BIT\_BUS} = t_{BIT\_BUS} - t_{BIT\_TXD}$ R_L = 60 Ω; C_L = 100 pF; C_{RXD} = 15 pF	−10		10	ns
Δt_{REC}	Receiver Timing Symmetry	$\Delta t_{REC} = t_{BIT\_RXD} - t_{BIT\_BUS}$ R_L = 60 Ω; C_L = 100 pF; C_{RXD} = 15 pF	−20		15	ns
Δt_{BIT_RXD}	Received Recessive Bit Width Deviation	$\Delta t_{BIT\_RXD} = t_{BIT\_RXD} - t_{BIT\_TXD}$ R_L = 60 Ω; C_L = 100 pF; C_{RXD} = 15 pF	−30		20	ns
t_{BIT_BUS}	Transmitted Recessive Bit Width	2 Mbps, t_{BIT_TXD} = 500 ns; 4.75 V ≤ V_{CC} ≤ 5.25 V R_L = 60 Ω; C_L = 100 pF; C_{RXD} = 15 pF	490		510	ns
		5 Mbps, t_{BIT_TXD} = 200 ns;	190		210	ns

Symbol	Parameter	Condition	Max	Typ	Min	Unit
		4.75 V ≤ V_{CC} ≤ 5.25 V R_L = 60 Ω; C_L = 100 pF; C_{RXD} = 15 pF				
		8 Mbps, t_{BIT_TXD} = 125 ns; 4.75 V ≤ V_{CC} ≤ 5.25 V R_L = 60 Ω; C_L = 100 pF; C_{RXD} = 15 pF	115		135	ns
t_{BIT_RXD}	RXD Bit Width	2 Mbps, t_{BIT_TXD} = 500 ns; 4.75 V ≤ V_{CC} ≤ 5.25 V R_L = 60 Ω; C_L = 100 pF; C_{RXD} = 15 pF	470		520	ns
		5 Mbps, t_{BIT_TXD} = 200 ns; 4.75 V ≤ V_{CC} ≤ 5.25 V R_L = 60 Ω; C_L = 100 pF; C_{RXD} = 15 pF	170		220	ns
		8 Mbps, t_{BIT_TXD} = 125 ns; 4.75 V ≤ V_{CC} ≤ 5.25 V R_L = 60 Ω; C_L = 100 pF; C_{RXD} = 15 pF	95		145	ns
CAN Partial Networking						
N_{IDLE_BITS}	Number of idle bits (1)	Before a new SOF is accepted	6		10	
t_{FLTR_DOM}	Dominant bit filter time(1)	arbitration data rate ≤ 500 kbps	5		8.75	%
Event Capture Timing Characteristics						
t_{D_EVENT}	Event Capture Delay Time	CAN offline mode	0.9		1.1	ms
t_{BLANK}	Blanking Time	Switching from offline to active/listen-only mode			25	µs
t_{MODE}	Normal Mode Activation Delay Time (1)	MC = 111; delay before CAN is activated after the device switches to normal mode			320	µs
Watchdog Timing Characteristics						
t_{TRIG_WD1}	Watchdog Trigger Time 1 (1)	Normal mode; watchdog window mode only	0.45 × NWP		0.55 × NWP	ms
t_{TRIG_WD2}	Watchdog Trigger Time 2 (1)	Normal/standby mode	0.9 × NWP		1.11 × NWP	ms
$t_{D\_SCSNH\_RSTNL}$	Delay Time from SCSN High to RSTN Low (1)				0.2	ms
RSTN Timing Characteristics						
t_{W_RST}	Reset Output Pulse Width	RLC = 00	20		25	ms
		RLC = 01 (1)	10		12.5	ms
		RLC = 10 (1)	3.6		5	ms
		RLC = 11 (1)	1		1.5	ms
	Reset Input Pulse Width (1)		18			µs
LIMP Timing Characteristics						
t_{D_LIMP}	Limp Delay Time (1)		117		145	ms
WAKE Timing Characteristics						

Symbol	Parameter	Condition	Max	Typ	Min	Unit
t_{WAKE}	Wake-up Time	RLC = 00	55			μs
MTP Non-volatile Timing Characteristics						
t_{D_MTPNV}	MTPNV Delay Time (1)	Before factory presets are restored; 6 V ≤ V_{BAT} ≤ 28 V	0.9		1.1	s
t_{RET_DATA}	Data Retention Time (1)	125℃	10			Year
t_{PROG_MTPNV}	MTPNV Programming Time (1)		0.8	1.2	1.4	ms

(1) The test data is based on bench tests and design simulation.

Typical Performance Characteristics

All test condition: V_{BAT} =12 V, T_A =+ 25°C, unless otherwise noted.

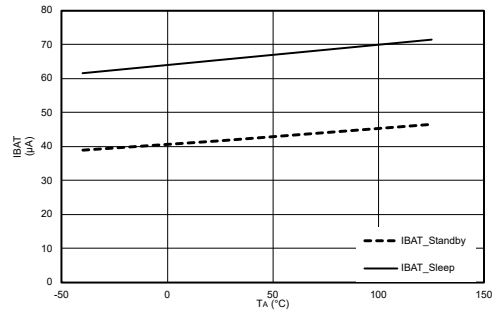


Figure 1. TPT1169 typical Standby and Sleep mode quiescent current (Vbat=12V)

Detailed Description

Overview

The TPT1169xQ is a system basis chip (SBC) designed for automotive applications. The device functions as a main power supply for the microcontroller and as a transceiver for the CAN bus networks.

The SBC integrates 250-mA main low drop-out voltage regulator for the microcontroller as a power supply with 5-V and 3.3-V output options. Additionally, it includes another 5-V 150-mA low drop-out voltage regulator for other on-board device power supply. The X version features a voltage regulator with off-board protection, designed for off-board devices power supply. Furthermore, the SBC integrates CAN transceiver that supports partial networking and enables data rates of up to 8 Mbps. This transceiver meets the ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5 Physical Layer Standards. Variants with signal improvement capability (SIC) also meets CiA601-4 standards. Moreover, the system integrates a configurable timeout/window watchdog with a reset feature, limp home outputs, and an undervoltage reset feature. It also includes an integrated 16-bit Serial Peripheral Interface (SPI) for configuration and monitoring purposes, and a LIMP output pin for indicating system failures.

The SBC offers low-power modes for low-power consumption applications. The device can be woken up from remote wake-up via bus.

The TPT1169xQ is available in the exposed pad DFN3.5X5.5-20L package, featuring enhanced automated optical inspection (AOI) capabilities. Additionally, it is AEC-Q100 qualified for automotive applications.

Functional Block Diagram

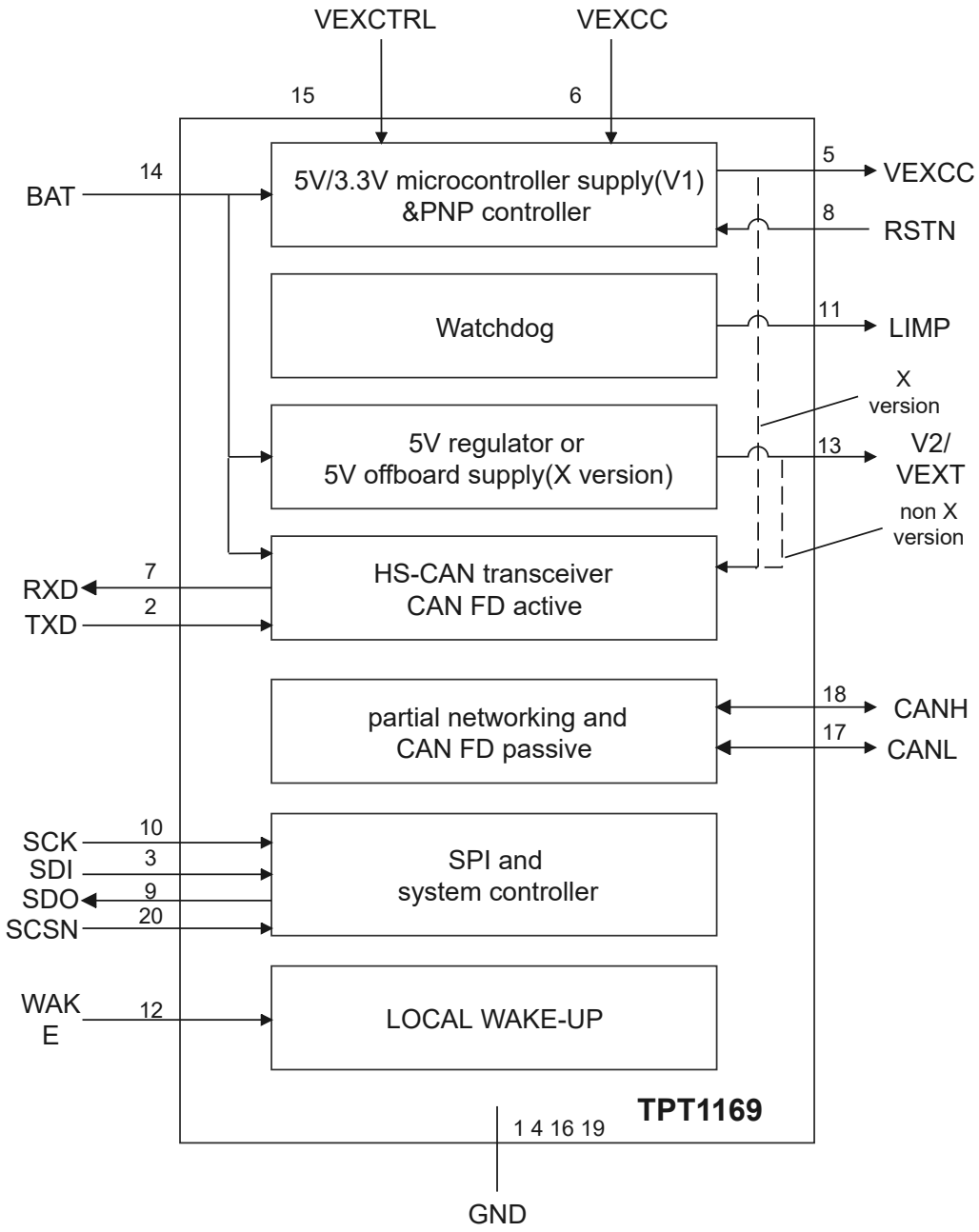


Figure 2. Functional Block Diagram

Feature Description

System Controller

The system controller handles all configurations, registers, and system features of the TPT1169.

Operating Modes

The system controller controls seven operating modes of the TPT1169 via the state machine: Normal, Standby, Sleep, Reset, Forced Normal, Overtemp, and Off. All the state transitions are shown in Figure 3. All the hardware resources mapping with the operating modes are shown as Table 2.

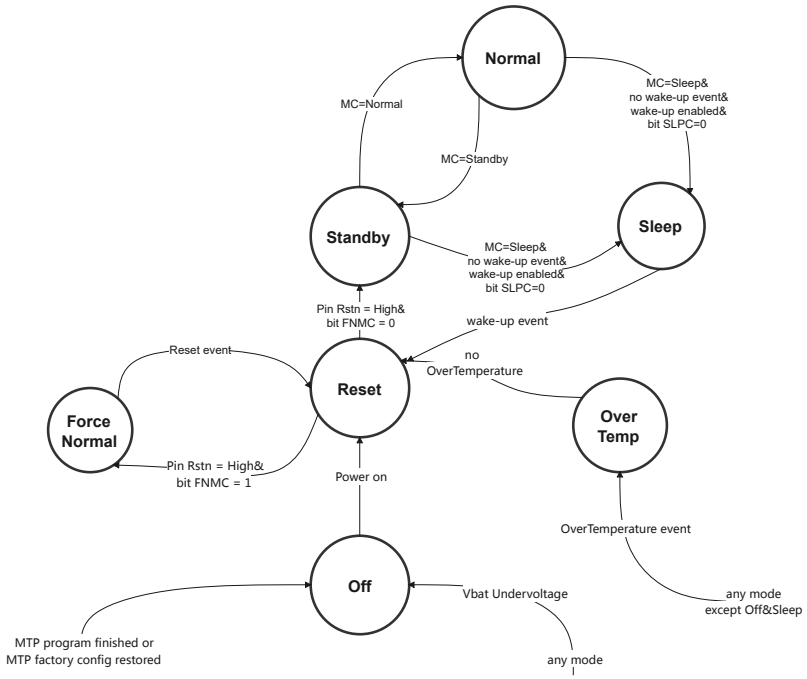


Figure 3. TPT1169 System Controller State Diagram

Normal Mode

Normal mode is the main operating mode in which all the hardware of the TPT1169 can be activated. Voltage regulator V1 is enabled to supply the microcontroller. The CAN interface can be activated via an SPI command to support CAN communication. Depending on the register settings, the watchdog can run in Window or Timeout mode, and the V2/VEXT output can be active. Normal mode can only be switched from Standby mode via an SPI command, and other modes are unable to switch to Normal mode directly.

Standby Mode

Standby mode is the first low-power level to reduce current consumption. In Standby mode, the CAN transceiver is disabled, unable to transmit or receive data to or from the CAN bus. Voltage regulator V1 is still active, and the state of voltage regulator V2/VEXT is determined by the SPI settings. The SPI command is still active. The watchdog is active, but can be disabled and only works in Timeout mode.

In Standby mode, the CAN bus is biased to GND via an internal pull-down resistor when no signal is on the bus for $t > t_{TO\_SILENCE}$. When a signal occurs on the CAN bus, the voltage biases to about 2.5 V.

If remote CAN wake-up is enabled, the CAN receiver monitors the bus for wake-up events. When a CAN bus wake-up event occurs, the RXD signal is low. The wake-up source can be either a wake-up pattern or a selective wake-up frame, which depends on the SPI settings. The default setting is a wake-up pattern.

Standby mode can be switched from Reset mode automatically unless RSTN is high and bit FNMC is 0. Also, Standby mode can be switched from Normal mode via an SPI command.

Sleep Mode

Sleep mode is the second low-power level and has very low power consumption. In Sleep mode, the CAN transceiver is disabled, unable to transmit or receive data to or from the CAN bus. Voltage regulator V1 is off, and the state of voltage regulator V2/VEXT is determined by the SPI settings. The SPI command is inactive. The watchdog is active but can be disabled according to the watchdog configuration shown in Table 5, and only works in Timeout mode. The over-temperature protection is inactive.

In Sleep mode, the CAN bus is biased to GND via an internal pull-down resistor when no signal is on the bus for $t > t_{TO\_SILENCE}$. When a signal occurs on the CAN bus, the voltage biases to about 2.5 V.

The CAN bus wake-up event or diagnostic event can wake up the TPT1169 from Sleep mode to Reset mode, and can set the corresponding event bits. SPI is inactive in Sleep mode, so the SPI command is unable to switch the TPT1169 to other operating modes or config registers.

Sleep mode can be switched from Normal mode or Standby mode via the SPI command, provided that all wake-up pending is clear and at least one wake-up source is enabled. When switching to Sleep mode, if the conditions above are not met, the TPT1169 switches to Reset mode rather than Sleep mode.

Sleep mode can be permanently disabled by setting bit SLPC to 0 in register 0x74h in the non-volatile memory area. Once bit SLPC is set to 1, an SPI command intended for Sleep mode is unable to switch the chip to Sleep mode, and if SPIFE is enabled, an SPI failure event is triggered. This feature is used in applications where the MCU must power on at all times.

Reset Mode

Reset mode is to reset and initiate the internal controller. In Reset mode, the CAN transceiver is disabled, unable to transmit or receive data to or from the CAN bus. Voltage regulator V1 is on, and the state of voltage regulator V2/VEXT is determined by the SPI settings. The SPI command is inactive, the watchdog is disabled, and the over-temperature protection is inactive.

The TPT1169 can switch to Reset mode from any mode in response to a certain reset source, as shown in Table 4. There are four paths after leaving Reset mode:

- To Standby mode if pin RSTN is released to a high level;
- To Forced Normal mode if bit FNMC is 1;
- To Off mode if the TPT1169 powers off;
- To Overtemp mode if an over-temperature event occurs.

If the TPT1169 switches to Reset mode by a V1 undervoltage event, it remains in Reset mode unless V1 is recovered.

Off Mode

Off mode is triggered when voltage V_{BAT} is below $V_{TH\_DEC\_POFF}$. In Off mode, only power-on detection is active. When the battery voltage exceeds the power-on detection threshold $V_{TH\_DEC\_PON}$, the TPT1169 starts to initialize and switches to Reset mode after t_{START_UP}.

In Off mode, pins CANH and L are high-impedance to the CAN bus network.

Overtemp Mode

Overtemp mode seeks to protect the chip from any potential damage caused by extreme temperature. When chip temperature exceeds the protection activation threshold T_{J_OTP}, the TPT1169 can switch to Overtemp mode from any mode except for Sleep and Off modes.

In Overtemp mode, the CAN transceiver is disabled, unable to transmit or receive data to or from the CAN bus. Both voltage regulators V1 and V2/VEXT are off. Any CAN bus wake-up or diagnostic events are monitored but existing wake-up pending remains. Pin RSTN is low.

The TPT1169 provides a register bit for MCU to monitor whether the temperature is high enough to trigger Overtemp mode. When the temperature exceeds the warning threshold $T_{J\_OTP\_WARN}$, the status bit OTWS is set. An over-temperature warning event (OTW) is captured if it is enabled (set OTWE to 1).

The TPT1169 switches from Overtemp mode to Reset mode when temperature falls below the protection release threshold $T_{J\_OTP\_R}$, or to Off mode if V_{BAT} falls below $V_{TH\_DET\_POFF}$.

Forced Normal Mode

In Forced Normal mode, the CAN transceiver is active, the watchdog is inactive, and voltage regulators V1 and V2/VEXT are on. CAN communication works without any software development, especially without serving the watchdog. This mode provides a simple way to use the TPT1169.

The TPT1169 is in Forced Normal mode by factory presetting, and the bit FNMC restored in non-volatile memory is set to 1. If the register is programmed to 0, the chip switches from Forced Normal mode to Reset mode first and then to Standby mode.

Certain reset events, such as V1 undervoltage or an external reset, trigger the TPT1169 to enter Reset mode, even when the TPT1169 is in Forced Normal mode. The reset behavior is almost the same as general Reset mode, except that the CAN transceiver is still active. When the TPT1169 exits Reset mode, it switches to Forced Normal mode instead of Standby mode.

In Forced Normal mode, only the main status register, watchdog status register, identification register, MTPNV status register, and registers stored in non-volatile memory can be read. The non-volatile memory area can be programmed if the chip is in the factory-preset state shown in Non-Volatile SBC Configuration.

Hardware Characterization for the TPT1169 Operating Modes

Table 2. Hardware Characterization by Functional Block

Function Module	Operation Mode						
	Off	Forced Normal	Standby	Normal	Sleep	Reset	Overtemp
V1	Off (4)	On	On	On	Off	On	Off
SPI	Disabled	Enabled (3)	Enabled	Enabled	Disabled	Disabled	Disabled
VEXT/V2	Off	On	(1)	(1)	(1)	(1)	Off
RSTN	Low	High	High	High	Low	Low	Low
Watchdog	Off	Off	(2)	(2)	(2)	Off	Off
CAN	Off	Active	Offline or Offline Bias	Active/Offline/Offline bias/Silent determined by CMC bits	Offline or Offline Bias	Offline or Offline Bias	Off
RXD	V1 level	CAN communication	V1 level/low, if wake-up detected	CAN communication, if CMC = 01/10/11; same as Standby/ Sleep, if CMC = 00	V1 level/low, if wake-up detected	V1 level/low, if wake-up detected	V1 level/low, if wake-up detected

(1) Depending on bits V2C/VEXTC and V2SUC/VEXTSUC (see Table 11).
(2) Depending on bits WMC.
(3) Only the Main status register, watchdog status register, identification register, MTPNV status register, and registers stored in non-volatile memory.
(4) V1 behaves as the current source when V_{BAT} falls from $V_{TH\_DET\_POFF}$ to 2 V (ram retention, shown in Battery Voltage).

System Control Register

Mode Control Register

The operating mode is selected via bits MC within the mode control register. The register address is 01h.

Table 3. Mode Control Register 01h

Bit	Symbol	Access	Value	Description
7:3	Reserved	R	-	-
2:0	MC	R/W		Mode control and status:
			001	Sleep mode
			100	Standby mode
			111	Normal mode

Main Status Register

The register can indicate the status of overtemperature, whether the chip has entered Normal mode after power-on, and the resource of the most recent reset causes.

Table 4. Main Status Register 03h

Bit	Symbol	Access	Value	Description
7	Reserved	R		
6	OTWS	R		Overtemperature warning status:
			0	IC temperature below the overtemperature warning threshold
			1	IC temperature above the overtemperature warning threshold
5	NMS	R		Normal mode status:
			0	The TPT1169 has entered Normal mode (after power-up)
			1	The TPT1169 has powered up but has not switched to Normal mode
4:0	RSS	R		Reset source status:
			00000	Leave Off mode (power-on)
			00001	CAN wake-up in Sleep mode
			00100	Wake-up via pin WAKE in Sleep mode
			01100	Watchdog overflow in Sleep mode (Timeout mode)
			01101	Diagnostic wake-up in Sleep mode
			01110	Watchdog triggered too early (Window mode)
			01111	Watchdog overflow (Window mode or Timeout mode with WDF =1)

Bit	Symbol	Access	Value	Description
			10000	Illegal watchdog mode control access
			10001	RSTN pulled down externally
			10010	Leave Overtemp mode
			10011	V1 undervoltage
			10100	Illegal Sleep mode command received
			10110	Wake-up from Sleep mode due to a frame detection error

Watchdog

Watchdog Overview

The TPT1169 offers three watchdog operating modes: Window, Timeout, and Autonomous. In Window mode, only a defined period is available in the watchdog window and can reset the watchdog counter. In Timeout mode, the watchdog can be triggered and reset at any time within the watchdog period, and it also serves to wake up the microcontroller cyclically. In Autonomous mode, the watchdog can be off or in Timeout mode, depending on the TPT1169 operating mode (shown in Watchdog Behavior in Autonomous Mode).

The watchdog mode is determined by bit WMC in the watchdog control register (see Table 6). The watchdog mode (including changing period or mode) can only be changed in Standby mode. Any access to change the mode (bit WMC) or period (bit NWP) in Normal mode switches the TPT1169 to Reset mode, and the reset source status (RSS) bits are set to 10000 ('illegal watchdog mode control access' as shown in Table 4); Meanwhile, an SPI failure occurs if bit SPIFE is enabled.

The watchdog remains in Timeout mode even when bit WMC is set to Window mode and the TPT1169 is in Standby mode. Only when the TPT1169 switches to Normal mode, the watchdog switches to Window mode.

The watchdog period is programmed via bit NWP, and 8 periods are supported, from 8 ms to 4096 ms. The configured period affects in both Timeout and Window mode. The default value is 128 ms. A correct SPI access to Watchdog control register is a valid trigger signal and resets the watchdog counter.

Table 5. Watchdog Configuration

Bit Config	FNMC	0	0	0	0	1
	SDMC	X	X	0	1	X
	WMC	100 (Window)	010 (Timeout)	001 (Autonomous)	001 (Autonomous)	X
Operation Mode	Normal	Window	Timeout	Timeout	Off	Off
	Standby (RXD High) (1)	Timeout	Timeout	Off	Off	Off
	Standby (RXD Low) (1)	Timeout	Timeout	Timeout	Off	Off
	Sleep	Timeout	Timeout	Off	Off	Off
	Others	Off	Off	Off	Off	Off

(1) RXD low indicates a wake-up pending.

Watchdog Control Register

Given that the watchdog is a valuable safety mechanism, it is important to configure it correctly. A configuration protection feature is available in Normal mode to prevent accidental changes to the watchdog.

Table 6. Watchdog Control Register 00h

Bit	Symbol	Access	Value	Description
7:5	WMC	R/W		Watchdog mode control:
			001	Autonomous mode
			010	Timeout mode
			100	Window mode
4	Reserved	R	-	-
3:0	NWP	R/W		Nominal watchdog period:
			1000	8 ms
			0001	16 ms
			0010	32 ms
			1011	64 ms
			0100	128 ms
			1101	256 ms
			1110	1024 ms
			0111	4096 ms

SBC Configuration Control Register

Forced Normal mode and Software Development mode greatly influence the operation of the watchdog. They are configured via bits FNMC and SDMC in the SBC configuration control register (note that this register is located in a non-volatile memory area). In Forced Normal mode, the watchdog is disabled. In Software Development mode, the watchdog can be enabled or disabled, depending on bit WMC.

Table 7. SBC Configuration Control Register 74h

Bit	Symbol	Access	Value	Description
7:6	Reserved	R		
5:4	V1RTSUC	R/W	(1)	V1 reset threshold (defined by bit V1RTC) at start-up:
			00 (2)	V1 undervoltage detection at 90% of nominal value at start-up (V1RTC = 00)
			01	V1 undervoltage detection at 80% of nominal value at start-up (V1RTC = 01)
			10	V1 undervoltage detection at 70% of nominal value at start-up (V1RTC = 10)
			11	V1 undervoltage detection at 60% of nominal value at start-up (V1RTC = 11)
3	FNMC	R/W	(3)	Forced Normal mode control:
			0	Forced Normal mode disabled
			1 (2)	Forced Normal mode enabled
2	SDMC	R/W		Software Development mode control:
			0 (2)	Software Development mode disabled
			1	Software Development mode enabled
1	Reserved	R		
0	SLPC	R/W		Sleep control:
			0 (2)	Sleep mode commands accepted
			1	Sleep mode commands ignored

(1) The threshold is fixed at 90% of nominal voltage in 3V3 version regardless of bit settings.
(2) Factory-preset value.
(3) FNMC settings priority to SDMC.

Watchdog Status Register

This register displays the watchdog status and shows whether Forced Normal mode and Software Development mode are enabled.

Table 8. Watchdog Status Register 05h

Bit	Symbol	Access	Value	Description
7:4	Reserved	R	-	
3	FNMS	R		Forced Normal mode status:
			0	SBC is not in Forced Normal mode
			1	SBC is in Forced Normal mode
2	SDMS	R		Software Development mode status:
			0	SBC is not in Software Development mode
			1	SBC is in Software Development mode

Bit	Symbol	Access	Value	Description
1:0	WDS	R		Watchdog status:
			00	Watchdog is off
			01	Watchdog is in the first half of the nominal period
			10	Watchdog is in the second half of the nominal period
			11	Reserved

Software Development Mode

Software Development mode is provided to simplify the software process in prototyping development. When Software Development mode is enabled, bit WMC is set to 001 (Autonomous mode), and the watchdog is inactive after a system reset. If Software Development mode is enabled, the watchdog is disabled in Autonomous mode. The watchdog can also be active in Software Development mode by setting the watchdog in Window mode or Timeout mode, as shown in Table 5.

Watchdog Behavior in Window Mode

The watchdog is in window mode by setting bit WMC to 100, and the TPT1169 is in Normal mode.

In Window mode, only the second half of the watchdog period is valid. If the watchdog overflows or is triggered in the first half of the watchdog period (t_{TRIG_WD1}), a system reset occurs. The reset source is set in bit RSS, indicating either 'watchdog triggered too early' or 'watchdog overflow'. If the watchdog is triggered in the second half of the watchdog period (after t_{TRIG_WD1} but before t_{TRIG_WD2}), the watchdog counter is reset.

Watchdog Behavior in Timeout Mode

The watchdog is in Timeout mode by setting bit WMC to 010, and the TPT1169 can be in Normal mode, Standby mode, and Sleep mode. The watchdog is in Timeout mode if bit WMC is 100 and the TPT1169 is in Standby or Sleep mode. The watchdog is in Timeout mode if WMC is 001 and one of the conditions is met in Table 9.

In Timeout mode, the watchdog can be triggered at any time. If the watchdog overflows, a watchdog failure (WDF) event occurs. An existing WDF combined with a new watchdog overflow causes a system reset. The watchdog can be used to cyclically wake up the microcontroller when the TPT1169 is in Standby or Sleep mode.

When the TPT1169 is in Sleep mode with watchdog Timeout mode, a wake-up event occurs after the watchdog period. The reset source is set in bit RSS, indicating 'watchdog overflow in Sleep mode (Timeout mode)'. Pin RXD is driven low, and WDF is set.

Watchdog Behavior in Autonomous Mode

The watchdog is in Timeout mode by setting bit WMC to 010, and the actual behavior of the watchdog is shown in Table 9.

Table 9. Watchdog Status in Autonomous Mode

TPT1169 Operating Mode	Watchdog Status	
	SDMC = 0	SDMC = 1
Normal	Timeout Mode	Off
Standby; RXD High	Off	Off
Sleep	Off	Off
Any Other Modes	Off	Off

TPT1169 Operating Mode	Watchdog Status	
	SDMC = 0	SDMC = 1
Standby; RXD Low	Timeout Mode	Off

When Autonomous mode is set, the watchdog is in Timeout mode if the TPT1169 is in Normal mode or Standby mode with pin RXD low.

The watchdog is off when the TPT1169 is in Sleep mode or Standby mode with pin RXD high. If a wake-up event occurs when the TPT1169 is in Sleep mode, the chip switches to Standby mode, and the watchdog is in Timeout mode. If a wake-up event occurs when the TPT1169 is in Standby mode, pin RXD is driven low, and the watchdog switches to Timeout mode.

If the watchdog is unnecessary to work in Sleep mode in this application, it should be set in Autonomous mode before switching the TPT1169 to Sleep mode.

System Reset

When a system reset occurs, the TPT1169 switches to Reset mode, begins to initiate, and drives a low-level pulse on pin RSTN. There are 13 reset resources as shown in Table 4.

Characteristics of Pin RSTN

Pin RSTN functions as a bidirectional open-drain low-side driver that has an internal pull-up resistor as shown in Figure 4. The TPT1169 can detect whether this pin is externally pulled down. An input pulse width shall be at least t_{W_RST} to ensure accurate detection of any external reset event.

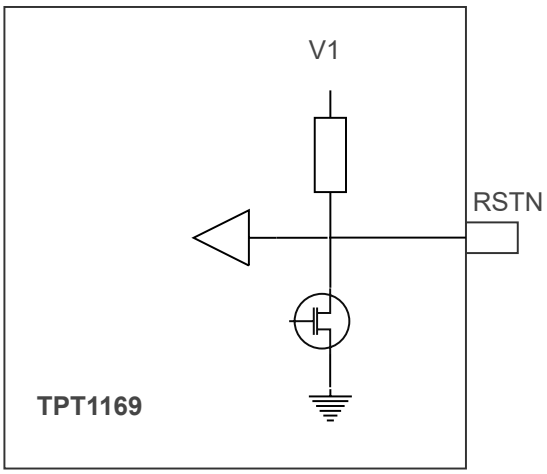


Figure 4. RSTN Internal Pin Configuration

Selection of the Output Reset Pulse Width

The TPT1169 has a cold start and a warm start. The following events cause the cold start: power-on reset, reset during Sleep mode, over-temperature reset, and V1 undervoltage. These events cause the warm start: external reset, watchdog failure, watchdog change attempt in Normal mode, and illegal Sleep mode command.

The interval of the cold reset output reset pulse width is configured by bits RLC in the start-up control register (see Table 10). The interval of the warm reset output reset pulse width is the shortest width regardless of bits RLC.

Table 10. Start-up Control Register 73h

Bit	Symbol	Access	Value	Description
7:6	Reserved	R	-	
5:4	RLC	R/W		RSTN output reset pulse width:
			00 (1)	t_{W_RST} = 20 ms to 25 ms
			01	t_{W_RST} = 10 ms to 12.5 ms
			10	t_{W_RST} = 3.6 ms to 5 ms
			11	t_{W_RST} = 1 ms to 1.5 ms
3	V2SUC (2) / VEXTSUC (3)	R/W		V2/VEXT start-up control:
			0 (1)	Bits V2C/VEXTC set to 00 during power-up
			1	Bits V2C/VEXTC set to 11 during power-up
2:0	Reserved	R	-	

(1) Factory preset value.
(2) Non-X version only.
(3) X version only.

Reset Resources

A system reset is triggered by the following events:

- V_{V1} drops below the selected V1 undervoltage threshold defined by bits V1RTC (except in Sleep mode or Overtemp mode);
- Via Off mode after an MTPNV programming cycle is completed;
- Pin RSTN is pulled down externally;
- The watchdog overflows in Window mode;
- The watchdog is triggered too early in Window mode (before t_{TRIG_WD1});
- The watchdog overflows in Timeout mode with WDF set to 1 (watchdog failure pending);
- Reconfigure the watchdog control register when the chip is in Normal mode;
- The chip leaves Off mode;
- Local or CAN-bus wake-up in Sleep mode;
- Diagnostic wake-up in Sleep mode;
- The SBC leaves Overtemp mode;
- Illegal Sleep mode command received;
- Wake-up from Sleep mode due to a frame detect error.

Global Temperature Protection

The TPT1169 monitors chip temperature except for in Sleep or Off mode. When the temperature exceeds the protection activation threshold T_{J_OTP}, the chip switches to Overtemp mode, the CAN transceiver is disabled, V1 and V2 are off, and pin RSTN is pulled low. When the temperature drops below the overtemperature protection release threshold $Tt_{J\_OTP\_R}$, the chip switches to Reset mode and automatically switches to Reset mode in the following process.

Meanwhile, when the temperature exceeds the warning threshold $T_{J\_OTP\_WARN}$, the status bit OTWS is set, and an over-temperature warning event (OTW) is set if it is enabled (set OTWE to 1).

Power Supplies

Battery Voltage

The internal circuitry and state machine are supplied via pin BAT which is usually connected to the vehicle battery. The TPT1169 switches to Reset mode from Off mode when the pin BAT voltage exceeds the power-on detection threshold $V_{TH\_DET\_PON}$. Bit PO is set to 1 after the chip is powered up, indicating a power-on event. The TPT1169 switches to Off mode from any mode when the pin BAT voltage falls below the power-off detection threshold $V_{TH\_DET\_POFF}$. In 5-V version, voltage regulator V1 keeps active until V_{BAT} falls below 2 V, guaranteeing memory in the microcontroller supplied by V1 stays as long as possible (ram retention feature). This feature is not implemented in the 3.3-V version.

Voltage Regulator V1

The TPT1169 provides 2 kinds of V1 chip: 5 V and 3.3 V. V1 can supply up to 250-mA current. In the X version, the CAN transceiver is supplied via V1. The typical application is shown as Figure 5.

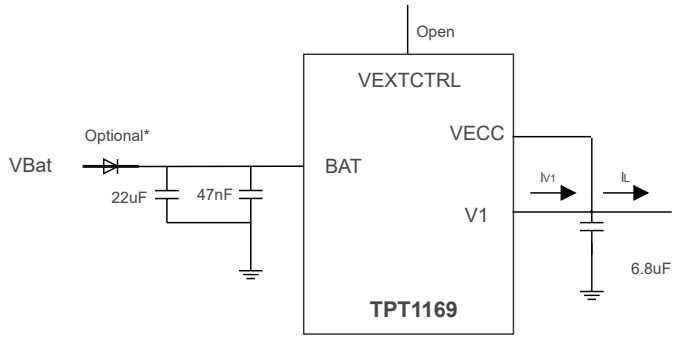


Figure 5. Typical Application without External PNP

The TPT1169 provides an external PNP transistor to enlarge the output current and protect the chip from overheating, as shown in Figure 6. The power is distributed between the chip (I_{V1}) and the PNP transistor (I_{PNP}).

When the output load reaches the PNP activation threshold, the PNP transistor starts to work by controlling the current on pin VEXCTRL $I_{TH\_ACT\_PNP}$. Bit PDC in the regulator control register (see Table 11) is used to distribute power dissipation between the chip and the PNP transistor.

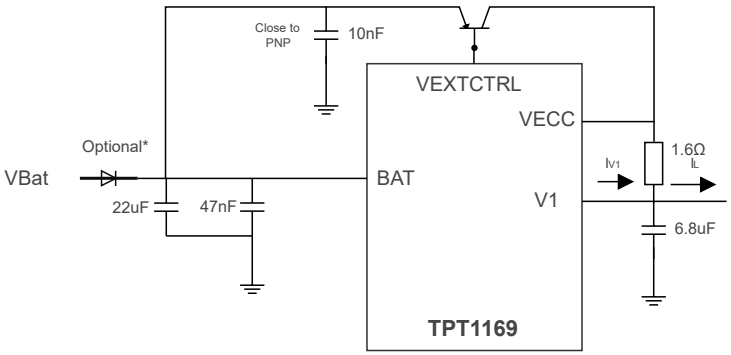


Figure 6. Typical Application with External PNP Transistor

A resistor between pin V1 and pin VECC can monitor the current and prevent shorting to GND. The output current of PNP doesn't increase if the voltage on the resistor reaches the PNP current limiting threshold $V_{TH\_ACT\_ILIM}$ by controlling the base current of PNP. Generally, the current amplification factor (β) of PNP between 50 and 500 can fit this application.

An undervoltage of V1 causes a system reset, and a cold start occurs after V1 resumes. The undervoltage threshold can be configured as 60%, 70%, 80%, or 90% of the nominal output via bits V1RTC in the regulator control register (see Table 11) in the 5-V version. For the 3.3-V version, the threshold is fixed to 90% regardless of register settings.

The undervoltage threshold of V1 is configured via bit V1RTSUC in the SBC configuration control register which is stored in non-volatile memory.

An undervoltage warning is triggered (bit V1U) when V1 drops below 90% of the nominal voltage, provided that V1 undervoltage detection is enabled, V1UE is set to 1, as shown in Table 30). This bit offers additional information for monitoring V1 status when V1 undervoltage is set to 60%, 70%, or 80%. In this application, the TPT1169 does not reset due to undervoltage, and bit V1S in the supply voltage status register (see Table 12) can indicate whether V1 is undervoltage in real time.

Voltage Regulator V2

In non-X version, pin 13 is the voltage regulator V2 output supplying up to 150-mA current.

The CAN transceiver is supplied via V2 internally, thus consuming parts current of V2. Shorting to battery or to negative voltage may cause permanent damage to V2, thus limiting V2 from supplying off-board components.

The status of V2 can be configured via bit V2C in the regulator control register (see Table 11). V2 must be on for successful CAN communication but not needed in CAN wake-up detection for both wake-up pattern and selective wake-up.

The default status of V2 at start-up is configured via V2SUC in the start-up control register stored in non-volatile memory, and the status of V2 can be read via bit V2S in the supply voltage status register (see Table 12).

Voltage Regulator VEXT

In X version, pin 13 is the voltage regulator VEXT output supplying up to 150-mA current.

The CAN transceiver is supplied via V1 internally, so the 150-mA supply current can be totally supplied to the output load. VEXT is designed to prevent shorting to battery, so it can supply off-board components considering potential short circuit risk.

The status of VEXT can be configured via bit VEXTC in the Regulator control register (see Table 11).

The default status of VEXT at start-up is configured via VEXTSUC in the start-up control register stored in non-volatile memory, and the status of VEXT can be read via bit VEXTS in the supply voltage status register (see Table 12).

Regulator Control Register

Table 11. Regulator Control Register 10h

Bit	Symbol	Access	Value	Description
7	Reserved	R	-	
6	PDC	R/W		Power distribution control:
			0	V1 threshold current for activating the external PNP transistor, load current rising; $I_{TH\_ACT\_PNP)}$ (higher value; see the Electrical Characteristics) V1 threshold current for deactivating the external PNP transistor, load current falling; $I_{TH\_DEACT\_PNP}$ (higher value; see the Electrical Characteristics)
			1	V1 threshold current for activating the external PNP transistor; load current rising; $I_{TH\_ACT\_PNP}$ (lower value; see the Electrical Characteristics) V1 threshold current for deactivating the external PNP transistor; load current falling; I_{TH_DEACT} (lower value; see the Electrical Characteristics)
5:4	Reserved	R	-	
3:2	V2C (1) VEXTC (2)	R/W		V2/VEXT configuration:
			00	V2/VEXT off in all modes
			01	V2/VEXT on in Normal mode
			10	V2/VEXT on in Normal, Standby, and Reset modes
			11	V2/VEXT on in Normal, Standby, Sleep, and Reset modes
1:0	V1RTC (3)	R/W		Set V1 reset threshold:
			00	Reset threshold set to 90 % of V1 nominal output voltage
			01	Reset threshold set to 80 % of V1 nominal output voltage
			10	Reset threshold set to 70 % of V1 nominal output voltage
			11	Reset threshold set to 60 % of V1 nominal output voltage

(1) Only in non-X version. Default value at start-up via bit V2SUC (see Table 10).
(2) Only in X version. Default value at start-up via bit VEXTSUC (see Table 10).
(3) Only in 5-V version. Default value at start-up via bits V1RTSUC (see Table 8); For 3.3-V version, the value is fixed to 00b (90%).

Supply Voltage Status Register

Table 12. Supply Voltage Status Register 1Bh

Bit	Symbol	Access	Value	Description
7:3	Reserved	R	-	
2:1	V2S (1) VEXTS (2)	R		V2/VEXT status:
			00 (3)	V2/VEXT voltage ok
			01	V2/VEXT output voltage below the undervoltage threshold
			10	V2/VEXT output voltage above the overvoltage threshold
			11	V2/VEXT disabled
0	V1S	R		V1 status:
			0 (3)	V1 output voltage above 90% undervoltage threshold
			1	V1 output voltage below 90% undervoltage threshold

(1) Only in non-X version.
(2) Only in X version.
(3) Default value at start-up.

LIMP Output

Pin LIMP is designed to achieve a 'limp home' function if some serious failures occur in ECU, such as overtemperature, watchdog failure, V1 undervoltage, or pin RSTN short-circuit. Pin LIMP is V_{BAT}-robust, active-low, and open-drain output. Also, this pin can be configured to active via bit LHC in the fail-safe control register (see Table 13).

Reset Counter

The TPT1169 has an internal counter to record the reset times. The counter is increased on every reset event occurrence. The application software must monitor and clear the counter in time to avoid unexpected LIMP active by expected reset event. The counter number is stored in bit RCC in the fail-safe control register (see Table 13).

Once the counter reaches 3 and another reset event occurs, the chip enters Reset mode, pin LIMP is active to low, bit LHC is set to 1, and bit RCC overflows to 0. All the actions indicate that the chip faces critical failure.

Bit LHC can also be set to 1 directly via an SPI command, and pin LIMP is driven low without countering overflow. This feature can be used to check the function and PCB assembly of LIMP.

The value of RCC can be configured to determine how many times can tolerate before LIMP is active. If RCC is set to 2, it means that after 2 reset events occur, the TPT1169 enters Reset mode, compared to 4 times within RCC default value 0.

Some events can cause direct LIMP activation, with bit LHC to 0 and without the RCC counter reaching overflow. The events are as below:

- Overtemperature has existed for longer than t_{D_LIMP};
- The TPT1169 stays in Reset mode longer than t_{D_LIMP}.

LIMP State Machine

The state machine of LIMP function is shown as Figure 7.

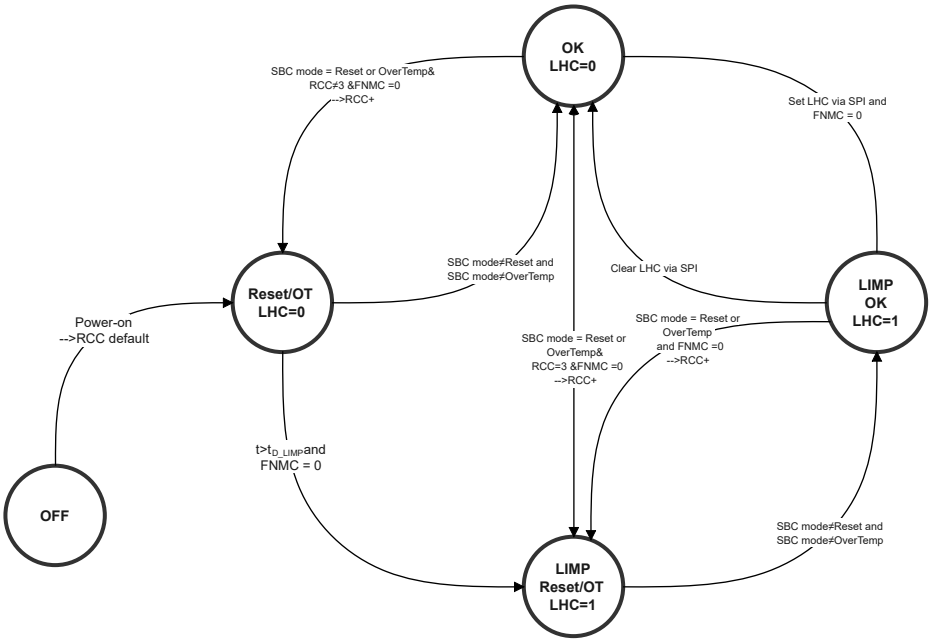


Figure 7. State Machine of LIMP Function

Since the TPT1169 switches from Sleep mode to Reset mode via wake-up event and V1 is powered on under this condition, RCC increases after every wake-up event. It is necessary to monitor and clear bit RCC after wake-up to avoid unexpected limp-home occurrence in the application software.

In Forced Normal mode, the limp-home function is disabled, bit LHC is fixed to 0, RCC stays unchanged, and pin LIMP is floating.

The pin LIMP circuit example is shown in Figure 8.

Table 13. Fail-safe Control Register 02h

Bit	Symbol	Access	Value	Description
7:3	Reserved			
2	LHC	R/W		LIMP home control:
			0	Pin LIMP is floating
			1	Pin LIMP is driven low
1:0	RCC	R/W		Reset counter control:
			XX	Incremented every time the SBC enters Reset mode while FNMC is set to 0; RCC overflows from 11 to 00; default at power-on is 00

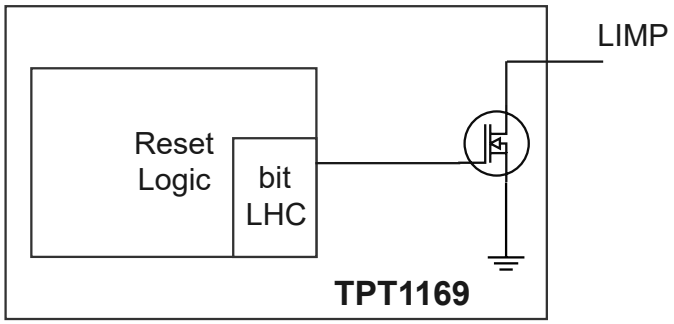


Figure 8. Pin LIMP Circuit Example

High-Speed CAN Transceiver

The high-speed CAN transceiver can support up to 8-Mbps CAN communication within the classic CAN or CANFD network. The transceiver is ISO 11898-2:2024 compliant. The power supply of the CAN transceiver depends on the chip version: the X version is supplied via V1, and the non-X version is supplied via V2.

The high-speed CAN transceiver also supports the features of 'autonomous CAN biasing' defined in ISO 11898-2:2024. In CAN Offline mode, the transceiver biases to 2.5 V while the signal exists on the bus, entering CAN Offline Bias mode, and to GND while no signal on the bus for t exceeds $t_{TO\_SILENCE}$. CANH and L are biased to 2.5 V in CAN Active mode or CAN Listen-only mode (set CMC to 01/10/11, see Table 14). The state diagram is shown as Figure 9.

CAN Operating Modes

The high-speed CAN transceiver has four operating modes when V_{BAT} exceeds V_{UVD_CAN}: CAN Active, CAN Offline, CAN Offline Bias, and Listen-only, depending on the configuration of bit CMC in the CAN control register and the TPT1169 operating mode. If V_{BAT} is below V_{UVD_CAN}, the CAN transceiver is in Off mode and is unable to switch to any other modes above.

When the TPT1169 is in Normal mode, the CAN transceiver operating mode can be configured as Active, Listen-only, or Offline modes via bit CMC. When the TPT1169 is in Standby or Sleep mode, the transceiver is forced to Offline or Offline Bias mode depending on bus activity.

CAN Active Mode

In CAN Active mode, the transceiver transmits data from the microcontroller on pin TXD to the CAN bus, and receives data from the CAN bus to the microcontroller on pin RXD.

This mode is configured by setting bit CMC to 01 or 10. The undervoltage detection of the CAN transceiver supply is enabled when CMC is set to 01, and disabled when CMC to 10. In both configurations, if pin V1 drops below the undervoltage protection active threshold (depending on the bit V1RTC setting), the transceiver is switched to Offline or Offline Bias mode.

The transceiver stays in Active mode if CMC is 01 with pin V1 voltage above V_{UVD_CAN} or 10 with pin V1 voltage above the undervoltage protection active threshold and the system operating mode is Normal mode. For the X version, the transceiver is supplied via V1, and for the non-X version supplied via V2.

If pin TXD is held low (e.g. by a short-circuit to GND) when CAN Active mode is set via bit CMC, the transceiver does not switch to CAN Active mode but switches to or remains in CAN Listen-only mode until pin TXD turns high. This feature seeks to prevent a long-time dominant state from transmitting on the CAN bus.

The status of the CAN transceiver can be read from bit CTS in the transceiver status register (see Table 15).

CAN Listen-Only Mode

The transceiver in CAN Listen-only mode can only receive data from the CAN bus, but is unable to transmit data to the CAN bus. This feature is usually used to monitor the bus for CAN network debug tools.

When the TPT1169 is in Normal mode and bit CMC is set to 11, the transceiver switches to Listen-only mode. Pins CANH and CANL are biased to 2.5 V in this mode. The chip stays in Listen-only mode under two conditions: pin TXD is held low, and voltage regulator V1 falls below 90% undervoltage threshold even when CMC is set to 01.

CAN Offline and Offline Bias Mode

The transceiver in CAN Offline and Offline Bias modes monitors CAN bus wake-up event if CWE is enabled (see Table 31). Pins CANH and CANL are biased to GND in CAN Offline mode, and to 2.5 V in Offline Bias mode.

The transition between CAN Offline and Offline Bias mode depends on bus activity. When the TPT1169 is in Standby or Sleep mode with no signal on the bus for t> $t_{TO\_SILENCE}$, the transceiver switches to CAN Offline mode. When the signal on the CAN bus is detected, the transceiver switches to CAN Offline bias mode and stays unchanged until no signal is on the bus for t > $t_{TO\_SILENCE}$.

The transceiver switches to CAN Offline or Offline bias mode under the following conditions:

- The operating mode is set to Standby or Sleep mode;
- The chip is in Normal mode, but CMC is set to 00;
- The chip is in Normal mode and CMC is set to 01 or 10, but VCAN is below 90%.

CAN Off Mode

The transceiver in CAN Off mode is totally off with pins CANH and CANL floating to prevent current flowing from the bus to the chip. When the TPT1169 switches to Off mode or Overtemp mode, or when V_{BAT} is below V_{UVD_CAN}, the transceiver enters CAN Off mode.

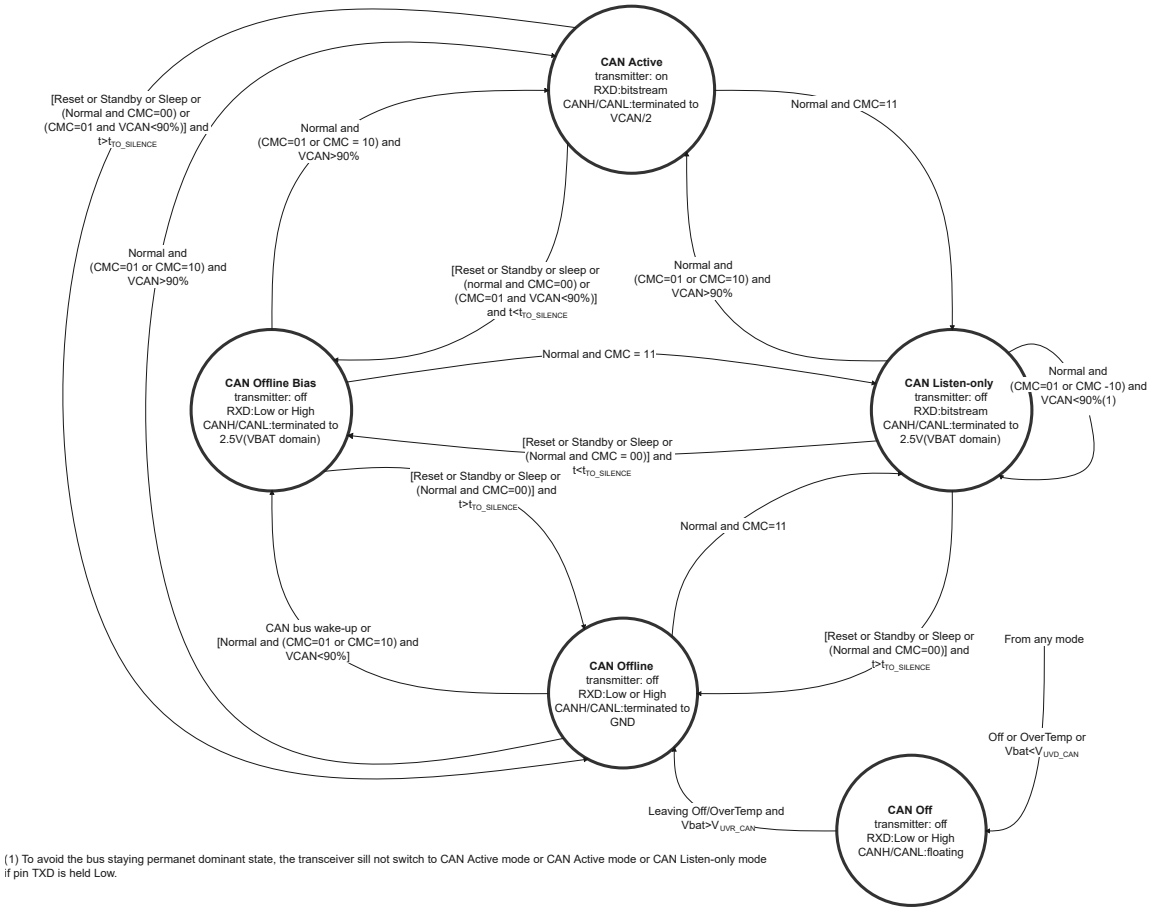


Figure 9. CAN Transceiver State Diagram

CAN Standard Wake-up

The TPT1169 monitors a standard wake-up pattern, as defined in ISO 11898-2: 2024, under the following conditions:

- The transceiver is in CAN Offline mode;
- CAN bus wake-up event is enabled (set CWE to 1);
- Partial networking is disabled (set CPNC or PNCOK to 0).

A standard wake-up pattern contains a dominant-to-recessive-to-dominant toggle and each state lasts at least $t_{WAKE\_BUS\_REC}$ and $t_{WAKE\_BUS\_DOM}$. The total pattern must be within a wake-up time-out time t_{WAKE_TO}. An analog filter is on the detection path to prevent any spurs or EMI interference transient.

Pin RXD is pulled low to indicate a valid CAN bus wake-up event in Standby mode. In Sleep mode, voltage regulator V1 is enabled after a wake-up pattern. Bit CW (see Table 27) is set after the CAN bus wake-up. The wake-up pattern timing is shown as Figure 10.

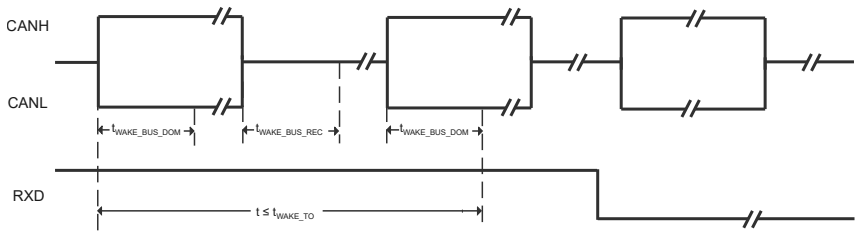


Figure 10. Wake-up Pattern Timing

CAN Control Register

Table 14. CAN Control Register 20h

Bit	Symbol	Access	Value	Description
7	Reserved	R	-	
6	CFDC (1)	R/W		CAN FD control:
			0	CAN FD tolerance disabled
			1	CAN FD tolerance enabled
5	PNCOK (1)	R/W		CAN partial networking configuration OK:
			0	Partial networking register configuration invalid (wake-up via standard wake-up pattern only)
			1	Partial networking registers configured successfully
4	CPNC (1)	R/W		CAN partial networking control:
			0	Disable CAN selective wake-up
			1	Enable CAN selective wake-up
3:2	Reserved	R	-	
1:0	CMC	R/W		CAN transceiver operating mode selection (available when the TPT1169 is in Normal mode; MC = 111):
			00	Offline mode
			01	Active mode; see CAN Active Mode
			10	Active mode; see CAN Active Mode
			11	Listen-only mode

(1) Version with partial networking function only.

Table 15. Transceiver Status Register 22h

Bit	Symbol	Access	Value	Description
7	CTS	R		CAN transceiver status:
			0	CAN transceiver not in Active mode
			1	CAN transceiver in Active mode

Bit	Symbol	Access	Value	Description
6	CPNERR (1)	R		CAN partial networking error:
			0	No CAN partial networking error detected (PNFDE = 0 and PNCOK = 1)
			1	CAN partial networking error detected (PNFDE = 1 or PNCOK = 0; wake-up via standard wake-up pattern only)
5	CPNS (1)	R		CAN partial networking status:
			0	CAN partial networking configuration error detected (PNCOK = 0)
			1	CAN partial networking configuration ok (PNCOK = 1)
4	COSCS (1)	R		CAN oscillator status:
			0	CAN partial networking oscillator not running at target frequency
			1	CAN partial networking oscillator running at target frequency
3	CBSS	R		CAN bus silence status:
			0	CAN bus active (communication detected on bus)
			1	CAN bus inactive (for t > $t_{TO\_SILENCE}$)
2	Reserved	R	-	
1	VCS (2)	R		VCAN status:
			0	CAN supply voltage is above the undervoltage threshold, V_{UVD_CAN}
			1	CAN supply voltage is below the undervoltage threshold, V_{UVD_CAN}
0	CFS	R		CAN failure status:
			0	No TXD dominant time-out event detected
			1	CAN transmitter disabled due to a TXD dominant time-out event

(1) Version with partial networking function only.
(2) Only active when CMC = 01.

CAN Partial Networking

The TPT1169 is compatible with ISO 11898-2 and ISO 11898-5, and supports partial networking (PN) with a selective wake-up function according to ISO 11898-6. This feature is disabled after power-on and must be activated before use. Nodes only respond to specified wake-up frames (WUF), while other nodes remain asleep to save power in the CAN network.

The simplified guide to configure partial networking features is a configure frame form including data rate, frame ID and ID mask, data length, data mask, and frame type; Enable partial networking (set bit CPNC to 1 and PNCOK to 1) and CAN bus wake-up (set CWE to 1). If all relative registers are configured correctly, bits CPNC, PNCOK, and CWE are set to 1, and

partial networking is enabled. Otherwise, partial networking is disabled, and only the wake-up pattern (WUP) can trigger a CAN bus wake-up event.

Wake-up Frame

A valid wake-up frame is defined in ISO 11898-1:2015, consisting of a Start of Frame (SOF), an identifier field (ID), a Data Length Code, a data field, and a Cyclic Redundancy Check (CRC) code.

The wake-up frame bit rate is defined in the data rate register. The valid rates are 50 kbps, 125 kbps, 250 kbps, 500 kbps, and 1 Mbps. The default rate is 500 kbps.

The type of wake-up frame can be standard format (11-bit ID) or extended format (29-bit ID) via bit IDE in the frame control register.

The WUF' identifier is configured in the ID register, and correspondence between the identifier and register bit changes in standard and extended format. In standard format, only registers 0x2A and 0x29 work; In extended format, registers 0x27 to 0x2A work.

The ID mask register can be used to allow a series of identifiers to be recognized as valid frames. Bit value "1" means "don't care about the corresponding ID bit". The example shows how ID mask registers operate as Figure 11. The identifier configuration is 0x490 via ID registers 0x29 and 0x2A. The two LSBs (least significant bit) of ID mask register 0x2D are set to "1". That means the frame IDs: 0x490, 0x491, 0x492, and 0x493 are valid wake-up frames to wake up the TPT1169.

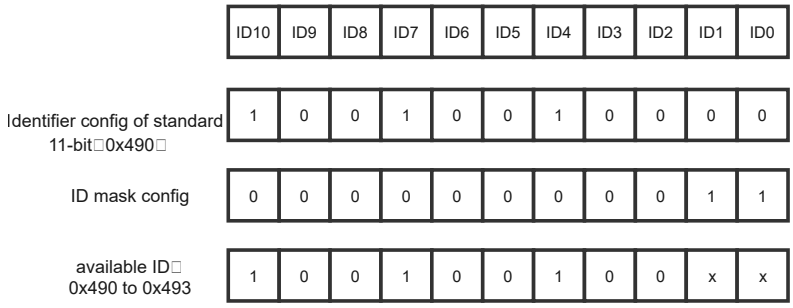


Figure 11. The Function of ID Mask Register

Whether the data field is evaluated is determined by bit PNDM in the frame control register. If PNDM is 0, only the identifier field is evaluated and the data field is ignored. The TPT1169 is woken up when the identifier field of the frame matches ID register configuration, and no CRC error occurs. If PNDM is 1, both the identifier and data field are evaluated. The TPT1169 is woken up when the identifier field of the frame matches the ID register configuration, and the data field matches the data length and data mask configuration, and no CRC error occurs.

Bits DLC in the frame control register determines the expected number of bytes (up to 8 bytes) in the data field as a valid wake-up frame. If a frame contains a valid identifier but the data length doesn't match the DLC value, the device cannot be woken up. If one or more bytes are expected, DLC configuration must match the actual number of bytes data fields, at least one bit of data field in the wake-up frame must be set to 1, and the corresponding bit in eight data mask registers must be set to 1. If the value of all data mask registers is 0, that means no frame can wake up the TPT1169 in partial networking mode.

Here is an example showing how the data mask register works as Figure 12. A frame with one-byte data field and data 0x01, 0x04, 0x05 are all valid wake-up frames while the identifier field matches ID and ID mask register while DLC is 1, and DM7 is 0x05.

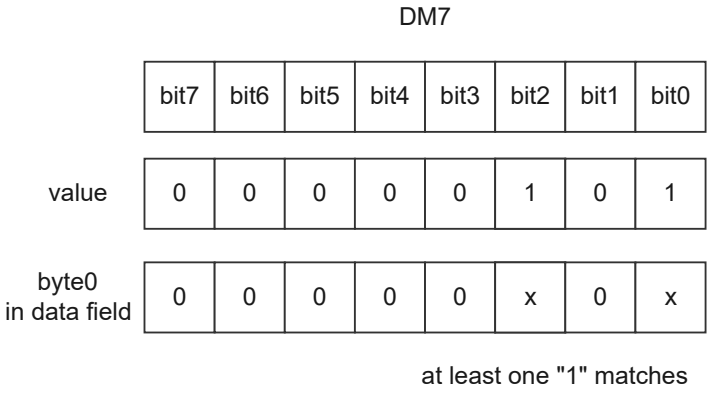


Figure 12. The Function of Data Mask Register

The sequence of the data mask register is shown in Figure 13. The data mask register 7 always masks the most significant byte of the data field.

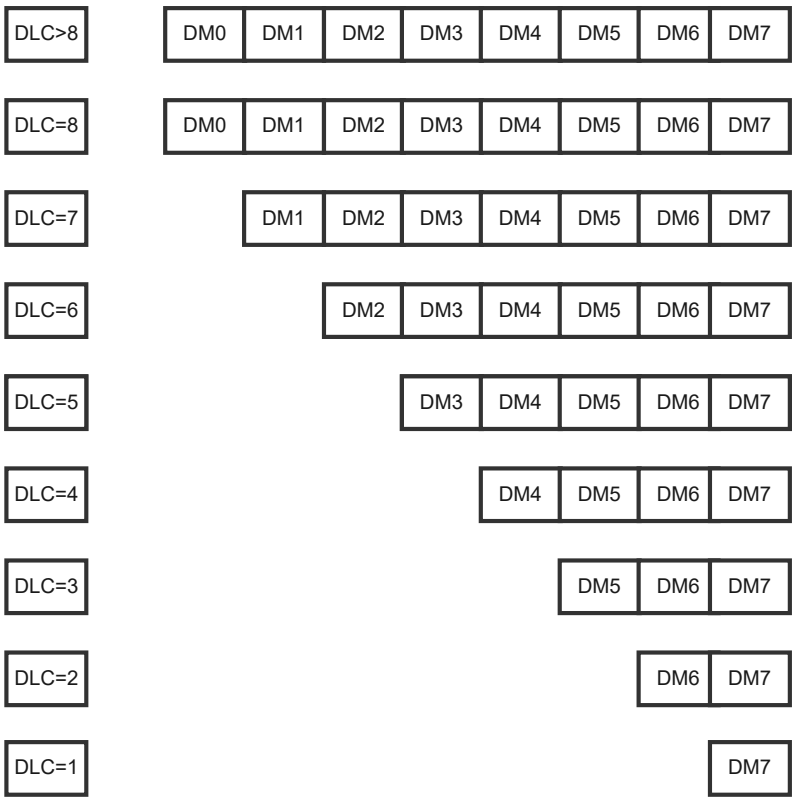


Figure 13. The Sequence of Data Mask Register

Only the data frame is valid WUF. The remote frame is not valid, so is unable to wake up the TPT1169.

Any SPI write command to partial networking configuration registers clears bit PNCOK in the CAN control register (0x20), thus leading to a wake-up pattern instead of the wake-up frame. It is recommended that the CAN control register should be written at the end of the register configuration procedure.

CAN FD Frames

CAN FD frame is not the available frame and causes SBC wake-up by diagnostic wake-up. Then "CAN FD tolerance" feature is useful if the CAN FD frame exists in the CAN network. Once CAN FD tolerance is enabled and CFDC is 1, the TPT1169Q is passive to the CAN FD frame and cannot be woken up by the CAN FD frame. If bit CFDC is 0 and the CAN FD frame is running in the CAN bus network, the TPT1169Q is woken up by the PNFDE event.

If the wake-up frame has some error, such as a stuff error, or CRC error in front of the ACK field, the internal error counter of the chip increases. Any correct received frame decreases the error counter until 0. Once the counter reaches the threshold (default 32), a PNFDE event occurs and if the TPT1169Q is in Sleep mode, it switches to standby mode by diagnostic wake-up.

CAN Partial Networking Configuration Registers

A series of registers are dedicated to configuring the CAN partial networking.

Data Rate Register

Table 16. Data Rate Register 26h

Bit	Symbol	Access	Value	Description
7:3	Reserved	R	-	
2:0	CDR	R/W		CAN data rate selection:
			000	50 kbit/s
			001	100 kbit/s
			010	125 kbit/s
			011	250 kbit/s
			100	Reserved (intended for future use; currently selects 500 kbit/s)
			101	500 kbit/s
			110	Reserved (intended for future use; currently selects 500 kbit/s)
			111	1000 kbit/s

ID Registers

Table 17. ID Register 27h to 2Ah

Address	Bit	Symbol	Access	Value	Description
27h	7:0	07:00	R/W	-	Bits ID07 to ID00 of the extended frame format
28h	7:0	15:08	R/W	-	Bits ID15 to ID08 of the extended frame format

Address	Bit	Symbol	Access	Value	Description
29h	7:2	23:18	R/W	-	Bits ID23 to ID18 of the extended frame format bits ID05 to ID00 of the standard frame format
	1:0	17:16	R/W	-	Bits ID17 to ID16 of the extended frame format
2Ah	7:5	Reserved	R	-	
	4:0	28:24	R/W	-	Bits ID28 to ID24 of the extended frame format; Bits ID10 to ID06 of the standard frame format

ID Mask Registers

Table 18. ID Mask Register 2Bh to 2Eh

Address	Bit	Symbol	Access	Value	Description
2Bh	7:0	M07:M00	R/W	-	Mask bits ID07 to ID00 of the extended frame format
2Ch	7:0	M15:M08	R/W	-	Mask bits ID15 to ID08 of the extended frame format
2Dh	7:2	M23:M18	R/W	-	Mask bits ID23 to ID18 of the extended frame format mask bits ID05 to ID00 of the standard frame format
	1:0	M17:M16	R/W	-	Mask bits ID17 to ID16 of the extended frame format
2Eh	7:5	Reserved	R	-	
	4:0	M28:M24	R/W	-	Mask bits ID28 to ID24 of the extended frame format; Mask bits ID10 to ID06 of the standard frame format

Frame Control Register

Table 19. Frame Control Register 2Fh

Bit	Symbol	Access	Value	Description
7	IDE	R/W	-	Identifier format:
			0	Standard frame format (11 bits)
			1	Extended frame format (29 bits)
6	PNDM	R/W	-	Partial networking data mask:
			0	Data length code and data field are "don't care" for wake-up

Bit	Symbol	Access	Value	Description
			1	Data length code and data field are evaluated at wake-up
5:4	Reserved	R	-	
3:0	DLC	R/W		Number of data bytes expected in a CAN frame:
			0000	0
			0001	1
			0010	2
			0011	3
			0100	4
			0101	5
			0110	6
			0111	7
			1000	8
			1001 to 1111	Tolerated, 8 bytes expected

Data Mask Registers

Table 20. Data Mask Registers 68h to 6Fh

Address	Bit	Symbol	Access	Value	Description
68h	7:0	DM0	R/W	-	Data mask 0 configuration
69h	7:0	DM1	R/W	-	Data mask 1 configuration
6Ah	7:0	DM2	R/W	-	Data mask 2 configuration
6Bh	7:0	DM3	R/W	-	Data mask 3 configuration
6Ch	7:0	DM4	R/W	-	Data mask 4 configuration
6Dh	7:0	DM5	R/W	-	Data mask 5 configuration
6Eh	7:0	DM6	R/W	-	Data mask 6 configuration
6Fh	7:0	DM7	R/W	-	Data mask 7 configuration

CAN Fail-Safe Features

TXD Dominant Time-out

The device features the TXD dominant time-out detection function. This function prevents a permanent low on pin TXD, and therefore the CAN bus is driven into permanent dominant, which causes the CAN bus network communication to be blocked. If the TXD remains low for t > t_{TXD_DTO}, the transmitter is disabled until the fault flag is cleared.

Once TXD dominant time-out occurs, bit CFS in the transceiver status register is set to 1 (see Table 15) and bit CTS is set to 0. A CAN failure event is triggered and can be read via bit CF in the transceiver event status register (see Table 25) if bit CFE is enabled.

Pull-up on Pin TXD

Pin TXD has an internal pull-up to V1 to ensure a defined recessive state in case the pin is left floating.

VCAN Undervoltage Event

If an undervoltage event occurs on the CAN transceiver supply VCAN, a CAN failure event is triggered and can be read via bit CF in the transceiver event status register (see Table 25) if bit CFE is enabled. Bit VCS in the transceiver status register is set to 1 additionally.

Loss of Power on V_{BAT}

The chip switches to CAN Off mode, and pins CANH and CANL are passive to the CAN bus when the voltage on pin BAT is lost, thus avoiding any effect on ongoing communication.

Wake-up and Interrupt Event

Pin WAKE

Local wake-up is enabled by setting bits in WPRE and WPFE in the pin WAKE event capture enable register (see Table 32). A local wake-up event is triggered via a rising or falling edge on pin WAKE, depending on the configuration. It is recommended to connect pin WAKE directly to GND for EMI performance improvement if this feature is unused.

The voltage level status can be read via bit WPVS in the pin WAKE status register (see Table 21) when the chip is in Normal mode.

Pin WAKE Status Register

Table 21. Pin WAKE Status Register 4Bh

Bit	Symbol	Access	Value	Description
7:2	Reserved	R	-	
1	WPVS	R		Pin WAKE status:
			0	Voltage on pin WAKE below the switching threshold ($V_{TH\_WAKE\_F}$)
			1	Voltage on pin WAKE above the switching threshold ($V_{TH\_WAKE\_R}$)
0	Reserved	R	-	

Wake-up Events and Diagnostic Events

Both regular wake-up events and diagnostic events can be captured by the TPT1169, providing chip status and events for the microcontroller to access. This information is stored in the event status register (see Table 25, Table 26, and Table 27) and causes a falling edge on pin RXD if enabled.

The difference between regular wake-up events and diagnostic events is shown as Table 22 and Table 23.

Table 22. Regular Wake-up Events

Symbol	Event	Status after Power-on	Description
CW	CAN wake-up	Disable	A Wake-up pattern or Wake-up frame detected on CAN bus

Symbol	Event	Status after Power-on	Description
WPR	Pin WAKE rising	Disable	A rising edge detected on pin WAKE
WPF	Pin WAKE falling	Disable	A rising edge detected on pin WAKE

Table 23. Diagnostic Events

Symbol	Event	Status after Power-on	Description
PO	Power-on	Always enabled	See the system event status register (Table 25)
OTW	Overtemperature warning	Disabled	
SPIF	SPI failure	Disabled	
WDF	Watchdog failure	Always enabled	
V2O (1)	V2 overvoltage	Disabled	See the supply event status register (Table 26)
VEXTO (2)	VEXT overvoltage	Disabled	
V2U (1)	V2 undervoltage	Disabled	
VEXTU (2)	VEXT undervoltage	Disabled	
V1U	V1 undervoltage	Disabled	
PNFDE (3)	PN frame detection error	Always enabled	See the transceiver event status register (Table 27)
CBS	CAN-bus silence	Disabled	
CF	CAN failure	Disabled	

(1) Non-X version only.
(2) X version only.
(3) Version with partial networking only.

All the events must be enabled via the associated event capture register before they take effect except PO, PNFDE, and WDF which are always enabled.

When an event occurs and the associated event capture register is enabled, the relevant event bit is set to 1. If the CAN transceiver is in CAN Offline mode and V1 is active (in Normal mode or Standby mode), pin RXD is pulled low, indicating interruption to the microcontroller. If the TPT1169 is in Sleep mode, the chip switches to Reset mode and automatically to Standby mode.

A global event status register, 0x60, can be used to accelerate software identification of which kind of event (system, supplies, CAN transceiver, or pin WAKE) occurs.

Once the event occurs, the status bit is set to 1. The method to clear the event is writing "1" to relevant bits (writing 0 takes no effect). A simple way to clear all the existing events is by writing "ff" to relevant registers so that all the bits are clear.

Event Delay

If some wake-up or diagnostic events occur very frequently (e.g. fast-voltage toggle on pin WAKE while local wake-up is enabled), the RXD is driven low within shot interval repeatedly. This causes fatal risks to the software in the microcontroller. The TPT1169 has a limitation to prevent such extreme conditions.

Once the event is cleared, pin RXD is driven high, and an internal counter starts running. During the counter timing, any new regular wake-up or diagnostic event is unable to trigger a new event or a falling edge on pin RXD until the counter reaches t_{D_EVENT}. This feature prevents the microcontroller from frequently responding to the interruption triggered by pin RXD.

The counter stops immediately when pin RSTN is pulled low.

Sleep Mode Protection

All event status restored in registers 0x61, 0x62, 0x63, and 0x64 must be clear and at least one regular wake-up source (CAN wake-up or local wake-up) must be enabled before the TPT1169 switches to Sleep mode to avoid deadlock. Otherwise, the TPT1169 switches to Reset mode instead of Sleep mode, and a reset resource "illegal Sleep mode command received" is generated.

Sleep mode can be disabled permanently by setting bit SLPC in the SBC configuration register to 1 (see Table 8). An SPI command of Sleep mode cannot switch to Sleep mode but triggers an SPI failure event after SLPC is set.

Event Status Registers

Table 24. Global Event Status Register 60h

Bit	Symbol	Access	Value	Description
7:4	Reserved	R	-	
3	WPE	R		Pin WAKE event:
			0	No pending pin WAKE event
			1	Pin WAKE event pending at address 64h
2	TRXE	R		Transceiver event:
			0	No pending transceiver event
			1	Transceiver event pending at address 63h
1	SUPE	R		Supply event:
			0	No pending supply event
			1	Supply event pending at address 62h
0	SYSE	R		System event:
			0	No pending system event
			1	System event pending at address 61h

Table 25. System Event Status Register 61h

Bit	Symbol	Access	Value	Description
7:5	Reserved	R	- w	
4	PO	R/W		Power-on:
			0	No recent battery power-on
			1	The TPT1169 has left Off mode after battery power-on
3	Reserved	R	-	
2	OTW	R/W		Overtemperature warning:
			0	Overtemperature not detected
			1	The global chip temperature has exceeded the overtemperature warning threshold, $T_{J\_OTP\_WARN}$ (not in Sleep mode)

Bit	Symbol	Access	Value	Description
1	SPIF	R/W		SPI failure:
			0	No SPI failure detected
			1	SPI clock count error (only 16-, 24- and 32-bit commands are valid), illegal WMC, NWP or MC code or attempted write access to locked register (not in Sleep mode)
0	WDF	R/W		Watchdog failure:
			0	No watchdog failure event captured
			1	Watchdog overflow in Window or Timeout mode or watchdog triggered too early in Window mode; a system reset is triggered immediately in response to a watchdog failure in Window mode; when the watchdog overflows in Timeout mode, a system reset is only performed if a WDF is already pending (WDF = 1)

Table 26. Supply Event Status Register 62h

Bit	Symbol	Access	Value	Description
7:3	Reserved	R	-	
2	V2O (1) / VEXTO (2)	R/W		V2/VEXT overvoltage:
			0	No V2/VEXT overvoltage event captured
			1	V2/VEXT overvoltage event captured
1	V2U (1) / VEXTU (2)	R/W		V2/VEXT undervoltage:
			0	No V2/VEXT undervoltage event captured
			1	V2/VEXT undervoltage event captured
0	V1U	R/W		V1 undervoltage:
			0	No V1 undervoltage event captured
			1	Voltage on V1 has dropped below the 90 % undervoltage threshold while V1 is active (event is not captured in Sleep mode because V1 is off); V1U event capture is independent of the setting of bits V1RTC

(1) Non-X version only.
(2) X version only.

Table 27. Transceiver Event Status Register 63h

Bit	Symbol	Access	Value	Description
7:6	Reserved	R	-	

Bit	Symbol	Access	Value	Description
5	PNFDE	R/W		Partial networking frame detection error:
			0	No partial networking frame detection error detected
			1	Partial networking frame detection error detected
4	CBS	R/W		CAN bus status:
			0	CAN bus active
			1	No activity on the CAN bus for $t_{TO\_SILENCE}$(detected only when CBSE = 1 with the bus active)
3:2	Reserved	R	-	
1	CF	R/W		CAN failure:
			0	No CAN failure detected
			1	(CMC = 01 & CAN transceiver deactivated due to VCAN undervoltage) OR dominant clamped TXD (not in Sleep mode)
0	CW	R/W		CAN wake-up:
			0	No CAN wake-up event detected
			1	CAN wake-up event detected while the transceiver is in CAN Offline Mode

Table 28. Pin WAKE Event Status Register 64h

Bit	Symbol	Access	Value	Description
7:2	Reserved	R	-	
1	WPR	R/W		WAKE pin rising edge:
			0	No rising edge detected on WAKE pin
			1	Rising edge detected on WAKE pin
0	WPF	R/W		WAKE pin falling edge:
			0	No falling edge detected on WAKE pin
			1	Falling edge detected on WAKE pin

Event Capture Enable Registers

Table 29. System Event Capture Enable Register 04h

Bit	Symbol	Access	Value	Description
7:3	Reserved	R	-	
2	OTWE	R/W		Overtemperature warning enable:
			0	Overtemperature warning disabled
			1	Overtemperature warning enabled

Bit	Symbol	Access	Value	Description
1	SPIFE	R/W		SPI failure enable:
			0	SPI failure detection disabled
			1	SPI failure detection enabled
0	Reserved	R	-	

Table 30. Supply Event Capture Enable Register 1Ch

Bit	Symbol	Access	Value	Description
7:3	Reserved	R	-	
2	V2OE (1) / VEXTOE (2)	R/W		V2/VEXT overvoltage enable:
			0	V2/VEXT overvoltage detection disabled
			1	V2/VEXT overvoltage detection enabled
1	V2UE (1) / VEXTUE (2)	R/W		V2/VEXT undervoltage enable:
			0	V2/VEXT undervoltage detection disabled
			1	V2/VEXT undervoltage detection enabled
0	V1UE	R/W		V1 undervoltage enable:
			0	V1 undervoltage detection disabled
			1	V1 undervoltage detection enabled

(1) Non-X version only.
(2) X version only.

Table 31. Transceiver Event Capture Enable Register 23h

Bit	Symbol	Access	Value	Description
7:5	Reserved	R	-	
4	CBSE	R/W		CAN bus silence enable:
			0	CAN bus silence detection disabled
			1	CAN bus silence detection enabled
3:2	Reserved	R	-	
1	CFE	R/W		CAN failure enable:
			0	CAN failure detection disabled
			1	CAN failure detection enabled
0	CWE	R/W		CAN wake-up enable:
			0	CAN wake-up detection disabled
			1	CAN wake-up detection enabled

Table 32. Pin WAKE Event Capture Enable Register 4Ch

Bit	Symbol	Access	Value	Description
7:2	Reserved	R	-	
1	WPRE	R/W		Pin WAKE rising-edge enable:
			0	Rising-edge detection on pin WAKE disabled
			1	Rising-edge detection on pin WAKE enabled
0	WPFE	R/W		Pin WAKE falling-edge enable:
			0	Falling-edge detection on pin WAKE disabled
			1	Falling-edge detection on pin WAKE enabled

Non-Volatile SBC Configuration

Registers related to start-up configuration are stored in Multiple Time Programmable Non-Volatile (MTPNV) memory cells, allowing re-programming for the TPT1169. The MTPNV memory located in registers 73h and 74h.

Program MTPNV Cells

The TPT1169 is in Forced Normal mode after manufacturing with default MTPNV configuration. MTPNV memory can only be configured when bit FNMS is 1 and NVMPS is 1 (means that MTPNV is ready to be programmed).

The flow to program MTPNV is as follows: first writing expected values to registers 73h and 74h, second writing correct CRC value to the MTPNV CRC control register (see MTPNV CRC Control Register). Once the CRC value is validated, the programming starts, and MTPNV memory is rewritten. System reset is triggered to indicate a successful reprogramming. If the CRC value is incorrect, the reprogramming is aborted. After reprogramming, the non-volatile memory is protected from another overwriting.

The MTPNV status register contains three parts: bit NVMPS indicates whether the MTPNV memory can be programmed; bit MTPNC indicated that the counter that the MTPNV memory has be written; and bit ECCS indicates that a single bit error in MTPNV memory has been detected and corrected by internal CRC check mechanism. The counter increases on every programming (also increase when return to factory mode) and does not overflow. Notice that the maximum value of the counter is 11111b, after the counter reaches the maximum value the MTPNV can still be programmed. The maximum value of programming time is 1000.

MTPNV Status Register

Table 33. MTPNV Status Register (Address 70h)

Bit	Symbol	Access	Value	Description
7:2	WRCNTS	R		Write counter status:
			xxxxxx	Contains the number of times the MTPNV cells are reprogrammed
1	ECCS	R		Error correction code status:
			0	No bit failure detected in non-volatile memory

Bit	Symbol	Access	Value	Description
			1	Bit failure detected and corrected in non-volatile memory
0	NVMPS	R		Non-volatile memory programming status:
			0	MTPNV memory cannot be overwritten
			1 (1)	MTPNV memory is ready to be reprogrammed

(1) Factory preset value.

MTPNV CRC Control Register

The CRC value is calculated by the registers 73h and 74h and stored in bits CRCC in the MTPNV CRC control register.

Bit	Symbol	Access	Value	Description
7:0	CRCC	R/W		Cyclic redundancy check control:
			-	CRC control data

The CRC algorithm is calculated with the generator polynomial: $X^8+ X^5 + X^3 + X^2 + X + 1$, and the result must be bitwise inverted shown as Figure 14.

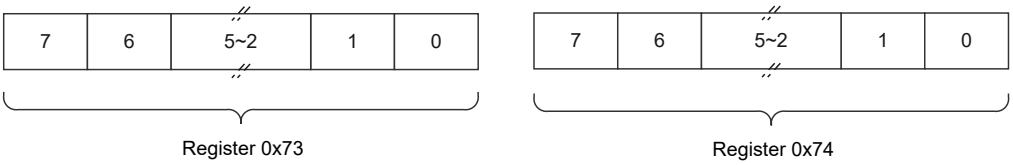


Figure 14. Data Sequence of CRC Calculation

These parameters can be used to calculate the CRC value as Table 34.

Table 34. Parameters for CRC Calculation

Parameter	Value
CRC Result Width	8 bits
Polynomial	0x2F
Initial Value	0xFF
Input Data Reverse	No
Result Data Reverse	No
XOR Value	0xFF

Here is the coding example for CRC calculation:

```
uint8_t data = 0;
uint8_t crc = 0xFF;
uint8_t Data[2] = { Reg73h, Reg74h };
for (int i = 0; i < 2; i++)
{
   data = Data[i] ^ crc;
   for (int j = 0; j < 8; j++)
   {
      if (data >= 128)
      {
         data <<= 1;
         data ^= 0x2F;
      }
      else
         data <<= 1;
   }
   crc = data;
}
crc ^= 0xFF;
return crc;
```

Restoring Factory Preset Values

Factory preset values are restored if the following conditions are met for at least t_{D_MTPNV} during start-up:

- Pin RSTN is pulled low;
- Pin CANH is pulled to V_{BAT};
- Pin CANL is pulled to GND.

After the factory preset values are restored, a system reset is triggered and then the chip switches to Forced Normal mode. Pin RXD is pulled low since the CAN bus is in dominant state. Bits WRCNTS also increase by one after factory preset values are restored. Bit PO in the system event status register is set to 1.

Device Identification

The device identification information is stored in the register 7Eh to distinguish different chip versions.

Table 35. Identification Register 7Eh

Bit	Symbol	Access	Value	Description
7:0	IDS [7:0]	R		Identification status:
			CFh	TPT11695Q-DFUR-S
			C9h	TPT11693Q-DFUR-S
			EFh	TPT11695FQ-DFUR

Bit	Symbol	Access	Value	Description
			E9h	TPT11693FQ-DFUR-S
			CEh	TPT11695XQ-DFUR-S
			EEh	TPT11695XFQ -DFUR-S

Register Locking

All the registers can be prevented from unexpected access via SPI commands by enabling lock control registers.

Lock Control Register

Table 36. Lock Control Register 0Ah

Bit	Symbol	Access	Value	Description
7	Reserved	R	-	
6	LK6C	R/W		Lock control 6: address area 68h to 6Fh - data mask
			0	SPI write access enabled
			1	SPI write access disabled
5	LK5C	R/W		Lock control 5: address area 50h to 5Fh - unused register range
			0	SPI write access enabled
			1	SPI write access disabled
4	LK4C	R/W		Lock control 4: address area 40h to 4Fh - pin WAKE control
			0	SPI write access enabled
			1	SPI write access disabled
3	LK3C	R/W		Lock control 3: address area 30h to 3Fh - unused register range
			0	SPI write access enabled
			1	SPI write access disabled
2	LK2C	R/W		Lock control 2: address area 20h to 2Fh - transceiver control
			0	SPI write access enabled
			1	SPI write access disabled
1	LK1C	R/W		Lock control 1: address area 10h to 1Fh - regulator control
			0	SPI write access enabled
			1	SPI write access disabled
0	LK0C	R/W		Lock control 0: address area 06h to 09h - general-purpose memory
			0	SPI write access enabled
			1	SPI write access disabled

General-Purpose Memory

The TPT1169 offers four registers to store user information. The values are kept safe unless the chip powers off.

SPI

The SPI interface works in full duplex mode that register value returns while new data is shifted in. The TPT1169 contains 4 SPI interface pins:

- SCSN: SPI chip-select, active low. The default value is high.
- SCK: SPI clock. The default value is low due to internal pull-down.
- SPI data input, also called MOSI. The default value depends on the signal from the microcontroller.
- SDO: SPI data output, also called MISO, floating when pin SCSN is high.

SPI is selected by pulling CSN low. Data samples at the falling edge of CLK, and CLK is low in idle state. SDI transmits addresses and new data, and SDO transmits address and current data. Figure 15 shows the access.

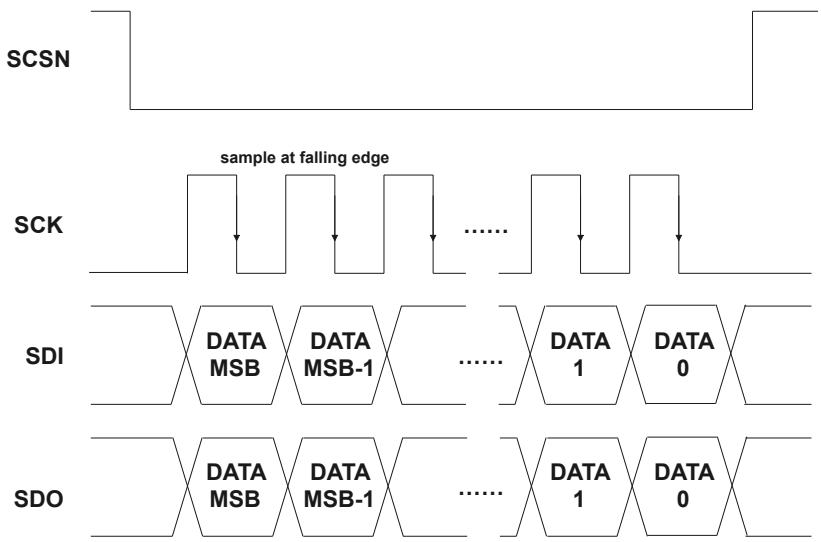


Figure 15. SPI Access Timing

Data on the SPI is a 16-bit form consisting of two bytes: the first byte contains 7-bit address and 1-bit indicating read or write; the other byte is an 8-bit register value, and the access sequence is MSB first. Setting bit 7 to "0" is writing mode while setting bit 7 to "1" is reading mode. Figure 16 shows the data form.

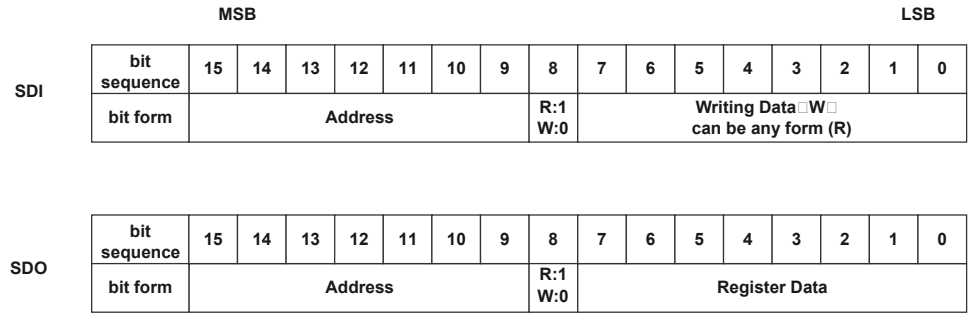


Figure 16. SPI Data Form

Register Map

An overview of the register map is shown from Table 37 to Table 46.

Table 37. System Basis Registers

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
00h	Watchdog control	WMC			Reserved	NWP			
01h	Mode control	Reserved					MC		
02h	Fail-safe control	Reserved					LHC	RCC	
03h	Main status	Reserved	OTWS	NMS	RSS				
04h	System event enable	Reserved					OTWE	SPIFE	Reserved
05h	Watchdog status	Reserved				FNMS	SDMS	SDMS	
06h	Memory 0	GPM [7:0]							
07h	Memory 1	GPM [15:8]							
08h	Memory 2	GPM [23:16]							
09h	Memory 3	GPM [31:24]							
0Ah	Lock control	Reserved	LK6C	LK5C	LK4C	LK3C	LK2C	LK1C	LK0C

Table 38. Voltage Regulator Registers

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
10h	Regulator control	Reserved (1)	PDC	Reserved		V2C (2) / VEXTC (3)		V1RTC	
1Bh	Supply status	Reserved					V2S(2) / VEXTS (3)		V1S
1Ch	Supply event enable	Reserved					V2OE (2) / VEXTOE (3)	V2UE (2) / VEXTUE (3)	V1UE

(1) Always 0.
(2) Non-X version only.
(3) X version only.

Table 39. Transceiver Control and Partial Networking Registers

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
20h	CAN control	Reserved	CFDC (1)	PNCOK (1)	CPNC (1)	Reserved		CMC	
22h	Transceiver status	CTS	CPNERR (1)	CPNS (1)	COSCS (1)	CBSS	Reserved	VCS	CFS
23h	Transceiver event enable	Reserved			CBSE	Reserved		CFE	CWE
26h	Data rate	Reserved					CDR (1)		
27h	Identifier 0	ID [7:0] (1)							
28h	Identifier 1	ID [15:8] (1)							
29h	Identifier 2	ID [23:16] (1)							
2Ah	Identifier 3	Reserved			ID [28:24] (1)				
2Bh	Mask 0	M [7:0] (1)							
2Ch	Mask 1	M [15:8] (1)							
2Dh	Mask 2	M [23:16] (1)							
2Eh	Mask 3	Reserved			M [28:24] (1)				
2Fh	Frame control	IDE (1)	PNDM (1)	Reserved		DLC (1)			
68h	Data mask 0	DM0 [7:0] (1)							
69h	Data mask 1	DM1 [7:0] (1)							
6Ah	Data mask 2	DM2 [7:0] (1)							
6Bh	Data mask 3	DM3 [7:0] (1)							
6Ch	Data mask 4	DM4 [7:0] (1)							
6Dh	Data mask 5	DM5 [7:0] (1)							

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
6Eh	Data mask 6	DM6 [7:0] (1)							
6Fh	Data mask 7	DM7 [7:0] (1)							

(1) Valid within partial networking version.

Table 40. Pin WAKE Control and Status Registers

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
4Bh	Pin WAKE status	Reserved						WPVS	Reserved
4Ch	Pin WAKE enable	Reserved						WPRE	WPFE

Table 41. Event Capture Registers

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
60h	Global event status	Reserved				WPE	TRXE	SUPE	SYSE
61h	System event status	Reserved			PO	Reserved	OTW	SPIF	WDF
62h	Supply event status	Reserved					V2O (1) / VEXTO (2)	V2U (1) / VEXTU (2)	V1U
63h	Transceiver event status	Reserved		PNFDE (3)	CBS	Reserved		CF	CW
64h	Pin WAKE event status	Reserved						WPR	WPF

(1) Non-X version only.
(2) X version only.
(3) Valid within partial networking version.

Table 42. MTPNV Status Register

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
70h	MTPNV status	WRCNTS						ECCS	NVMPS

Table 43. Start-up Control Register

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
73h	Start-up control	Reserved		RLC		V2SUC (1) / VEXTSUC (2)	Reserved		

(1) Non-X version only.
(2) X version only.

Table 44. Configuration Control Register

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
74h	SBC configuration control	Reserved		V1RTSUC		FNMC	SDMC	Reserved	SLPC

Table 45. CRC Control Register

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
75h	MTPNV CRC control	CRCC [7:0]							

Table 46. Identification Register

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
7Eh	Identification	IDS [7:0]							

Register Status in System Operating Mode

Parts of the register value change depending on the system operating mode (see Table 47).

Table 47. Register Value in Different Operating Mode

Symbol	Default	Standby	Normal	Sleep	Overtemp	Reset
CPNS	0	Actual state	Actual state	Actual state	Actual state	Actual state
CRCC	0	No change	No change	No change	No change	No change
CTS	0	0	Actual state	0	0	0
CW	0	No change	No change	No change	No change	No change

Symbol	Default	Standby	Normal	Sleep	Overtemp	Reset
CWE	0	No change	No change	No change	No change	No change
DMn	11111111	No change	No change	No change	No change	No change
DLC	0	No change	No change	No change	No change	No change
ECCS	Actual state	Actual state	Actual state	Actual state	Actual state	Actual state
FNMC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
FNMS	0	Actual state	Actual state	Actual state	Actual state	Actual state
GPMn	0	No change	No change	No change	No change	No change
IDn	0	No change	No change	No change	No change	No change
IDE	0	No change	No change	No change	No change	No change
IDS	See Table 35	No change	No change	No change	No change	No change
LHC	0	No change	No change	No change	1, if t > $t_{d(limp)}$; change	1 if RCC = 3 or t > $t_{d(limp)}$; otherwise, no change
LKnC	0	No change	No change	No change	No change	No change
MC	100	100	111	1	Don't care	100
NMS	1	No change	0	No change	No change	No change
NVMPS	Actual state	Actual state	Actual state	Actual state	Actual state	Actual state
NWP	100	No change	No change	No change	100	100
OTW	0	No change	No change	No change	No change	No change
OTWE	0	No change	No change	No change	No change	No change
OTWS	0	Actual state	Actual state	Actual state	Actual state	Actual state
PDC	0	No change	No change	No change	No change	No change
PNCOK	0	No change	No change	No change	No change	No change
PNDM	1	No change	No change	No change	No change	No change
PNFDE	0	No change	No change	No change	No change	No change
PO	1	No change	No change	No change	No change	No change
RCC	0	No change	No change	No change	No change	RCC++
RLC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
RSS	0	No change	No change	No change	10010	Reset source
SDMC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
SDMS	0	Actual state	Actual state	Actual state	Actual state	Actual state
SLPC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
SPIF	0	No change	No change	No change	No change	No change
SPIFE	0	No change	No change	No change	No change	No change
SUPE	0	No change	No change	No change	No change	No change
SYSE	1	No change	No change	No change	No change	No change
TRXE	0	No change	No change	No change	No change	No change

Symbol	Default	Standby	Normal	Sleep	Overtemp	Reset
V1RTC	Defined by V1 RTSUC	No change	No change	No change	No change	No change
V1RTSUC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
V1S	0	Actual state	Actual state	Actual state	Actual state	Actual state
V1UE	0	No change	No change	No change	No change	No change
V1U	0	No change	No change	No change	No change	No change
VCS	0	Actual state	Actual state	Actual state	Actual state	Actual state
V2C/	Defined by V2SUC/ VEXTSUC	No change	No change	No change	No change	No change
V20/VEXTO	0	No change	No change	No change	No change	No change
V2OE/VEXTOE	0	No change	No change	No change	No change	No change
V2S/VEXTS	0	Actual state	Actual state	Actual state	Actual state	Actual state
V2SUC/ VEXTSUC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
V2U/VEXTU	0	No change	No change	No change	No change	No change
V2UE/VEXTUE	0	No change	No change	No change	No change	No change
WDF	0	No change	No change	No change	No change	No change
WDS	0	Actual state	Actual state	Actual state	Actual state	Actual state
WMC	010	No change	No change	No change	No change	010
WPE	0	No change	No change	No change	No change	No change
WPF	0	No change	No change	No change	No change	No change
WPR	0	No change	No change	No change	No change	No change
WPFE	0	No change	No change	No change	No change	No change
WPRE	0	No change	No change	No change	No change	No change
WPVS	0	No change	No change	No change	No change	No change
WRCNTS	Actual state	Actual state	Actual state	Actual state	Actual state	Actual state

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

Figure 17 shows the typical application schematic.

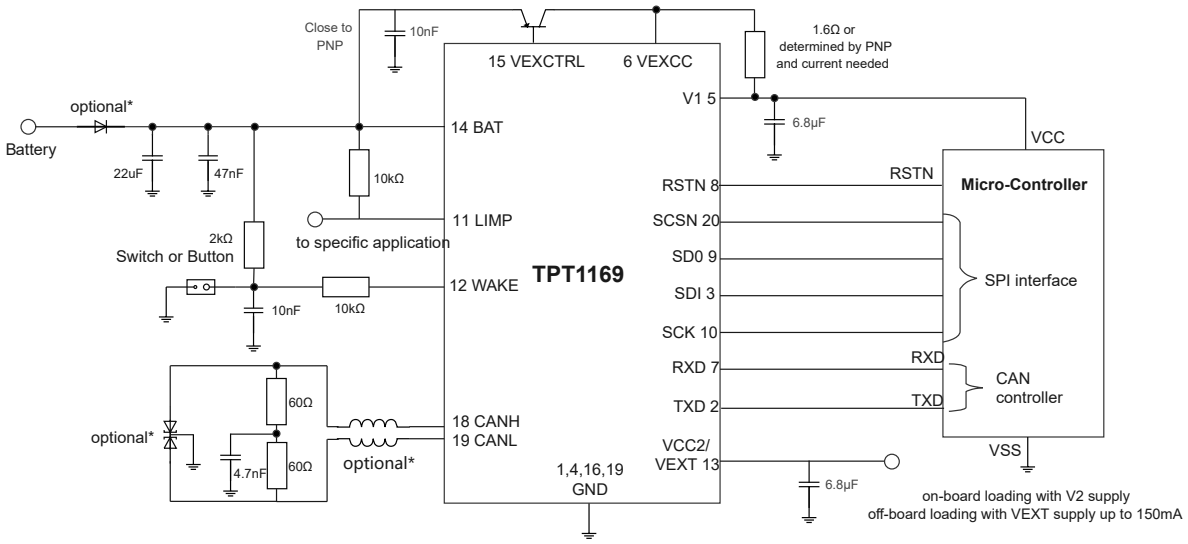
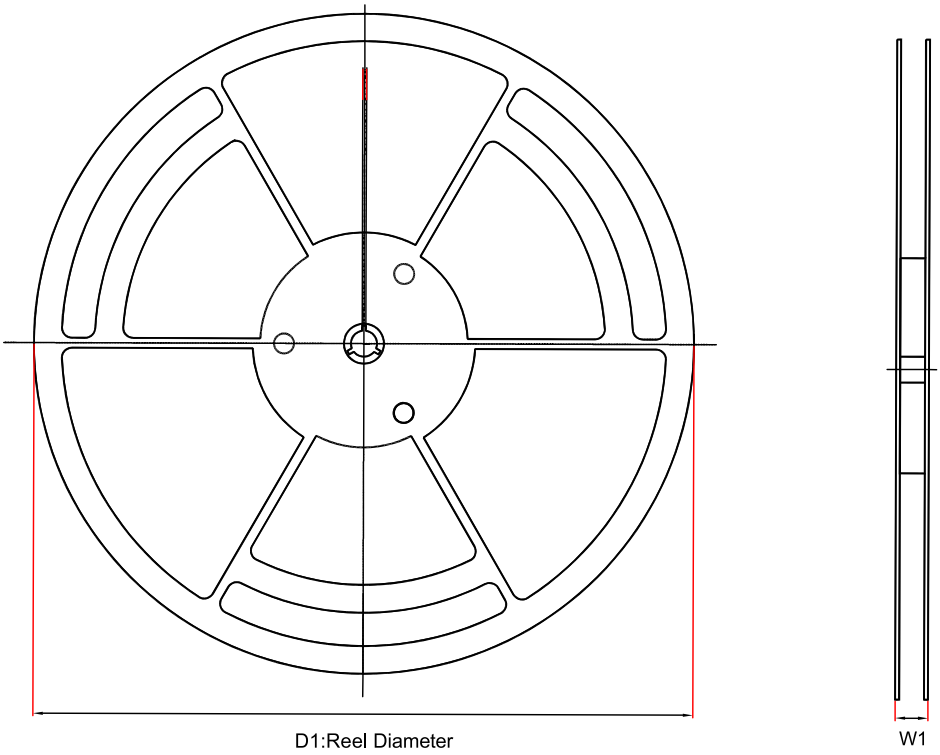
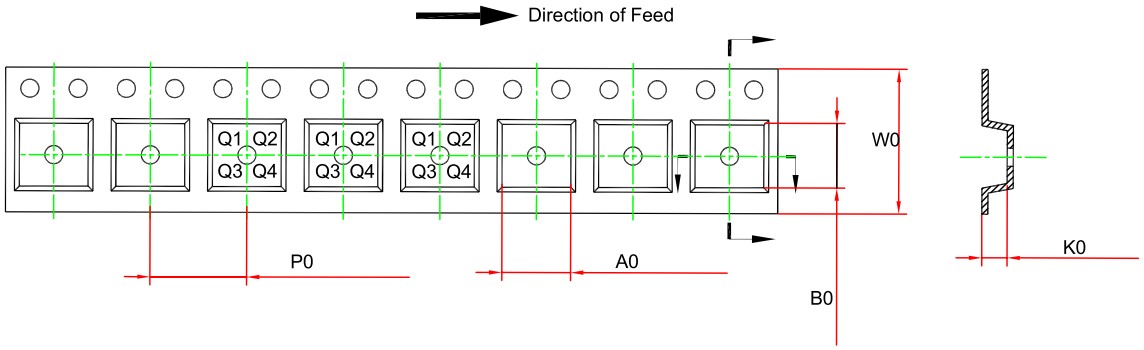


Figure 17. Typical Application Circuit

Tape and Reel Information



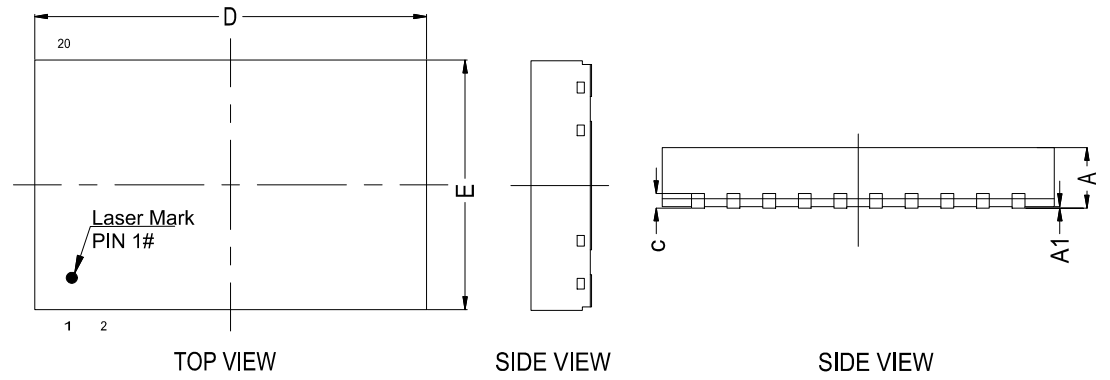


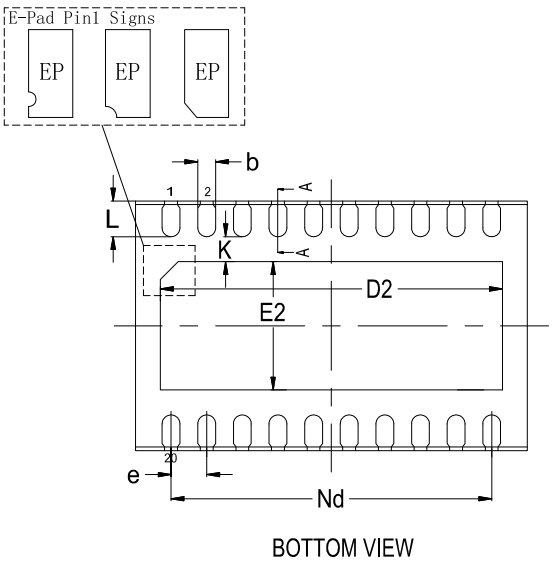
Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
TPT11695Q-DFUR-S	DFN5.5x3.5-20	329	3.8	1.05	12	16.4	5.8	8	Q1
TPT11695XQ-DFUR-S	DFN5.5x3.5-20	329	3.8	1.05	12	16.4	5.8	8	Q1
TPT11695FQ-DFUR-S	DFN5.5x3.5-20	329	3.8	1.05	12	16.4	5.8	8	Q1
TPT11695XFQ-DFUR-S	DFN5.5x3.5-20	329	3.8	1.05	12	16.4	5.8	8	Q1
TPT11693Q-DFUR-S	DFN5.5x3.5-20	329	3.8	1.05	12	16.4	5.8	8	Q1
TPT11693FQ-DFUR-S	DFN5.5x3.5-20	329	3.8	1.05	12	16.4	5.8	8	Q1

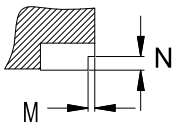
Package Outline Dimensions

DFN5.5X3.5-20-WET-A

Package Outline Dimensions DFU(DFN5.5X3.5-20-WET-A)







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
c	0.203 REF		0.008 TYP	
D	5.400	5.600	0.213	0.220
E	3.400	3.600	0.134	0.142
e	0.500 BSC		0.020 BSC	
D2	4.700	4.900	0.185	0.193
E2	1.700	1.900	0.067	0.075
L	0.450	0.550	0.018	0.022
k	0.350 REF		0.014 REF	
M	0.010	0.090	0.000	0.004
N	0.080	0.180	0.003	0.007
Nd	4.500 BSC		0.117 BSC	

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT11695Q-DFUR-S	−40 to 125°C	DFN3.5x5.5-20L	T695Q	MSL1	Tape and Reel, 3000	Green
TPT11695XQ-DFUR-S	−40 to 125°C	DFN3.5x5.5-20L	T695XQ	MSL1	Tape and Reel, 3000	Green
TPT11695FQ-DFUR-S	−40 to 125°C	DFN3.5x5.5-20L	T695Q	MSL1	Tape and Reel, 3000	Green
TPT11695XFQ-DFUR-S	−40 to 125°C	DFN3.5x5.5-20L	T695XQ	MSL1	Tape and Reel, 3000	Green
TPT11693Q-DFUR-S	−40 to 125°C	DFN3.5x5.5-20L	T693Q	MSL1	Tape and Reel, 3000	Green
TPT11693FQ-DFUR-S	−40 to 125°C	DFN3.5x5.5-20L	T693Q	MSL1	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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