P25Q16SH

Ultra Low Power, 16M-bit

Serial Multi I/O Flash Memory Datasheet

Performance Highlight

- *Supply Range from 2.3V to 3.6V for Read, Erase and Program*
- *Ultra Low Power consumption for Read, Erase and Program*
- *X1, X2 and X4 Multi I/O, QPI, DTR Support*
- *High reliability with 100K cycling and 20 Year-retention*

1 Overview

General

- **Single 2.3V to 3.60V supply**
- **Industrial Temperature Range -40C to 85C**
- **Serial Peripheral Interface (SPI) Compatible: Mode 0 and Mode 3**
- **Single, Dual, Quad SPI, QPI, DTR**
  - Standard SPI: SCLK,CS#,SI,SO,WP#,HOLD#
  - Dual SPI: SCLK,CS#,IO0,IO1,WP#, HOLD#
  - Quad SPI: SCLK,CS#,IO0,IO1,IO2,IO3
  - QPI: SCLK,CS#,IO0,IO1,IO2,IO3
  - DTR: Double Transfer Rate Read
- **Flexible Architecture for Code and Data Storage**
  - Uniform 256-byte Page Program
  - Uniform 256-byte Page Erase
  - Uniform 4K-byte Sector Erase
  - Uniform 32K/64K-byte Block Erase
  - Full Chip Erase
- **Hardware Controlled Locking of Protected Sectors by WP Pin**
- **One Time Programmable (OTP) Security Register**
  - 3*1024-Byte Security Registers With OTP Lock
- **128 bit unique ID for each device**
- **Fast Program and Erase Speed**
  - 1.5ms Single/Dual/Quad Page(s) program time
  - 16ms Page erase time
  - 16ms 4K-byte sector erase time
  - 16ms 32K/64K-byte block erase time
- **JEDEC Standard Manufacturer and Device ID Read Methodology**
- **Ultra Low Power Consumption**
  - 0.5uA Deep Power Down current
  - 10.0uA Standby current
  - 5.0mA Active Read current at 85MHz
  - 3.0mA Active Program or Erase current
- **High Reliability**
  - 100,000 Program / Erase Cycles
  - 20-year Data Retention
- **Industry Standard Green Package Options**
  - 8-Lead SOP (150mil/208mil)
  - 8-Pad USON (3x2x0.55mm, 3x4x0.55mm, 3x2x0.45mm)
  - 8-Pad WSON (6x5x0.75mm)
  - 8-Lead TSSOP
  - KGD for SiP

2 Description

The P25Q16SH is a serial interface Flash memory device designed for use in a wide variety of high-volume consumer based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the device, with its page erase granularity it is ideal for data storage as well, eliminating the need for additional data storage devices.

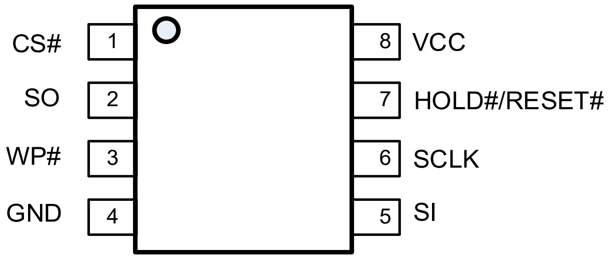
The erase block sizes of the device have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own erase regions, the wasted and unused memory space that occurs with large sectored and large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density.

The device also contains an additional 3*1024-byte security registers with OTP lock (One-Time Programmable), can be used for purposes such as unique device serialization, system-level Electronic Serial Number (ESN) storage, locked key storage, etc.

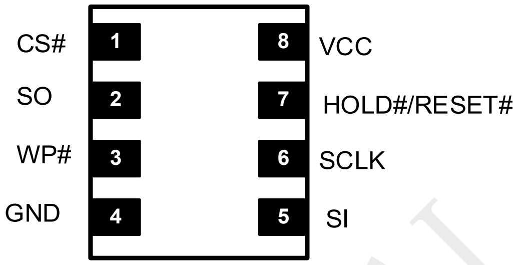
Specifically designed for use in many different systems, the device supports read, program, and erase operations with a wide supply voltage range of 2.3V to 3.6V. No separate voltage is required for programming and erasing.

3 Pin Definition

3.1 Pin Configurations



8-Lead SOP (150mil/208mil) and TSSOP



8-Pad USON (3x2/3x4mm) and WSON(6x5mm)

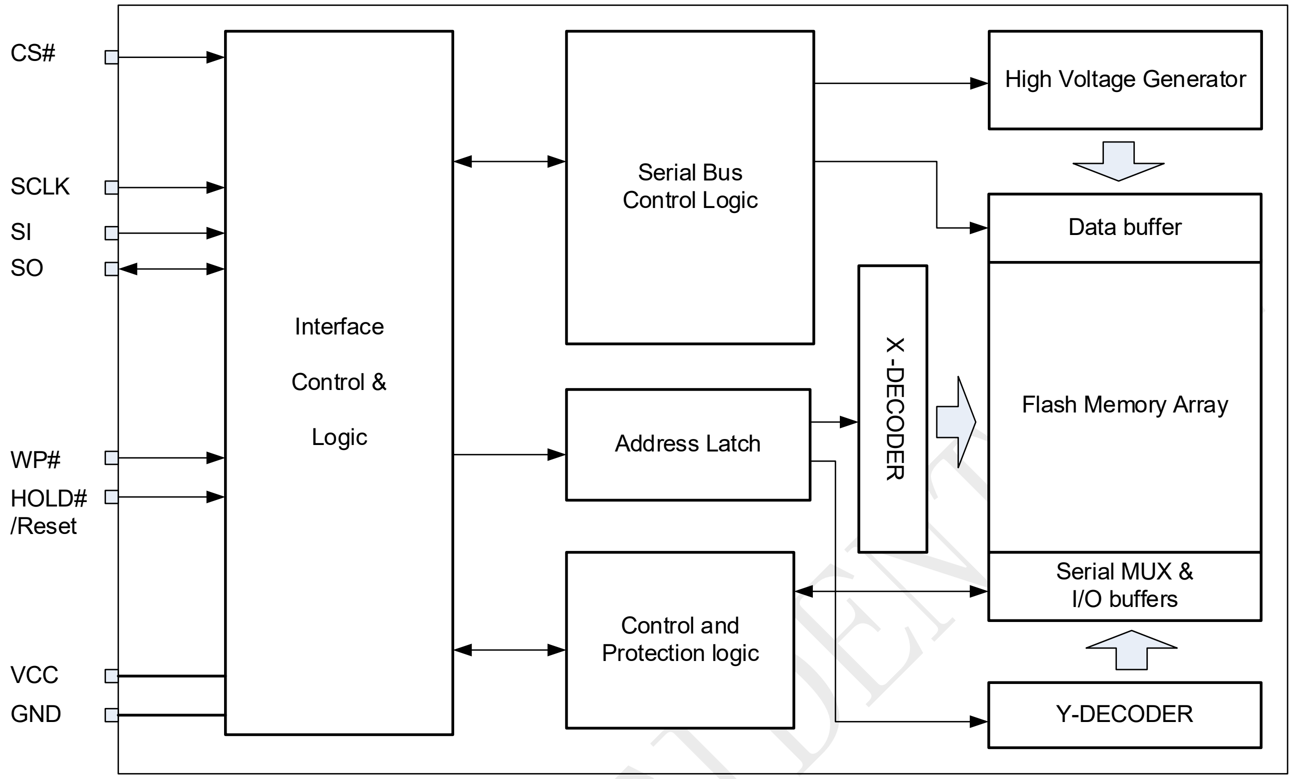
3.2 Pin Descriptions

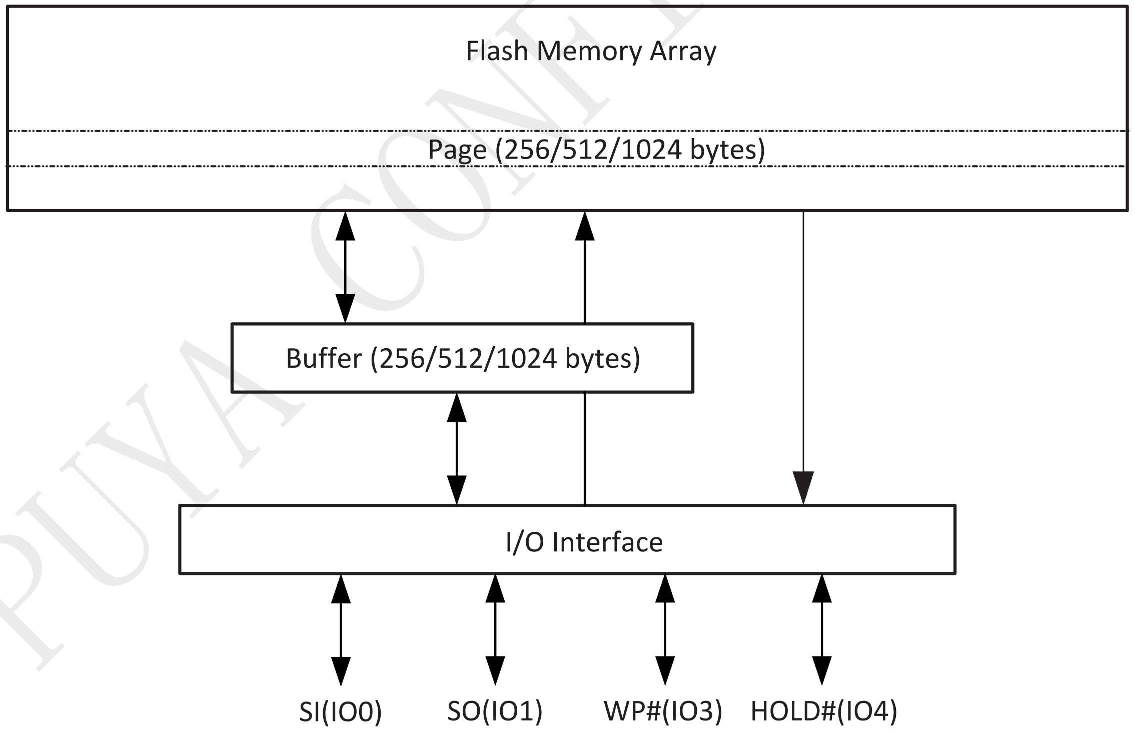
No.	Symbol	Extension	Remarks
1	CS#	-	Chip select
2	SO	SIO1	Serial data output for 1 x I/O Serial data input and output for 4 x I/O read mode
3	WP#	SIO2	Write protection active low Serial data input and output for 4 x I/O read mode
4	GND	-	Ground of the device
5	SI	SIO0	Serial data input for 1x I/O Serial data input and output for 4 x I/O read mode
6	SCLK	-	Serial interface clock input
7	HOLD#/RESET#	SIO3	Hardware Reset Pin Active low or to pause the device without deselecting the device Serial data input and output for 4 x I/O read mode
8	VCC	-	Power supply of the device

Note:

1. SIO0 and SIO1 are used for Standard and Dual SPI instructions
2. SIO0 – SIO3 are used for Quad SPI/QPI instructions, WP# & HOLD# (or RESET#) functions are only available for Standard/Dual SPI.

4 Block Diagram





5 Electrical Specifications

5.1 Absolute Maximum Ratings

- Storage Temperature ....-65°C to +150°C
- Operation Temperature ....-40°C to +85°C
- Maximum Operation Voltage............. 4.0V
- Voltage on Any Pin with respect to Ground. ....-0.6V to VCC+0.5V
- DC Output Current ....5.0 mA

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Pin Capacitance [1]

Symbol	Parameter	Max	Units	Test Condition
C_{OUT}	Output Capacitance	8	pF	V_{OUT}=GND
C_{IN}	Input Capacitance	6	pF	V_{IN}=GND

Note:

1. Test Conditions: T_A = 25°C, F = 1MHz, VCC = 3.0V.

Figure 5-1 Input Test Waveforms and Measurement Level

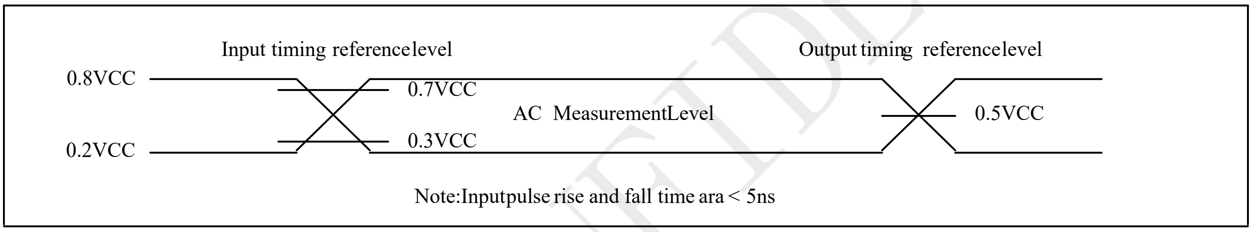
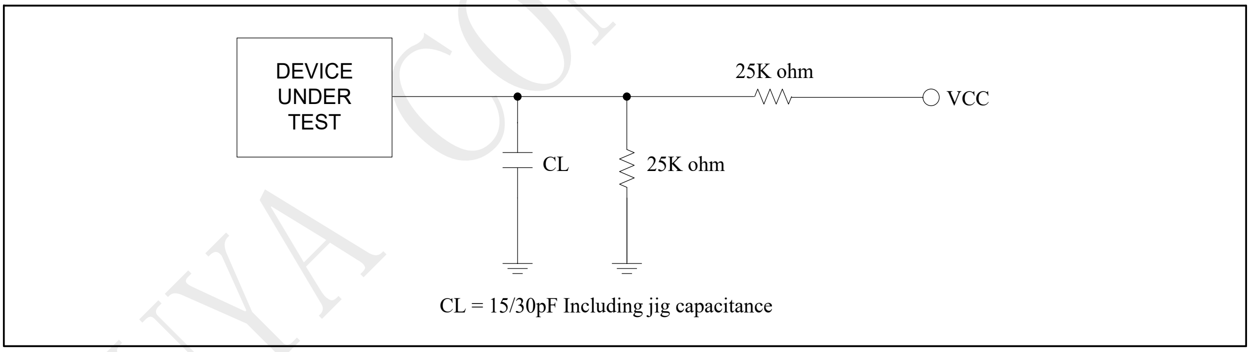

Input timing referencelevel
Output timing referencelevel
0.8VCC
0.7VCC
AC MeasurementLevel
0.5VCC
0.2VCC
0.3VCC
Note:Inputpulse rise and fall time ara < 5ns

Figure 5-2 Output Loading



5.2 DC Characteristics

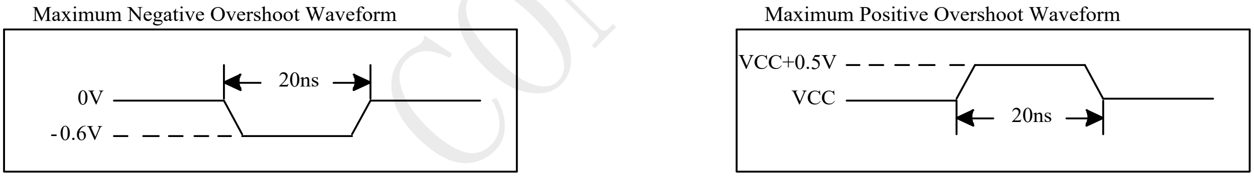
Table 5-2 DC parameters (Ta=-40°C ~ +85°C)

Symbol	Parameter	Conditions	2.3V~3.6V			Units
			Min	Typ[1]	Max	
I_{DPD}	Deep power down current	CS#=Vcc, all other inputs at 0V or Vcc		0.5	5	uA
I_{SB}	Standby current	CS#, HOLD#, WP#=VIH all inputs at CMOS levels		10.0		uA
I_{CC1}	Read current(STR) (1, 2, 4 IO)	f=85MHz; IOUT=0mA		5	8	mA
		f=120MHz; IOUT=0mA		6	10	mA
I_{CC2}	Read current (DTR) (1, 2, 4 IO)	f=50MHz; IOUT=0mA				mA
		f=66MHz; IOUT=0mA		5	8	mA
I_{CC3}	Program current	CS#=Vcc		3.0	4.0	mA
I_{CC4}	Erase current	CS#=Vcc		3.0	4.0	mA
I_{LI}	Input load current	All inputs at CMOS level			2.0	uA
I_{LO}	Output leakage	All inputs at CMOS level			2.0	uA
V_{IL}	Input low voltage		-0.5		0.3Vcc	V
V_{IH}	Input high voltage		0.7Vcc		Vcc+0.3	V
V_{OL}	Output low voltage	IOL=100uA			0.2	V
V_{OH}	Output high voltage	IOH=-100uA	Vcc-0.2			V

Note:

1. Typical values measured at 3.0V @ 25°C for the 2.3V to 3.6V range.

Figure 5-3 Maximum Overshoot Waveform


Maximum Negative Overshoot Waveform
0V
-0.6V
20ns
Maximum Positive Overshoot Waveform
VCC+0.5V
VCC
20ns

During DC conditions, input or I/O signals should remain equal to or between VSS and VCC. During voltage transitions, inputs or I/Os may negative overshoot to –0.6V or positive overshoot to VCC + 0.5 V, for periods up to 20 ns.

5.3 AC Characteristics

Table 5-3-1 AC parameters(Ta=-40°C ~ +85°C)

Symbol	Alt.	Parameter	2.3V~3.6V			Units
			Min	Typ	Max	
fSCLK	fC	Clock Frequency for the following instructions except for special marking	D.C		133	MHz
fRSCLK	fR	Clock Frequency for READ instructions	D.C		55	MHz
fTSCLK	fT	Clock Frequency for 2READ,4READ instructions			104	MHz
	fQ	Clock Frequency for DREAD, QREAD,C0H, QPI 0Bh, QPI EBh, QPI 0Ch instructions			133	MHz
		Clock Frequency for WREAD instructions			104	MHz
	fD	Clock Frequency for DTR instructions			66	MHz
fQPP		Clock Frequency for QPP (Quad page program)			133	MHz
tCH(1)	tCLH	Clock High Time	3.3			ns
tCL(1)	tCLL	Clock Low Time (fSCLK) 45% x (1fSCLK)	3.3			ns
tCLCH(7)		Clock Rise Time (peak to peak)	0.1			v/ns
tCHCL(7)		Clock Fall Time (peak to peak)	0.1			v/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)	5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)	5			ns
tDVCH	tDSU	Data In Setup Time	2			ns
tCHDX	tDH	Data In Hold Time	3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)	5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)	6			ns
tSHSL	tCSH	CS# Deselect Time From Read to next Read	20			ns
		CS# Deselect Time From Write,Erase,Program to Read Status Register	30			ns
tSHQZ(7)	tDIS	Output Disable Time			6	ns
tCLQV	tV	Clock Low to Output Valid Loading 30pF			7	ns
		Clock Low to Output Valid Loading 15pF			6	ns
tCLQX	tHO	Output Hold Time	0			ns
tHLCH		HOLD# Active Setup Time (relative to SCLK)	5			ns
tCHHH		HOLD# Active Hold Time (relative to SCLK)	5			ns
tHHCH		HOLD# Not Active Setup Time (relative to SCLK)	5			ns
tCHHL		HOLD# Not Active Hold Time (relative to SCLK)	5			ns
tHHQX	tLZ	HOLD# to Output Low-Z			6	ns
tHLQZ	tHZ	HOLD# to Output High-Z			6	ns
tWHSL(3)		Write Protect Setup Time	20			ns
tSHWL(3)		Write Protect Hold Time	100			ns
tDP		CS# High to Deep Power-down Mode			3	us
tRES1		CS# High To Standby Mode Without Electronic Signature Read			8	us
tRES2		CS# High To Standby Mode With Electronic Signature Read			8	us
tW		Write Status Register Cycle Time		8	12	ms
tReady		Reset recovery time(for erase/program operation except WRSR/WRCR)			30	us
		Reset recovery time(for WRSR/WRCR operation)		8	12	ms
tBL		Load memory page data to buffer time(256Byte)			60	us
		Load memory page data to buffer time(512Byte)			120	us
tBC		Buffer clear to next instruction latency	200			ns

Table 5-3-2 SPI Read Command Performance Comparison(MHz)

Read command	Dummy Cycles (VCC=2.3V~3.6V)			
	4	6	8	10
FREAD	-	-	133	-
DTR_FREAD	-	66	-	-
DREAD	-	-	133	-
2READ	104(default)	-	133	-
DTR_2READ	66	-	-	-
QREAD	-	-	133	-
4READ	-	104(default)	-	133
DTR_4READ	-	-	66	-

Table 5-3-3 QPI Read Command Performance Comparison(MHz)

Read command	Dummy Cycles (VCC=2.3V~3.6V)			
	4	6	8	10
FREAD	80	104	120	133(default)
DTR_FREAD	-	-	66	-
4READ	80	104	120	133(default)
DTR_4READ	-	-	66	-
BURST READ	80	104	120	133(default)
DTR_BURST READ	-	-	66	-

5.4 AC Characteristics for Program and Erase

Table 5-4 AC parameters for program and erase(Ta=-40°C ~ +85°C)

Symbol	Parameter	2.3V~3.6V			Units
		Min	Typ	Max	
T_{ESL}(6)	Erase Suspend Latency			30	us
T_{PSL}(6)	Program Suspend Latency			30	us
T_{PRS}(4)	Latency between Program Resume and next Suspend	20			us
T_{ERS}(5)	Latency between Erase Resume and next Suspend	20			us
t_{PP}	Page program time (up to 256 bytes)		1.5	3	ms
t_{PE}	Page erase time		16	30	ms
t_{SE}	Sector erase time		16	30	ms
t_{BE1}	Block erase time for 32K bytes		16	30	ms
t_{BE2}	Block erase time for 64K bytes		16	30	ms
t_{CE}	Chip erase time		130	180	ms

Note:

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR instruction.
4. Program operation may be interrupted as often as system request. The minimum timing of tPRS must be observed before issuing the next program suspend command. However, in order for a Program operation to make progress, tPRS ≥ 100us must be included in resume-to-suspend loop(s). Not 100% tested.
5. Erase operation may be interrupted as often as system request. The minimum timing of tERS must be observed before issuing the next erase suspend command. However, in order for an Erase operation to make progress, tERS ≥ 100us must be included in resume-to-suspend loop(s). Notes. Not 100% tested.
6. Latency time is required to complete Erase/Program Suspend operation.
7. The value guaranteed by characterization, not 100% tested in production.

Figure 5-4 Serial Input Timing

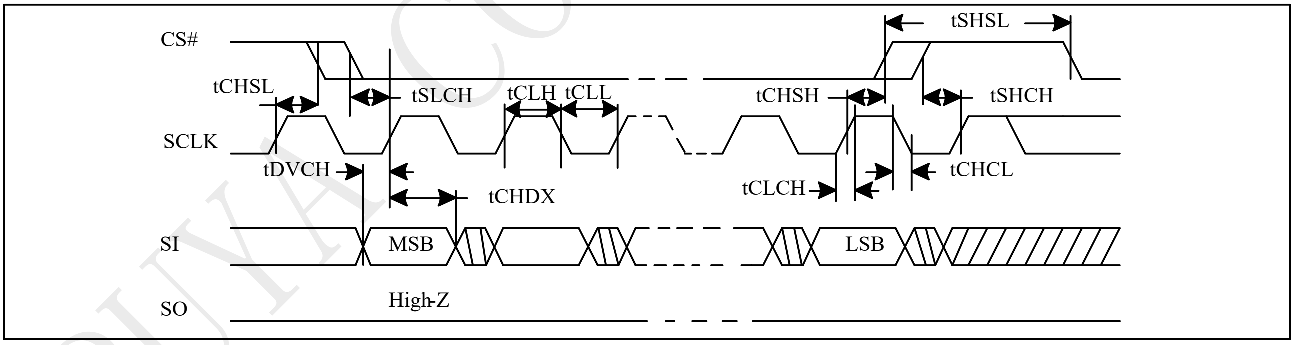


Figure 5-5 Output Timing

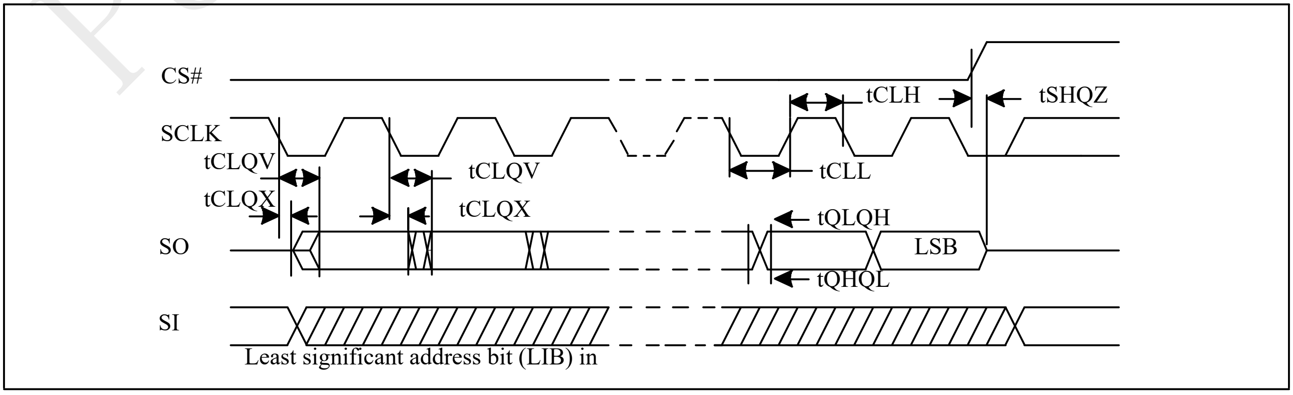


Figure 5-6 Hold Timing

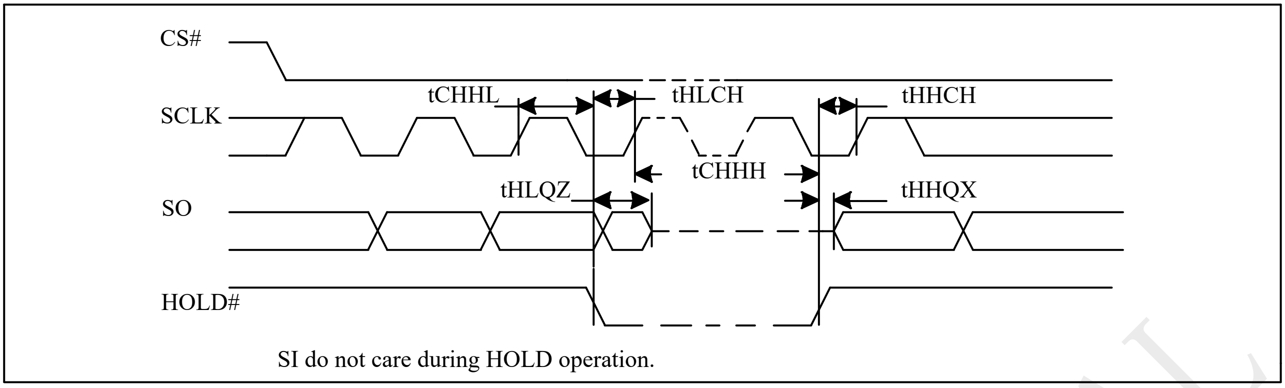
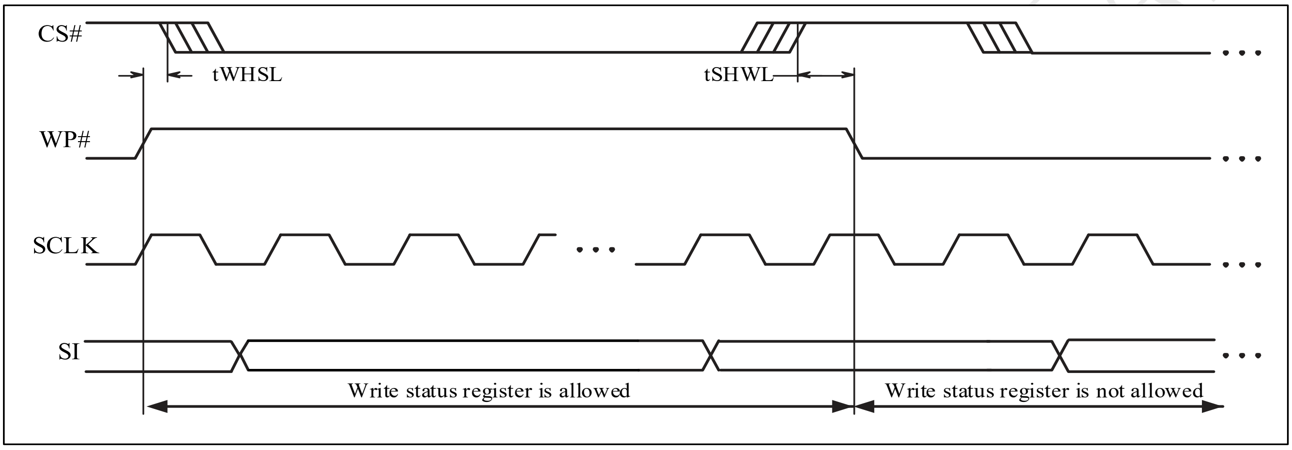


Figure 5-7 WP Timing


CS#
tWHSL
tSHWL
WP#
SCLK
SI
Write status register is allowed
Write status register is not allowed

5.5 Operation Conditions

At Device Power-Up and Power-Down

AC timing illustrated in "Figure AC Timing at Device Power-Up" and "Figure Power-Down Sequence" are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 5-8 AC Timing at Device Power-Up

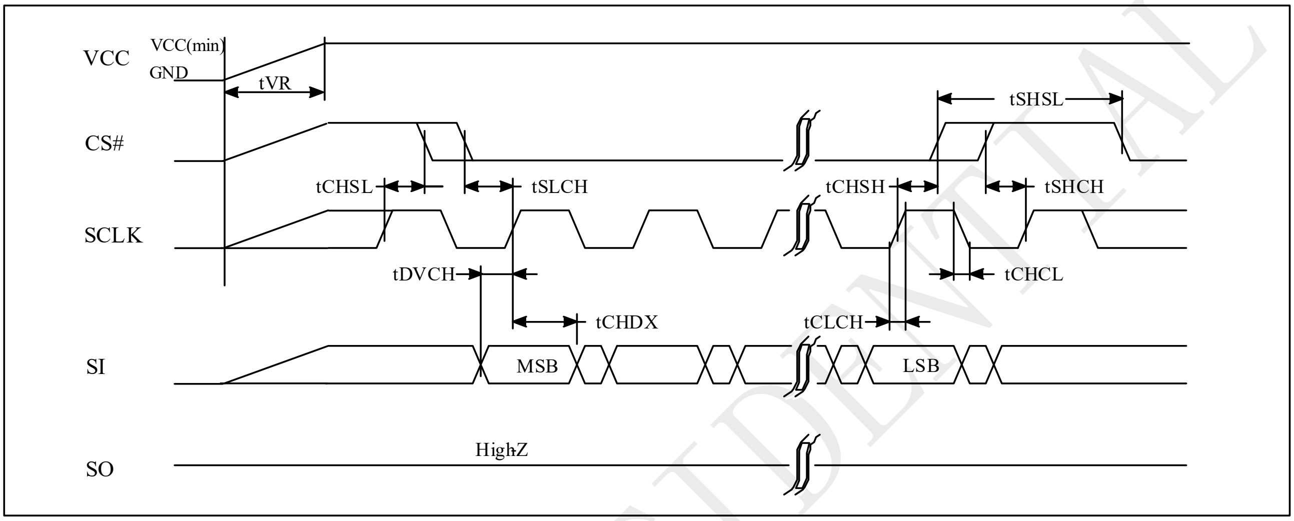
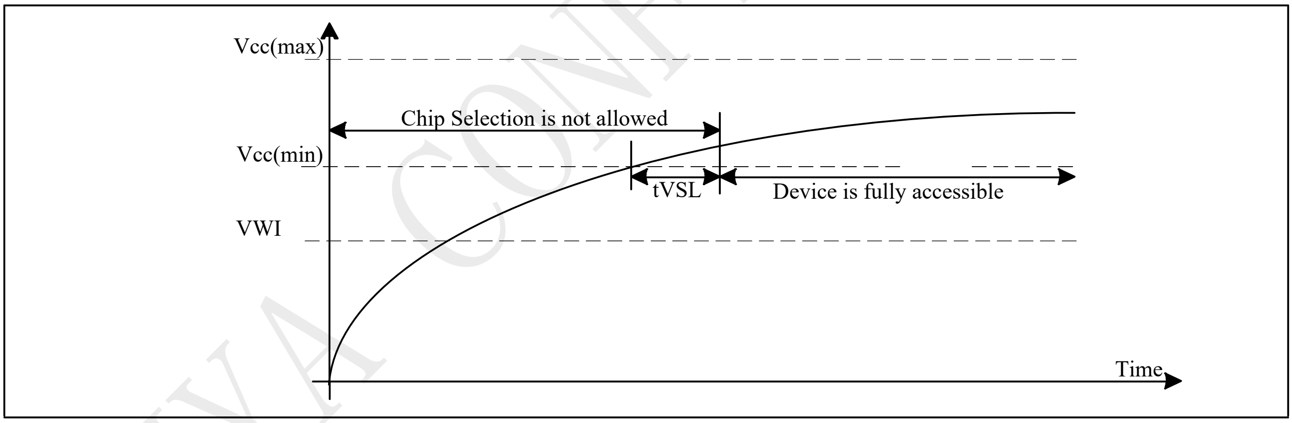


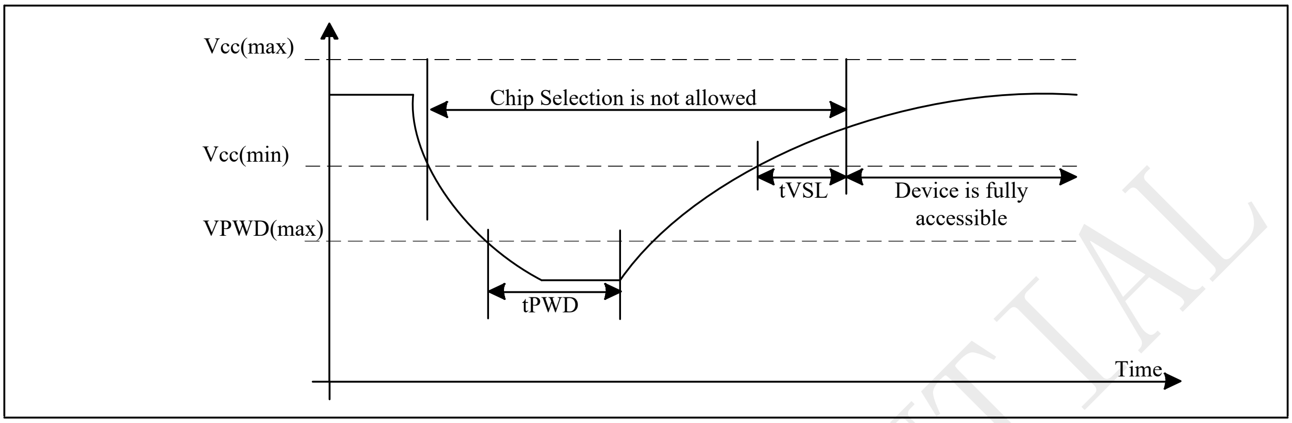
Figure 5-9 Power-up Timing



Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the VCC of flash device must below VPWD for at least tPWD timing. Please check the table below for more detail.

Figure 5-10 Power down-up Timing



Symbol	Parameter	Min	Max	Units
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		1	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVSL	VCC(min.) to device operation	70		us
tVR	VCC Rise Time	1	500000	us/V
VWI	Write Inhibit Voltage	1.45	1.55	V

Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

6 Data Protection

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Power-on reset: to avoid sudden power switch by system power supply transition, the power-on reset may protect the Flash.
- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data.
- Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits define the section of the memory array that can be read but not change.
- Hardware Protection Mode: WP# going low to protected the BP0~BP4bits and SRP0~1bits
- Deep Power-Down Mode: By entering deep power down mode, the flash device is under protected from writing all commands except the Release from Deep Power-Down Mode command.

Protected Area Sizes

Table 6-1. P25Q16SH Protected Area Sizes (WPS=0, CMP bit = 0)

Status bit					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
x	x	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	31	1F0000H-1FFFFFH	64KB	Upper 1/32
0	0	0	1	0	30 and 31	1E0000H-1FFFFFH	128KB	Upper 1/16
0	0	0	1	1	28 to 31	1C0000H-1FFFFFH	256KB	Upper 1/8
0	0	1	0	0	24 to 31	180000H-1FFFFFH	512KB	Upper 1/4
0	0	1	0	1	16 to 31	100000H-1FFFFFH	1MB	Upper 1/2
0	1	0	0	1	0	000000H-00FFFFH	64KB	Lower 1/32
0	1	0	1	0	0 and 1	000000H-01FFFFH	128KB	Lower 1/16
0	1	0	1	1	0 to 3	000000H-03FFFFH	256KB	Lower 1/8
0	1	1	0	0	0 to 7	000000H-07FFFFH	512KB	Lower 1/4
0	1	1	0	1	0 to 15	000000H-0FFFFFH	1MB	Lower 1/2
x	x	1	1	x	0 to 31	000000H-1FFFFFH	2MB	ALL
1	0	0	0	1	31	1FF000H-1FFFFFH	4KB	Upper 1/512
1	0	0	1	0	31	1FE000H-1FFFFFH	8KB	Upper 1/256
1	0	0	1	1	31	1FC000H-1FFFFFH	16KB	Upper 1/128
1	0	1	0	x	31	1F8000H- 1FFFFFH	32KB	Upper 1/64
1	1	0	0	1	0	000000H-000FFFH	4KB	Lower 1/512
1	1	0	1	0	0	000000H-001FFFH	8KB	Lower 1/256
1	1	0	1	1	0	000000H-003FFFH	16KB	Lower 1/128
1	1	1	0	x	0	000000H-007FFFH	32KB	Lower 1/64

Table 6-2. P25Q16SH Protected Area Sizes (WPS=0, CMP bit = 1)

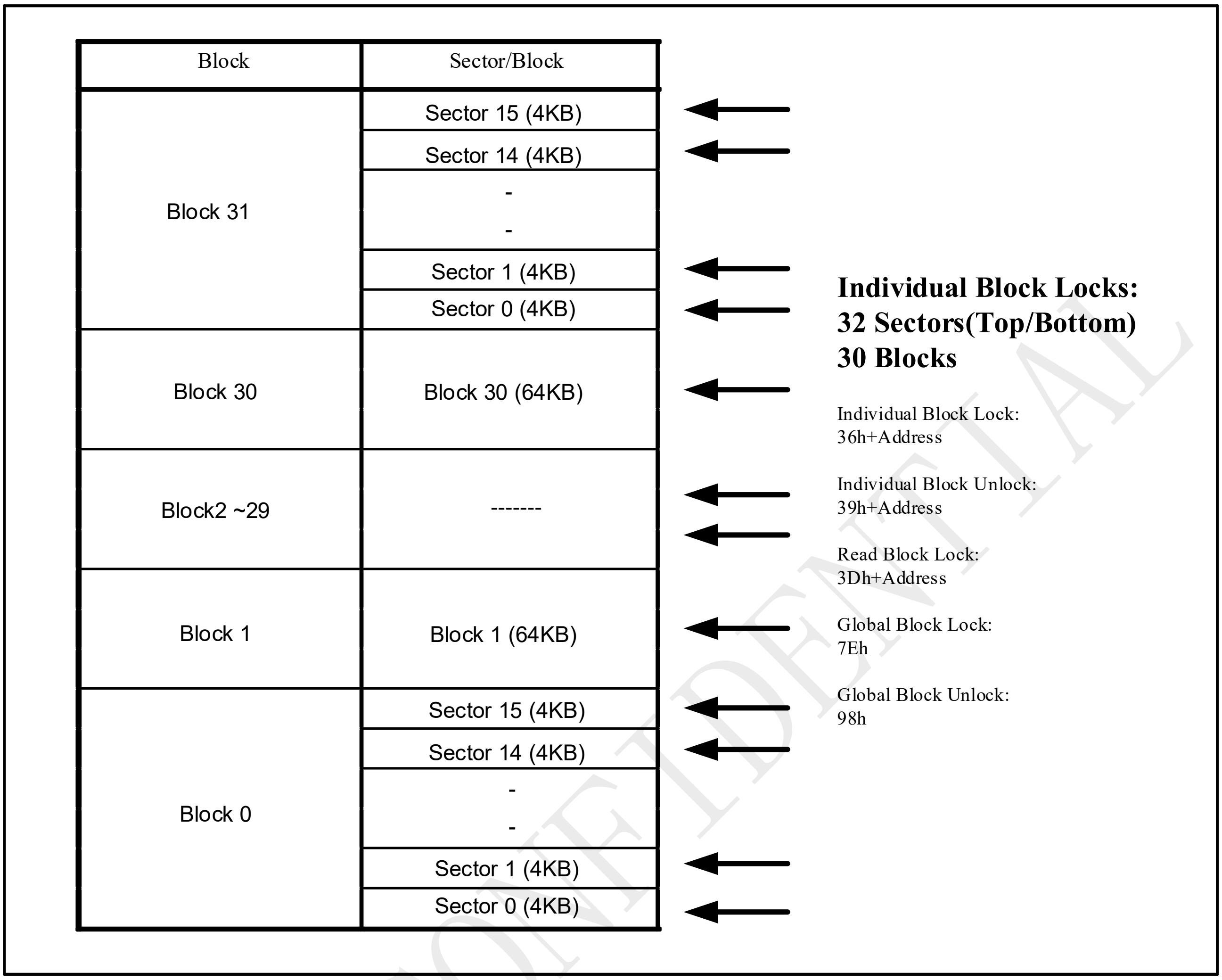
Status bit					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
x	x	0	0	0	0 to 31	000000H-1FFFFFH	2MB	ALL
0	0	0	0	1	0 to 30	000000H-1EFFFFH	1984KB	Lower 31/32
0	0	0	1	0	0 to 29	000000H-1DFFFFH	1920KB	Lower 15/16
0	0	0	1	1	0 to 27	000000H-1BFFFFH	1792KB	Lower 7/8
0	0	1	0	0	0 to 23	000000H-17FFFFH	1536KB	Lower 3/4
0	0	1	0	1	0 to 15	000000H-0FFFFFH	1MB	Lower 1/2
0	1	0	0	1	1 to 31	010000H-1FFFFFH	1984KB	Upper 31/32
0	1	0	1	0	2 to 31	020000H-1FFFFFH	1920KB	Upper 15/16
0	1	0	1	1	4 to 31	040000H-1FFFFFH	1792KB	Upper 7/8
0	1	1	0	0	8 to 31	080000H-1FFFFFH	1536KB	Upper 3/4
0	1	1	0	1	16 to 31	100000H-1FFFFFH	1MB	Upper 1/2
x	x	1	1	x	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 31	000000H-1FEFFFH	2044KB	Lower 511/512
1	0	0	1	0	0 to 31	000000H-1FDFFFH	2040KB	Lower 255/256
1	0	0	1	1	0 to 31	000000H-1FBFFFH	2032KB	Lower 127/128
1	0	1	0	x	0 to 31	000000H-1F7FFFH	2016KB	Lower 63/64
1	1	0	0	1	0 to 31	001000-1FFFFFH	2044KB	Upper 511/512
1	1	0	1	0	0 to 31	002000-1FFFFFH	2040KB	Upper 255/256
1	1	0	1	1	0 to 31	004000-1FFFFFH	2032KB	Upper 127/128
1	1	1	0	x	0 to 31	008000-1FFFFFH	2016KB	Upper 63/64

Note:

1. X=don’t care

2. If any erase or program command specifies a memory that contains protected data portion, this command will be ignored.

Table 6-3. P25Q16SH Individual Block Protection (WPS=1)



Block	Sector/Block
Block 31	Sector 15 (4KB)
	Sector 14 (4KB)
	- -
	Sector 1 (4KB)
	Sector 0 (4KB)
Block 30	Block 30 (64KB)
Block2 ~29	-------
Block 1	Block 1 (64KB)
Block 0	Sector 15 (4KB)
	Sector 14 (4KB)
	- -
	Sector 1 (4KB)
	Sector 0 (4KB)

Individual Block Locks:
32 Sectors(Top/Bottom)
30 Blocks

Individual Block Lock:
36h+Address

Individual Block Unlock:
39h+Address

Read Block Lock:
3Dh+Address

Global Block Lock:
7Eh

Global Block Unlock:
98h

Note:

1. Individual Block/Sector protection is only valid when WPS=1.
2. All individual block/sector lock bits are set to 1 by default after power up, all memory array is protected.

7 Memory Address Mapping

The memory array can be erased in three levels of granularity including a full chip erase. The size of the erase blocks is optimized for both code and data storage applications, allowing both code and data segments to reside in their own erase regions.

Each device has	Each block has	Each sector has	Each page has	
2M	64/32K	4K	256	bytes
8K	256/128	16	-	pages
512	16/8	-	-	sectors
32/64	-	-	-	blocks

P25Q16SH Memory Organization

Block64K	Block32K	Sector	Address Range	
31	63-62	511	1FF000H	1FFFFFH
		……	……	……
		496	1F0000H	1F0FFFH
30	61-60	495	1EF000H	1EFFFFH
		……	……	……
		480	1E0000H	1E0FFFH
……	……	……	……	……
		……	……	……
		……	……	……
……	……	……	……	……
		……	……	……
		……	……	……
2	5 - 4	47	02F000H	02FFFFH
		……	……	……
		32	020000H	020FFFH
1	3 - 2	31	01F000H	01FFFFH
		……	……	……
		16	010000H	010FFFH
0	1 - 0	15	00F000H	00FFFFH
		……	……	……
		0	000000H	000FFFH

8 Device Operation

Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

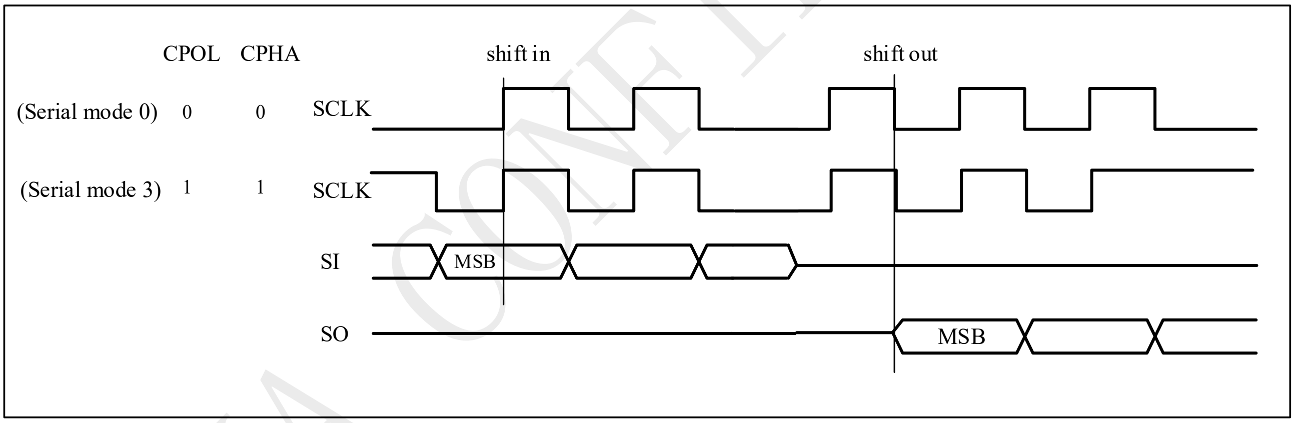
When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.

Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of serial peripheral interface mode 0 and mode 3 is shown as Figure 8-1.

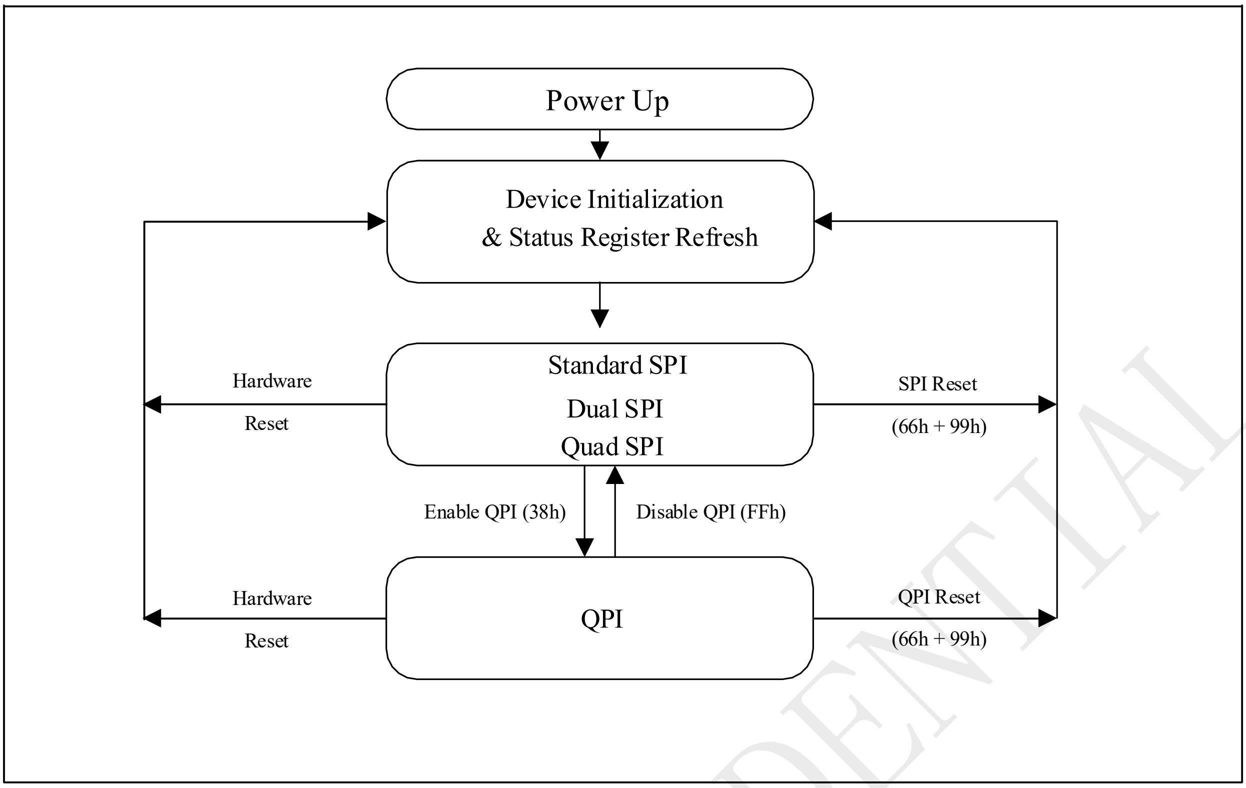
For the following instructions: RDID, RDSR, RDSR1, RDSCUR, READ, FREAD, DREAD, 2READ, 4READ, QREAD, RDSFDP, RES, REMS, DREMS, QREMS, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, PE, SE, BE32K, BE, CE, PP, QPP, DP, ERSCUR, PRSCUR, SUSPEND, RESUME, RSTEN, RST, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 8-1 Serial Peripheral Interface Modes Supported



Note: CPOL indicates clock polarity of serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which serial mode is supported.



Standard SPI

The P25Q16SH features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The P25Q16SH supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3BHand BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

The P25Q16SH supports Quad SPI operation when using the “Quad Output Fast Read”,” Quad I/O Fast Read” (6BH, EBH, E7H) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 andIO3. Quad SPI commands require the non-volatile Quad Enable bit(QE) in Status Register to be set.

QPI

The P25Q16SH supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enable the QPI (38H)” command. The QPI mode utilizes all four IO pins to input the command code. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given times. “Enable the QPI(38H)”and “Disable the QPI(FFH)” commands are used to switch between these two modes. Upon power-up and after software reset using “Reset (99H)” command, the default state of the device is Standard/Dual/Quad SPI mode. The QPI mode requires the non-volatile Quad Enable bit (QE) in Status Register to be set.

SPI / QPI DTR Read Instructions

To effectively improve the read operation throughput without increasing the serial clock frequency, P25Q16SH introduces multiple DTR (Double Transfer Rate) Read instructions that support Standard/Dual/Quad SPI and

QPI modes. The byte-long instruction code is still latched into the device on the rising edge of the serial clock similar to all other SPI/QPI instructions. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

Software Reset

The P25Q16SH can be reset to the initial power-on state by a software Reset sequence, either in SPI mode or QPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the command sequence is successfully accepted, the device will take approximately 30uS (tReady) to reset. No command will be accepted during the reset period.

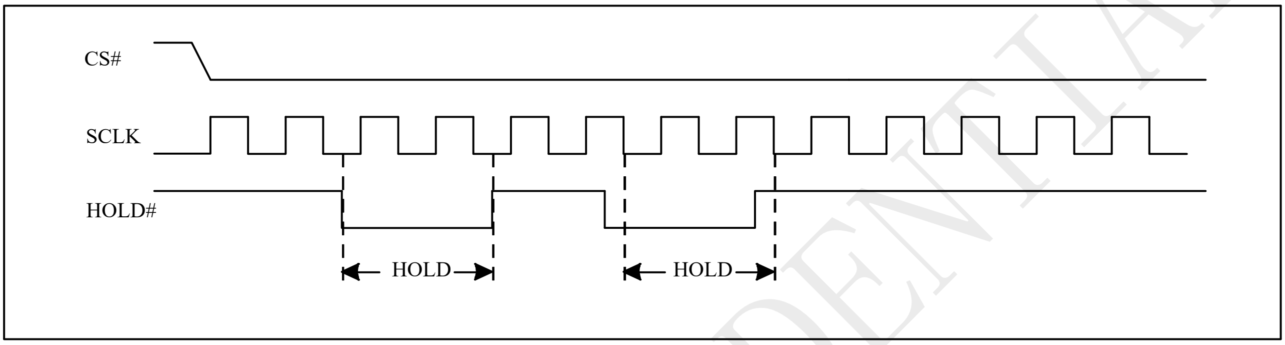
If QE bit is set to 1, the HOLD or RESET function will be disabled, the pin will become one of the four data I/O pins.

9 Hold Feature

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select(CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low).

Figure 9-1 Hold Condition Operation



During the HOLD operation, the Serial Data Output (SO) is high impedance when Hold# pin goes low and will keep high impedance until Hold# pin goes high. The Serial Data Input (SI) is don't care if both Serial Clock (SCLK) and Hold# pin goes low and will keep the state until SCLK goes low and Hold# pin goes high. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.
Note: The HOLD feature is disabled during Quad I/O mode.

10 Commands

10.1 Commands listing

Figure 10-1 Command set(STR Standard/Dual/Quad SPI instruction)

Commands	Abbr.	Code	ADR Bytes	DMY Bytes	Data Bytes	Function description
Read						
Read Array (fast)	FREAD	0Bh	3	1	1+	n bytes read out until CS# goes high
Read Array (low power)	READ	03h	3	0	1+	n bytes read out until CS# goes high
Read Dual Output	DREAD	3Bh	3	1	1+	n bytes read out by Dual output
Read 2IO	2READ	BBh	3	1(2)	1+	n bytes read out by 2IO
Read Quad Output	QREAD	6Bh	3	1	1+	n bytes read out by Quad output
Read 4IO	4READ	EBh	3	3(5)	1+	n bytes read out by 4IO
Read Word 4IO	WREAD	E7h	3	1	1+	n bytes word read out by 4IO
Program and Erase						
Page Erase	PE	81h	3	0	0	erase selected page
Sector Erase (4K bytes)	SE	20h	3	0	0	erase selected sector
Block Erase (32K bytes)	BE32	52h	3	0	0	erase selected 32K block
Block Erase (64K bytes)	BE	D8h	3	0	0	erase selected 64K block
Chip Erase	CE	60h/C7h	0	0	0	erase whole chip
Page Program	PP	02h	3	0	1+	program selected page
Quad page program	QPP	32h	3	0	1+	quad input to program selected page
Program/Erase Suspend	PES	75h	0	0	0	suspend program/erase operation
Program/Erase Resume	PER	7Ah	0	0	0	continue program/erase operation
Protection						
Write Enable	WREN	06h	0	0	0	sets the write enable latch bit
Write Disable	WRDI	04h	0	0	0	resets the write enable latch bit
Volatile SR Write Enable	VWREN	50h	0	0	0	Write enable for volatile SR
Individual Block Lock	SBLK	36h	3	0	0	Individual block lock
Individual Block Unlock	SBULK	39h	3	0	0	Individual block unlock
Read Block Lock Status	RDBLOCK	3Dh	3	0	0	Read individual block lock register
Global Block Lock	GBLK	7Eh	0	0	0	Whole chip block protect
Global Block Unlock	GBULK	98h	0	0	0	Whole chip block unprotect
Security						
Erase Security Registers	ERSCUR	44h	3	0	0	Erase security registers
Program Security Registers	PRSCUR	42h	3	0	1+	Program security registers
Read Security Registers	RDSCUR	48h	3	1	1+	Read value of security register

Command set(Standard/Dual/Quad SPI) Cont'd

Commands	Abbr.	Code	ADR Bytes	DMY Bytes	Data Bytes	Function
Status Register						
Read Status Register	RDSR	05h	0	0	1	read out status register
Read Status Register-1	RDSR1	35h	0	0	1	Read out status register-1
Read Configure Register	RDCR	15h	0	0	1	Read out configure register

Write Status Register	WRSR	01h	0	0	1 to 2	Write data to status registers
Write Status Register-1	WRSR1	31h	0	0	1	Write data to status registers-1
Write Configure Register	WRCR	11h	0	0	1	Write data to configuration register
Data Buffer						
Buffer clear	BFCR	9Eh	0	0	0	Clear all buffer data
Buffer Load	BFLD	9Ah	3	0	0	Load data from main memory to buffer
Buffer Read	BFRD	9Bh	3	1	1+	Read data out from buffer
Buffer Write	BFWR	9Ch	3	0	1+	Write data to buffer
Buffer to Main Memory Page Program	BFPP	9Dh	3	0	0	Program buffer data to main memory
Other Commands						
Reset Enable	RSTEN	66h	0	0	0	Enable reset
Reset	RST	99h	0	0	0	Reset
Enable QPI	QPIEN	38h	0	0	0	Enable QPI mode
Read Manufacturer/device ID	RDID	9Fh	0	0	1 to 3	output JEDEC ID: 1-byte manufacturer ID & 2-byte device ID
Read Manufacture ID	REMS	90h	3		1+	Read manufacturer ID/device ID data
Dual Read Manufacture ID	DREMS	92h	3	1	1+	Dual output read manufacture/device ID
Quad Read Manufacture ID	QREMS	94h	3	1	1+	Quad output read manufacture/device ID
Deep Power-down	DP	B9h	0	0	0	enters deep power-down mode
Release Deep Power-down / Read Electronic ID	RDP/RES	ABh	3	0	1	Read electronic ID data
Set burst length	SBL	77h	0	0	0	Set burst length
Read SFDP	RDSFDP	5Ah				Read SFDP parameter
Release read enhanced		FFh				Release from read enhanced
Read unique ID	RUID	4Bh		4	1+	Read unique ID

Command set(STR QPI Instructions)

Commands	Abbr.	Code	ADR Bytes	DMY Bytes	Data Bytes	Function description
Write Enable		06h	0	0	0	sets the write enable latch bit
Volatile SR Write Enable		50h	0	0	0	Write enable for volatile status register
Write Disable		04h	0	0	0	resets the write enable latch bit
Individual Block Lock		36h	3	0	0	Individual block lock
Individual Block Unlock		39h	3	0	0	Individual block unlock
Read Block Lock Status		3Dh	3	0	0	Read individual block lock register
Global Block Lock		7Eh	0	0	0	Whole chip block protect
Global Block Unlock		98h	0	0	0	Whole chip block unprotect
Read Status Register		05h	0	0	1	read out status register
Read Status Register-1		35h	0	0	1	Read out status register-1
Read Configure Register		15h	0	0	1	Read out configure register
Write Status Register		01h	0	0	1 to 2	Write data to status registers
Write Status Register-1		31h	0	0	1	Write data to status registers-1
Write Configure Register		11h	0	0	1	Write data to configuration register
Page Program		02h	3	0	1+	program selected page
Page Erase		81h	3	0	0	erase selected page
Sector Erase (4K bytes)		20h	3	0	0	erase selected sector

Commands	Abbr.	Code	ADR Bytes	DMY Bytes	Data Bytes	Function description
Block Erase (32K bytes)		52h	3	0	0	erase selected 32K block
Block Erase (64K bytes)		D8h	3	0	0	erase selected 64K block
Chip Erase		60h/C7h	0	0	0	erase whole chip
Program/Erase Suspend		75h	0	0	0	suspend program/erase operation
Program/Erase Resume		7Ah	0	0	0	continue program/erase operation
Buffer Clear		9Eh	0	0	0	Clear all buffer data
Buffer Load		9Ah	3	0	0	Load data from memory to buffer
Buffer Read		9Bh	3	1	1+	Read data out from buffer
Buffer Write		9Ch	3	0	1+	Write data to buffer
Buffer to Main Memory Page Program		9Dh	3	0	0	Program buffer data to main memory
Deep Power-down		B9h	0	0	0	enters deep power-down mode
Release Deep Power-down/Read Electronic ID		ABh	3	0	1	Read electronic ID data
Set Read Parameters		C0h	0	0	1	Set read dummy and wrap
Fast read		0Bh	3	5/2/3/4	1+	n bytes read out until CS# goes high
Burst Read with Wrap		0Ch	3	5/2/3/4	1+	n bytes burst read with wrap by 4IO
Read Word 4x I/O		EBh	3	5/2/3/4	1+	n bytes read out by 4IO
Read Manufacture ID		90h	3		1+	Read manufacturer ID/device ID data
Read Manufacturer/device ID		9Fh	0	0	1 to 3	output JEDEC ID: 1-byte manufacturer ID & 2-byte device ID
Read SFDP		5Ah				Read SFDP parameter
Disable QPI		FFh				Release from read enhanced
Reset Enable		66h	0	0	0	Enable reset
Reset		99h	0	0	0	Reset

Command set(DTR SPI Instructions)

Commands	Abbr.	Code	ADR Bytes	DMY Cycles	Data Bytes	Function description
DTR Fast Read	DTRFRD	0Dh	3	6	1+	DTR n byte fast read out
DTR 2IO Read	2DTRD	BDh	3	2+4	1+	DTR n byte read out by 2IO
DTR 4IO Read	4DTRD	EDh	3	1+7	1+	DTR n byte read out by 4IO

Command set(DTR QPI Instructions)

Commands	Abbr.	Code	ADR Bytes	DMY Cycles	Data Bytes	Function description
DTR Burst Read with Wrap		0Eh	3	8	1+	DTR n bytes burst read with wrap by 4IO
DTR Fast Read	DTRFRD	0Dh	3	8	1+	DTR n byte fast read out
DTR 4IO Read	4DTRD	EDh	3	1+7	1+	DTR n byte fast read out

NOTE:

1. Dual Output data
IO0 = (D6, D4, D2, D0)
IO1 = (D7, D5, D3, D1)

2. Dual Input Address
IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data

IO0 = (D4, D0, …..)
IO1 = (D5, D1, …..)
IO2 = (D6, D2, …..)
IO3 = (D7, D3,…..)

4. Quad Input Address
IO0 = A20, A16, A12, A8, A4, A0, M4, M0
IO1 = A21, A17, A13, A9, A5, A1, M5, M1
IO2 = A22, A18, A14, A10, A6, A2, M6, M2
IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Fast Read Quad I/O Data
IO0 = (x, x, x, x, D4, D0,…)
IO1 = (x, x, x, x, D5, D1,…)
IO2 = (x, x, x, x, D6, D2,…)
IO3 = (x, x, x, x, D7, D3,…)

6. Fast Word Read Quad I/O Data
IO0 = (x, x, D4, D0,…)
IO1 = (x, x, D5, D1,…)
IO2 = (x, x, D6, D2,…)
IO3 = (x, x, D7, D3,…)

7. Fast Word Read Quad I/O Data: the lowest address bit must be 0.

8. QPI Command, Address, Data input/output format:
CLK #0 1 2 3 4 5 6 7 8 9 10 11
IO0= C4, C0, A20, A16, A12, A8, A4, A0, D4, D0, D4, D0,
IO1= C5, C1, A21, A17, A13, A9, A5, A1, D5, D1, D5, D1
IO2= C6, C2, A22, A18, A14, A10, A6, A2, D6, D2, D6, D2
IO3= C7, C3, A23, A19, A15, A11, A7, A3, D7, D3, D7, D3

9. Security Registers Address:
Security Register1: A23-A16=00H, A15-A9=000100, A9-A0= Byte Address;
Security Register2: A23-A16=00H, A15-A9=001000, A9-A0= Byte Address;
Security Register3: A23-A16=00H, A15-A9=001100, A9-A0= Byte Address;

10.2 Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, QPP, PE, SE, BE32K, BE, CE, BFPP and WRSR, WRCR, ERSCUR, PRSCUR which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high.

Figure 10-2 Write Enable (WREN) Sequence (Command 06)

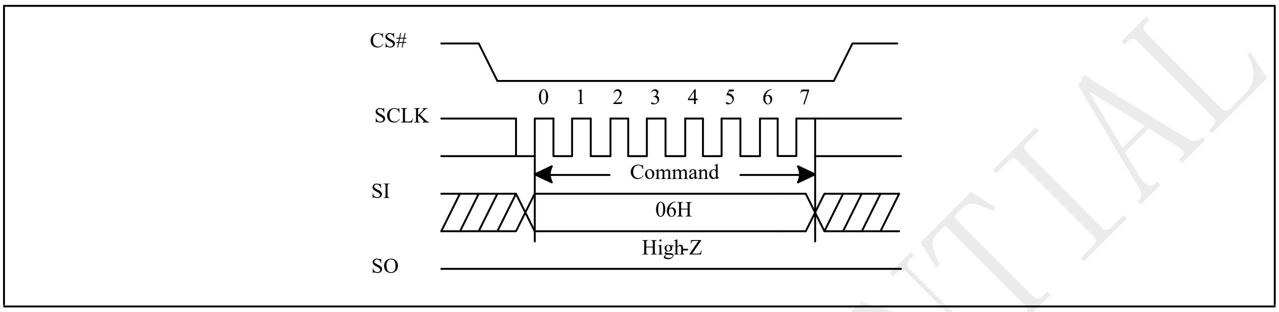
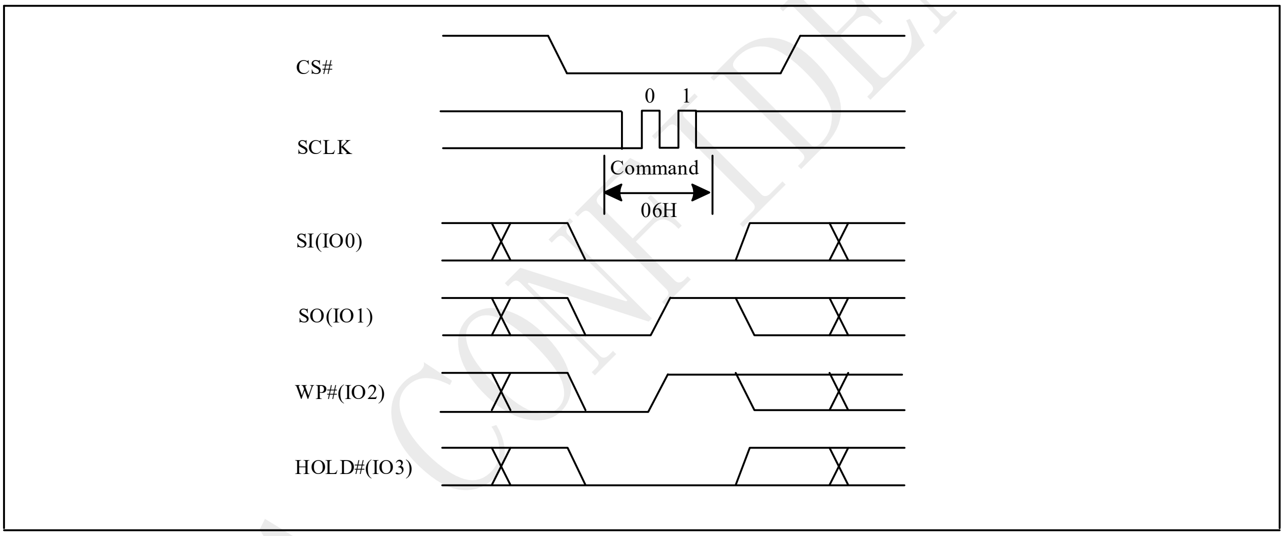


Figure 10-2a Write Enable (WREN) Sequence (QPI)



10.3 Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high.

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR/WRCR) instruction completion
- Page Program (PP) instruction completion
- Quod Page Program (QPP) instruction completion
- Page Erase (PE) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE32K, BE) instruction completion
- Chip Erase (CE) instruction completion
- Buffer to Main Memory Page Program(BFPP) instruction completion
- Erase Security Register (ERSCUR) instruction completion
- Program Security Register (PRSCUR) instruction completion
- Reset (RST) instruction completion

Figure 10-3 Write Disable (WRDI) Sequence (Command 04)

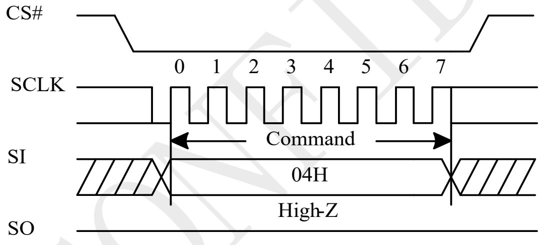
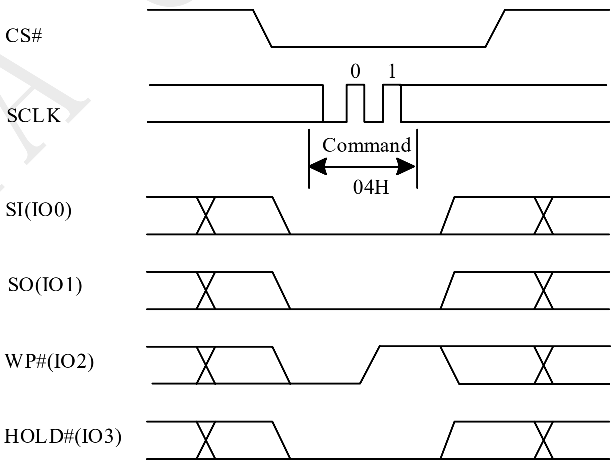


Figure 10-3a Write Disable (WRDI) Sequence (QPI)



10.4 Write Enable for Volatile Status Register

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

The sequence of issuing Write Enable for Volatile Status Register instruction is: CS# goes low→ sending Write Enable for Volatile Status Register instruction code→ CS# goes high.

Figure 10-4 Write Enable for Volatile Status Register Sequence (Command 50)

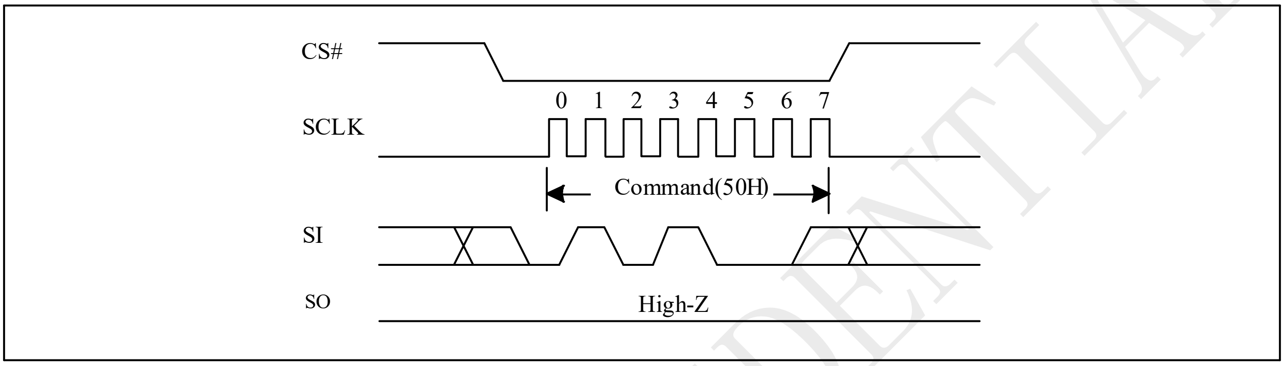
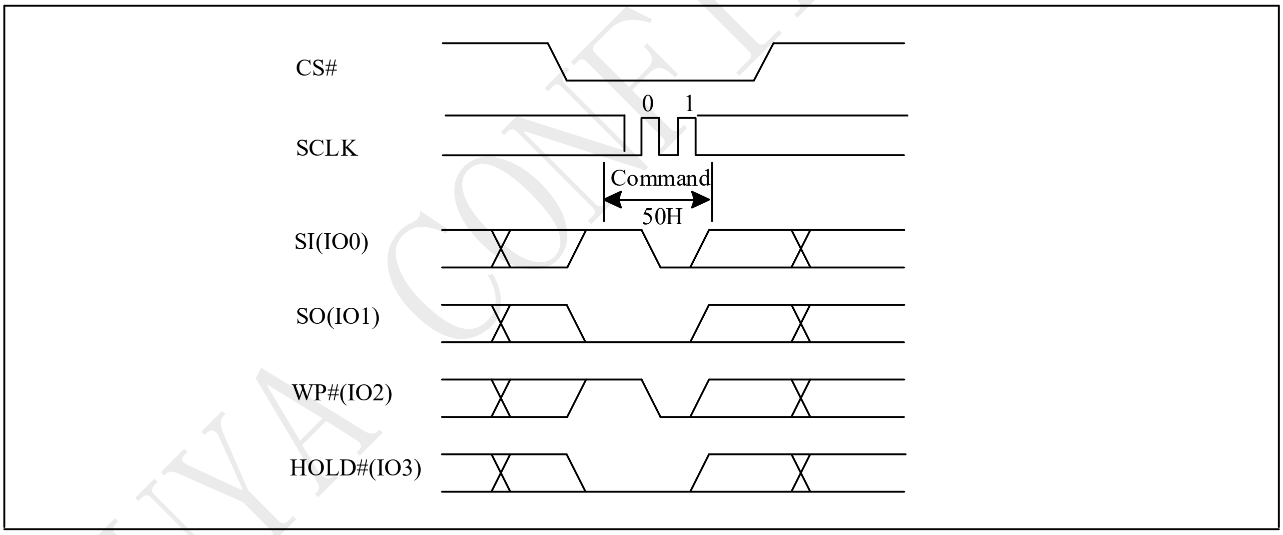


Figure 10-4a Write Enable for Volatile Status Register Sequence (QPI)



10.5 Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress. For command code “05H”, the SO will output Status Register bits S7~S0. The command code “35H”, the SO will output Status Register bits S15~S8.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO. The SIO[3:1] are "don't care".

Figure 10-5 Read Status Register (RDSR) Sequence (Command 05 or 35)

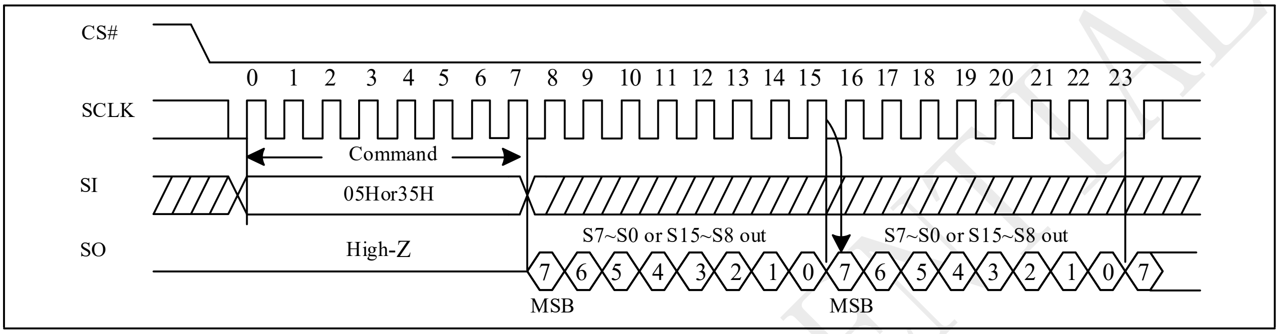
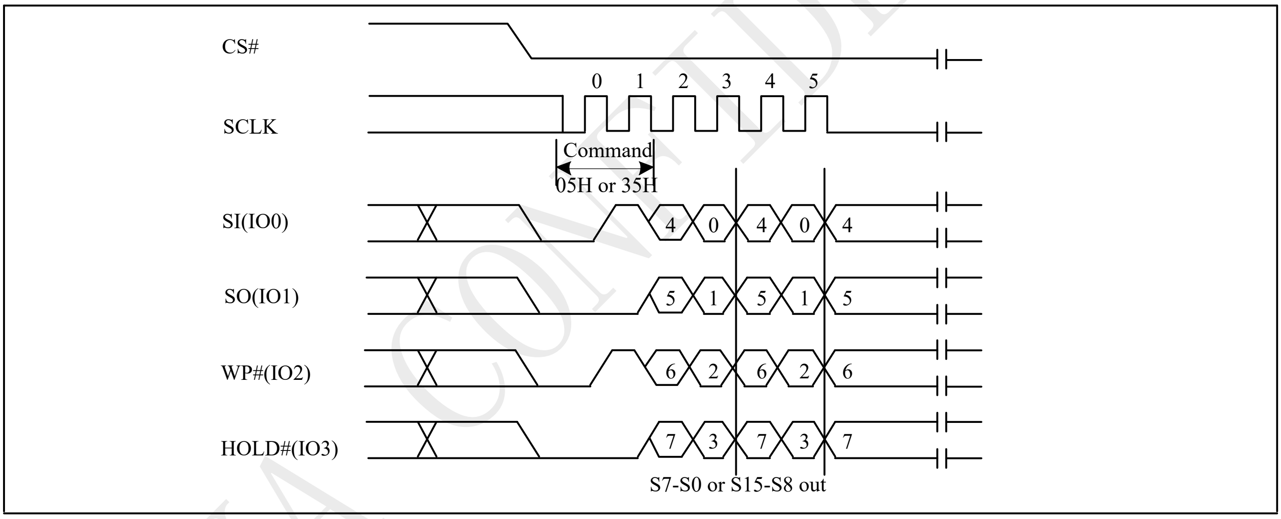


Figure 10-5a Read Status Register (RDSR) Sequence (QPI)



Status Register

S15	S14	S13	S12	S11	S10	S9	S8
SUS	CMP	LB3	LB2	LB1	EP_FAIL	QE	SRP1

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP

The definition of the status register bits is as below:

WIP bit.

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits.

The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table "Protected Area Sizes"). Becomes protected against Page Program (PP), Page Erase (PE), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, only if the Block Protect (BP4, BP3, BP2, BP1and BP0) are set to "None protected".

SRP1, SRP0 bits.

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection

SRP1	SRP0	WP#	Status Register	Description
0	0	x	Software Protected	The Status Register and Configure Register can be written to after a Write Enable command, WEL=1.(Default)
0	1	0	Hardware Protected	WP#=0, the Status Register and Configure Register locked and cannot be written to.
0	1	1	Hardware Unprotected	WP#=1, the Status Register and Configure Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	x	Power Supply Lock-Down(1)	Status Register and Configure Register are protected and cannot be written to again until the next Power-Down, Power-Up cycle.
1	1	x	One Time Program(2)	Status Register and Configure Register are permanently protected and cannot be written to.

Note:

1. When SRP1, SRP0=(1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available on special order. Please contact PUYA for details.

QE bit.

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground)

EP_FAIL bit.

The Erase/Program Fail bit is a read only bit which shows the status of the last Program/Erase operation. The bit will be set to "1" if the program/erase operation failed or interrupted by reset or the program/erase region was protected. It will be automatically cleared to "0" if the next program/erase operation succeeds. Please note that it will not interrupt or stop any operation in the flash memory.

LB3, LB2, LB1, bits.

The LB3, LB2, LB1, bits are non-volatile One Time Program (OTP) bits in Status Register (S13-S11) that provide the write protect control and status to the Security Registers. The default state of LB3-LB1are0, the security registers are unlocked. The LB3-LB1bitscan be set to 1 individually using the Write Register instruction. The LB3-LB1bits are One Time Programmable, once its set to 1, the Security Registers will become read-only permanently.

CMP bit

The CMP bit is a non-volatile Read/Write bit in the Status Register(S14). It is used in conjunction the BP4-BP0 bits to provide more flexibility for the array protection. Please see the table “Protected Area Size” for details. The default setting is CMP=0.

SUS bit

The SUS bit is read only bit in the status register (S15) that is set to 1 after executing a Program/Erase Suspend (75H) command. The SUS bit is cleared to 0 by Program/Erase Resume (7AH) command as well as a power-down, power-up cycle.

10.6 Read Configure Register (RDCR)

The RDCR instruction is for reading Configure Register Bits. The Read Configure Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low→ sending RDCR instruction code→ Configure Register data out on SO. The SIO[3:1] are "don't care".

Figure 10-6 Read Status Register (RDCR) Sequence (Command 15)

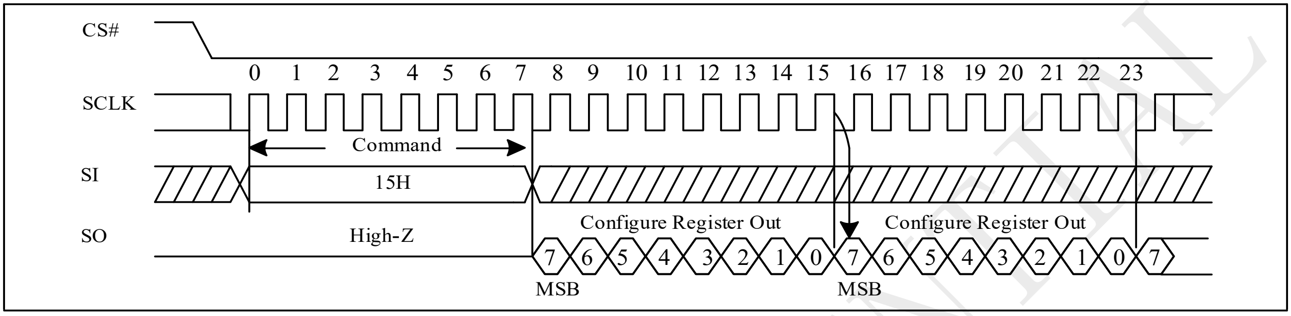
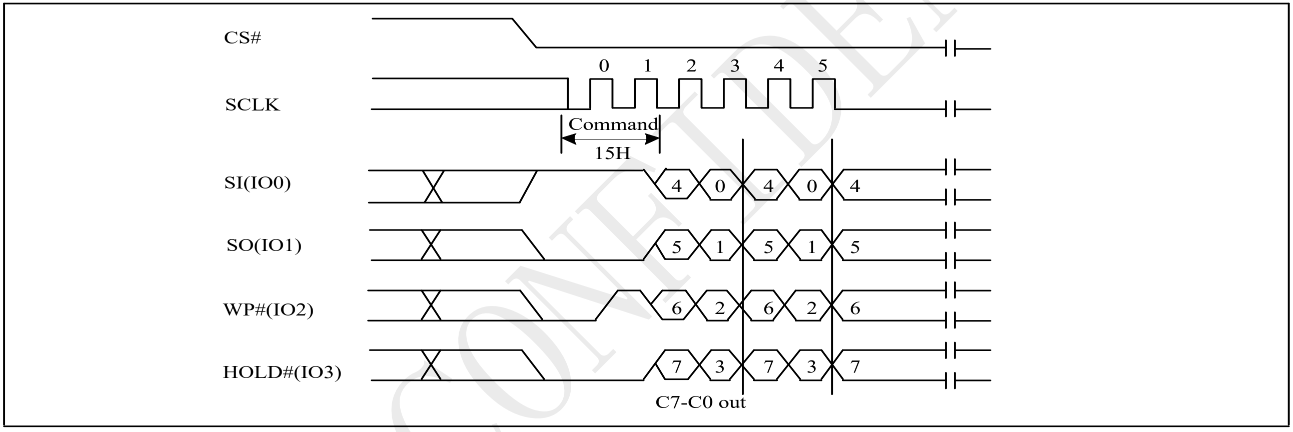


Figure 10-6a Read Status Register (RDCR) Sequence (QPI)



Configure Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HOLD/RST	DRV1	DRV0	MPM1	MPM0	WPS	DC	DLP

HOLD/RST bit.
The HOLD/RST bit is a non-volatile Read/Write bit in the Configure Register which is used to determine whether /HOLD or /RESET function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0 (factory default), the pin acts as /HOLD; when HOLD/RST=1, the pin acts as /RESET. However, /HOLD or /RESET functions are only available when QE=0. If QE is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as a dedicated data I/O pin.

DRV1 & DRV0 bit.
The DRV1 & DRV0 bits are non-volatile Read/Write bits which are used to determine the output driver strength for the Read operations.

DRV1,DRV0	Drive Strength
0,0	60%
0,1(default)	100%
1,0	140%
1,1	40%

MPM1 & MPM0 bit.

The Multi Page Mode(MPM) bits are volatile Read/Write bits which allows Quad/Dual Page operation.

MPM1,MPM0	Page Size
0,0 (default)	256byte
0,1	512byte
1,0	1024byte
1,1	reserved

The page size is defined by MPM bits as above table. When the MPM bits are set to (0,0) (Default) the page size is 256bytes. When the MPM bits are set to (0,1), the page size is 512bytes. When the MPM bits are set to (1,0), the page size is 1024bytes.

This bit controls the page programming buffer address wrap point. Legacy SPI devices generally have used a 256 Byte page programming buffer and defined that if data is loaded into the buffer beyond the 255 Byte locations, the address at which additional bytes are loaded would be wrapped to address zero of the buffer. The P25Q16SH provides a 512/1024 Byte page programming buffer that can increase programming performance. For legacy software compatibility, this configuration bit provides the option to continue the wrapping behavior at the 256 Byte boundary or to enable full use of the available 512/1024 Byte buffer by not wrapping the load address at the 256 Byte boundary. When the MPM bits are set to (0,1), the page erase instruction (81h) will erase the data of the chosen Dual Page to be "1". When the MPM bits are set to (1,0), the page erase instruction (81h) will erase the data of the chosen Quad Page to be "1".

WPS bit.

The WPS bit is a non-volatile Read/Write bit in the Configure Register which is used to select which Write Protect scheme should be used. When WPS=0(default), the device will use the combination of CMP, BP[4:0] bits to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

DC bit

The Dummy Cycle (DC) bit is a volatile bit. The Dummy Cycle (DC) bit can be used to configure the number of dummy clocks for “SPI 2 X IO Read (BBH)” command, “SPI 4X I/O Read (EBH)” command.

Dummy Cycle Table

Mode	Command	DC1	Number of dummy cycles
SPI command	BB SPI	0(default)	4
		1	8
	EB SPI	0(default)	6
		1	10

DLP bit

The DLP bit is Data Learning Pattern Enable bit, which is volatile writable by 11H command. For DTR Read commands, a pre-defined “Data Learning Pattern” can be used by the flash memory controller to determine the flash data output timing on I/O pins. When DLP=1, in dummy cycles, the flash will output “00110100” Data Learning Pattern sequence on each of the I/O pins. During this period, controller can fine tune the data latching timing for each I/O pins to achieve optimum system performance. DLP=0(default) will disable the Data Learning Pattern output.

10.7 Write Status Register (WRSR)

The Write Status Register (WRSR) and Write Status Register-1 (WRSR1) commands allow new values to be written to the Status Register-0 and Status Register-1. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The WRSR and WRSR1 command has no effect on S15, S10, S1 and S0 of the Status Register. CS# must be driven high after the eighth bit or sixteen bit (just for WRSR command) of the data byte has been latched in. If not, the command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The WRSR command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table6-1 and Table6-2. The WRSR and WRSR1 commands also allow the user to set or reset the Status Register Protect (SRP0 and SRP1) bits respectively in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP0 and SRP1) bits and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→CS# goes high.

Figure 10-7Write Status Register (WRSR) Sequence (Command 01h or 31h)

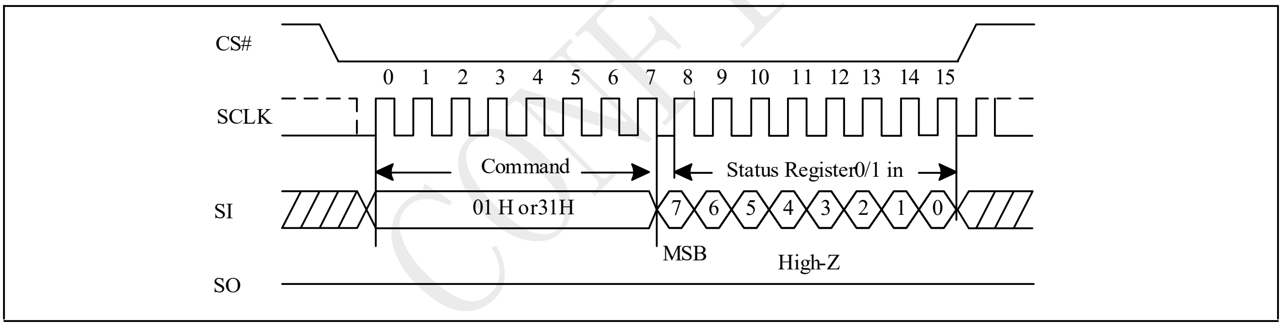
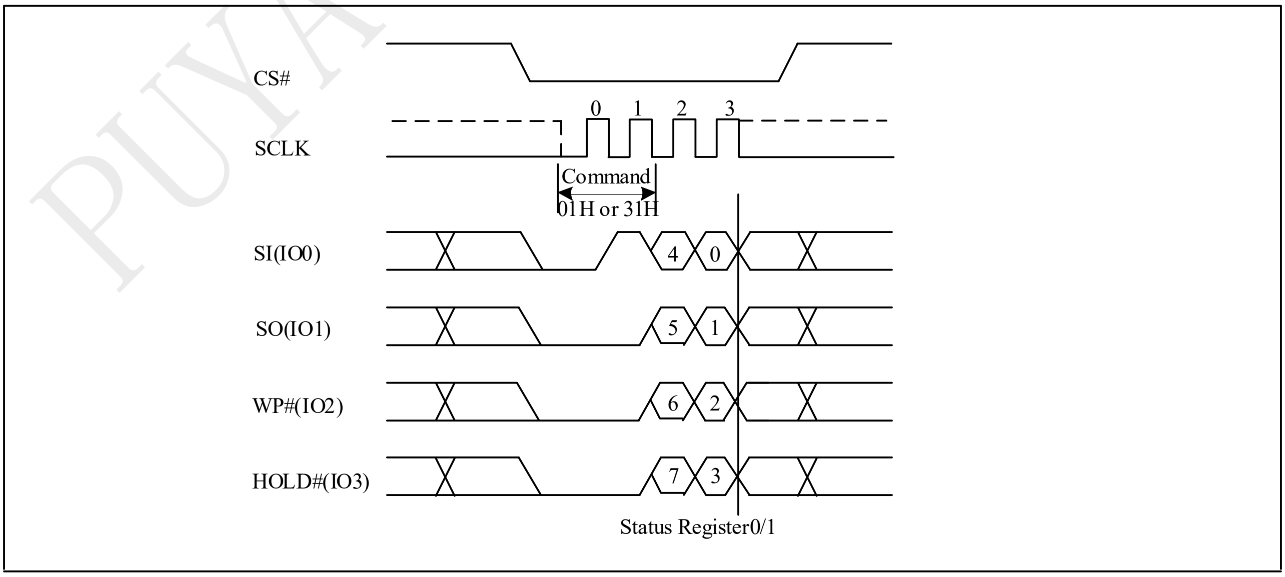


Figure 10-7a Write Status Register (WRSR) Sequence (QPI)



To be backward compatible to Puya's previous serial flash product, The Write Status Register (WRSR) command also support to write Status Register-0 and Status Register-1 in same time. To complete this function, CS# must be driven high after the sixteenth bit of the data byte has been latched in. If CS# is driven high after the eighth clock, the Write Status Register (01h) command will only program the Status Register-0, the Status Register-1 will not be affected (Previous product will clear CMP and QE bits).

Figure 10-7b Write Status Register (WRSR) with 2 Byte data Sequence (SPI)

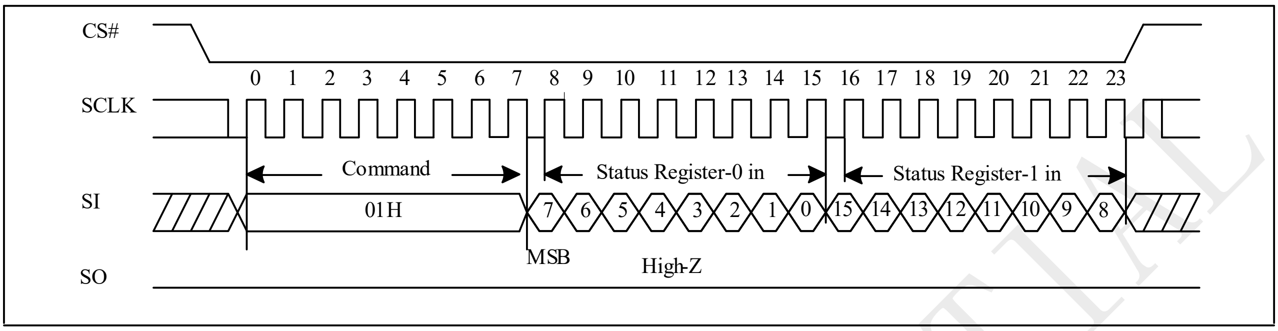
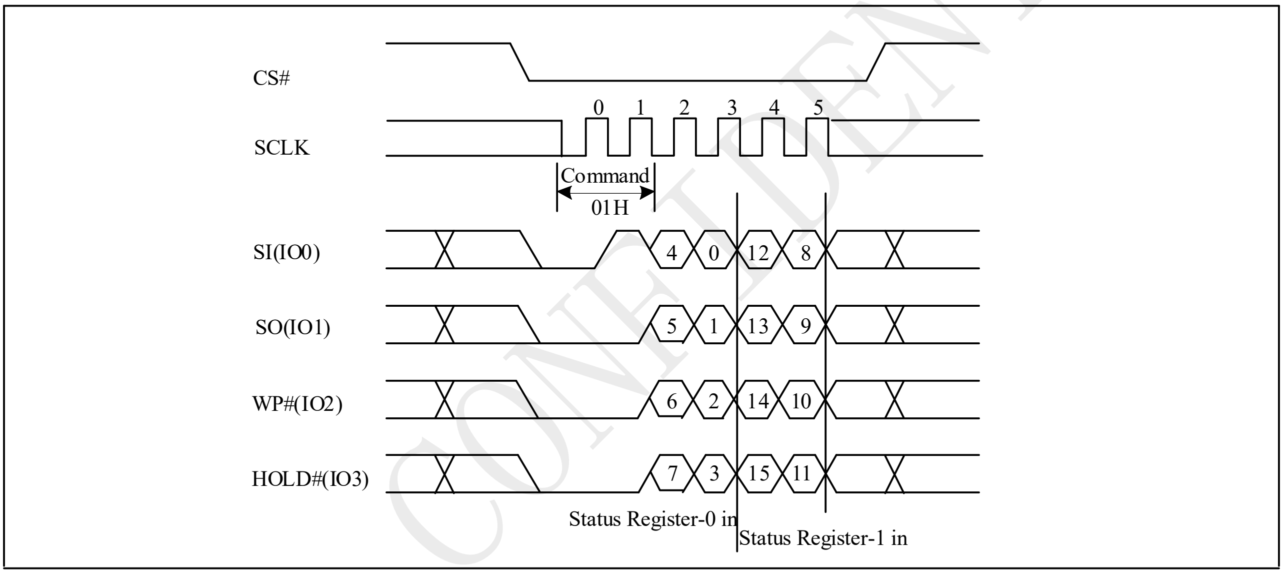


Figure 10-7c Write Status Register (WRSR) with 2 Byte data Sequence (QPI)



10.8 Write Configure Register (WRCR)

The Write Configure Register (WRCR) command allows new values to be written to the Configure Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The sequence of issuing WRCR instruction is: CS# goes low→ sending WRCR instruction code→ Configure Register data on SI→CS# goes high.

The CS# must go high exactly at the 8 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Configure Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 10-8 Write Configure Register (WRCR) Sequence (Command 11)

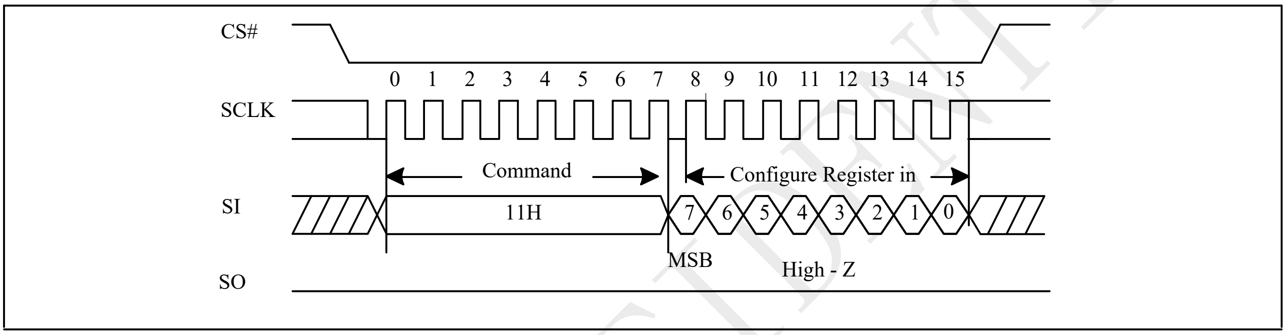
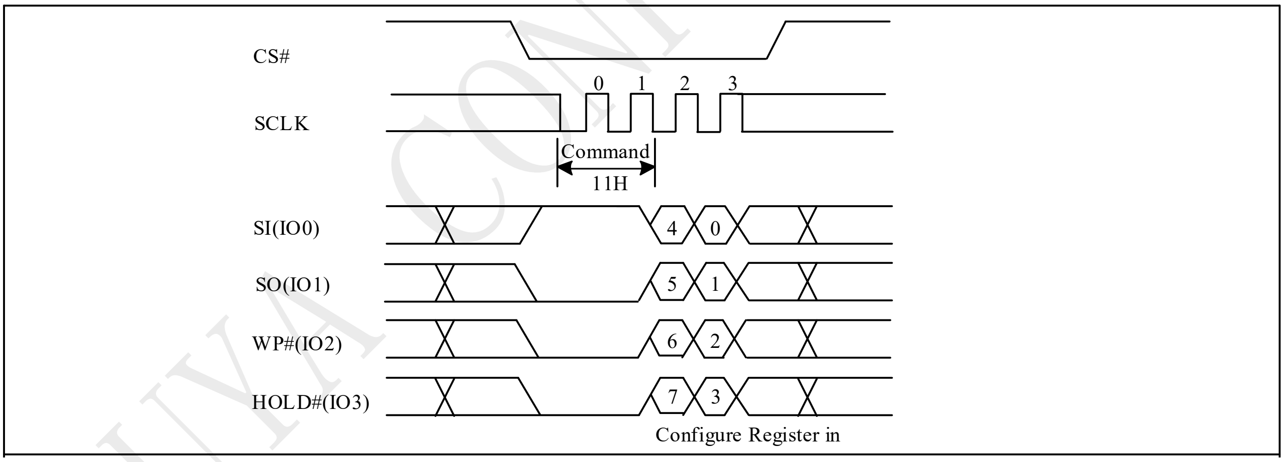


Figure 10-8a Write Configure Register (WRCR) Sequence (QPI)

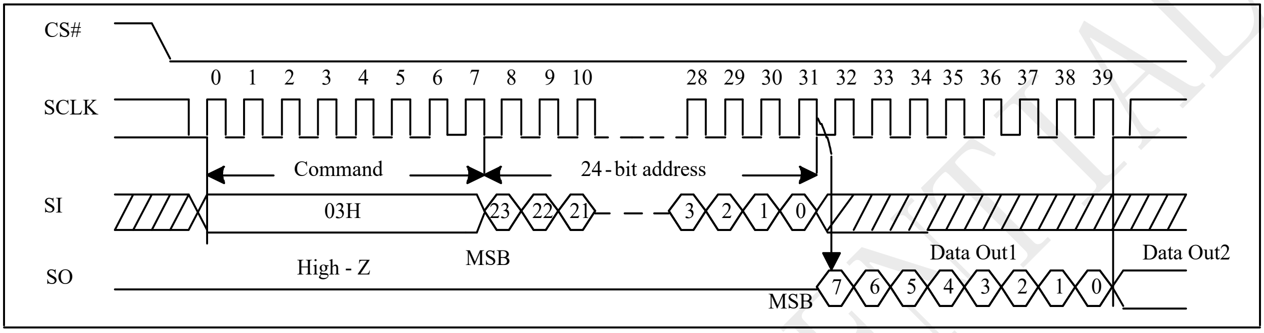


10.9 Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→ sending READ instruction code→ 3-byte address on SI→ data out on SO→ to end READ operation can use CS# to high at any time during data out.

Figure 10-9 Read Data Bytes (READ) Sequence (Command 03)



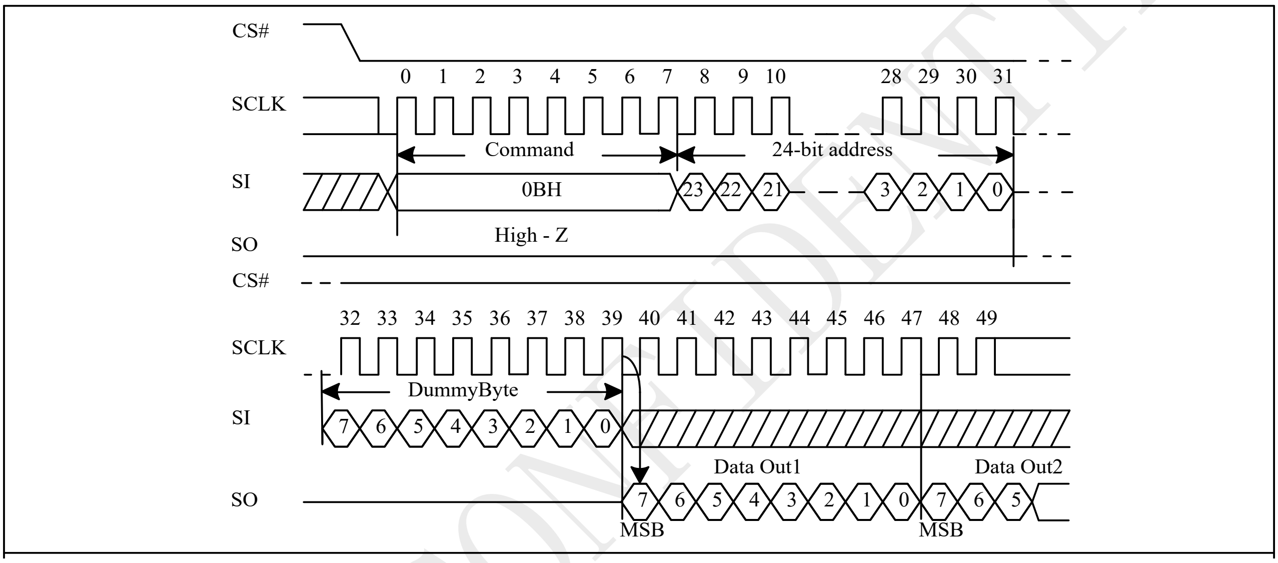
10.10 Fast Read (FREAD)

The FAST READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FREAD instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FREAD instruction is: CS# goes low→ sending FREAD instruction code→3-byte address on SI→ 1-dummy byte address on SI→data out on SO→ to end FREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, FREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

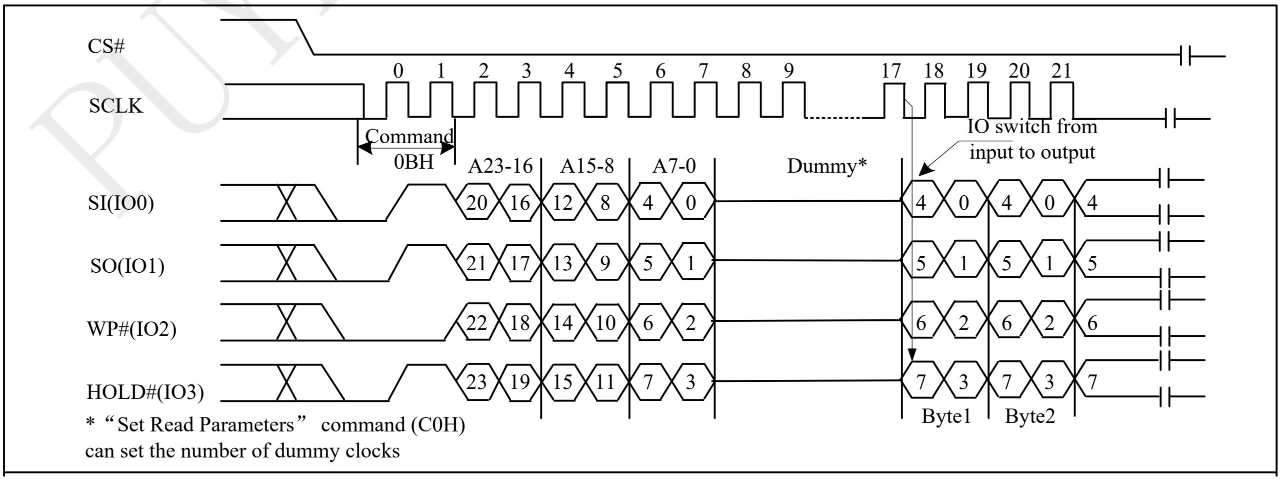
Figure 10-10 Fast Read (FREAD) Sequence (Command 0B)



Fast Read in QPI mode

The Fast Read command is also supported in QPI mode. In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured.

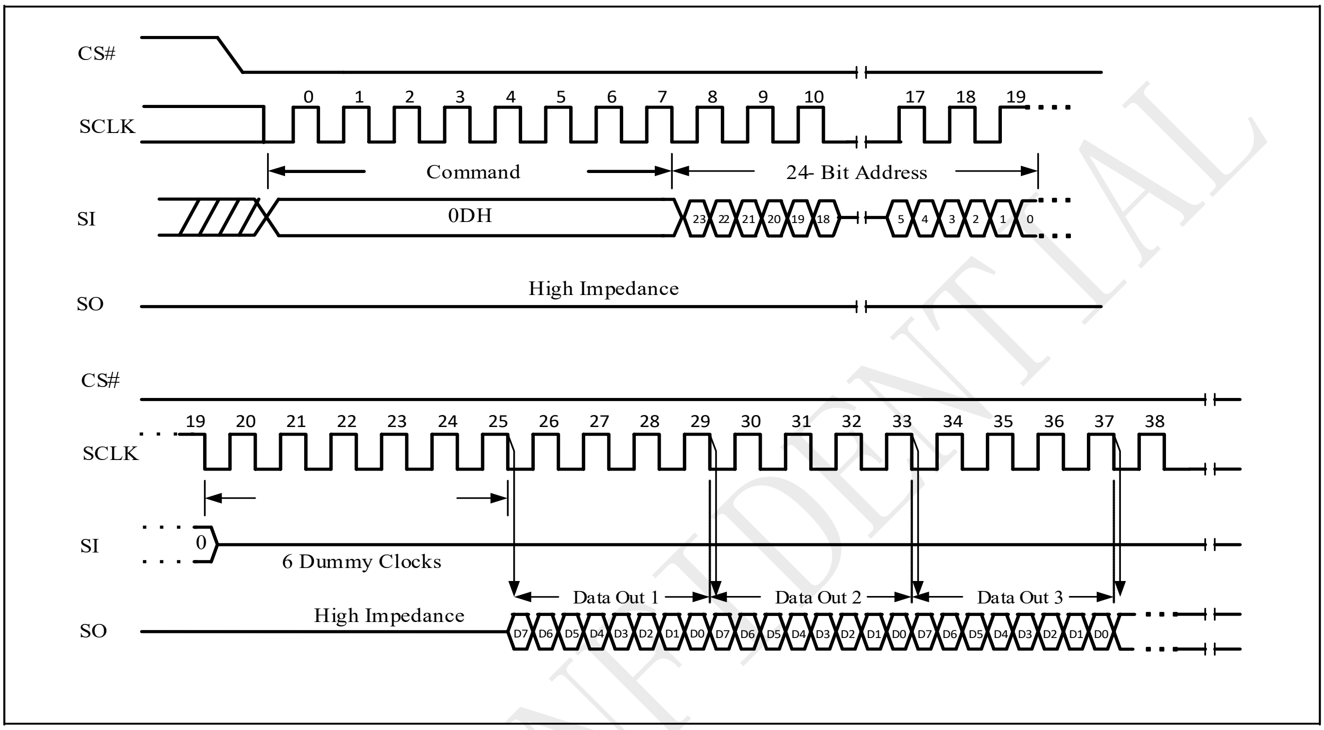
Figure 10-10a Fast Read Sequence (QPI)



10.11 DTR Fast Read(DTR_FREAD)

The DTR Fast Read instruction is similar to the Fast Read instruction except that the 24-bit address input and the data output require DTR (Double Transfer Rate) operation. This is accomplished by adding six “dummy” clocks after the 24-bit address. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a “don’t care”.

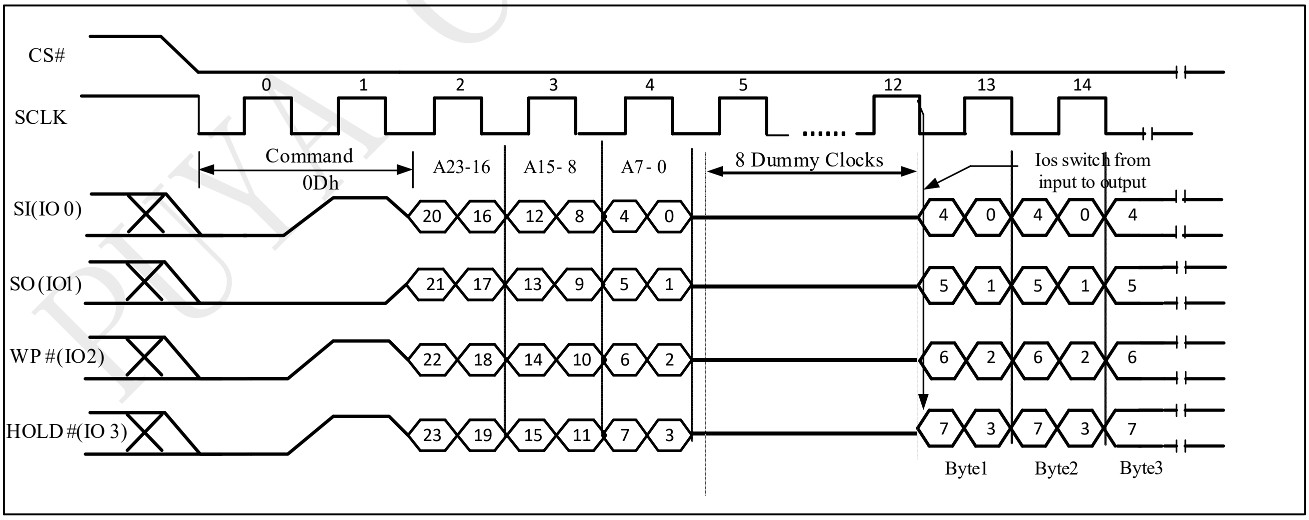
Figure 10-11 DTR Fast Read Sequence (Command 0D)



DTR Fast Read in QPI Mode

The DTR Fast Read instruction is also supported in QPI mode.

Figure 10-11a DTR Fast Read Sequence (QPI)



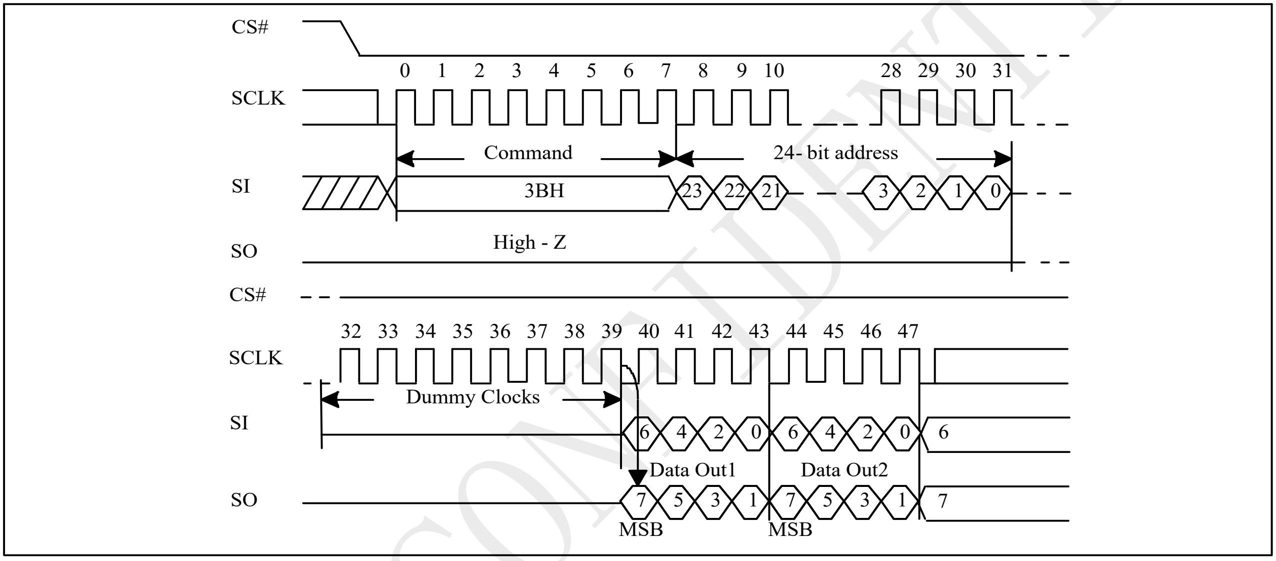
10.12 Dual Read (DREAD)

The DREAD instruction enable double throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low → sending DREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SIO1 & SIO0 → to end DREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 10-12 Dual Read Mode Sequence (Command 3B)



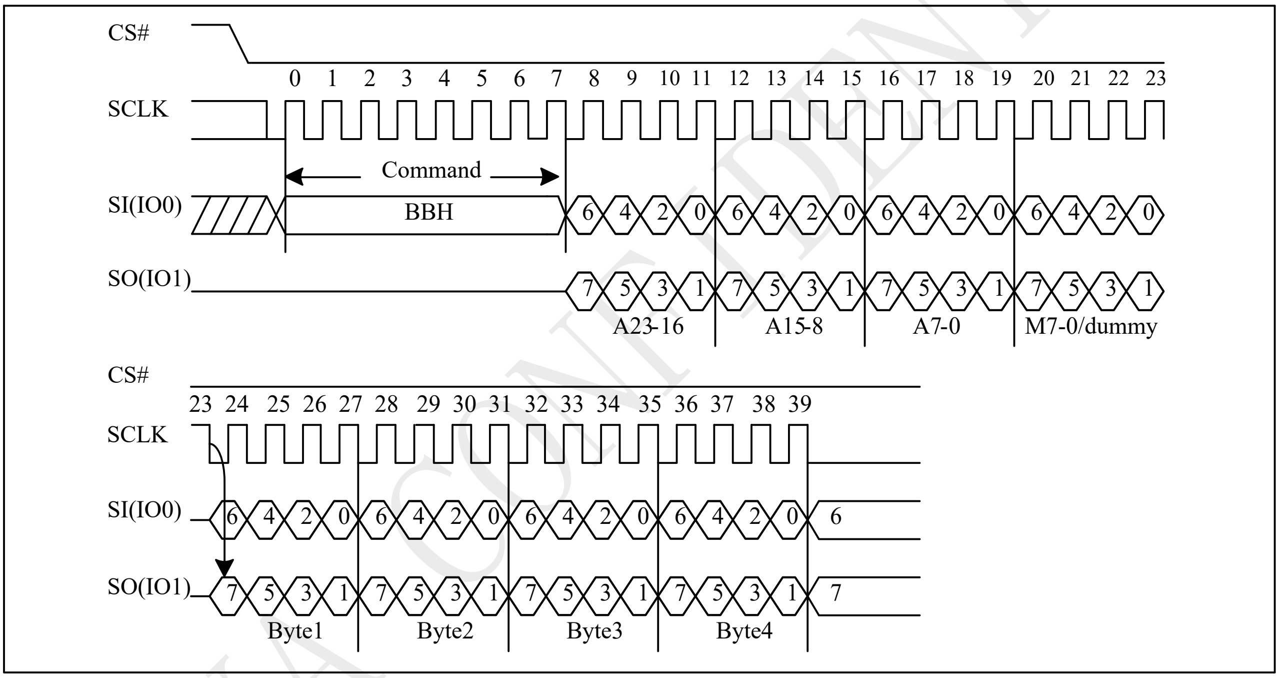
10.13 2IO Read (2READ)

The 2READ instruction enables Double Transfer Rate of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→ 8-bit dummy cycle on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 10-13 2IO Read Sequence (Command BB M5-4 ≠ (1,0))



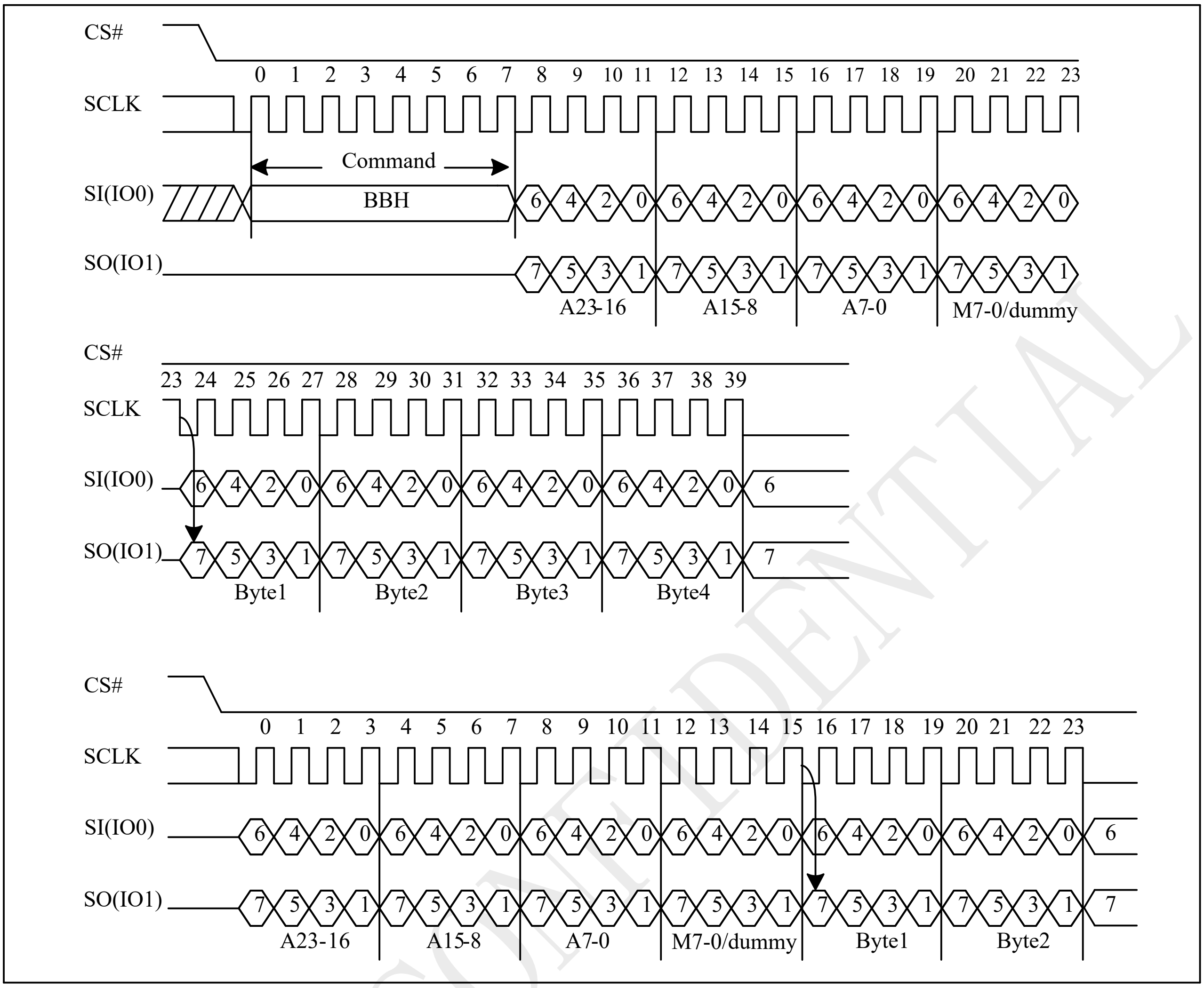
Note:
1. M[5-4] = (1,0) is inhibited.
2. DC bit can set the number of dummy clocks.

2IO Continuous Read

“BBh” command supports 2IO Continuous Read which can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next 2IO Read command (after CS# is raised and then lowered) does not require the BBH command code.

If the “Continuous Read Mode” bits (M5-4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5-4) before issuing normal command.

Figure 10-13a 2IO Continue Read (M5-4 = (1,0))



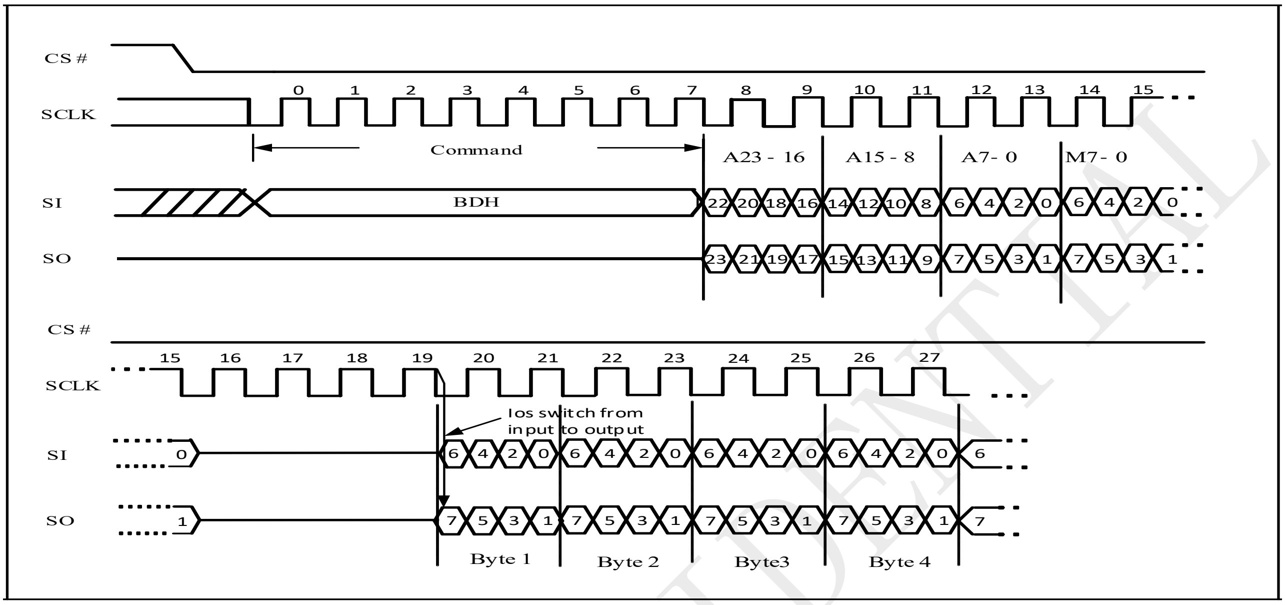
Note:

1. 2IO Continue Read, if M5-4 = 1, 0. If not using Continue Read recommend to set M5-4 ≠ 1, 0.
2. DC bit can set the number of dummy clocks.

10.14 DTR 2IO Read (DTR_2READ)

The DTR 2IO Read (BDh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the DREAD (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Figure 10-14 DTR 2IO Read Sequence (Command BD M5-4 ≠ (1,0))

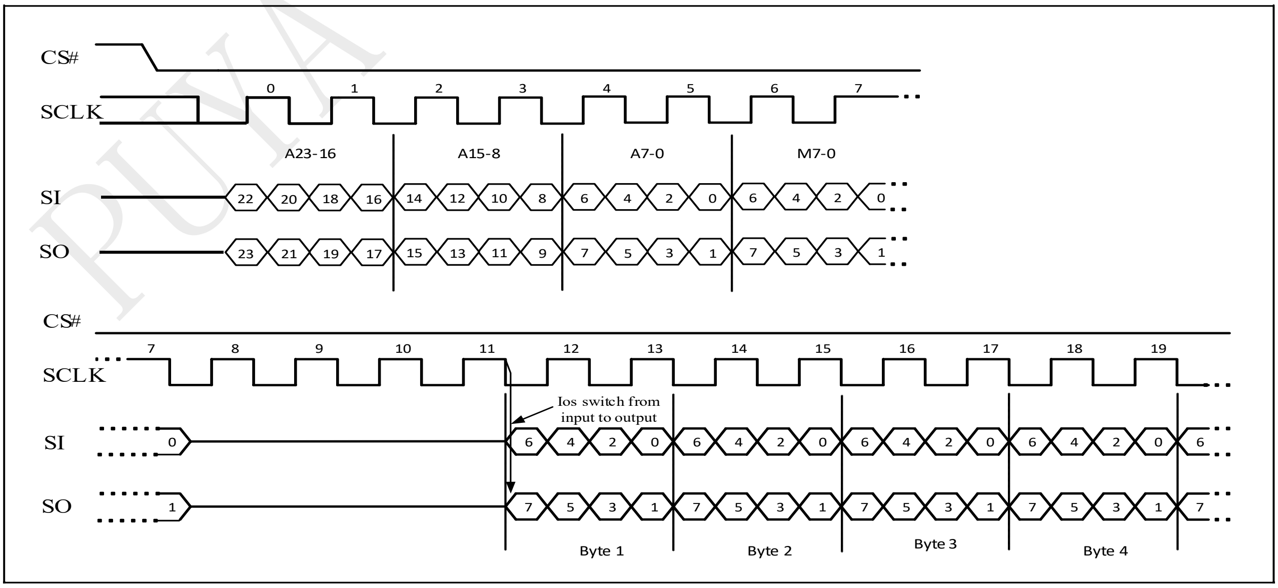


DTR 2IO Continuous Read

The BDh instruction supports Continuous Read Mode which can further reduce overhead through setting the "continuous Read Mode" bits(M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Read command (after CS# is raised and then lowered) does not require the BDH command code.

If the “Continuous Read Mode” bits (M5-4) do not equal (1, 0), the next command requires the first BDH command code, thus returning to normal operation. It is recommended to input FFFFh on IO0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

Figure 10-14a DTR 2IO Continuous Read Sequence (Command BD M5-4 = (1,0))



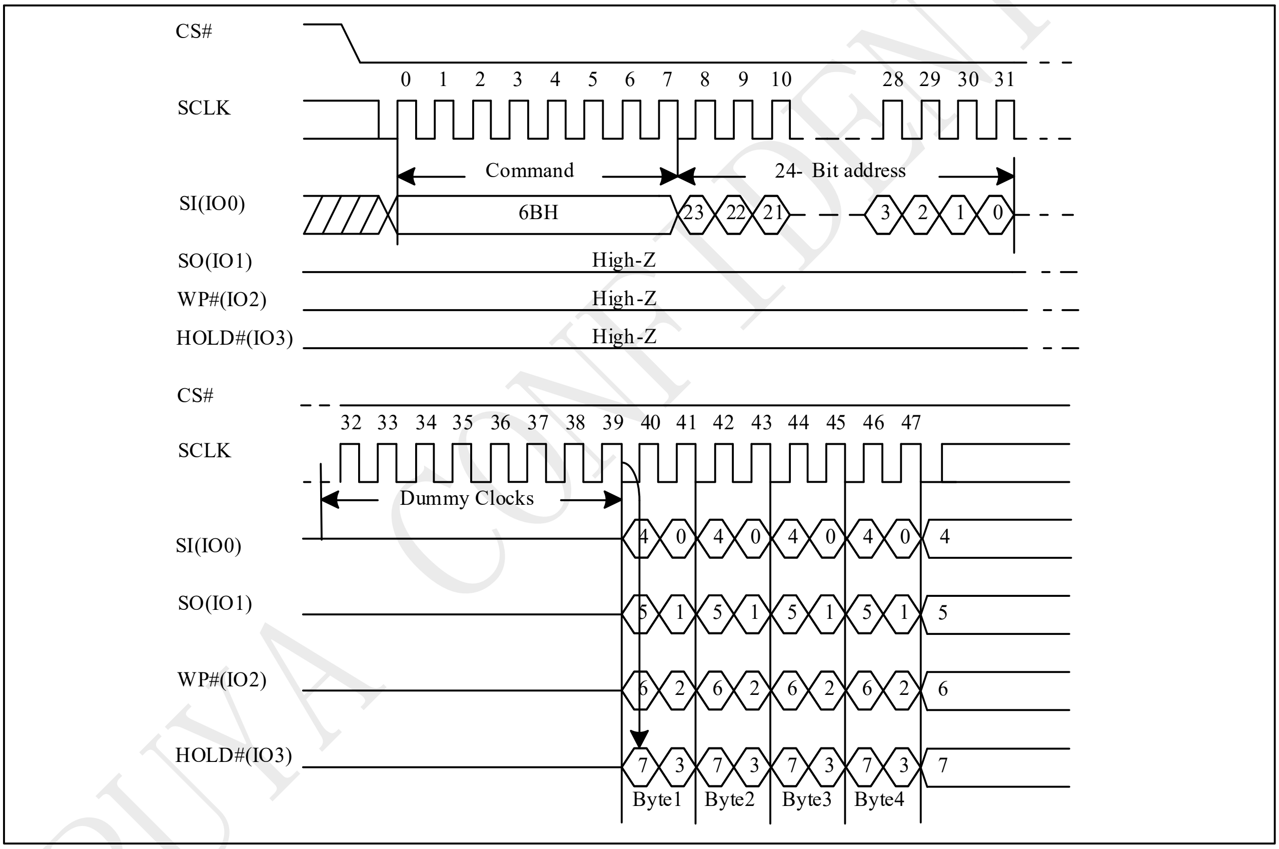
10.15 Quad Read (QREAD)

The QREAD instruction enable quad throughput of Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the QREAD instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing QREAD instruction is: CS# goes low→ sending QREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 10-15 Quad Read Sequence (Command 6B)



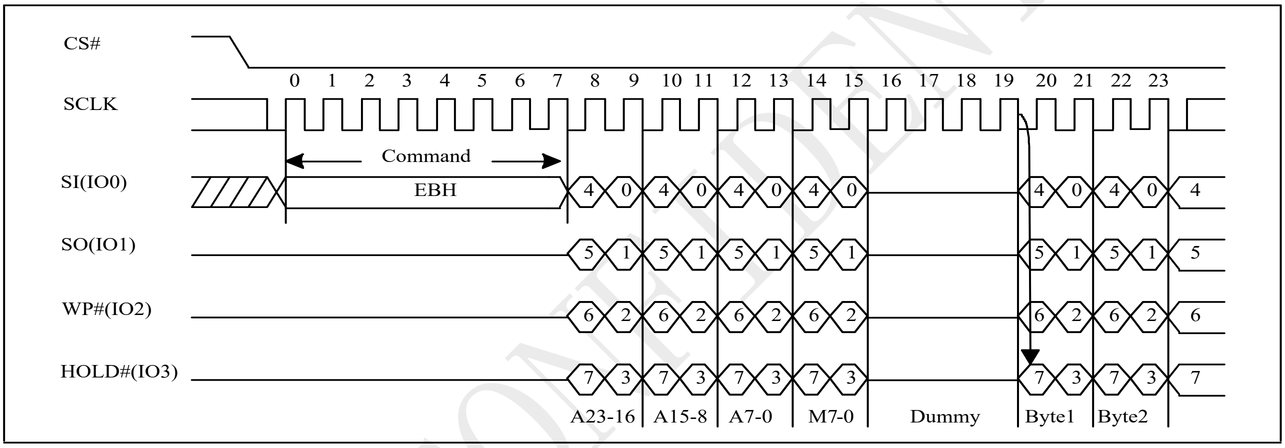
10.16 4IO Read (4READ)

The 4READ instruction enable quad throughput of Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→2+4 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 10-16 4IO Read Sequence (Command EB M5-4 ≠ (1,0))



Note:
1. Hi-impedance is inhibited for the two clock cycles.
2. M[5-4] = (1,0) is inhibited.
3. DC bit can set the number of dummy clocks.

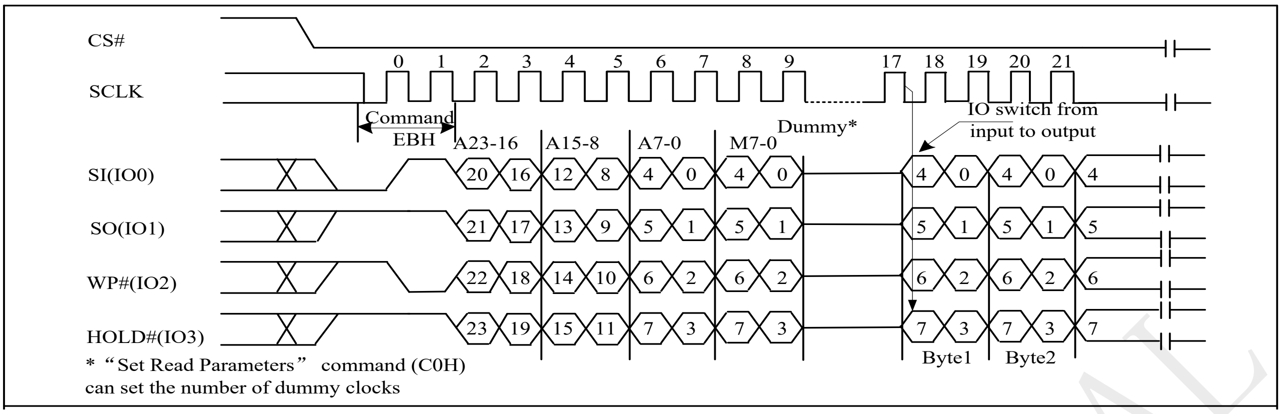
4IO Read in QPI mode

The 4READ instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 10, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 10. In QPI mode, the “Continuous Read Mode” bits M7- 0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

“Continuous Read Mode” feature is also available in QPI mode for 4IO Read instruction. Please refer to the description on next pages.

“Wrap Around” feature is not available in QPI mode for 4IO Read instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated “Burst Read with Wrap” (0Ch) instruction must be used.

Figure 10-16a 4IO Read in QPI mode Sequence (QPI M5-4 ≠ (1,0))



Note:

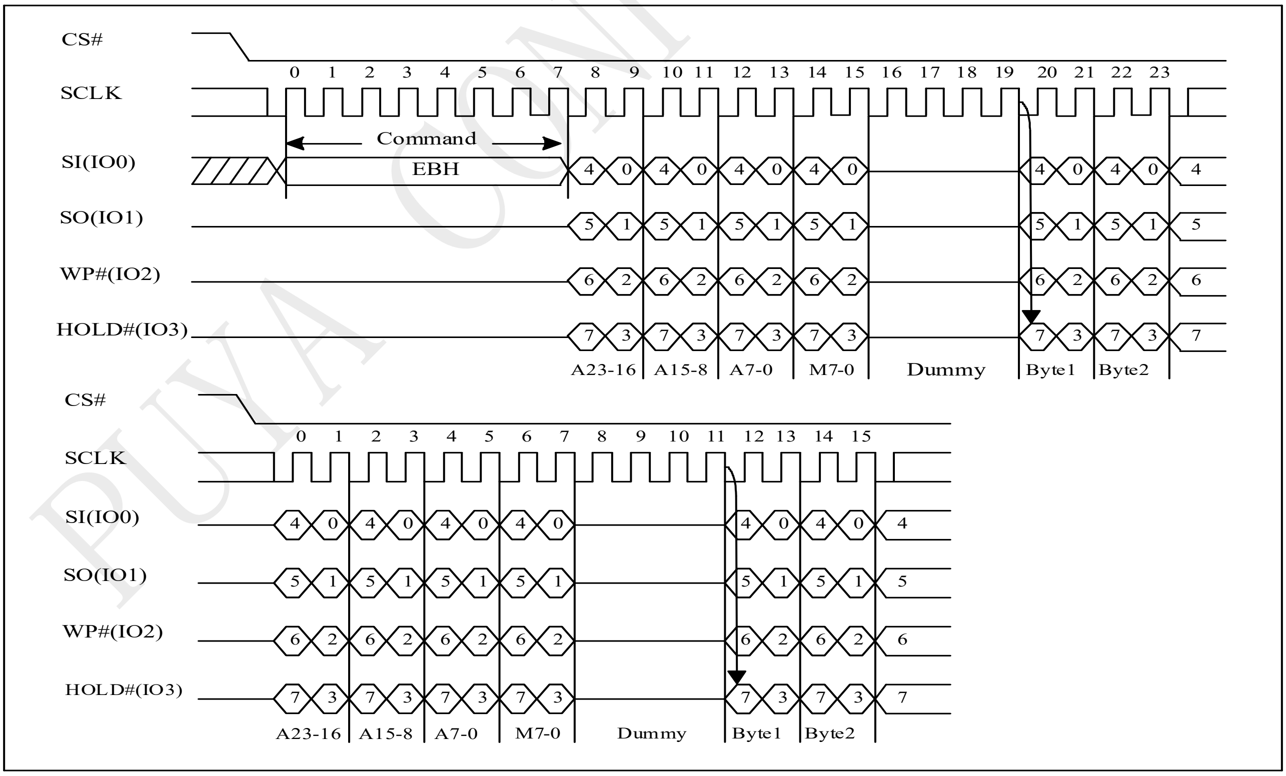
1. Hi-impedance is inhibited for the two clock cycles.
2. M[5-4] = (1,0) is inhibited.

4IO Continuous Read

"EBh" command supports 4IO Continuous Read which can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next 4IO Read command (after CS# is raised and then lowered) does not require the EBH command code.

If the "Continuous Read Mode" bits (M5-4) do not equal (1, 0), the next command requires the first EBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5-4) before issuing normal command.

Figure 10-16b 4IO Continuous Read Sequence (M5-4 = (1,0))



Note:

1. 4IO Continuous Read Mode, if M5-4 = 1, 0. If not using Continuous Read recommend to set M5-4 ≠ 1, 0.
2. DC bit can set the number of dummy clocks.

10.17 Set Burst Read

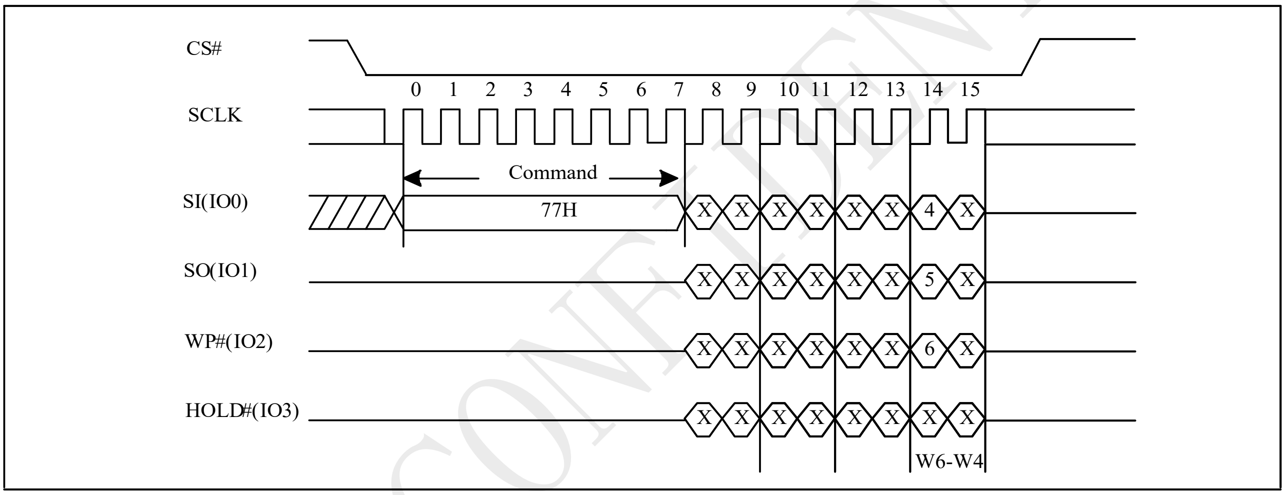
The Set Burst with Wrap command is used in conjunction with “4IO Read” command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap command sequence: CS# goes low → Send Set Burst with Wrap command → Send 24 dummy bits→ Send 8 bits “Wrap bits” → CS# goes high.

W6,W5	W4=0		W4=1 (default)	
	Wrap Aroud	Wrap Length	Wrap Aroud	Wrap Length
0,0	Yes	8-byte	No	N/A
0,1	Yes	16-byte	No	N/A
1,0	Yes	32-byte	No	N/A
1,1	Yes	64-byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following “4IO Read” command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

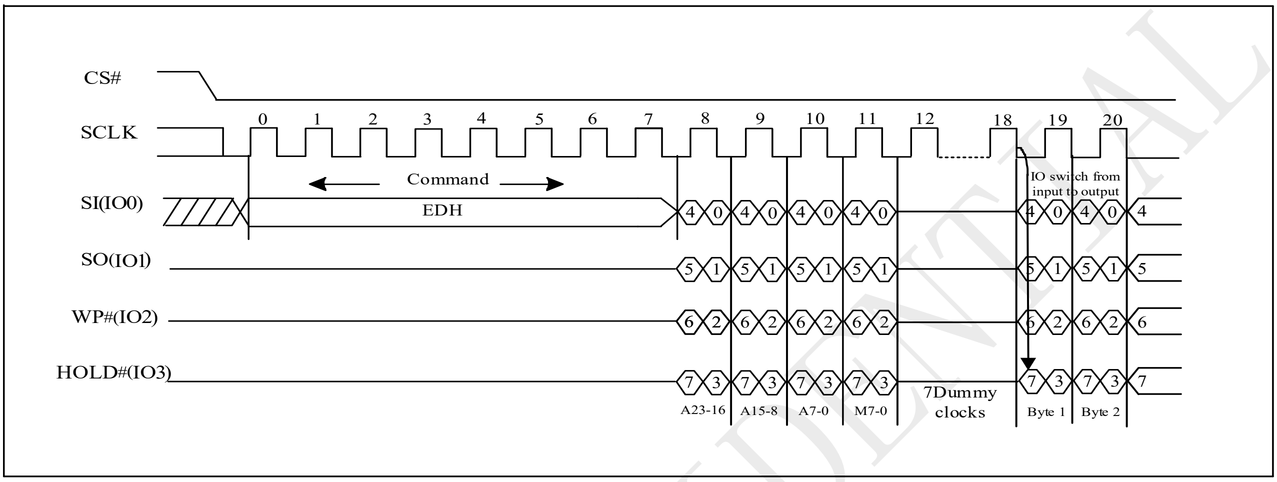
Figure 10-17 Set Burst Read (SBL) Sequence (Command 77)



10.18 DTR 4IO Read (DTR_4READ)

The DTR 4IO Read (EDh) instruction is similar to the DTR 2IO Read (BDh) instruction, except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3, and 1 byte "Continuous Read Mode" data(M7-0) and 7 Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the DTR 4IO Read Instruction.

Figure 10-18 DTR 4IO Read Mode Sequence (Command ED M5-4 ≠ (1,0)



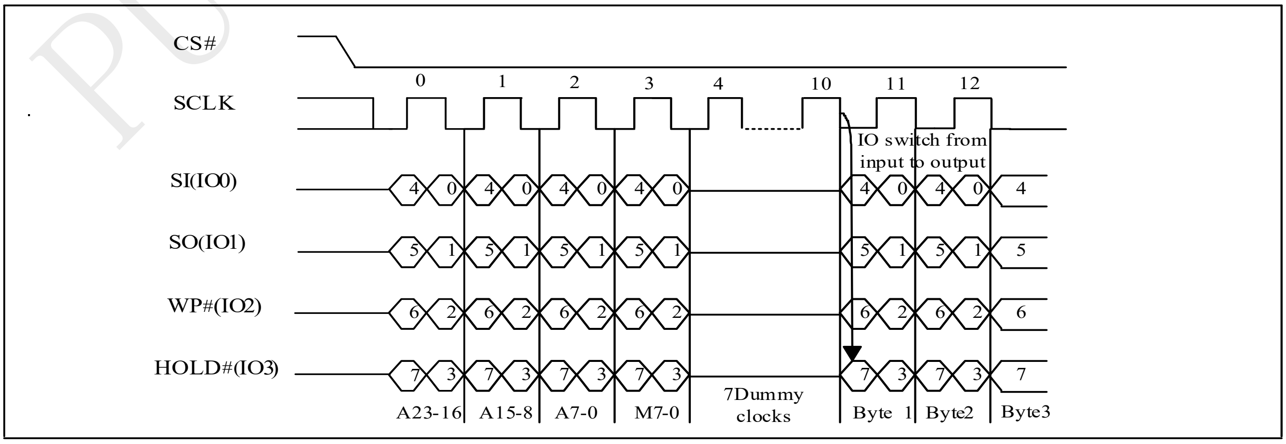
Note: Hi-impedance is inhibited for the mode clock cycles. 2. M[5-4] = (1,0) is inhibited.

DTR 4IO Continuous Read

The DTR 4IO Read instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23/A31-0). The upper nibble of the (M7-4) controls the length of the next DTR 4IO Read instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next DTR 4IO Read instruction (after /CS is raised and then lowered) does not require the EDh instruction code. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

Figure 10-18a DTR 4IO Continuous Read Mode Sequence (Command ED M5-4 = (1,0))



Note:
1. Hi-impedance is inhibited for the mode clock cycles.
2. DTR 4IO Continuous Read Mode, if M5-4 = 1, 0. If not using Continuous Read recommend to set M5-4 ≠ 1, 0.

DTR 4IO Read with “8/16/32/64-Byte Wrap Around” in Standard SPI mode

The DTR 4IO Read instruction can also be used to access a specific portion within a page by issuing a “Set Burst Read” (77h) command prior to EDh. The “Set Burst Read” (77h) command can either enable or disable the “Wrap Around” feature for the following EDh commands. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The “Set Burst Read” instruction allows three “Wrap Bits”, W6-4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-5 is used to specify the length of the wrap around section within a page.

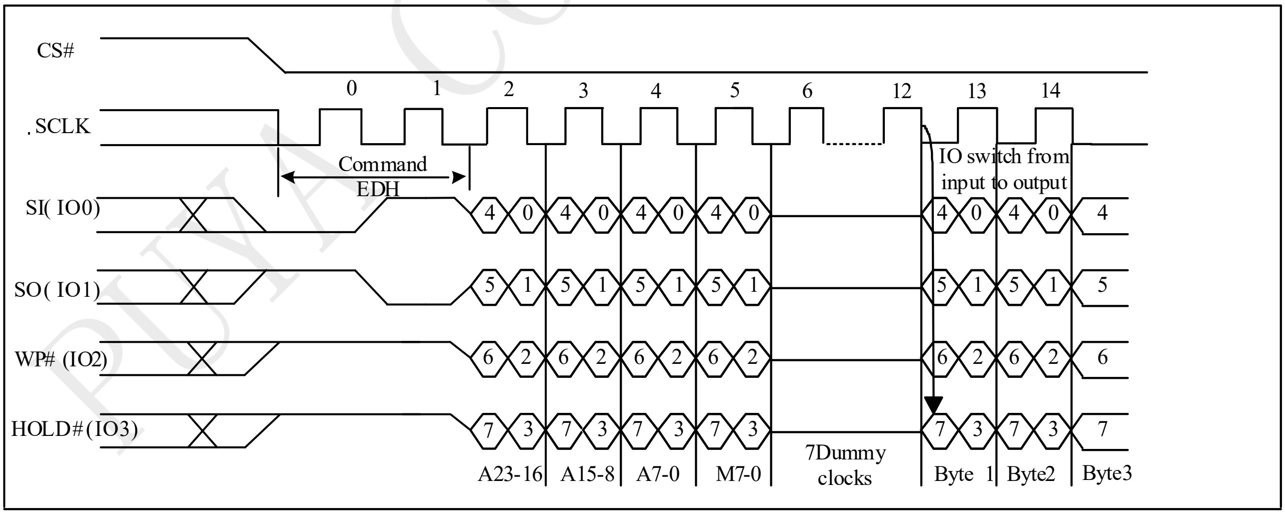
DTR 4IO Read (EDh) in QPI Mode

The DTR 4IO Read instruction is also supported in QPI mode. In QPI mode, the “Continuous Read Mode” bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

“Continuous Read Mode” feature is also available in QPI mode for Fast Read Quad I/O instruction.

“Wrap Around” feature is not available in QPI mode for DTR 4IO Read instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated “Burst Read with Wrap” (0Ch) instruction must be used.

Figure 10-18b DTR 4IO Read Mode Sequence (QPI ED M5-4 ≠ (1,0))

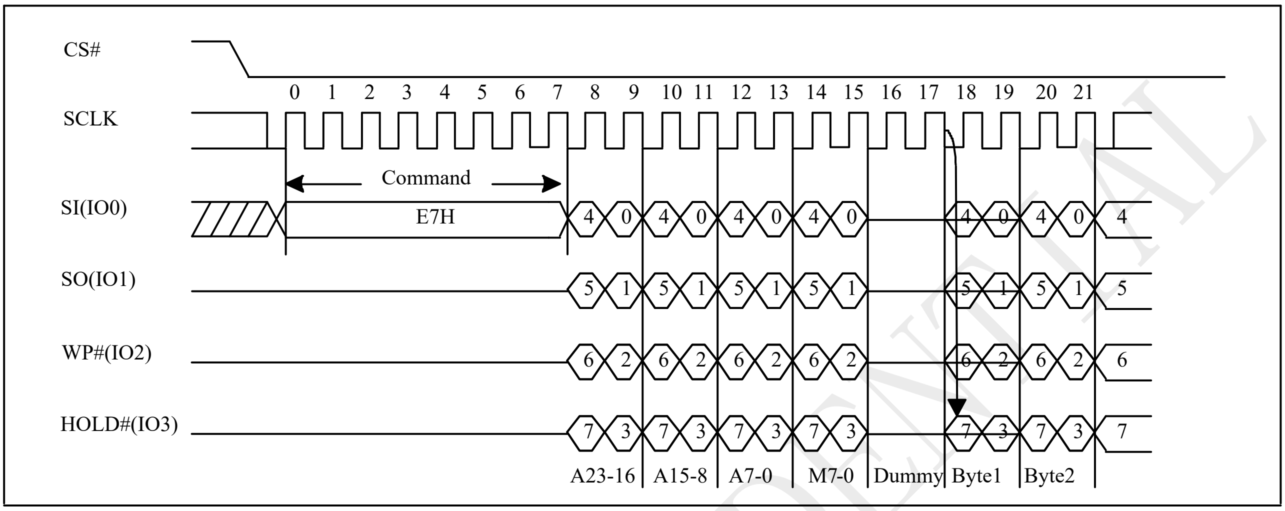


Note:
1. Hi-impedance is inhibited for the two clock cycles.
2. M[5-4] = (1,0) is inhibited.

10.19 4IO Word Read(E7h)

The 4IO Word Read command is similar to the 4 IO Read command except that the lowest address bit (A0) must equal 0 and only 2-dummy clock. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the 4IO Word read command.

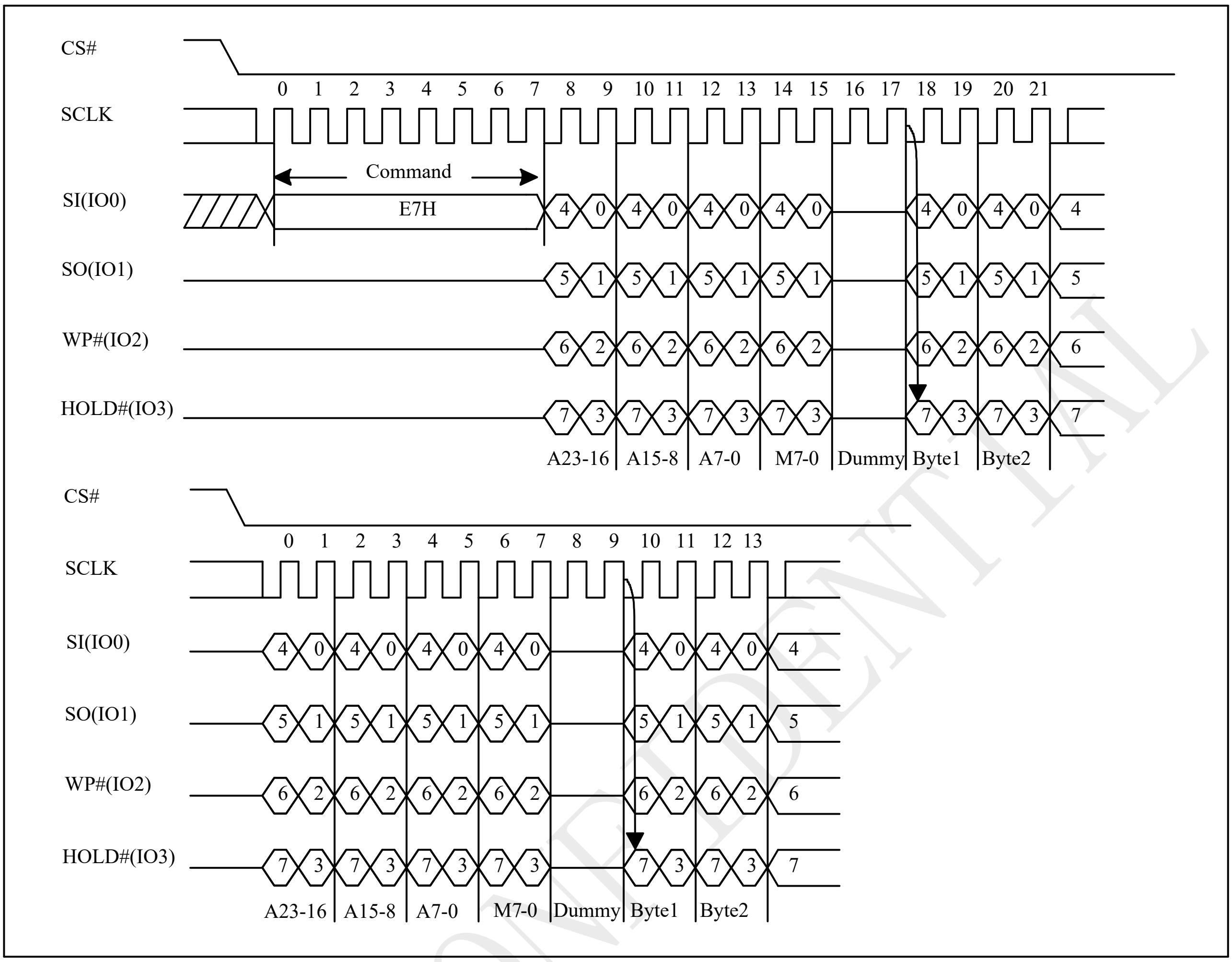
Figure 10-19 4IO Word Read Sequence (M5-4 ≠ (1,0))



4IO Word Read with "Continuous Read Mode"

The 4IO Word Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next 4IO Word Read command (after CS# is raised and then lowered) does not require the E7H command code. If the "Continuous Read Mode" bits (M5-4) do not equal to (1, 0), the next command requires the first E7H command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5-4) before issuing normal command.

Figure 10-19a 4IO Word Read Sequence (M5-4 = (1,0))



4IO Word Read with “8/16/32/64-Byte Wrap Around” in Standard SPI mode

The 4IO Word Read command can be used to access a specific portion within a page by issuing “Set Burst with Wrap”(77H) commands prior to E7H. The “Set Burst with Wrap”(77H) command can either enable or disable the “Wrap Around” feature for the following E7H commands. When “Wrap Around” is enabled, the data being accessed can be limited to either an8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The “Set Burst with Wrap” command allows three “Wrap Bits”W6-W4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-W5 is used to specify the length of the wrap around section within a page.

10.20 Set Read Parameters (C0h)

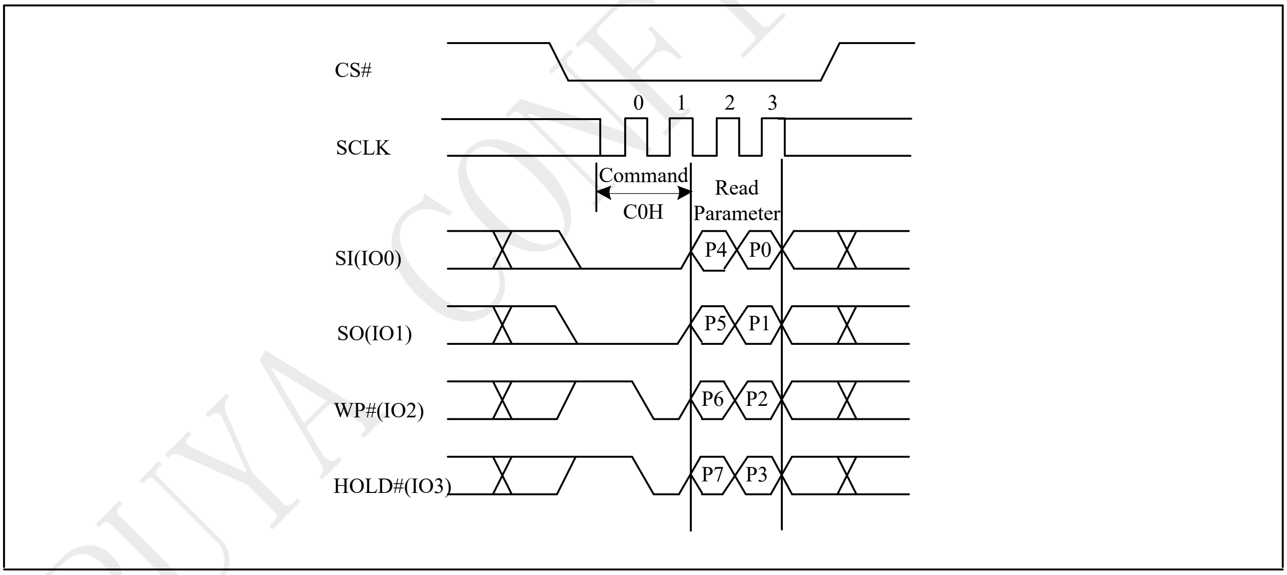
In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0h)” instruction can be used to configure the number of dummy clocks for “Fast Read (0Bh)”, “4IO Read (EBh)” , “Burst Read with Wrap (0Ch)” , “Buffer Read (9Bh)” & “Read SFDP Mode (5Ah)” instructions, and to configure the number of bytes of “Wrap Length” for the “Burst Read with Wrap (0Ch)” instruction.

In Standard SPI mode, the “Set Read Parameters (C0h)” instruction is not accepted. The dummy clocks for various Fast Read instructions in Dual/Quad SPI mode are configured by DC bit. The “Wrap Length” is set by W5-4 bit in the “Set Burst with Wrap (77h)” instruction. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

The default “Wrap Length” after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 10 which includes “Continuous Read Mode” byte M7-0. The number of dummy clocks is only programmable for “Fast Read (0Bh)”, “4IO Read (EBh)” & “Burst Read with Wrap (0Ch)” instructions in the QPI mode. Whenever the device is switched from SPI mode to QPI mode, the number of dummy clocks should be set again, prior to any 0Bh, EBh or 0Ch instructions.

P5-P4	Dummy Clocks	P1-P0	Wrap Length
0,0	10	0,0	8-byte
0,1	4	0,1	16-byte
1,0	6	1,0	32-byte
1,1	8	1,1	64-byte

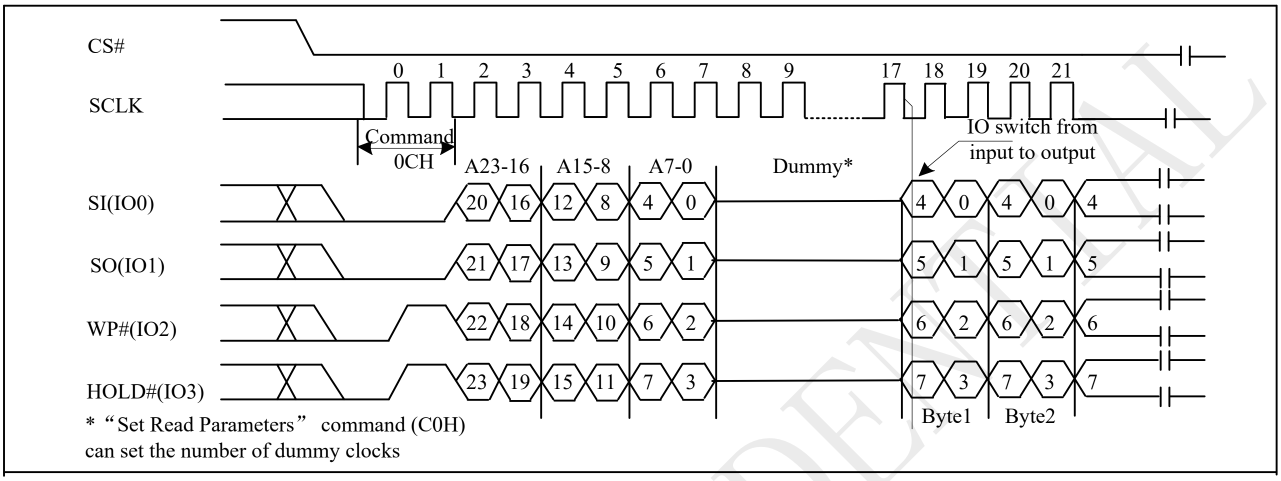
Figure 10-20 Set Read Parameters Sequence (QPI)



10.21 Burst Read with Wrap (0Ch)

The “Burst Read with Wrap (0CH)” command provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. This command is similar to the “Fast Read (0BH)” command in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Around” once the ending boundary is reached. The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0H)” command.

Figure 10-21 Burst Read with Wrap Sequence (QPI)

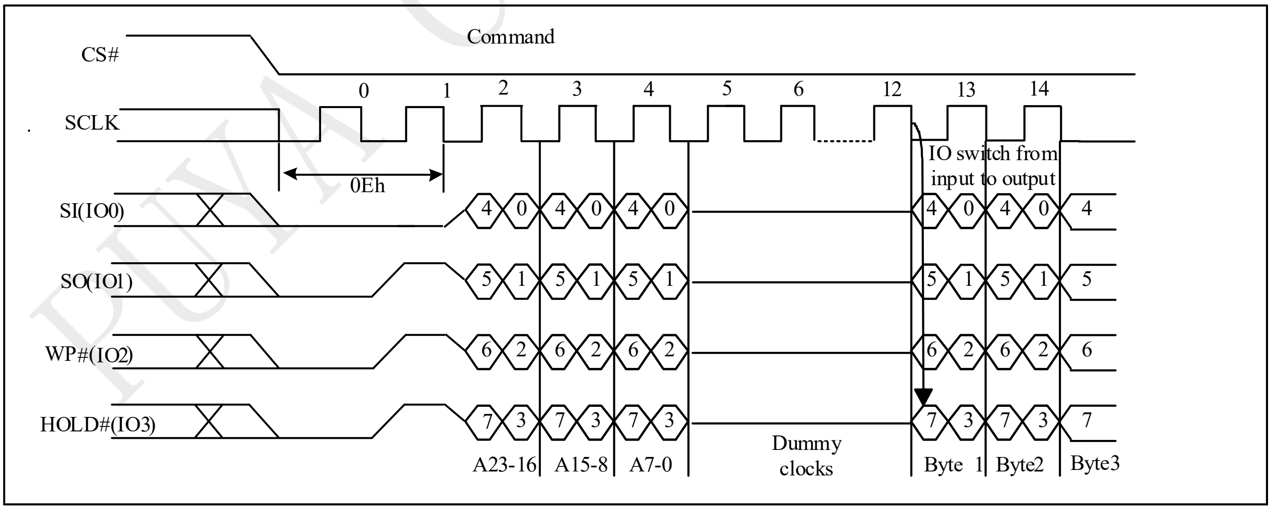


* “Set Read Parameters” command (C0H) can set the number of dummy clocks

10.22 DTR Burst Read with Wrap (0Eh)

The “DTR Burst Read with Wrap (0EH)” command provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. This command is similar to the “Fast Read (0BH)” command in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Around” once the ending boundary is reached. The “Wrap Length” can be configured by the “Set Read Parameters (C0H)” command.

Figure 10-22 Burst Read with Wrap Sequence (QPI)



10.23 Data Learning Pattern

The data learning pattern supports system/memory controller determine valid window of data output more easily and improve data capture reliability while the flash memory is running in high frequency.

Data learning pattern can be enabled or disabled by setting the bit0 of Configure Register (data learning pattern enable bit). Once the DLP bit is set, the data learning pattern is inputted into dummy cycles.

Enabling data learning pattern bit (DLP bit) will not affect the function of continue read mode bit. In dummy cycles, continuous mode bit still operates with the same function. Data learning pattern will output after continuous mode bit.

The data learning pattern is a fixed 8-bit data pattern (00110100). For STR (single transfer rate) instructions, the complete 8 bits will start to output right after the continuous mode bit. While dummy cycle is not sufficient of 8 cycles, the rest of the DLP bits will be cut. For DTR (double transfer rate) instructions, the complete 8 bits will start to output during the last 4 dummy cycle.

Figure 10-23 Fast Read with DLP bits output Sequence

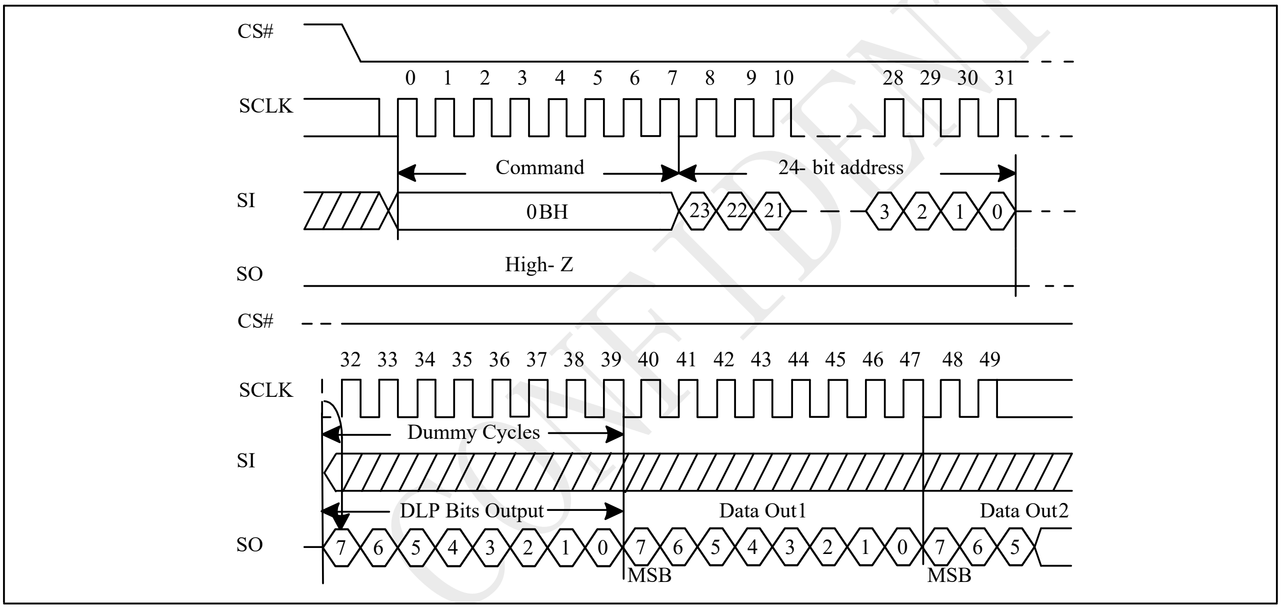


Figure 10-23a Dual Read with DLP bits output Sequence

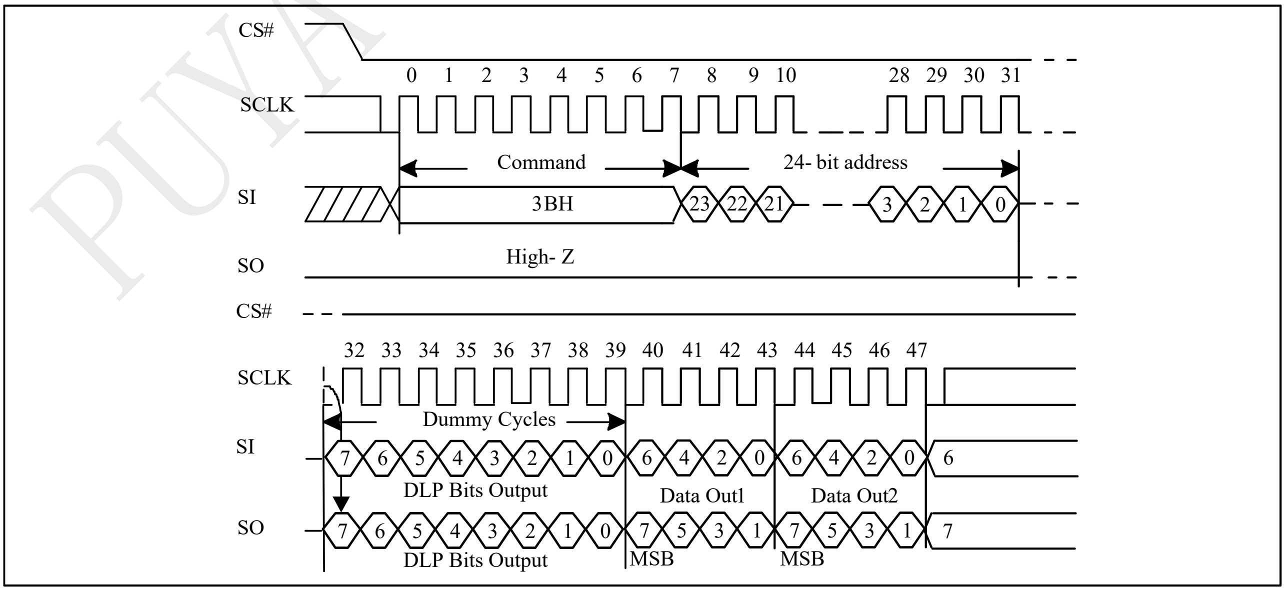


Figure 10-23b Quad Read with DLP bits output Sequence

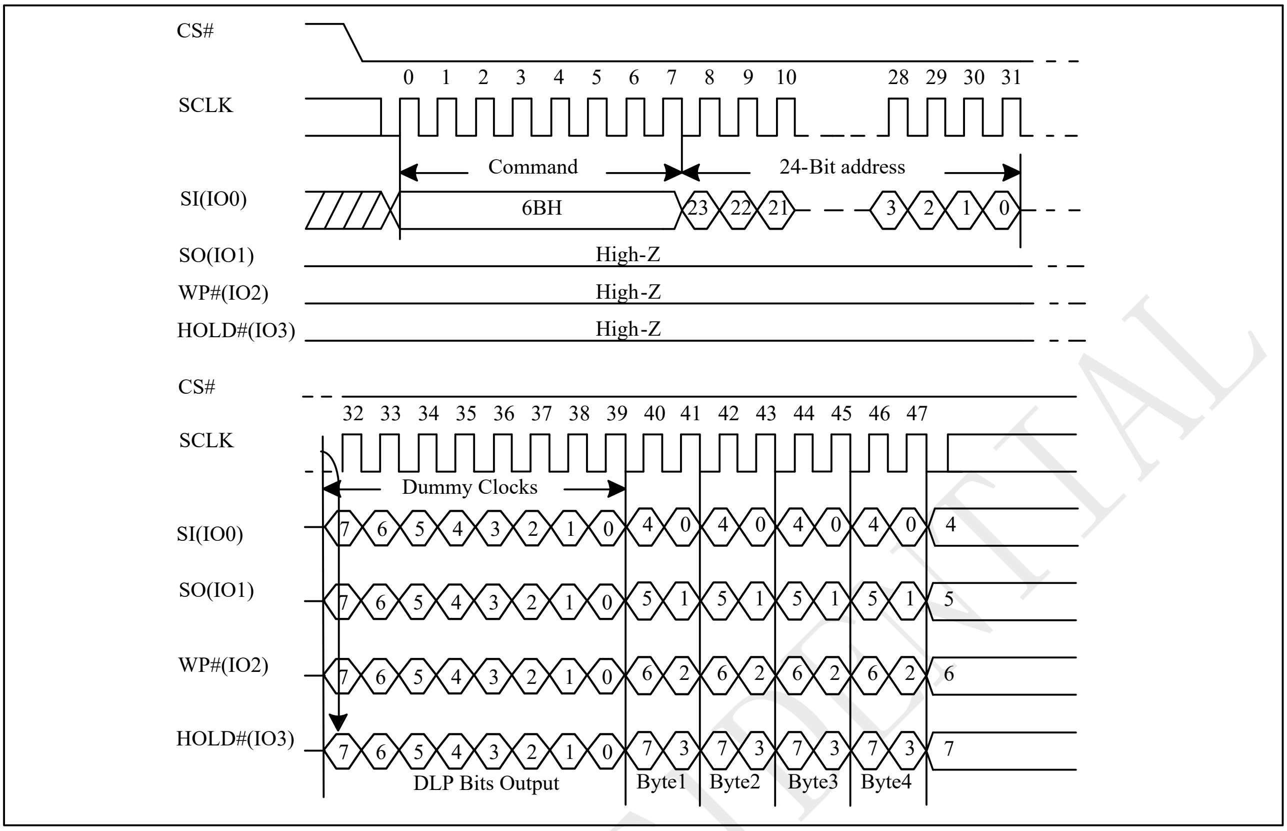


Figure 10-23c 4IO Read and Burst Read with DLP bits output Sequence

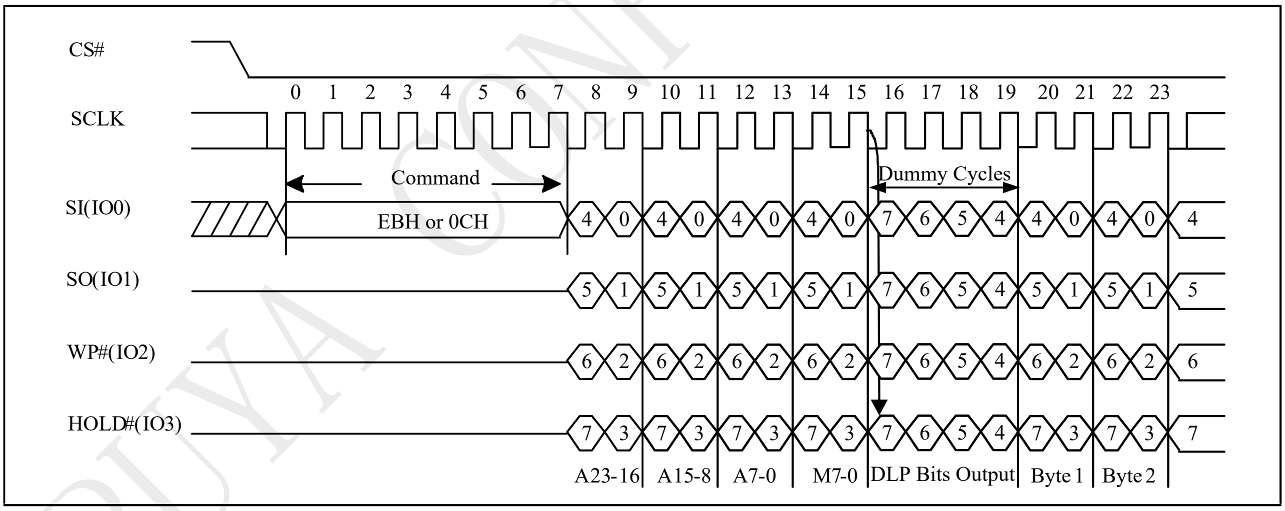


Figure 10-23d 4IO Read and Burst Read with DLP bits output Sequence in QPI mode

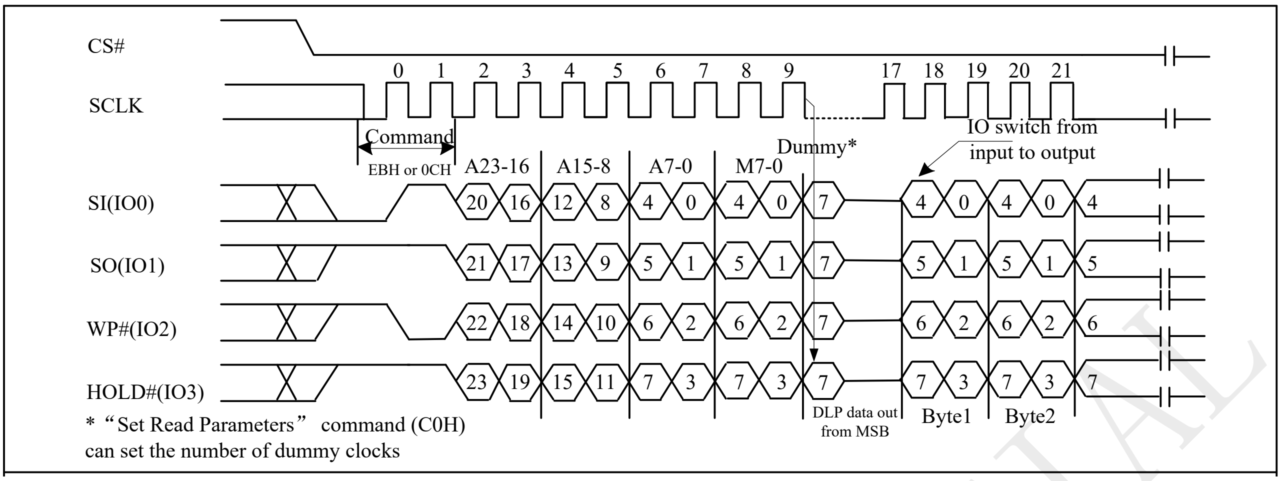
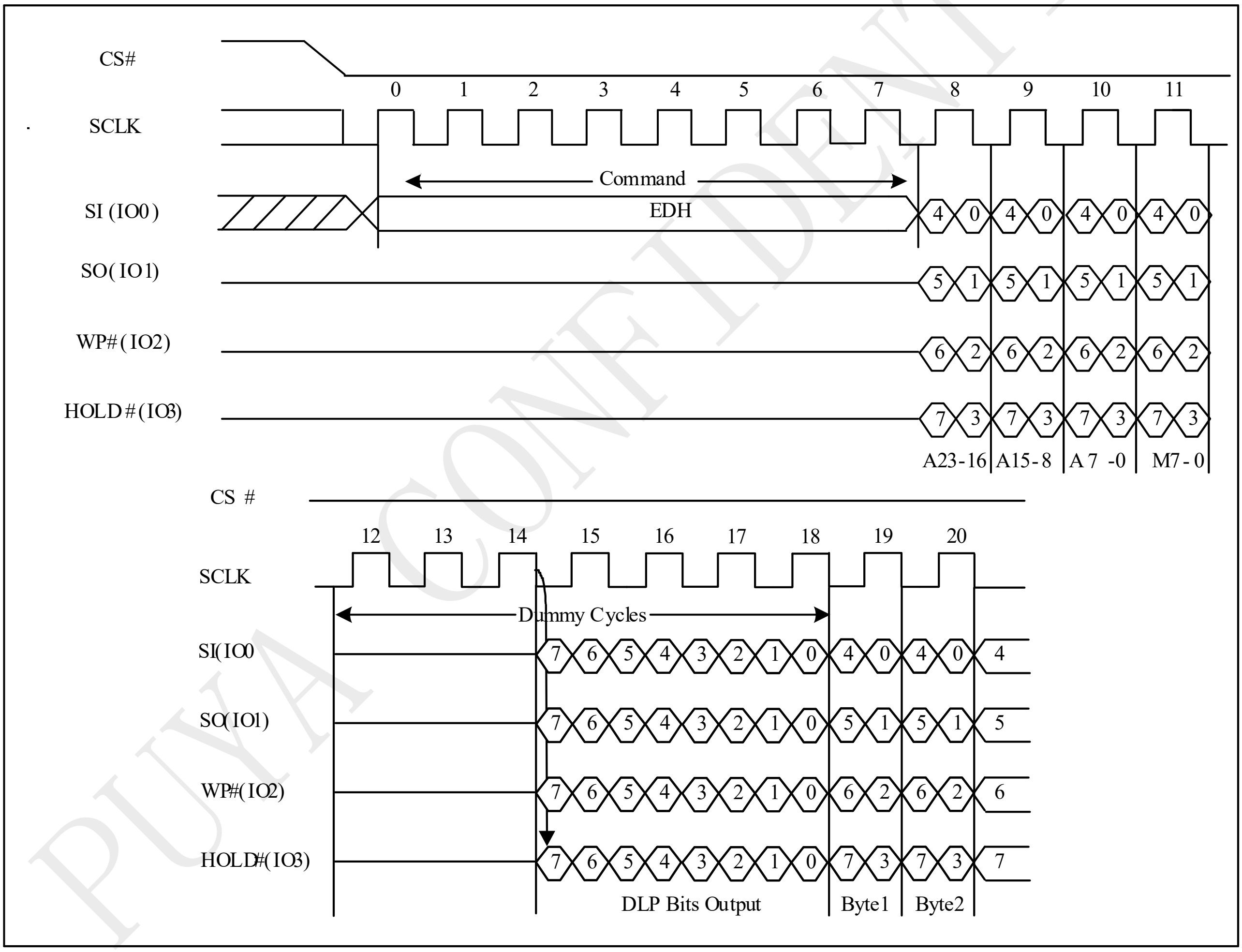


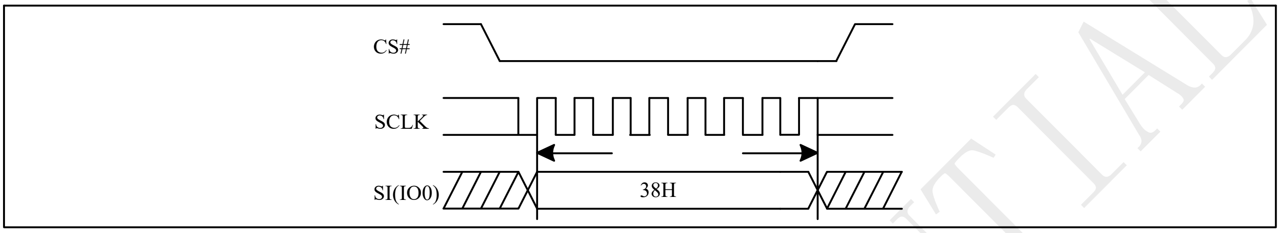
Figure 10-23e DTR 4IO Read with DLP bits output Sequence



10.24 Enable QPI (38H)

The device support both Standard/Dual/Quad SPI and QPI mode. The “Enable QPI (38H)” command can switch the device from SPI mode to QPI mode. See the command Table 2a for all support QPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-1 must be set to 1 first, and “Enable QPI (38H)” command must be issued. If the QE bit is 0, the “Enable QPI (38H)” command will be ignored and the device will remain in SPI mode. When the device is switched from SPI mode to QPI mode, the existing Write Enable Latch and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

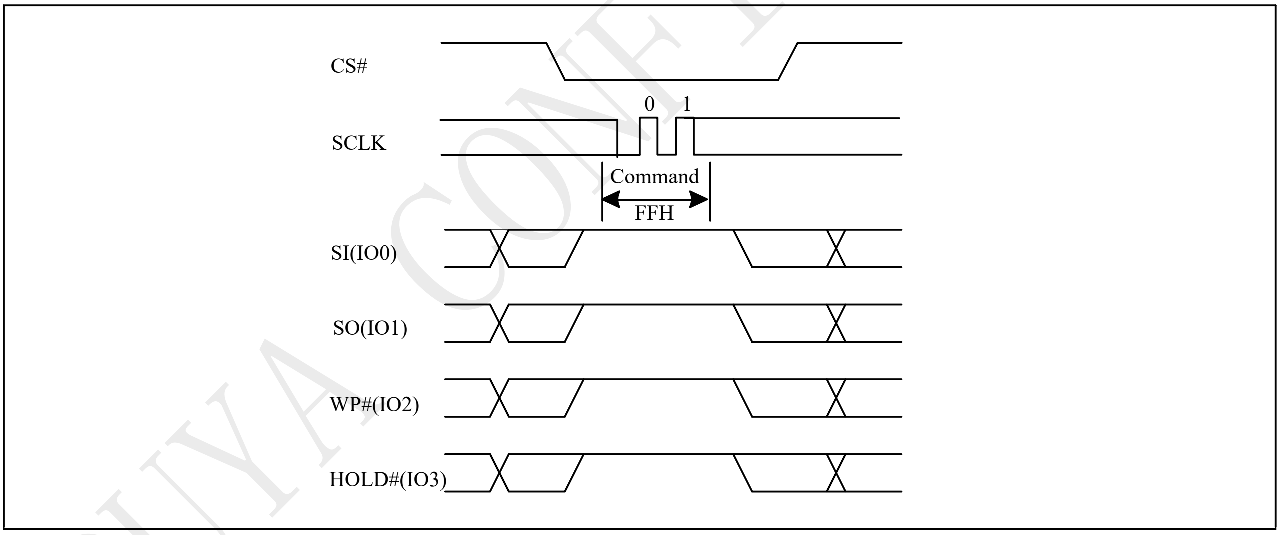
Figure 10-24 Enable QPI Sequence (38H)



10.25 Disable QPI (FFH)

To exit the QPI mode and return to Standard/Dual/Quad SPI mode, the “Disable QPI (FFH)” command must be issued. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

Figure 10-25 Disable QPI Sequence (QPI)



10.26 Page Erase (PE)

The Page Erase (PE) instruction is for erasing the data of the chosen Page to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Erase (PE).

To perform a Page Erase with the standard page size (256 bytes), an instruction of 81h must be clocked into the device followed by three address bytes comprised of 2-page address bytes that specify the page in the main memory to be erased, and 1 dummy byte.

The sequence of issuing PE instruction is: CS# goes low → sending PE instruction code→ 3-byte address on SI → CS# goes high.

Figure 10-26 Page Erase Sequence (Command 81)

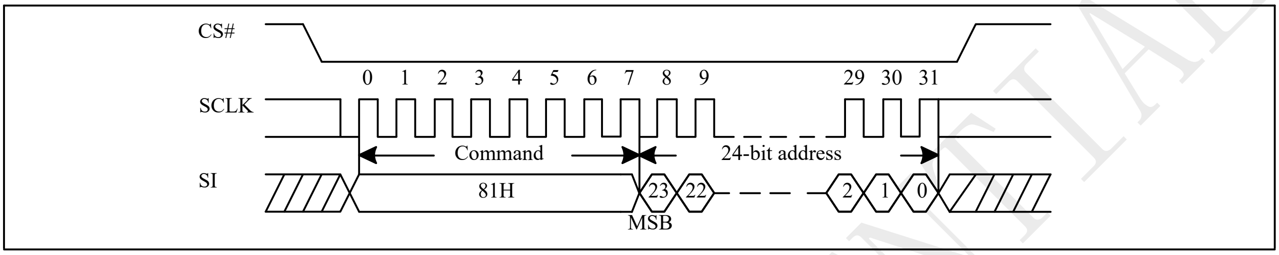
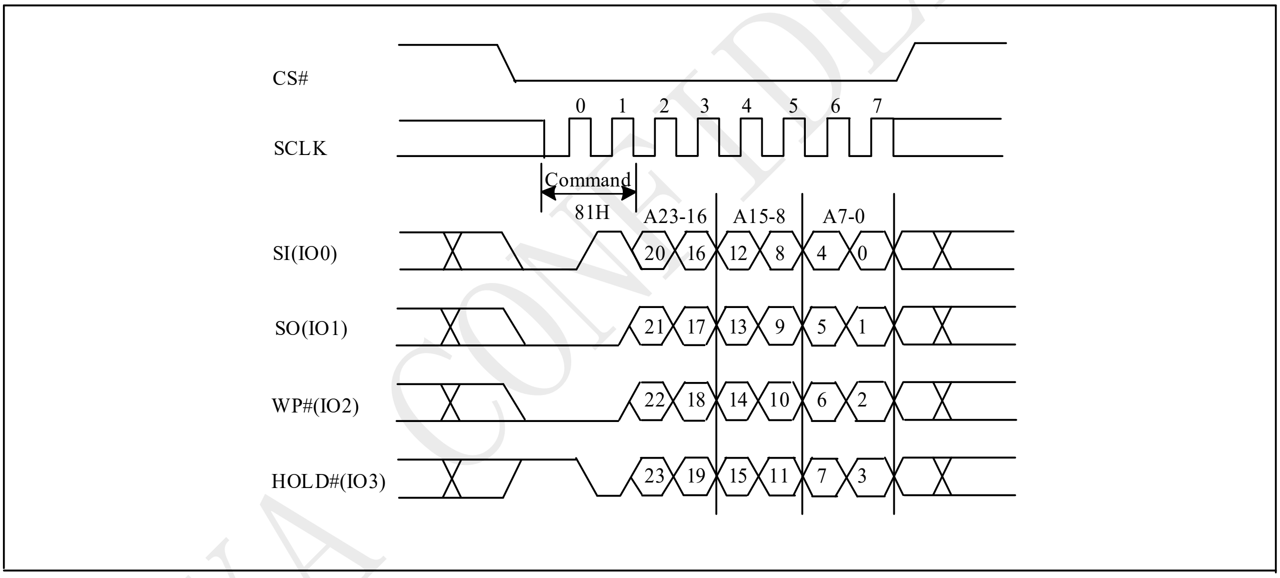


Figure 10-26a Page Erase Sequence (QPI)



10.27 Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low → sending SE instruction code→ 3-byte address on SI → CS# goes high. The SIO[3:1] are don't care.

Figure 10-27 Sector Erase (SE) Sequence (Command 20)

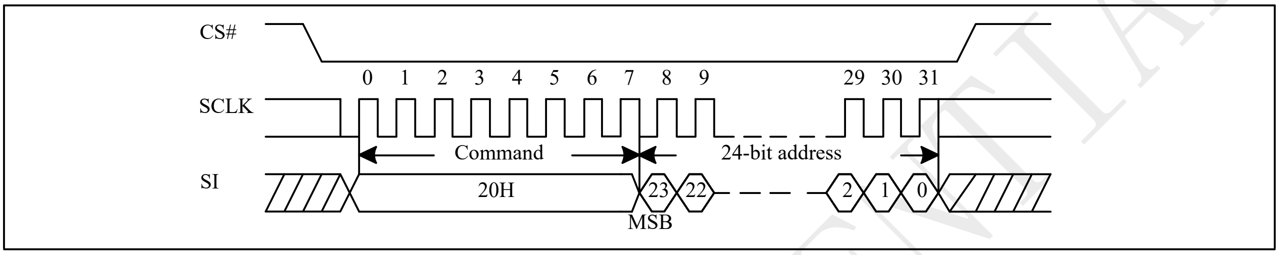
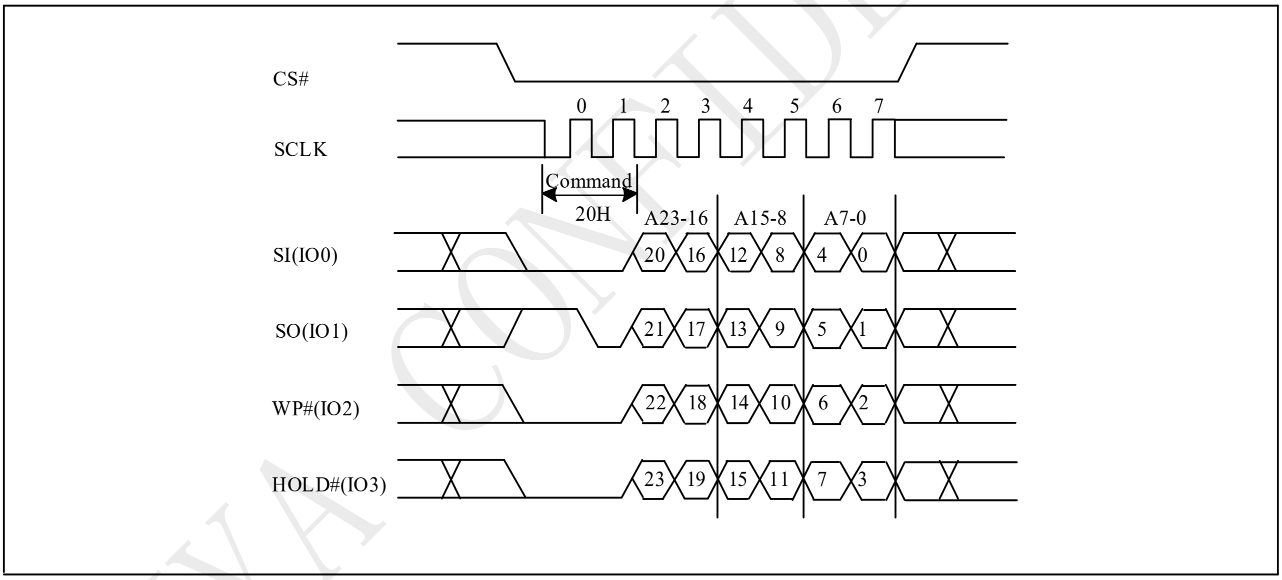


Figure 10-27a Sector Erase (SE) Sequence (QPI)



The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected by BP4, BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the sector.

10.28 Block Erase (BE32K)

The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte has been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32K instruction is: CS# goes low → sending BE32K instruction code → 3-byte address on SI → CS# goes high. The SIO[3:1] are don't care.

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP4, BP3, BP2, BP1, BP0 bits, the array data will be protected (no change) and the WEL bit still be reset.

Figure 10-28 Block Erase 32K(BE32K) Sequence (Command 52)

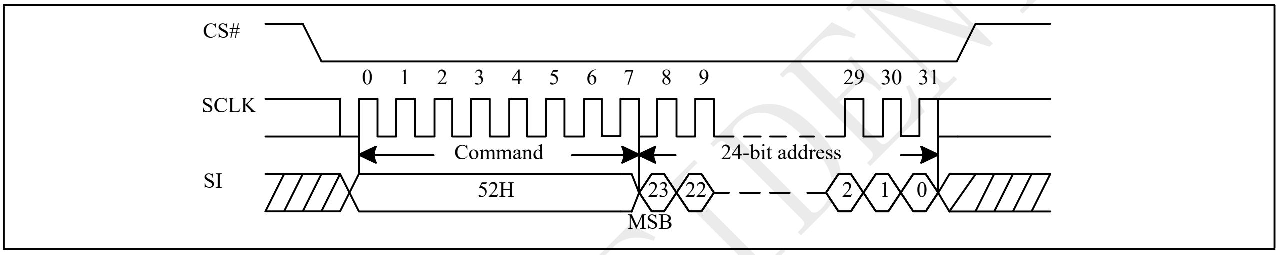
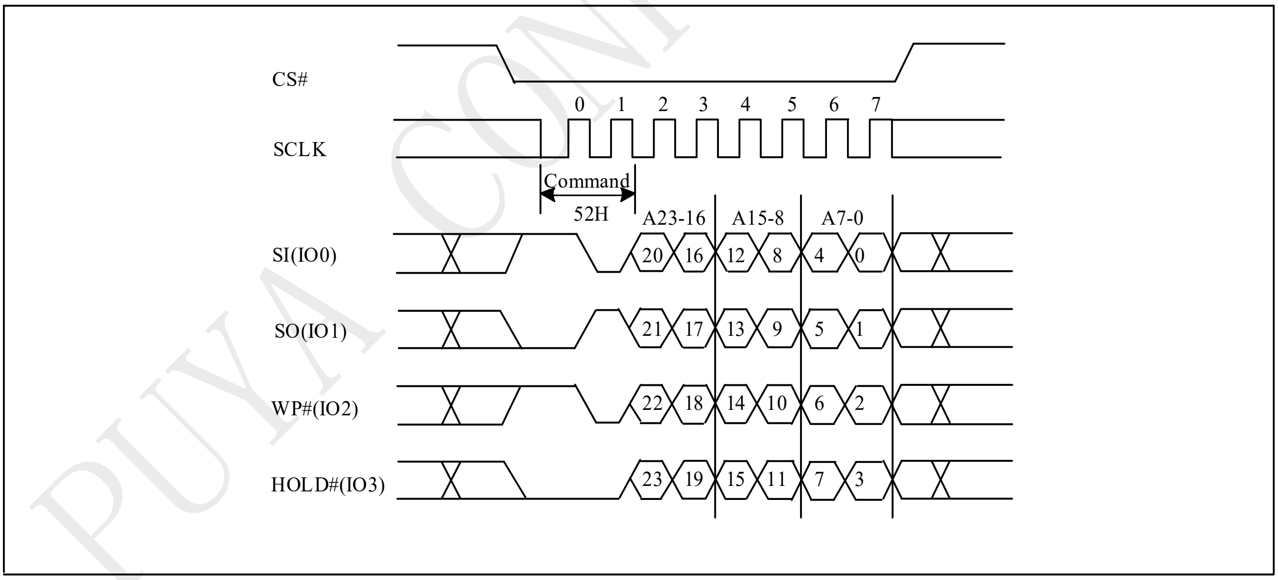


Figure 10-28a Block Erase 32K(BE32K) Sequence (QPI)



10.29 Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low→ sending BE instruction code→ 3-byte address on SI→CS# goes high. The SIO[3:1] are "don't care".

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Block Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP4, BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the block.

Figure 10-29 Block Erase (BE) Sequence (Command D8)

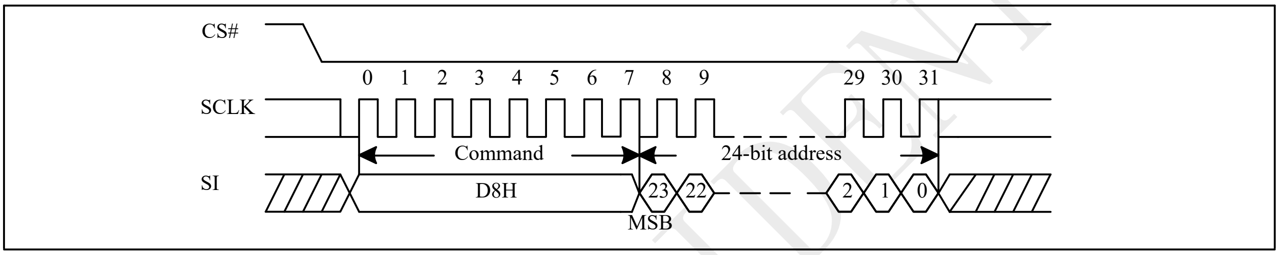
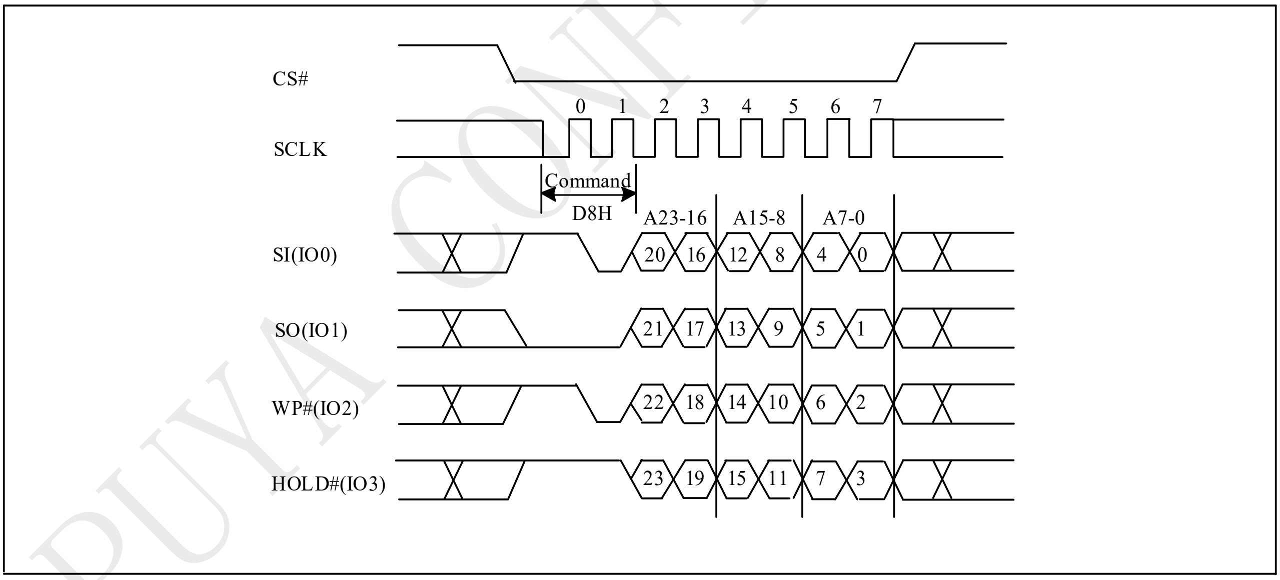


Figure 10-29a Block Erase (BE) Sequence (QPI)



10.30 Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→ sending CE instruction code→ CS# goes high. The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP4, BP3, BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when all Block Protect (BP4, BP3, BP2, BP1, BP0) are set to “None protected”.

Figure 10-30 Chip Erase (CE) Sequence (Command 60 or C7)

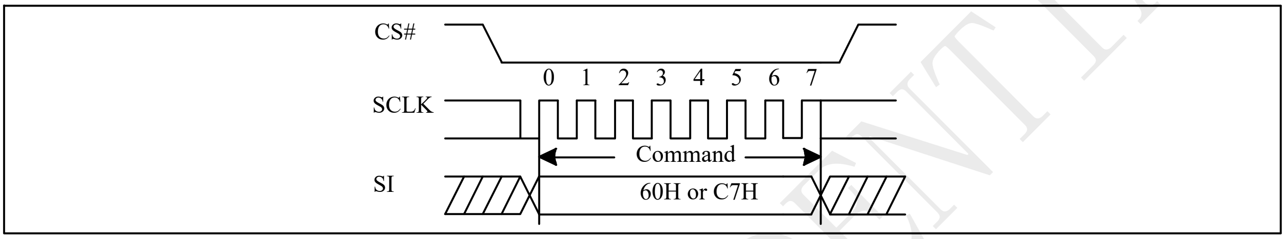
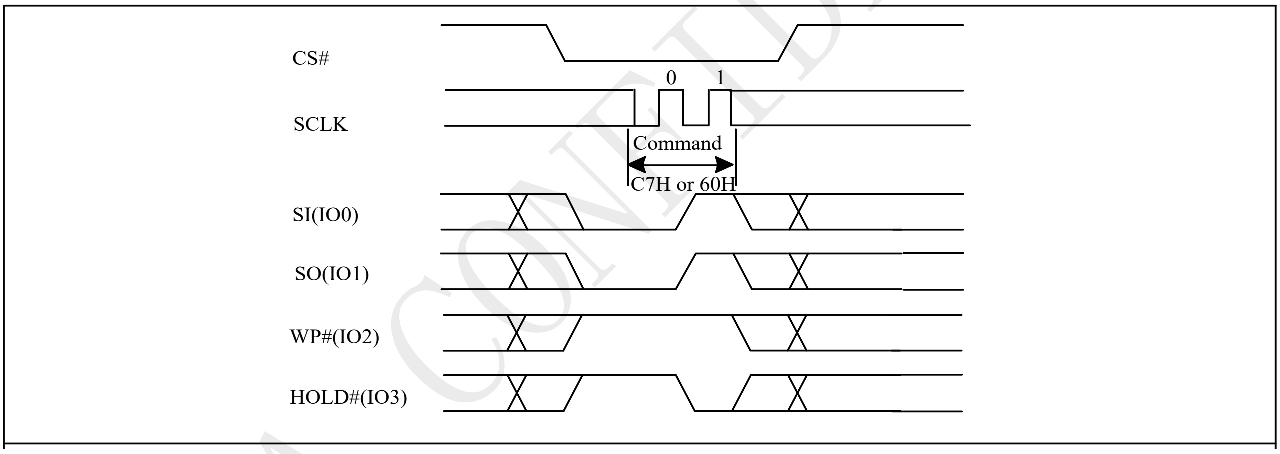


Figure 10-30a Chip Erase (CE) Sequence (QPI)



10.31 Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A7-A0 (The eight least significant address bits) should be set to 0. If the eight least significant address bits (A7-A0) are not all 0, all transmitted data going beyond the end of the current page are programmed from the start address of the same page (from the address A7-A0 are all 0). If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the requested address of the page.

Each page programming operation should be done only once after erase operation. It is possible to program from one byte up to a page size in each Page programming operation.

For the very best performance, programming should be done in full pages of 256 bytes aligned on 256 byte boundaries with each Page being programmed only once.

The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high.

The CS# must be kept low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP4, BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed. The SIO[3:1] are "don't care".

Figure 10-31 Page Program (PP) Sequence (Command 02)

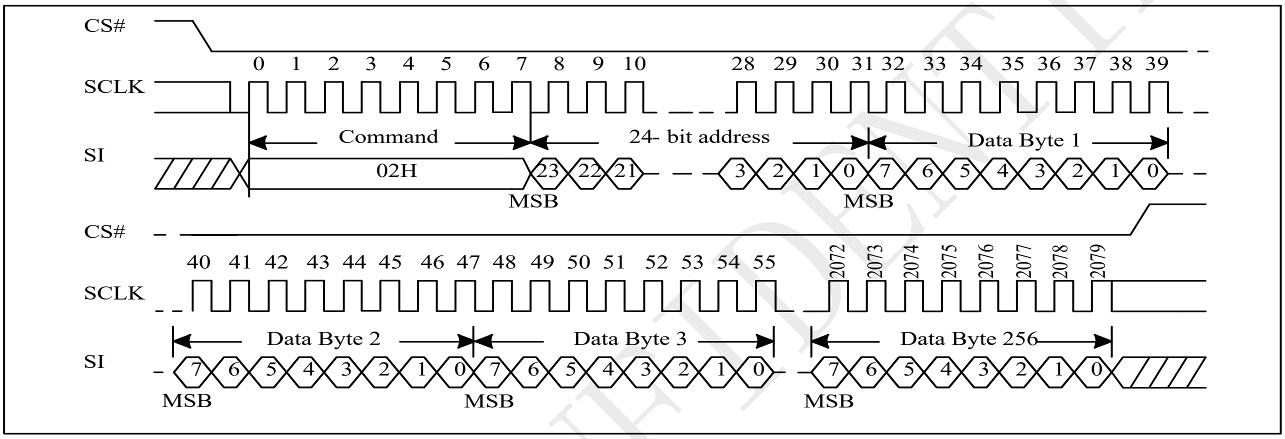
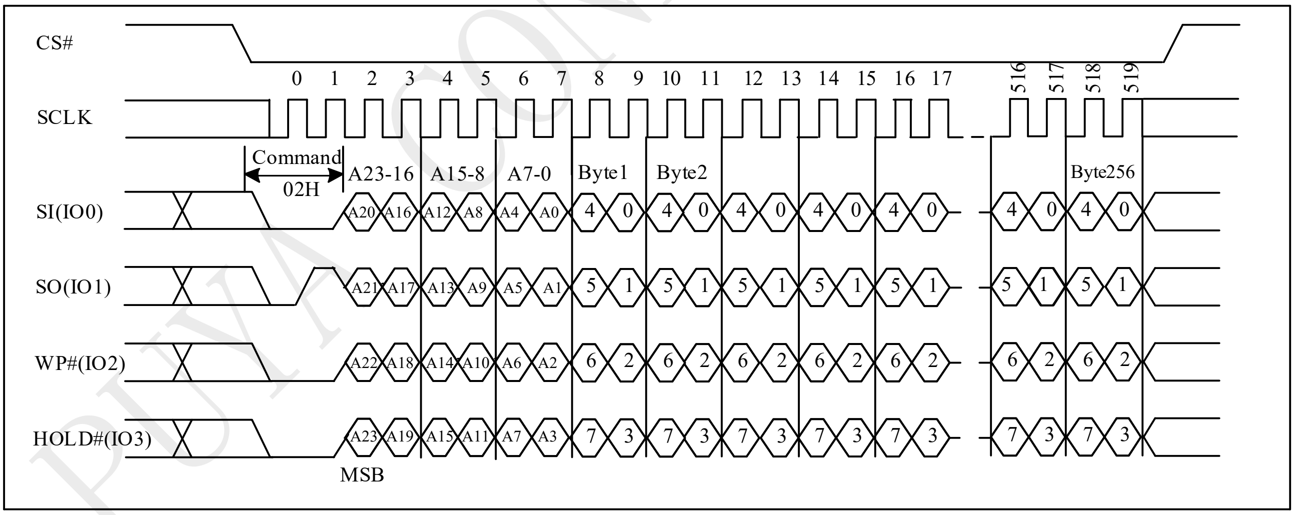


Figure 10-31a Page Program (PP) Sequence (QPI)

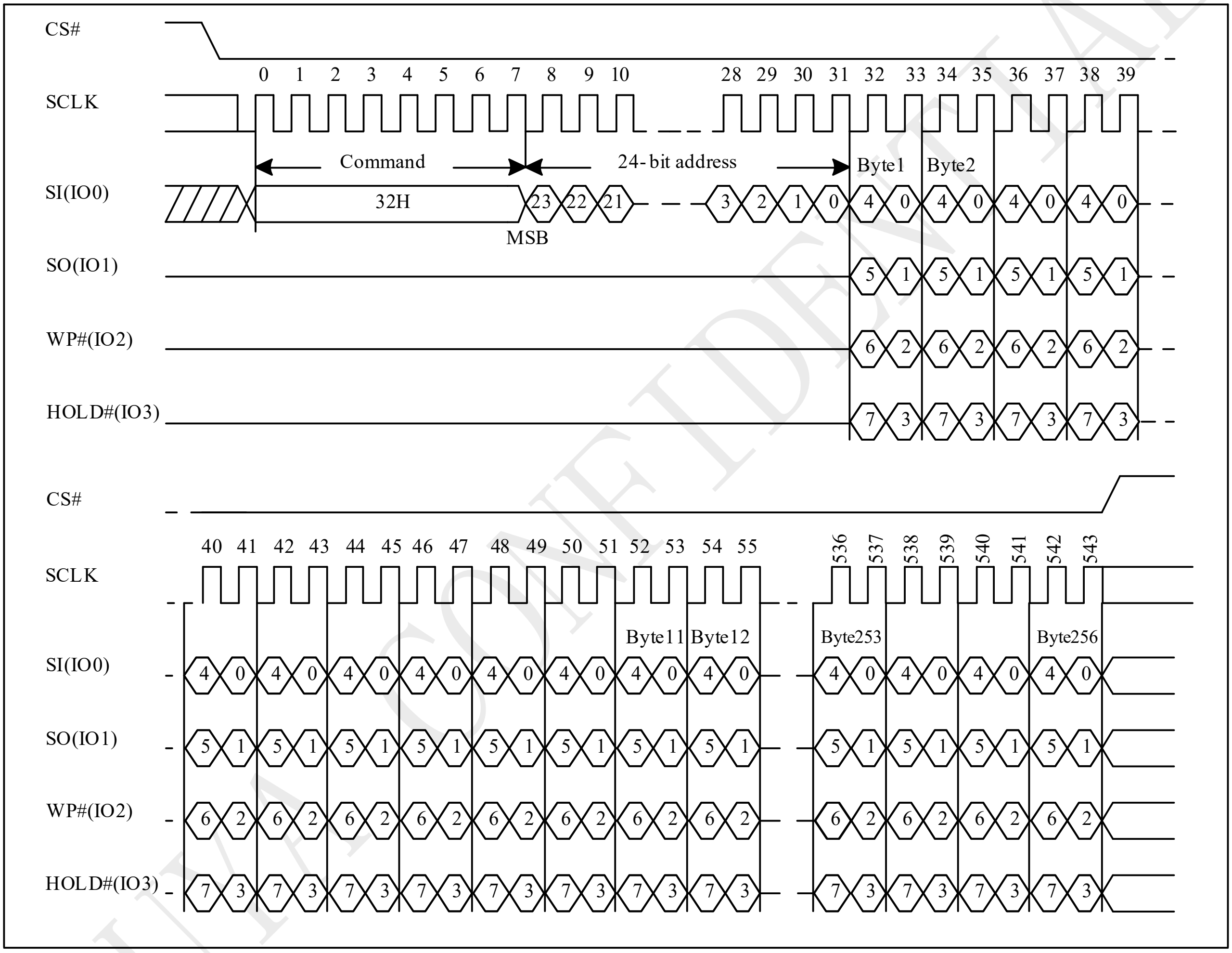


10.32 Quad Page Program (QPP)

The Quad Page Program (QPP) instruction is for programming the memory to be "0". A Write Enable (WREN)instruction must execute to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (QPP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as data input, which can improve programmer performance and the effectiveness of application. The QPP operation frequency supports as fast as fQPP. The other function descriptions are as same as standard page program.

The sequence of issuing QPP instruction is: CS# goes low→ sending QPP instruction code→ 3-byte address on SIO0 → at least 1-byte on data on SIO[3:0]→CS# goes high.

Figure 10-32 Quad Page Program (QPP) Sequence (Command 32)



10.33 Buffer Clear

The Buffer Clear instruction is for reset all buffer data to "FF". The data buffer will be 256 bytes (normal mode) or 512bytes (dual page mode) or 1024 bytes (quad page mode). The Buffer data reset will begin when the CS# pin goes high. There is a latency of tBC, after which the device is ready to accept the next instruction.

The sequence of issuing Buffer Clear instruction is: CS# goes low → sending Buffer Clear instruction code → CS# goes high.

Figure 10-33 Buffer Clear Sequence (Command 9E)

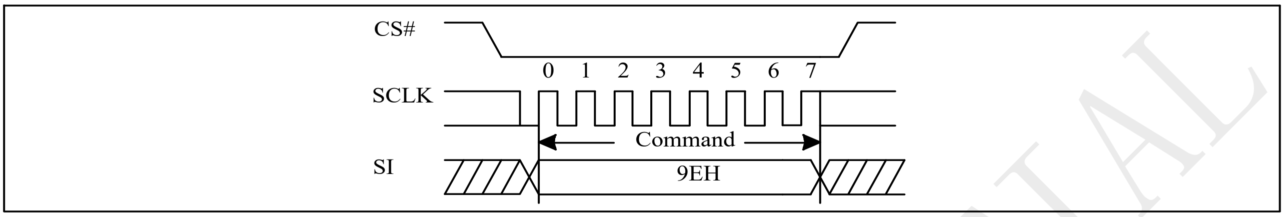
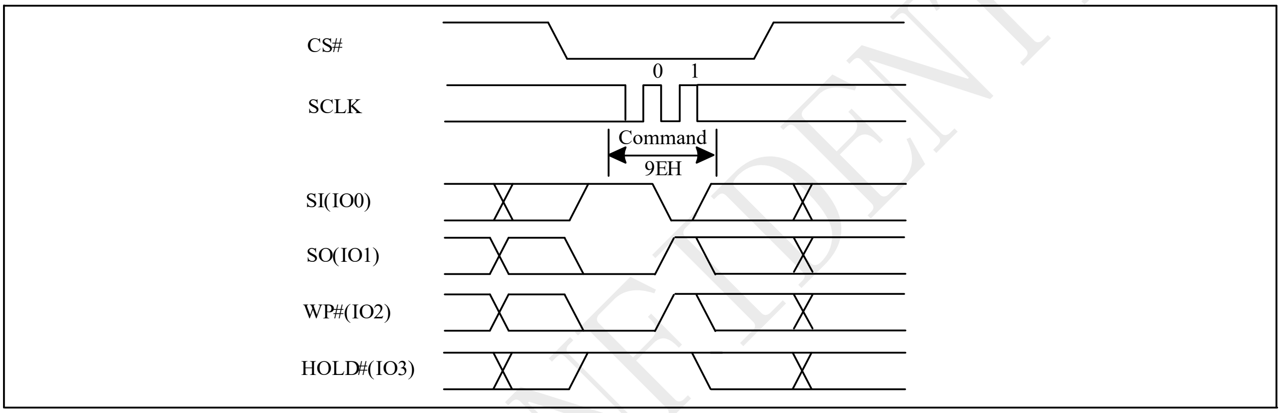


Figure 10-33a Buffer Clear Sequence (QPI)



10.34 Buffer Load

The Buffer Load instruction is for load main memory data to the data buffer. The data buffer will be 256 bytes (normal mode) or 512bytes (dual page mode) or 1024 bytes (quad page mode). The address A23-A8(normal mode) or A23-A9(dual page mode) or A23-A10(quad page mode) which specify the page in main memory to be load data to buffer.

The sequence of issuing Buffer Load instruction is: CS# goes low → sending Buffer Load instruction code → 3-byte address on SI → CS# goes high.

The transfer of the page of data from the main memory to the buffer will begin when the CS# pin goes high. During the page transfer time (tXFR), the WIP bit in the Status Register can be read to determine whether or not the transfer has been completed.

Figure 10-34 Buffer Load Sequence (Command 9A)

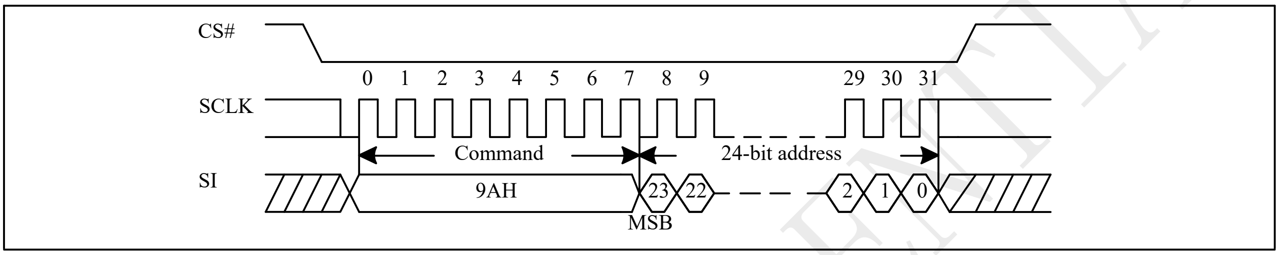
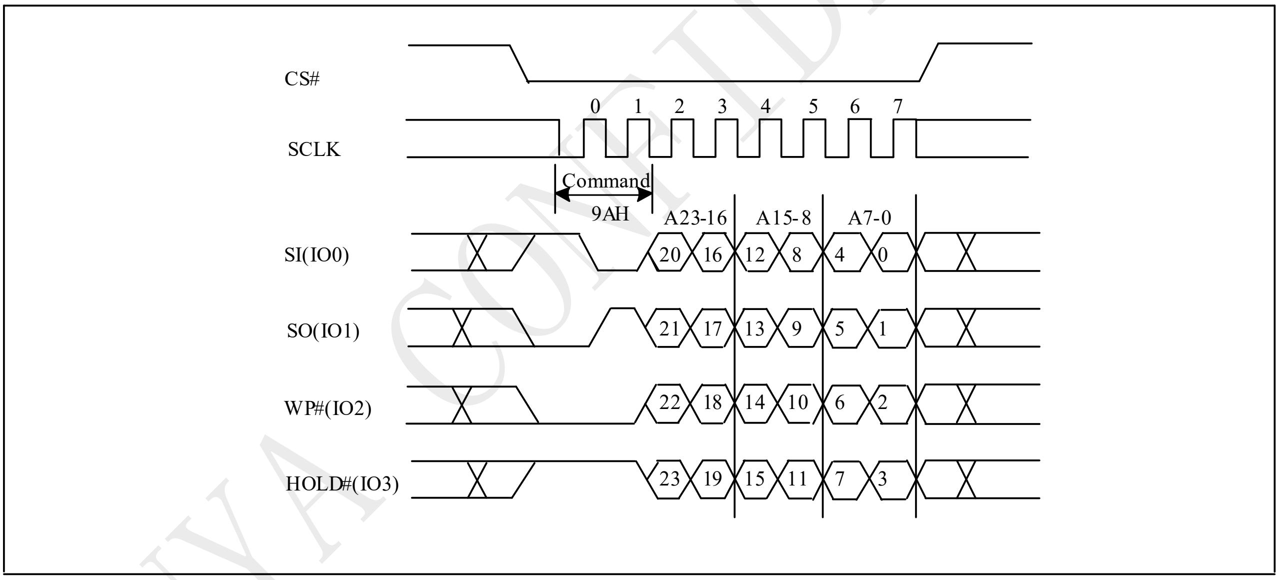


Figure 10-34a Buffer Load Sequence (QPI)



10.35 Buffer Read

The Buffer Read instruction is for reading data out from the data buffer. The data buffer will be 256 bytes (normal mode) or 512bytes (dual page mode) or 1024 bytes (quad page mode). The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole data buffer can be read out at a single Buffer Read instruction. The address counter rolls over to 0 when the highest address (FFh for normal mode /1FF for dual page mode /3FF for quad page mode) has been reached.

The sequence of issuing Buffer Read instruction is: CS# goes low→ sending Buffer Read instruction code→3-byte address on SI→ 1-dummy byte address on SI→ data out on SO→ to end Buffer Read operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, Buffer Read instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 10-35 Buffer Read Sequence (Command 9B)

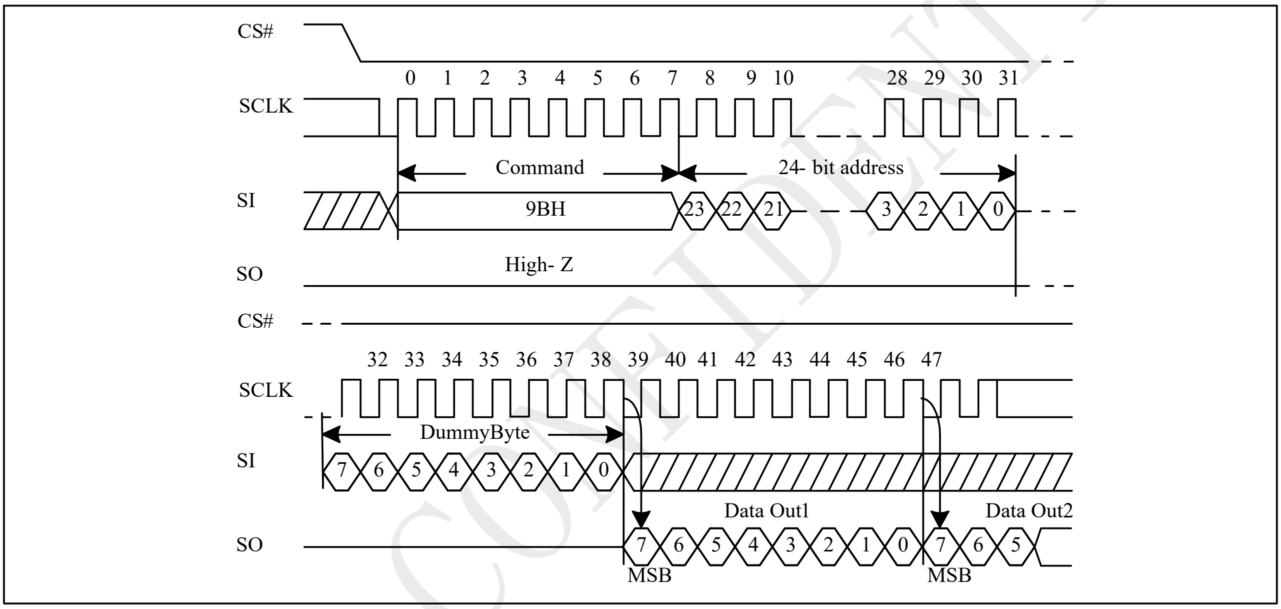
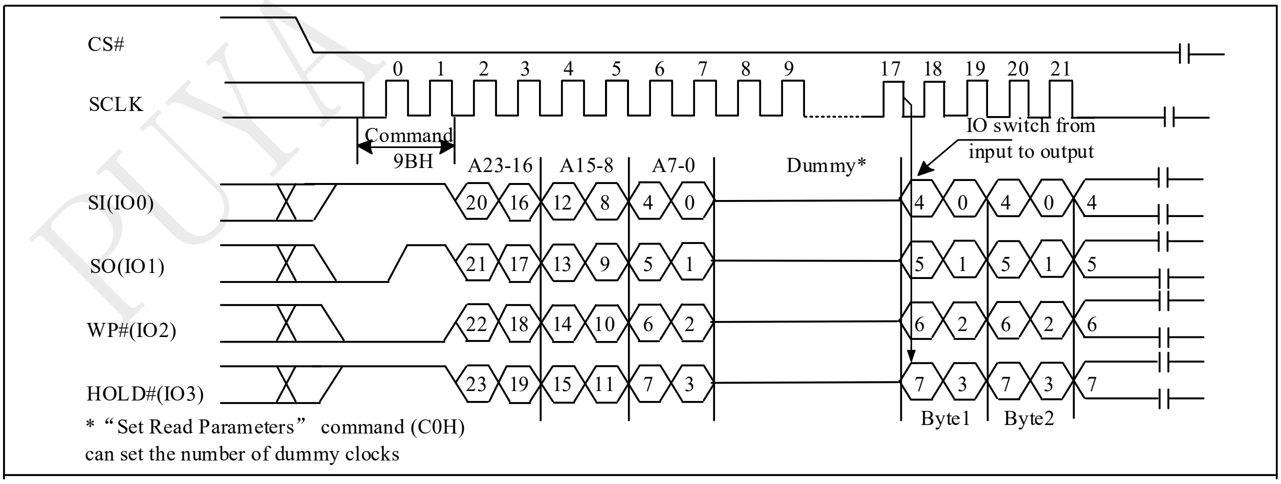


Figure 10-35a Buffer Read Sequence (QPI)



10.36 Buffer Write

The Buffer Write instruction is for send data to data buffer. The data buffer size will be 256 bytes (normal mode) or 512bytes (dual page mode) or 1024 bytes (quad page mode). The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted in.

If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the data buffer until CS Pin goes to high.

The sequence of issuing Buffer Write instruction is: CS# goes low → sending Buffer Write instruction code → 3-byte address on SI → at least 1-byte on data on SI → CS# goes high.

Figure 10-36 Buffer Write Sequence (Command 9C)

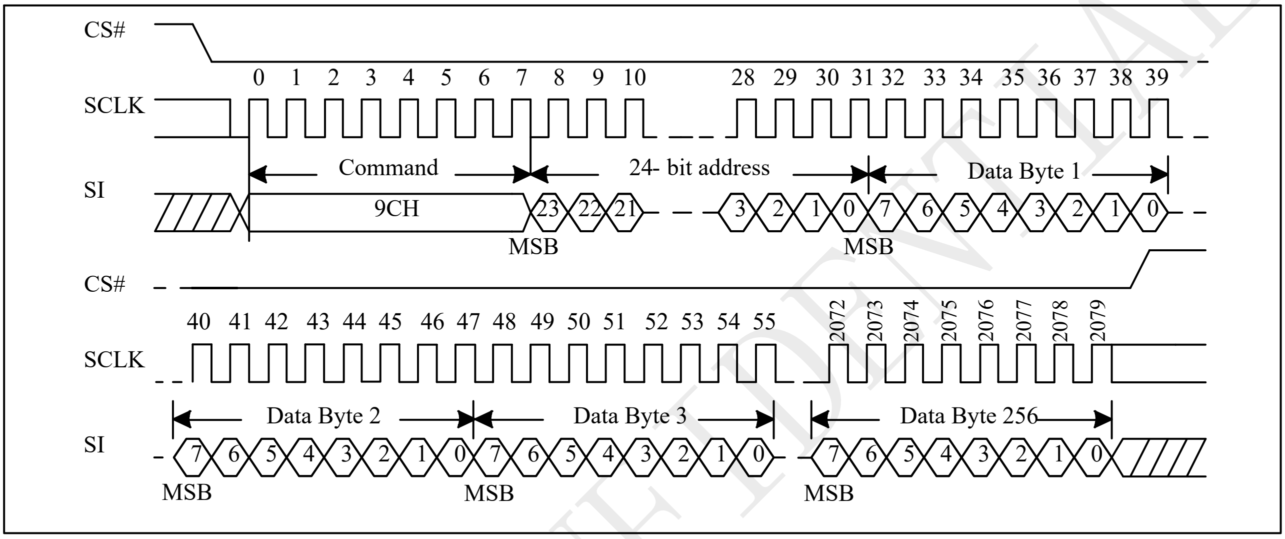
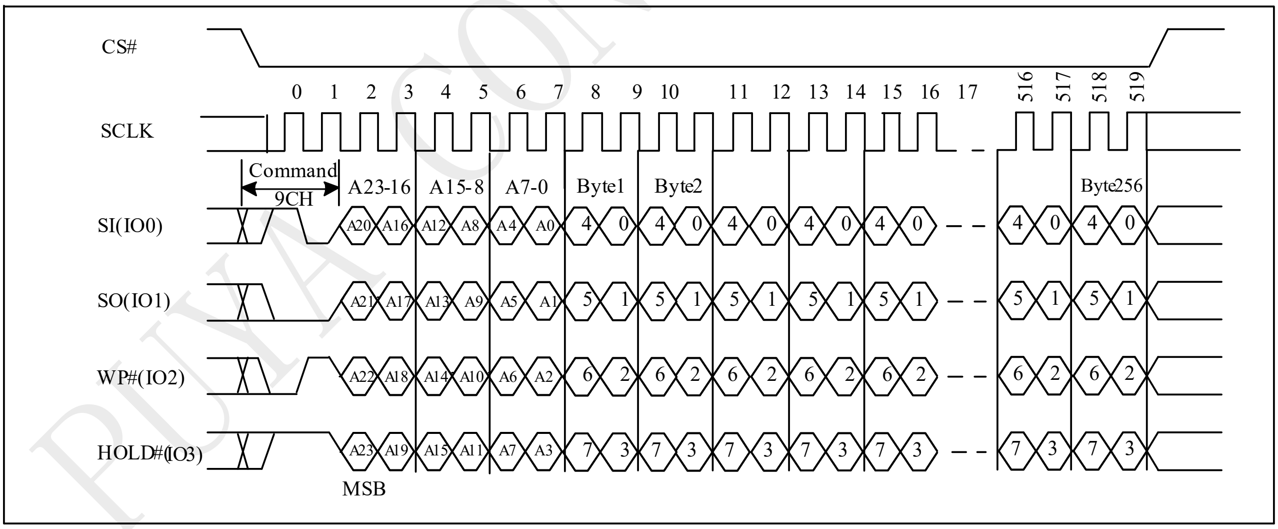


Figure 10-36a Buffer Write Sequence (QPI)



10.37 Buffer to Main Memory Page Program

The Buffer to Main Memory Page Program instruction allows data that is stored in the data buffers to be written into a pre-erased page in the main memory array. It is necessary that the page in main memory to be written be previously erased in order to avoid programming errors. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Buffer to Main Memory Page Program instruction. The data buffer will be 256 bytes (normal mode) or 512bytes (dual page mode) or 1024 bytes (quad page mode). The address A23-A8(normal mode) or A23-A9(dual page mode) or A23-A10(quad page mode) which specify the page in main memory to be programmed.

The sequence of issuing Buffer to Main Memory Page Program instruction is: CS# goes low → sending Buffer to Main Memory Page Program instruction code → 3-byte address on SI → CS# goes high.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Buffer to Main Memory Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP4, BP3, BP2, BP1, BP0 bits, the Buffer to Main Memory Page Program instruction will not be executed.

Figure 10-37 Buffer to Main Memory Page Program Sequence (Command 9D)

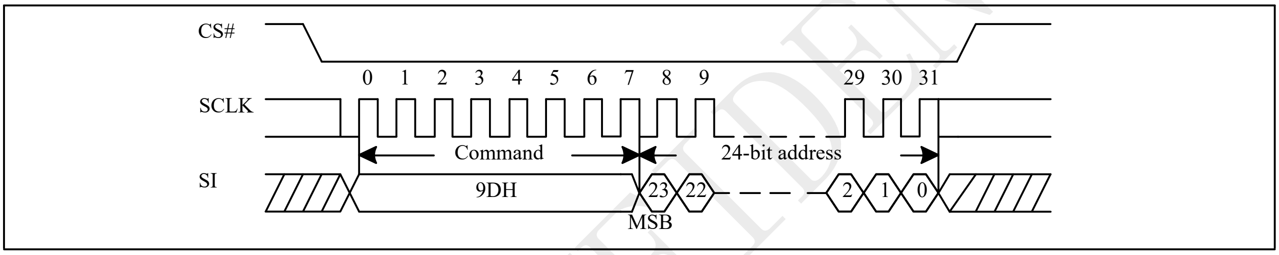
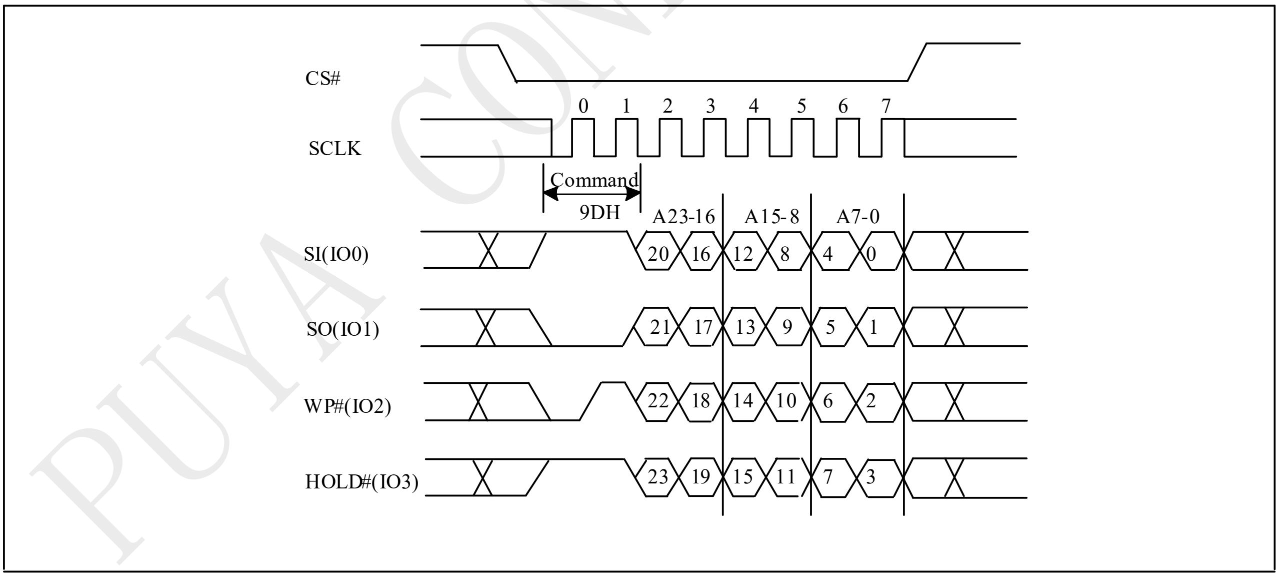


Figure 10-37a Buffer to Main Memory Page Program Sequence (QPI)



10.38 Erase Security Registers (ERSCUR)

The product provides three 1024-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

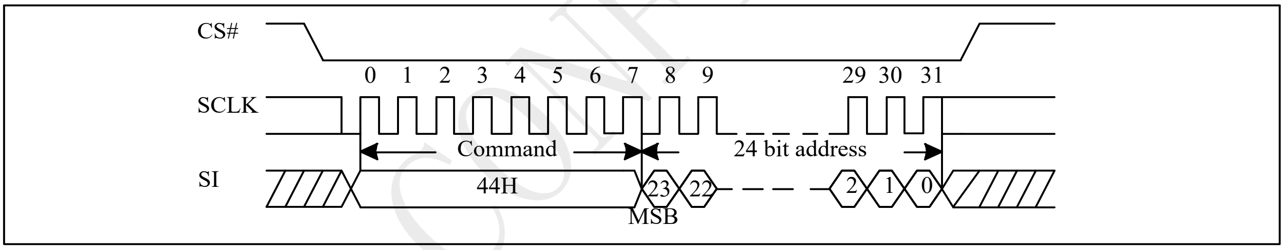
The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending ERSCUR instruction →□sending 24 bit address → CS# goes high.

CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. The Security Registers Lock Bit (LB3-1) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-16	A15-12	A11-10	A9-0
Security Register #1	00H	0001	00	Byte Address
Security Register #2	00H	0010	00	Byte Address
Security Register #3	00H	0011	00	Byte Address

Figure 10-38 Erase Security Registers (ERSCUR) Sequence (Command 44)



10.39 Program Security Registers (PRSCUR)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 1024 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command.

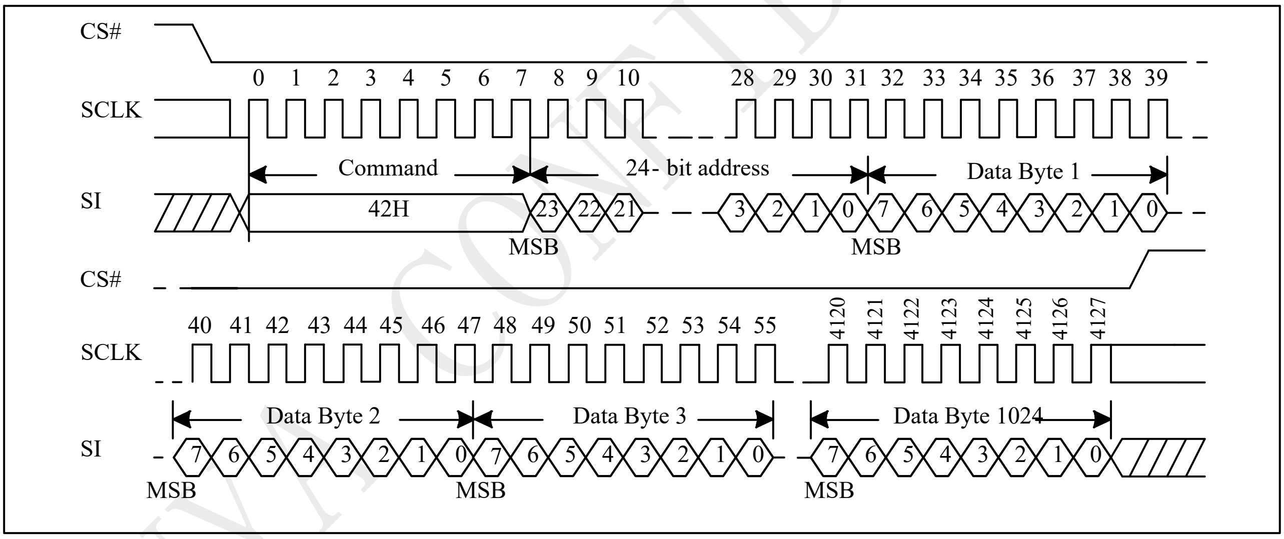
The Program Security Registers command sequence: CS# goes low → sending PRSCUR instruction →sending 24 bit address → sending at least one byte data → CS# goes high.

As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed.

If the Security Registers Lock Bit (LB3-1) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-16	A15-12	A11-10	A9-0
Security Register #1	00H	0001	00	Byte Address
Security Register #2	00H	0010	00	Byte Address
Security Register #3	00H	0011	00	Byte Address

Figure 10-39 Program Security Registers (PRSCUR) Sequence (Command 42)



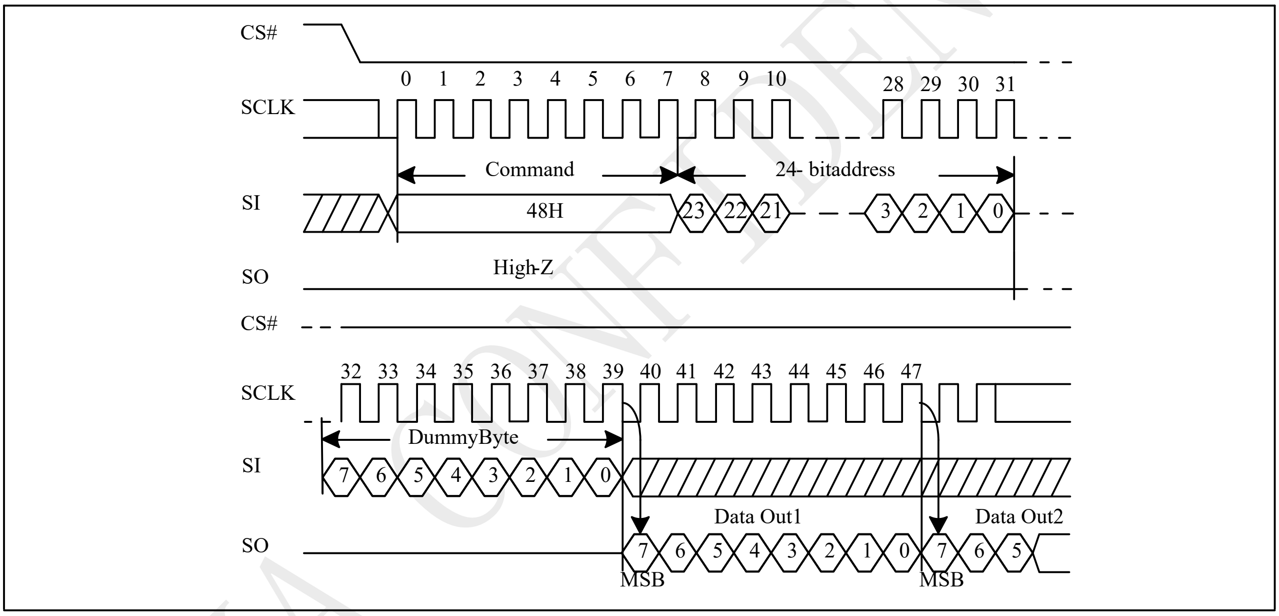
10.40 Read Security Registers (RDSCUR)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 1FFH), it will reset to 000H, the command is completed by driving CS# high.

The sequence of issuing RDSCUR instruction is: CS# goes low → sending RDSCUR instruction → sending 24-bit address → 8-bit dummy byte → Security Register data out on SO → CS# goes high.

Address	A23-16	A15-12	A11-10	A9-0
Security Register #1	00H	0001	00	Byte Address
Security Register #2	00H	0010	00	Byte Address
Security Register #3	00H	0011	00	Byte Address

Figure 10-40 Read Security Registers (RDSCUR) Sequence (Command 48)



10.41 Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored.

The sequence of issuing DP instruction is: CS# goes low→ sending DP instruction code→ CS# goes high.

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) , Read Electronic Signature (RES) instruction, and soft reset instruction(66H, 99H). (RES instruction to allow the ID been read out). When Power- down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not be executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

Figure 10-41 Deep Power-down (DP) Sequence (Command B9)

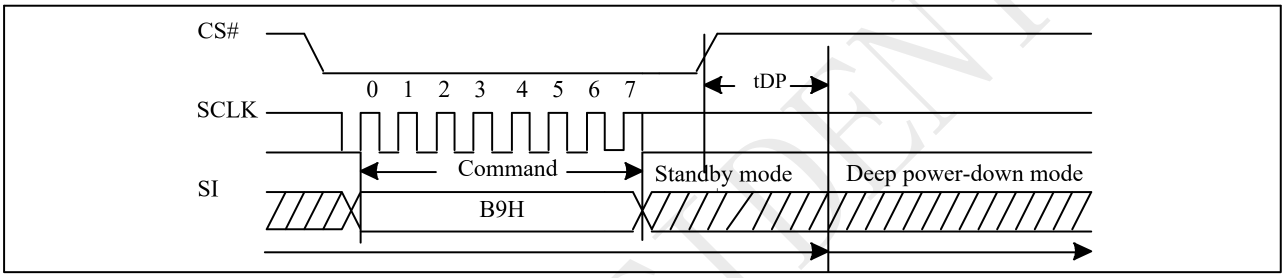
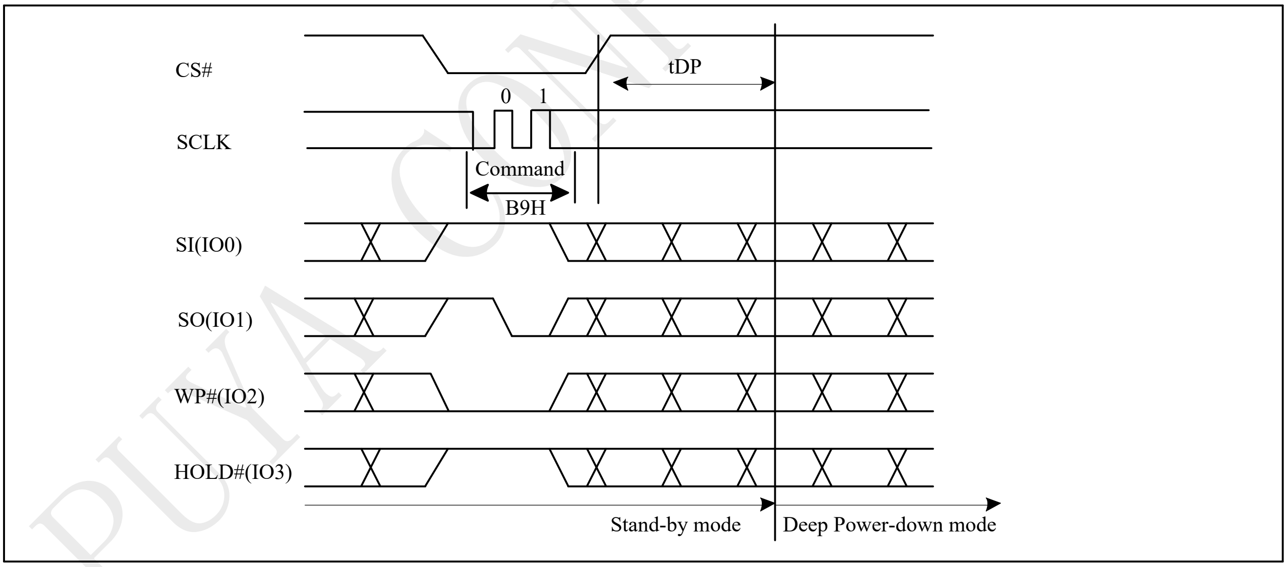


Figure 10-41a Deep Power-down (DP) Sequence (QPI)



10.42 Release form Deep Power-Down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven high, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max). Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/ write cycle in progress.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2 (max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power-Down Mode.

Figure 10-42 Read Electronic Signature (RES) Sequence (Command AB)

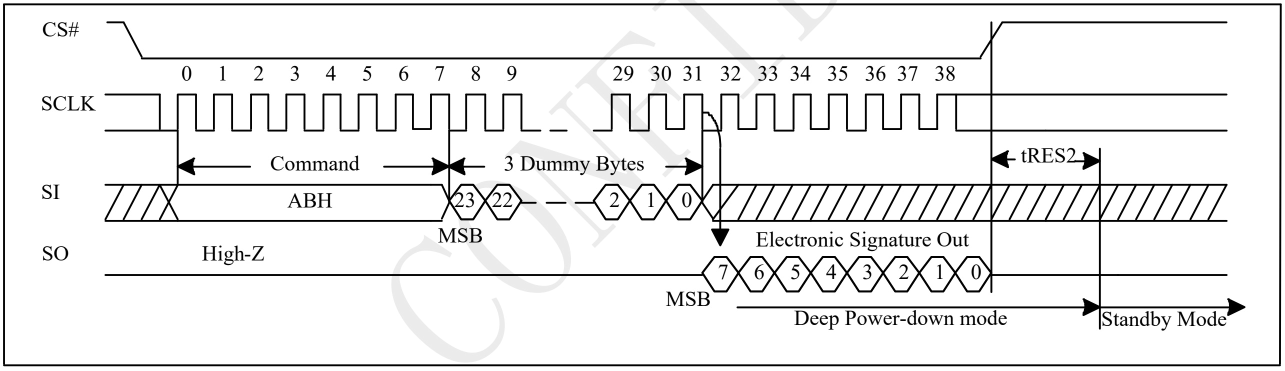


Figure 10-42a Read Electronic Signature (RES) Sequence (QPI)

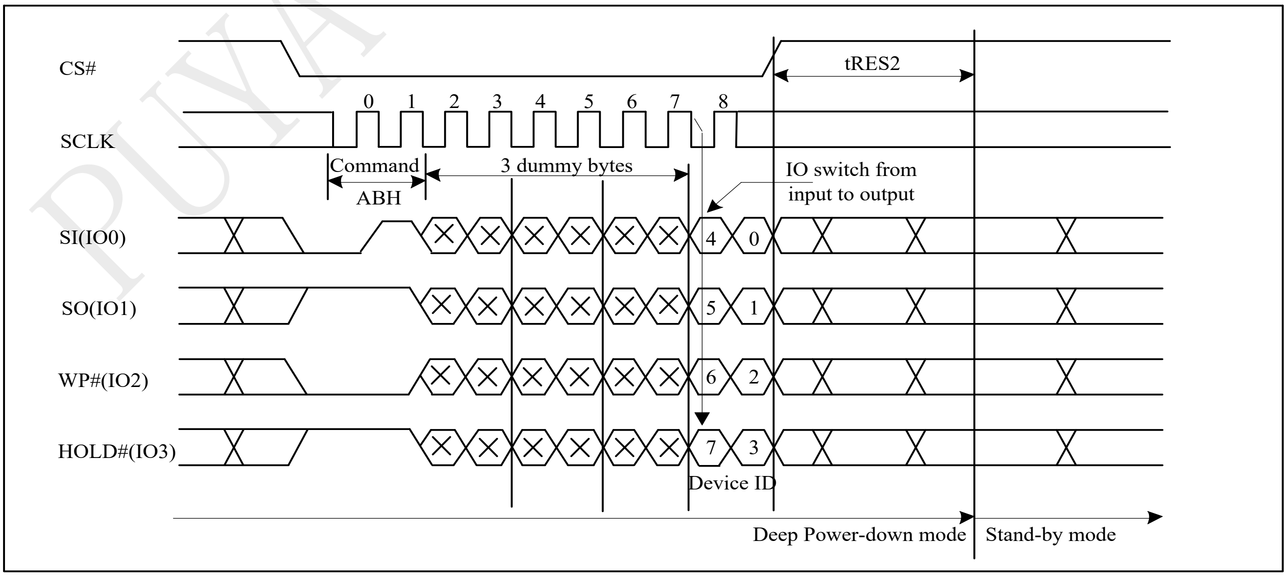


Figure 10-42b Release from Deep Power-down (RDP) Sequence (Command AB)

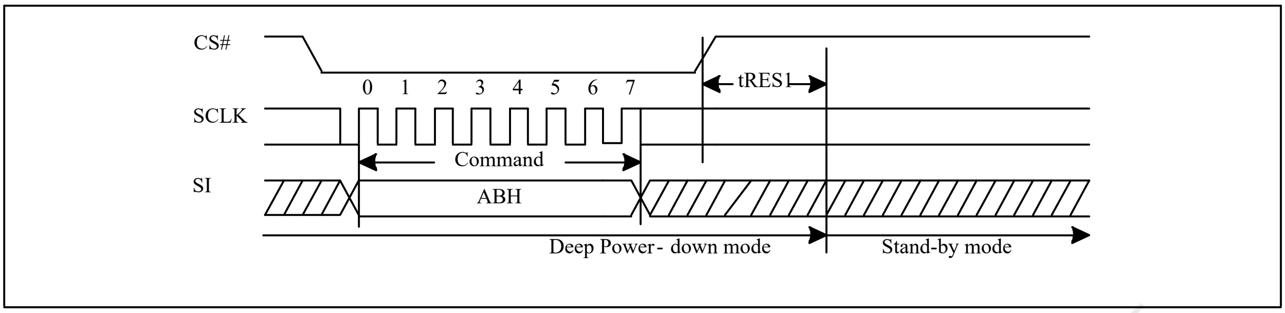
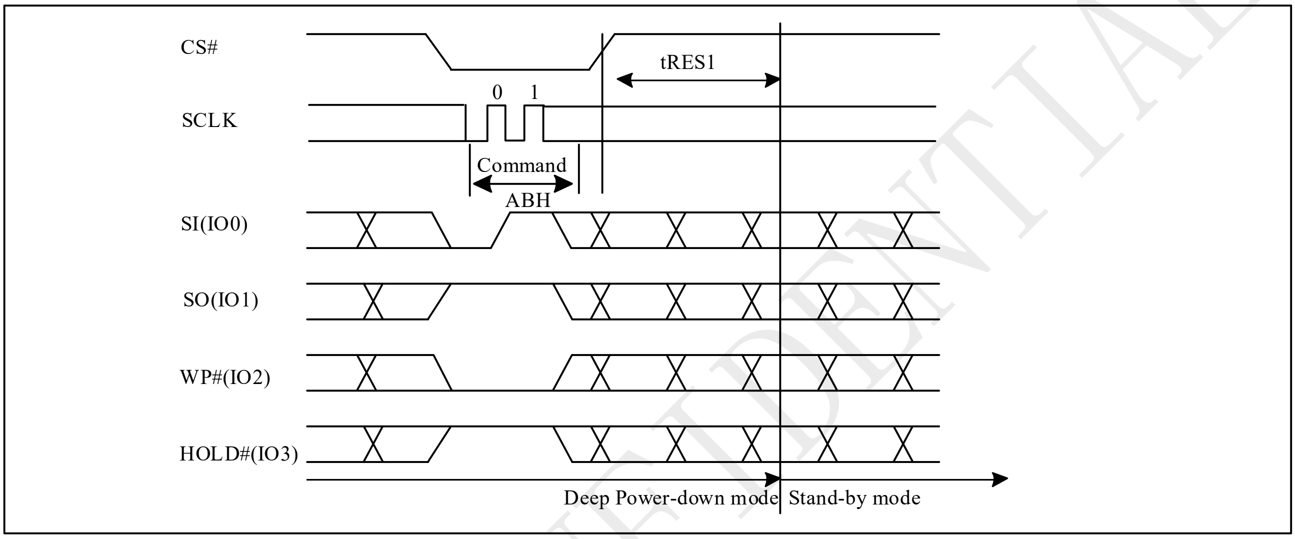


Figure 10-42c Release from Deep Power-down (RDP) Sequence (QPI)



10.43 Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in "Table ID Definitions".

The REMS instruction is initiated by driving the CS# pin low and sending the instruction code "90h" followed by two dummy bytes and one address byte (A7~A0). After which the manufacturer ID for PUYA (85h) and the device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the manufacturer and device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 10-43 Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90)

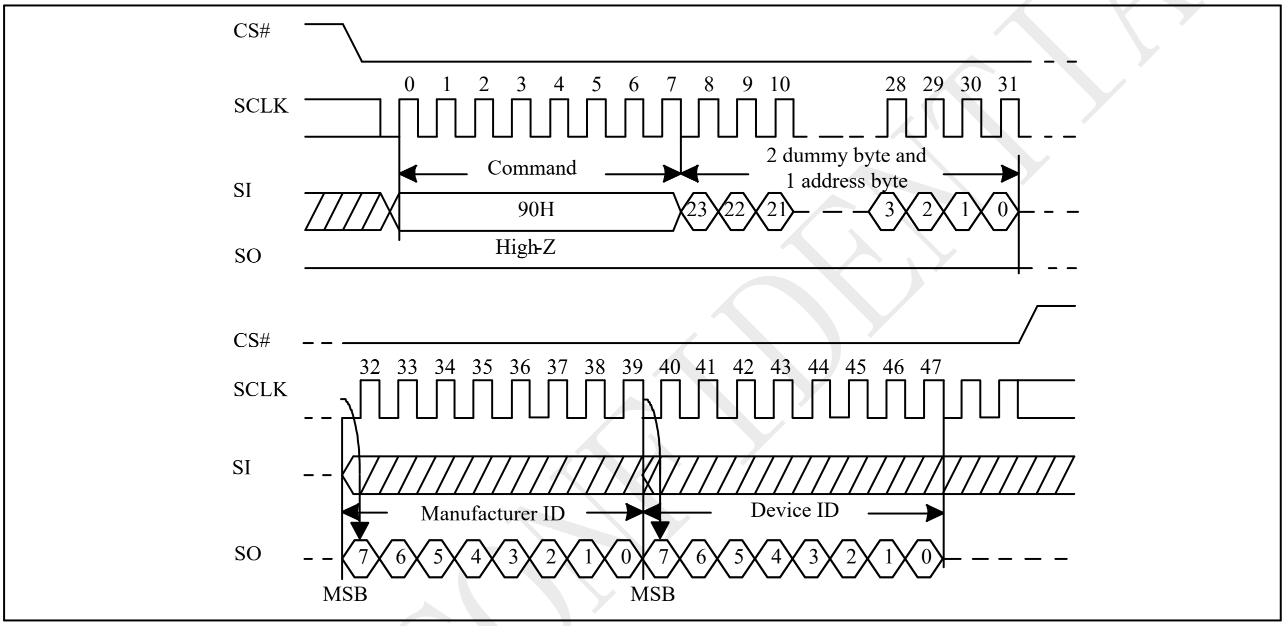
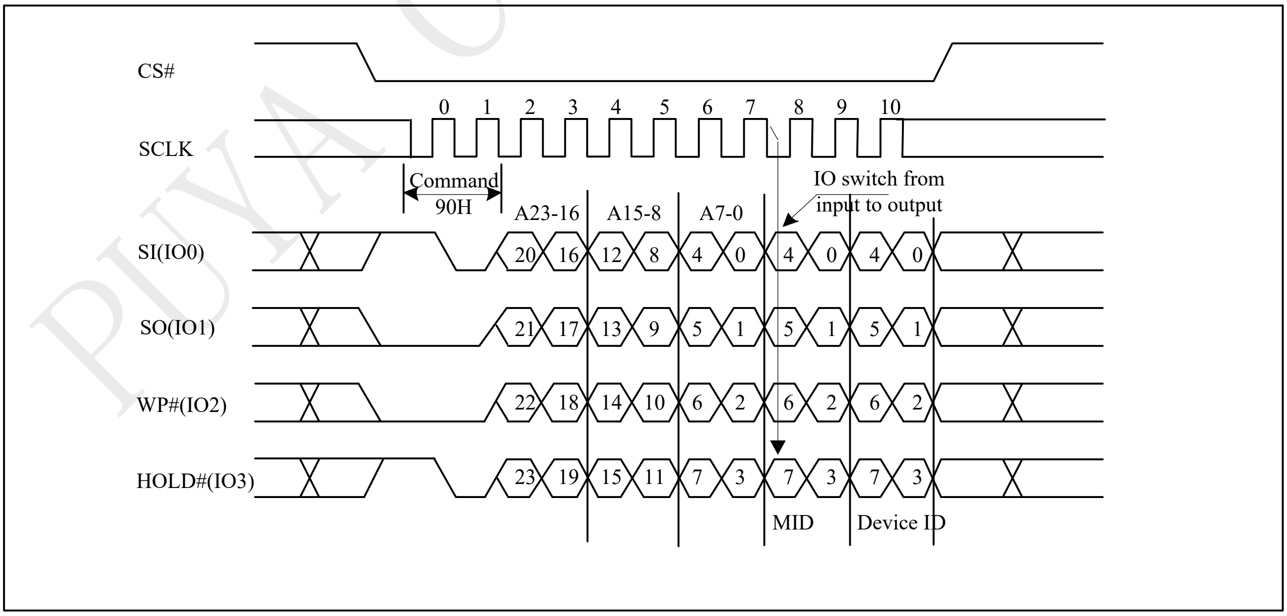


Figure 10-43a Read Electronic Manufacturer & Device ID (REMS) Sequence (QPI)

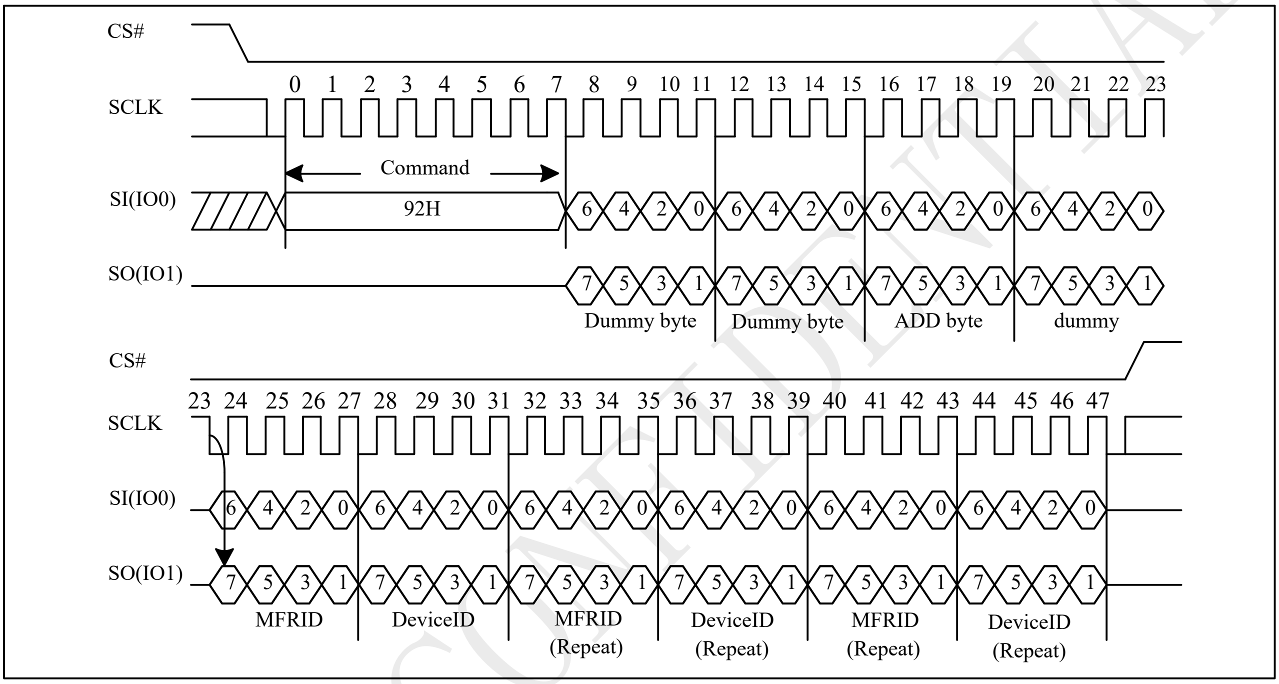


10.44 Dual I/O Read Electronic Manufacturer ID & Device ID (DREMS)

The DREMS instruction is similar to the REMS command and returns the JEDEC assigned manufacturer ID which takes two pins: SIO0, SIO1 as address input and ID output I/O

The instruction is initiated by driving the CS# pin low and shift the instruction code "92h" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for PUYA (85h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 10-44 DUAL I/O Read Electronic Manufacturer & Device ID (DREMS) Sequence (Command 92)

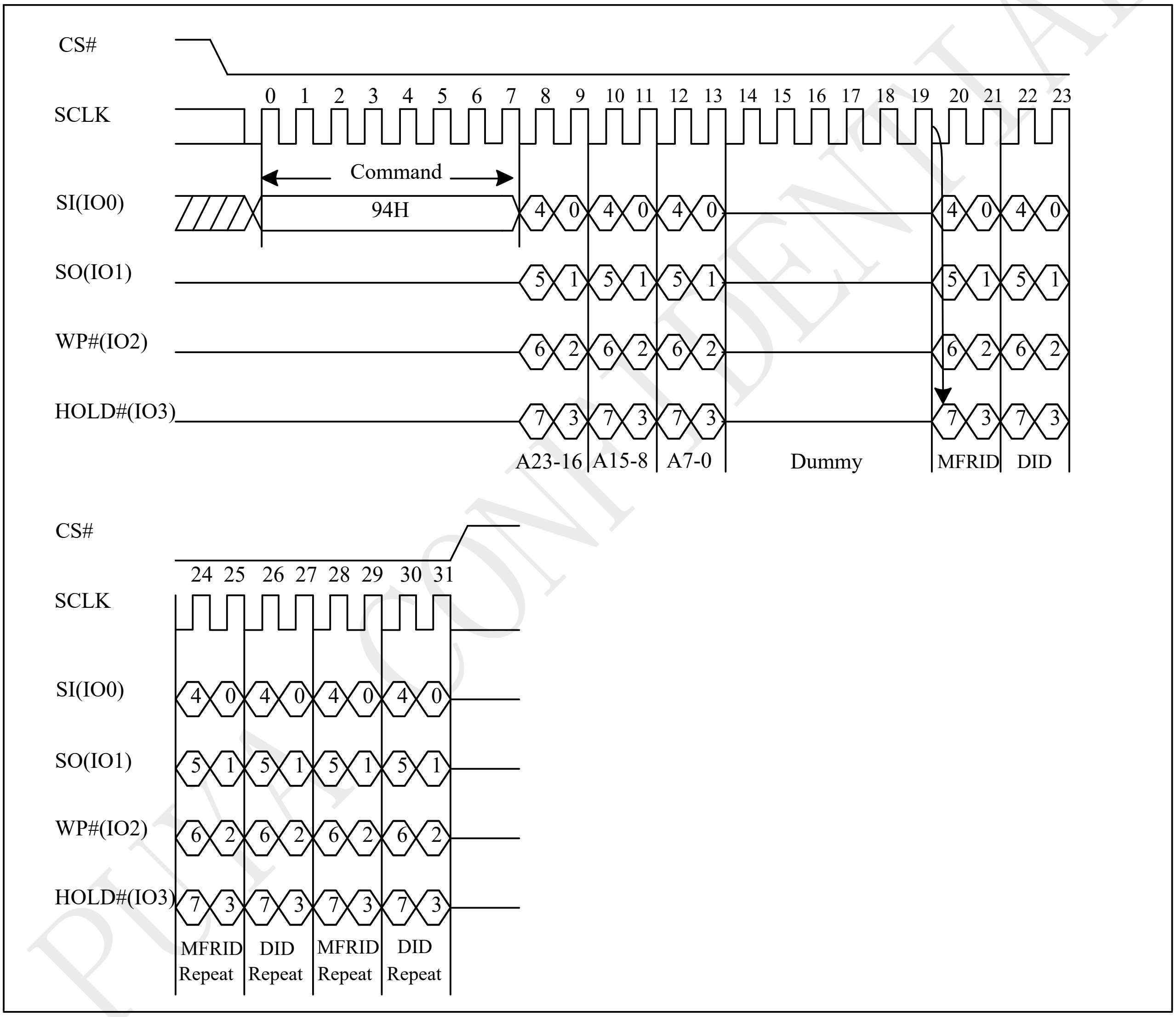


10.45 Quad I/O Read Electronic Manufacturer ID & Device ID (QREMS)

The QREMS instruction is similar to the REMS command and returns the JEDEC assigned manufacturer ID which takes four pins: SIO0, SIO1,SIO2,SIO3 as address input and ID output I/O

The instruction is initiated by driving the CS# pin low and shift the instruction code "94h" followed by two dummy bytes and one byte's address (A7~A0). After which, the Manufacturer ID for PUYA (85h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 10-45 QUAD I/O Read Electronic Manufacturer & Device ID (QREMS) Sequence (Command 94)



10.46 Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The PUYA Manufacturer ID and Device ID are list as "Table ID Definitions”.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code → 24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out. While Program /Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 10-46 Read Identification (RDID) Sequence (Command 9F)

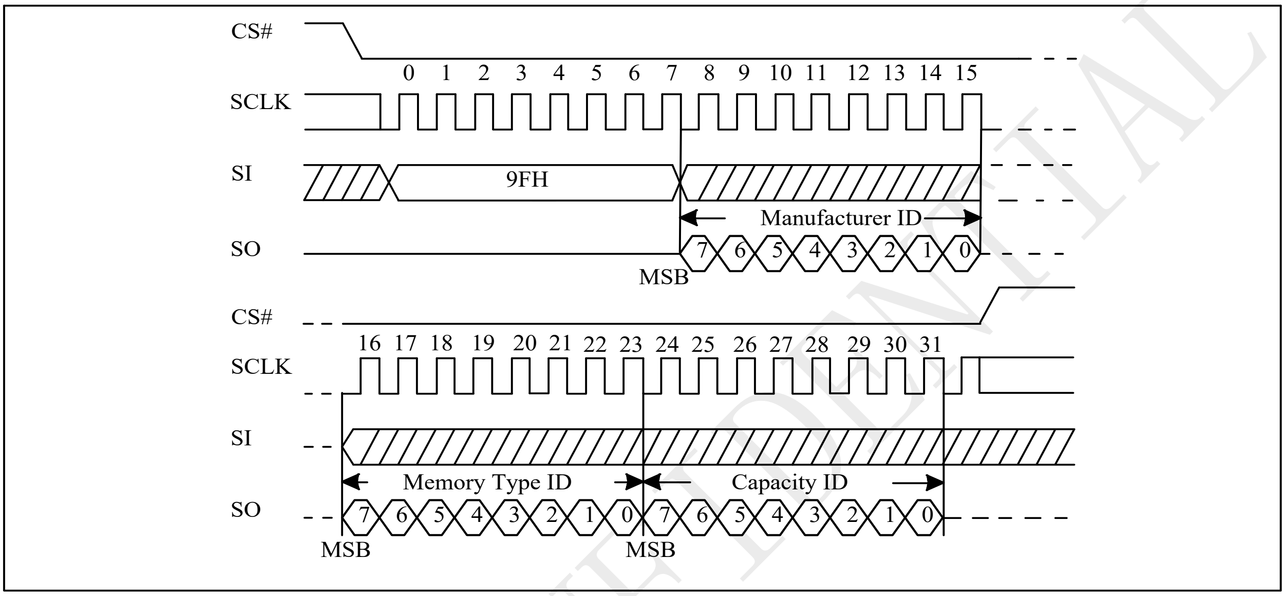


Figure 10-46a Read Identification (RDID) Sequence (QPI)

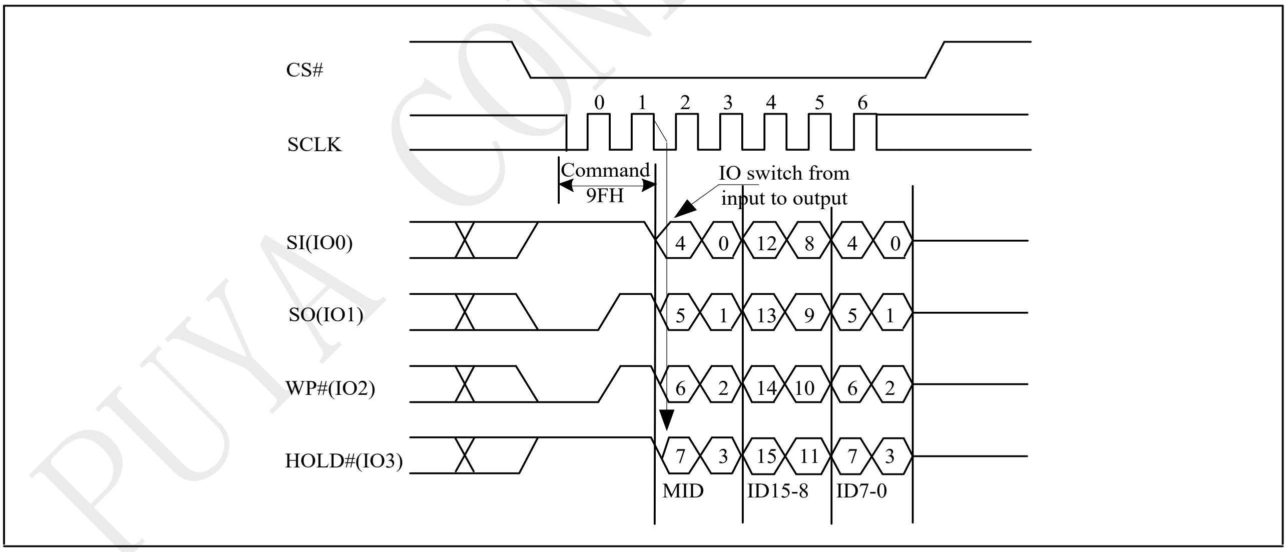


Table ID Definitions

P25Q16SH	RDID command	manufacturer ID	memory type	memory density
		85	60	15
	RES command	electronic ID		
		14		
	REMS command	manufacturer ID		device ID
		85		14

10.47 Program/Erase Suspend/Resume

The Suspend instruction interrupts a Page Program, Page Erase, Sector Erase, or Block Erase operation to allow access to the memory array. After the program or erase operation has entered the suspended state, the memory array can be read except for the page(s) being programmed or the page(s) or sector or block being erased.

Readable Area of Memory While a Program or Erase Operation is Suspended

Suspended Operation	Readable Region of Memory Array
Page(s) Program	All but the Page(s) being programmed
Page(s) Erase	All but the Page(s) being erased
Sector Erase(4KB)	All but the 4KB Sector being erased
Block Erase(32KB)	All but the 32KB Block being erased
Block Erase(64KB)	All but the 64KB Block being erased

When the Serial NOR Flash receives the Suspend instruction, there is a latency of tPSL or tESL before the Write Enable Latch (WEL) bit clears to “0” and the SUS sets to “1”, after which the device is ready to accept one of the commands listed in "Table Acceptable Commands During Program/Erase Suspend after tPSL/tESL" (e.g. FAST READ). Refer to " AC Characteristics" for tPSL and tESL timings. "Table Acceptable Commands During Suspend (tPSL/tESL not required)" lists the commands for which the tPSL and tESL latencies do not apply. For example, RDSR, RDSCUR, RSTEN, and RST can be issued at any time after the Suspend instruction.

Status Register bit 15 (SUS) can be read to check the suspend status. The SUS (Program/Erase Suspend Bit) sets to “1” when a program or erase operation is suspended. The SUS clears to “0” when the program or erase operation is resumed.

Acceptable Commands During Program/Erase Suspend after tPSL/tESL

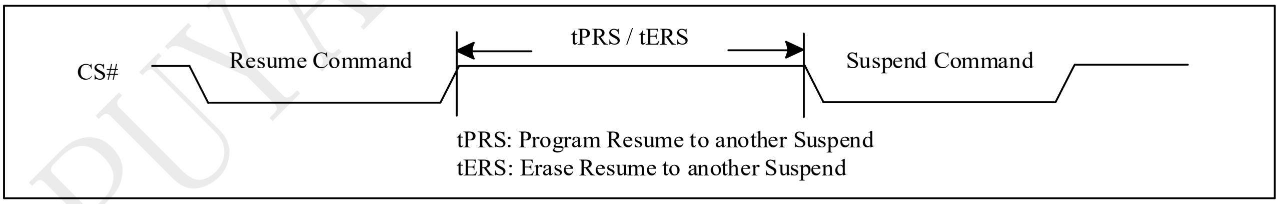
Command name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
READ	03H	•	•
FAST READ	0BH	•	•
DTRFRD	0DH	•	•
DREAD	3BH	•	•
QREAD	6BH	•	•
2READ	BBH	•	•
2DTRD	BDH	•	•
4READ	EBH	•	•
Word read	E7H	•	•
4DTRD	EDH	•	•
Burst Read with Wrap	0CH	•	•
DTR Burst Read with Wrap	0EH	•	•
QPIEN	38H	•	•
Disable QPI	FFH	•	•
RDSFDP	5AH	•	•
RDID	9FH	•	•
REMS	90H	•	•
DREMS	92H	•	•
QREMS	94H	•	•
SBL	77H	•	•

Command name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
Set Read Parameter	C0H	•	•
WREN	06H		•
RESUME	7AH	•	•
PP	02H		•
QPP	32H		•
Erase Security Registers	44H		
Program Security Registers	42H		•
read Security Registers	48H	•	•
Buffer clear	9EH		•
Buffer load	9AH		•
Buffer read	9BH	•	•
Buffer write	9CH		•
Buffer to memory program	9DH		•
Individual Block Lock	36H		
Individual Block Unlock	39H		•
Read Block Lock Status	3DH	•	•
Global Block Lock	7EH		
Global Block Unlock	98H		•

Acceptable Commands During Suspend（tPSL/tESL not required）

Command name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
WRDI	04H	•	•
RDSR	05H	•	•
RDSR2	35H	•	•
RES	ABH	•	•
RSTEN	66H	•	•
RST	99H	•	•
NOP	00H	•	•

Figure 10-47 Resume to Suspend Latency



tPRS: Program Resume to another Suspend
tERS: Erase Resume to another Suspend

10.48 Erase Suspend to Program

The “Erase Suspend to Program” feature allows Page Programming while an erase operation is suspended. Page Programming is permitted in any unprotected memory except within the sector of a suspended Sector Erase operation or within the block of a suspended Block Erase operation. The Write Enable (WREN) instruction must be issued before any Page Program instruction.

A Page Program operation initiated within a suspended erase cannot itself be suspended and must be allowed to finish before the suspended erase can be resumed. The Status Register can be polled to determine the status of the Page Program operation. The WEL and WIP bits of the Status Register will remain “1” while the Page Program operation is in progress and will both clear to “0” when the Page Program operation completes.

Figure 10-48 Suspend to Read/Program Latency

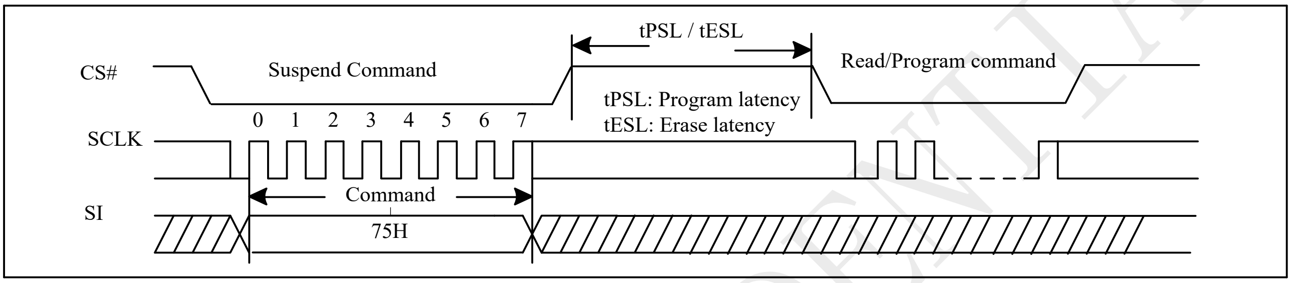
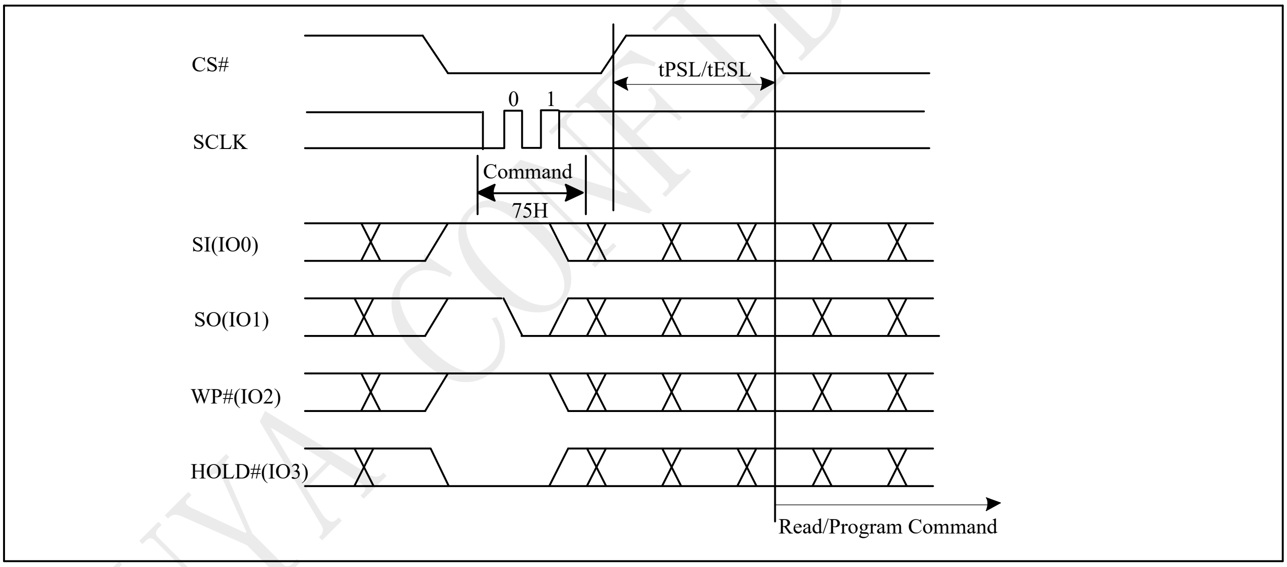


Figure 10-48a Suspend to Read/Program Latency(QPI)



Note:
1. Please note that Program only available after the Erase-Suspend operation
2. To check suspend ready information, please read status register bit15 (SUS2) and bit10(SUS1)

10.49 Program Resume and Erase Resume

The Resume instruction resumes a suspended Page Program, Page Erase, Sector Erase, or Block Erase operation. Before issuing the Resume instruction to restart a suspended erase operation, make sure that there is no Page Program operation in progress.

Immediately after the Serial NOR Flash receives the Resume instruction, the WEL and WIP bits are set to “1” and the SUS2 or SUS1 is cleared to “0”. The program or erase operation will continue until finished ("Resume to Read Latency") or until another Suspend instruction is received. A resume-to-suspend latency of tPRS or tERS must be observed before issuing another Suspend instruction ("Resume to Suspend Latency").

Figure 10-49 Resume to Read Latency

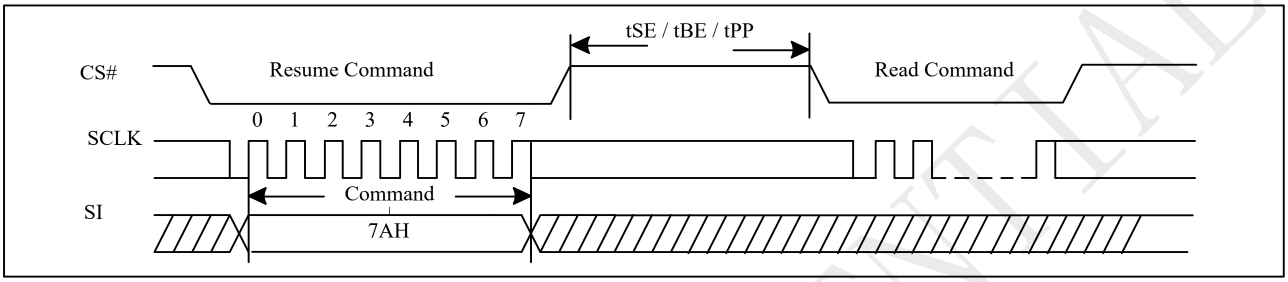
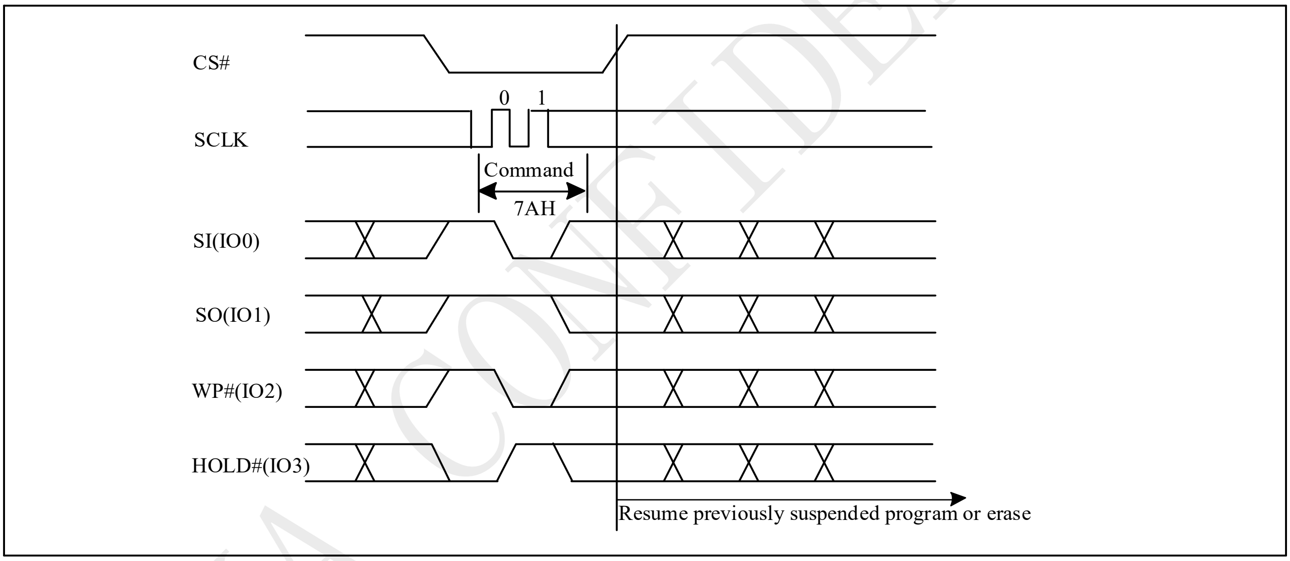


Figure 10-49a Resume to Read Latency(QPI)



10.50 No Operation (NOP)

The "No Operation" command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

The SIO[3:1] are don't care.

10.51 Individual Block Lock (SBLK)

The Individual Block Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block Locks, the WPS bit in Configure Register must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, BP[4:0] bits in the Status Registers. The Individual Block Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

The SBLK instruction is for write protection a specified block (or sector) of memory, using AMAX-A16 or (AMAX-A12) address bits to assign a 64Kbyte block (or 4K bytes sector) to be protected as read only.

The WREN (Write Enable) instruction is required before issuing SBLK instruction.

The sequence of issuing SBLK instruction is: CS# goes low → send SBLK (36h) instruction→ send 3-byte address assign one block (or sector) to be protected on SI pin → CS# goes high. The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not be executed.

Figure 10-51 Individual Block Lock(Command 36H)

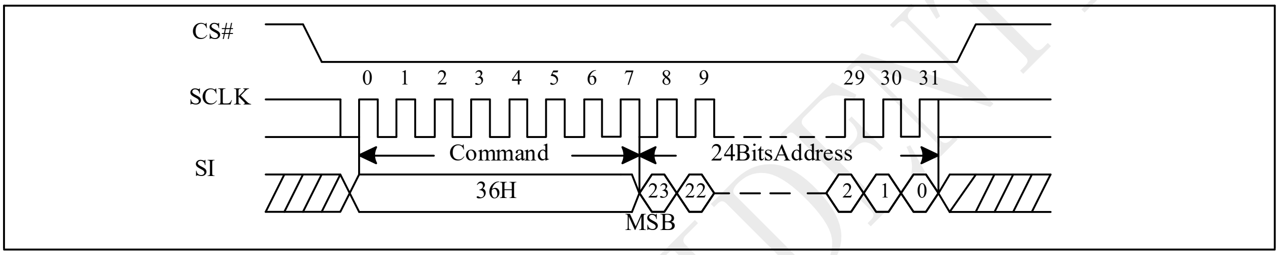
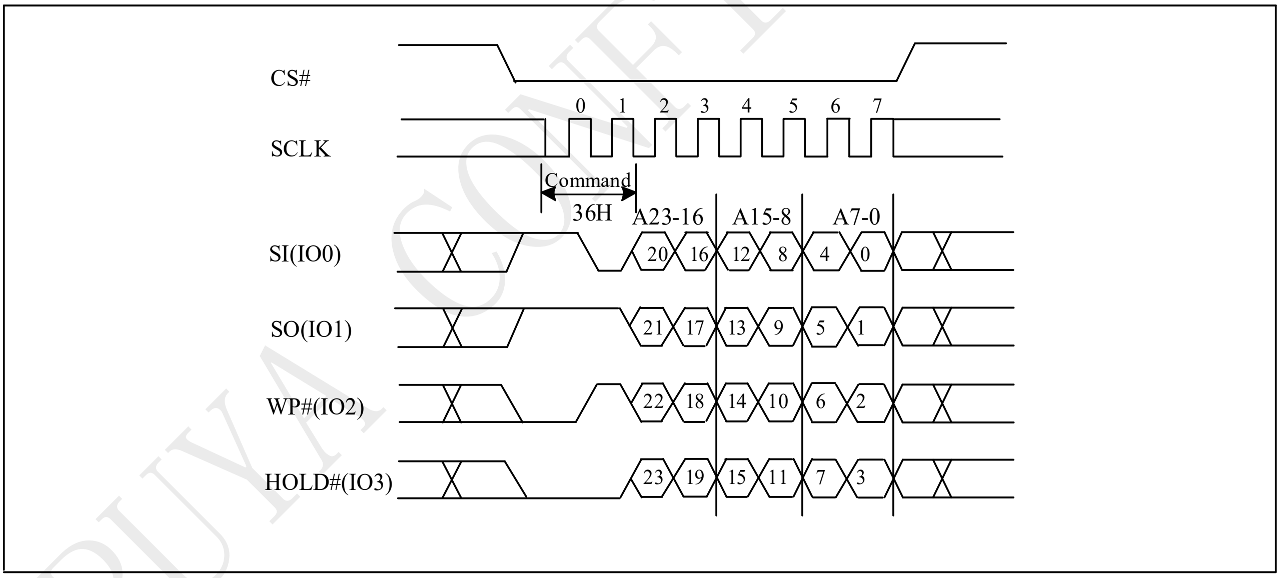


Figure 10-51a Individual Block Lock(QPI)



10.52 Individual Block Unlock (SBULK)

The Individual Block Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block Locks, the WPS bit in Configure Register must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, BP[4:0] bits in the Status Registers. The Individual Block Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

The SBULK instruction will cancel the block (or sector) write protection state using AMAX-A16 or (AMAX-A12) address bits to assign a 64Kbyte block (or 4K bytes sector) to be unprotected.

The WREN (Write Enable) instruction is required before issuing SBULK instruction.

The sequence of issuing SBULK instruction is: CS# goes low → send SBULK (39h) instruction→ send 3-byte address assign one block (or sector) to be protected on SI pin → CS# goes high. The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not be executed.

Figure 10-52 Individual Block Unlock(Command 39H)

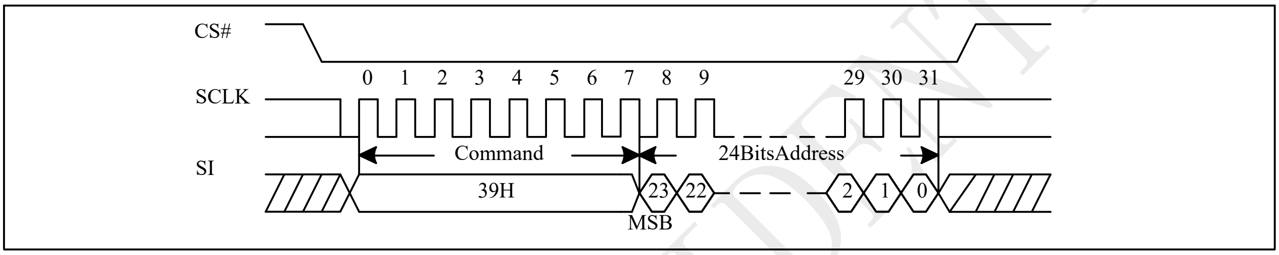
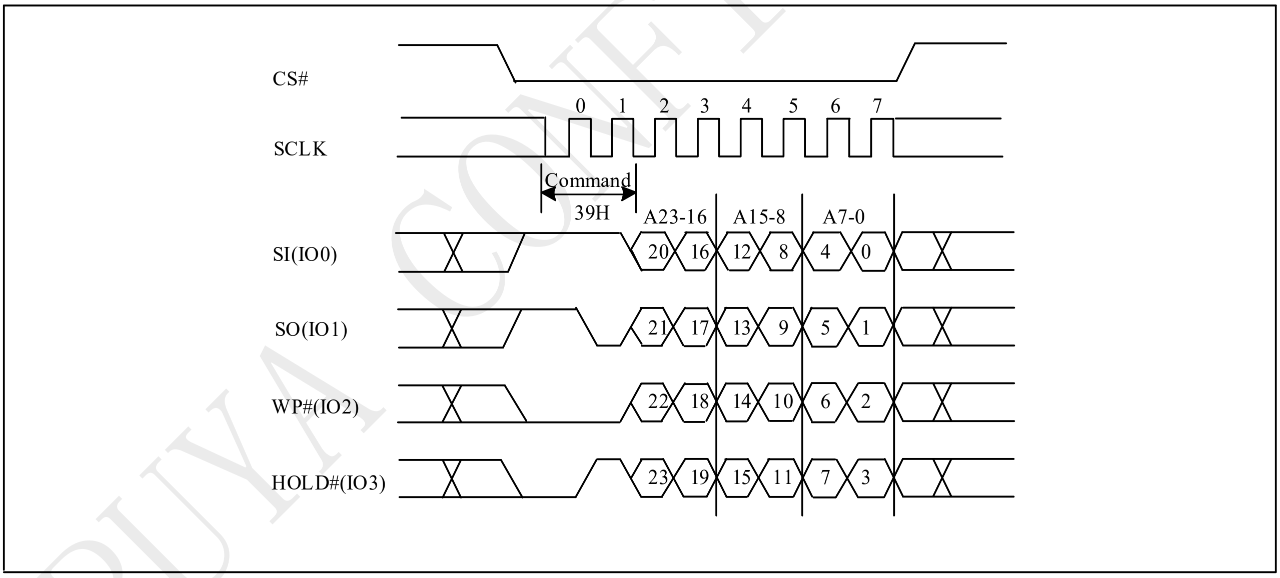


Figure 10-52a Individual Block Unlock(QPI)



10.53 Read Block Lock Status (RDBLK)

The Individual Block Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block Locks, the WPS bit in Configure Register must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, BP[4:0] bits in the Status Registers. The Individual Block Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

The RDBLOCK instruction is for reading the status of protection lock of a specified block (or sector), using AMAX-A16 (or AMAX-A12) address bits to assign a 64K bytes block (4K bytes sector) and read protection lock status bit which the first byte of Read-out cycle. The status bit is"1" to indicate that this block has be protected, that user can read only but cannot write/program /erase this block. The status bit is "0" to indicate that this block hasn't be protected, and user can read and write this block.

The sequence of issuing RDBLOCK instruction is: CS# goes low → send RDBLOCK (3Dh) instruction → send 3-byte address to assign one block on SI pin → read block's protection lock status bit on SO pin → CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction.

Figure 10-53 Read Block Lock Status (Command 3DH)

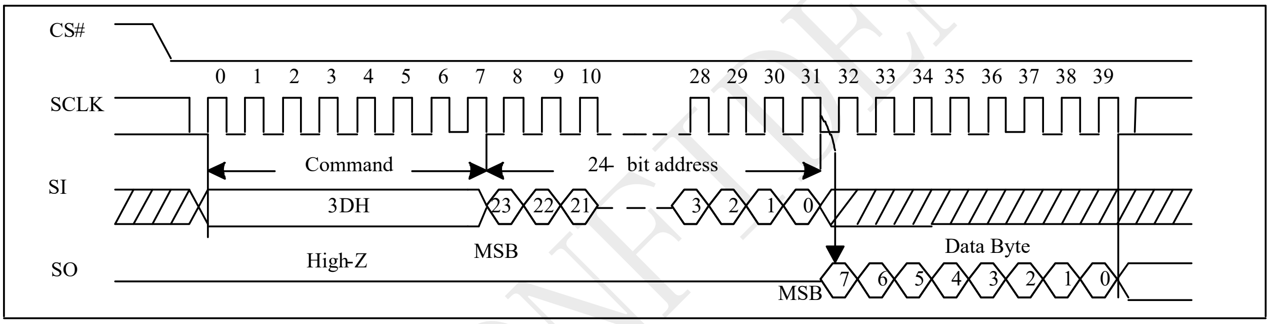
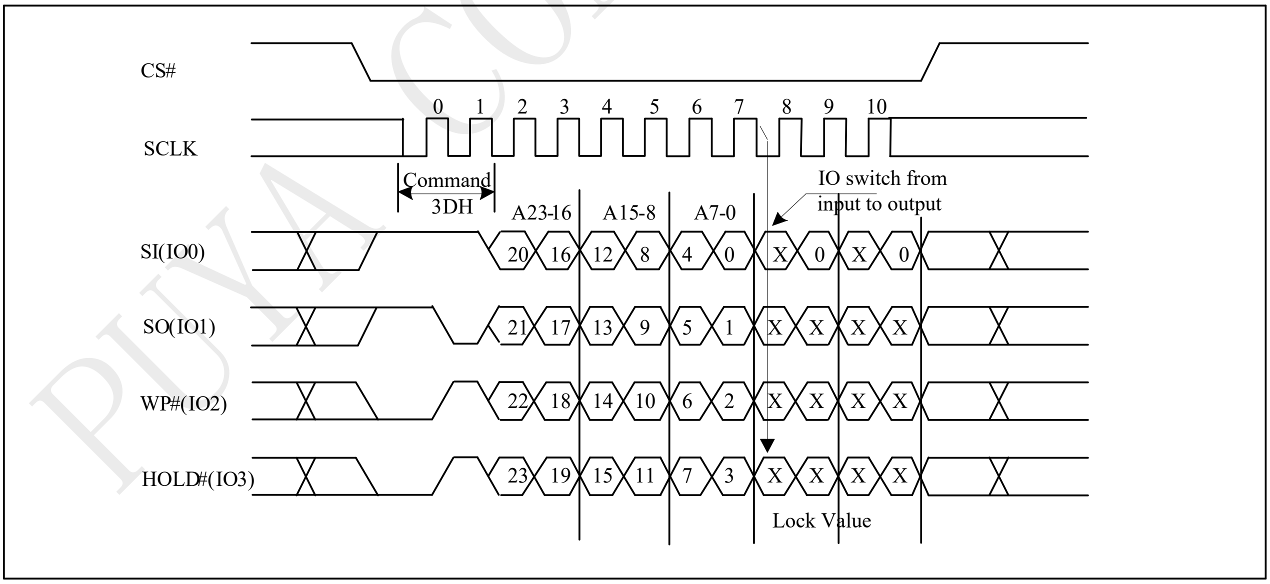


Figure 10-53a Read Block Lock Status (QPI)



10.54 Global Block Lock (GBLK)

The GBLK instruction is for enable the lock protection block of the whole chip. The WREN (Write Enable) instruction is required before issuing GBLK instruction.

The sequence of issuing GBLK instruction is: CS# goes low → send GBLK (7Eh) instruction →CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

The CS# must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

Figure 10-54 Global Block Lock (Command 7EH)

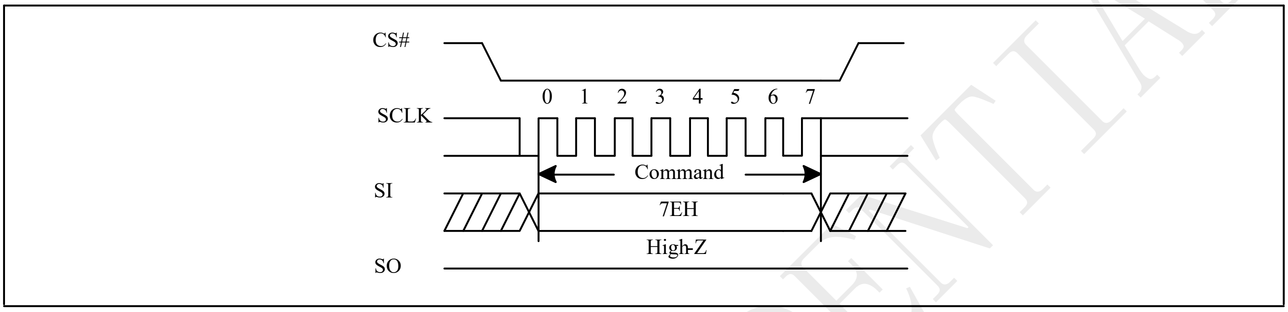
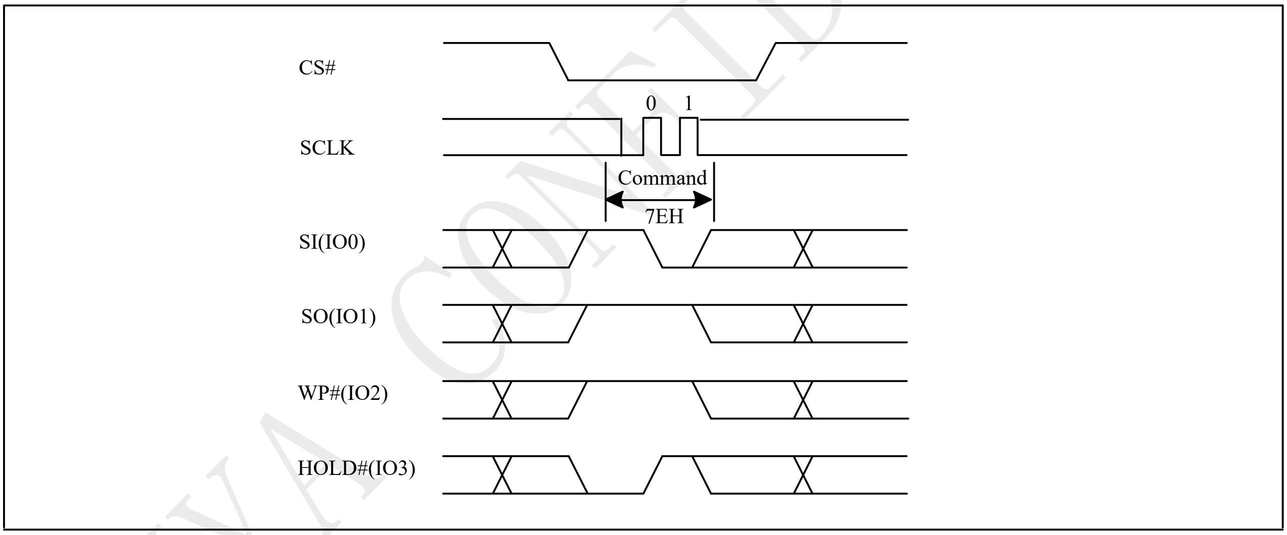


Figure 10-54a Global Block Lock(QPI)



10.55 Global Block Unlock (GBULK)

The GBULK instruction is for disable the lock protection block of the whole chip. The WREN (Write Enable) instruction is required before issuing GBULK instruction.

The sequence of issuing GBULK instruction is: CS# goes low → send GBULK (98h) instruction →CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

The CS# must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

Figure 10-55 Global Block Unlock (Command 98H)

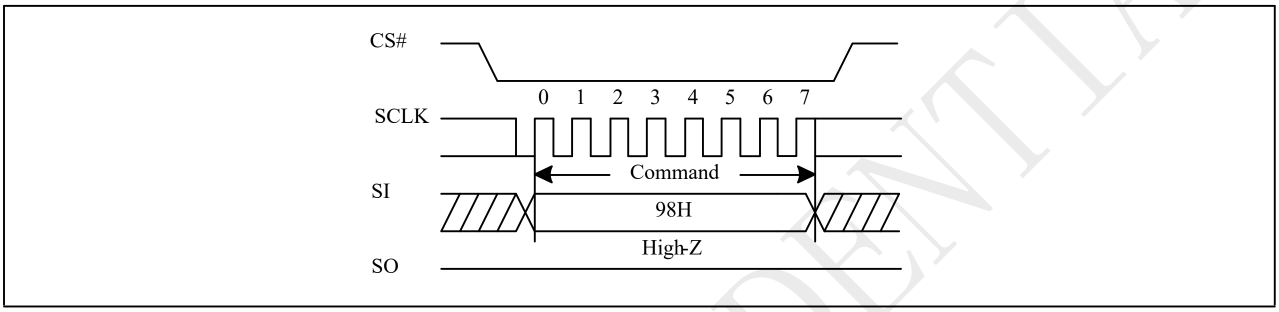
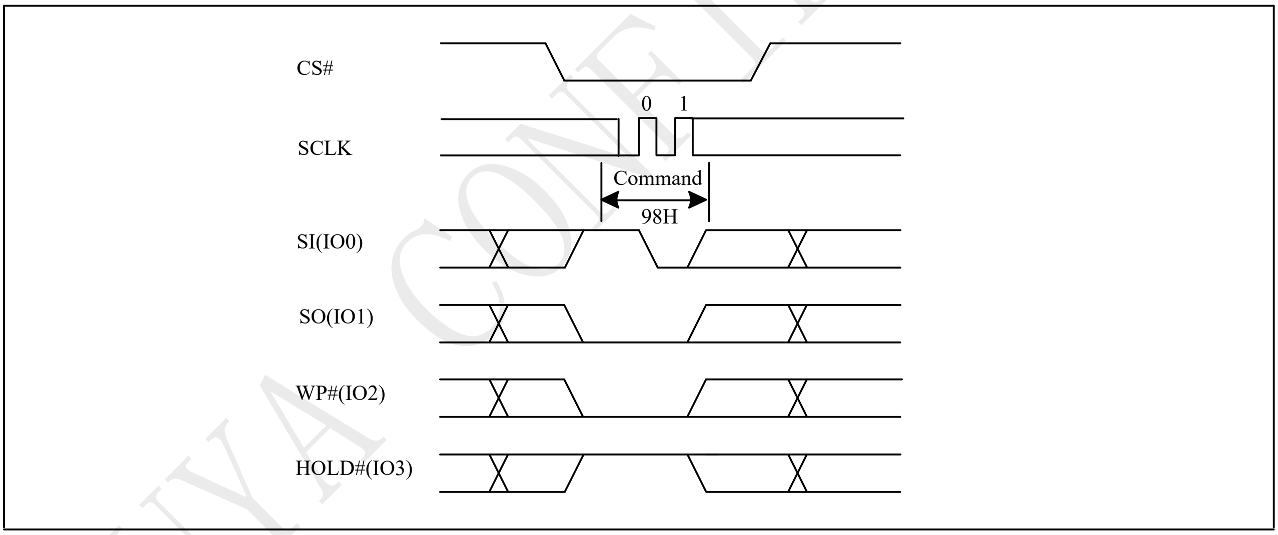


Figure 10-55a Global Block Unlock(QPI)



10.56 Software Reset (RSTEN/RST)

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to a standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on, except the EP_FAIL bit.

To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

The SIO[3:1] are "don't care".

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

Figure 10-56 Software Reset Recovery

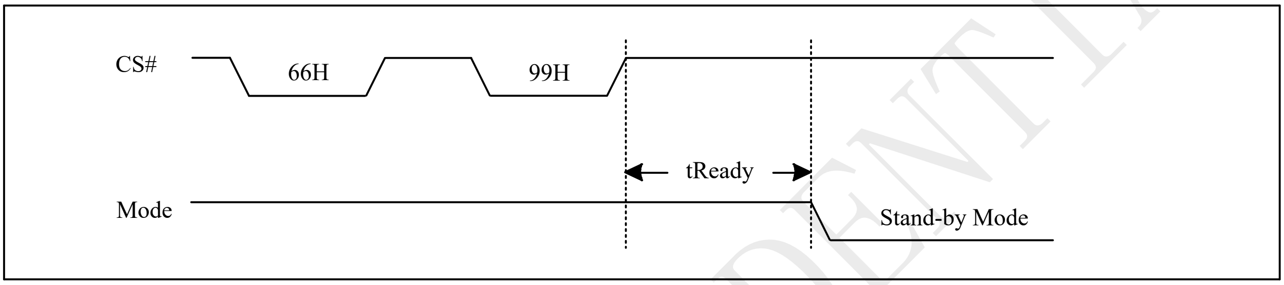


Figure 10-56a Reset Sequence

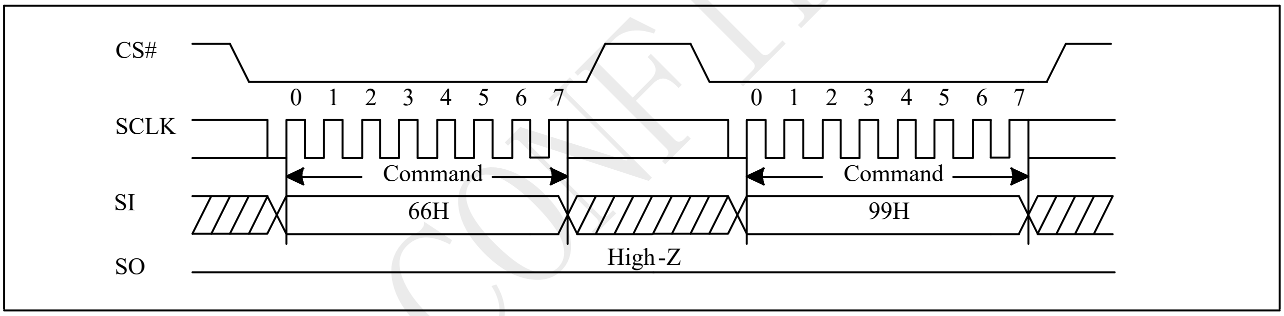
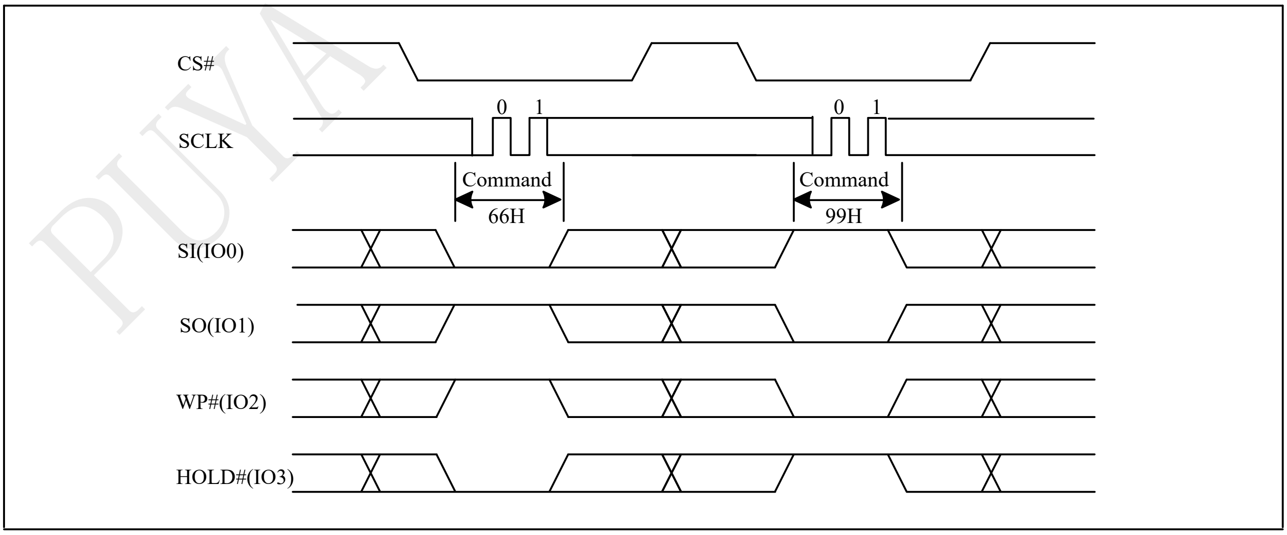


Figure 10-56b Reset Sequence(QPI)



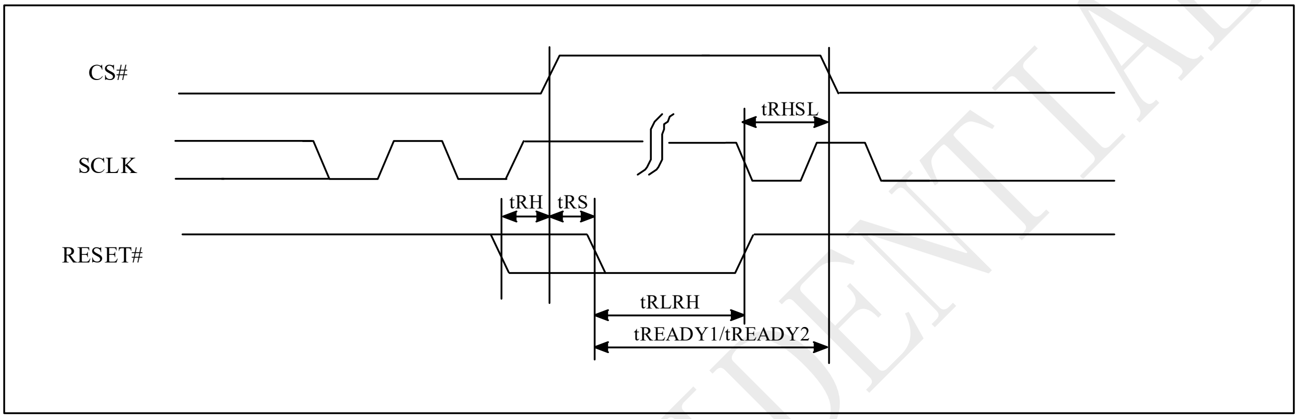
10.57 RESET

Driving the RESET# pin low for a period of tRLRH or longer will reset the device. After reset cycle, the device is at the following states:

- Standby mode
- All the volatile bits such as WEL/WIP/SRAM lock bit will return to the default status as power on.

If the device is under programming or erasing, driving the RESET# pin low will also terminate the operation and data could be lost. During the resetting cycle, the SO data becomes high impedance and the current will be reduced to minimum.

Figure 10-57 RESET Timing



RESET Timing (Power On)

Symbol	Parameter	Min	Typ	Max	Unist
tRHSL	Reset# high before CS# low	10			us
tRS	Reset# setup time	150			ns
tRH	Reset# hold time	150			ns
tRLRH	Reset# low pulse width	10			us
tREADY1	Reset Recovery time			30	us

RESET Timing (Other Operation)

Symbol	Parameter	Min	Typ	Max	Units
tRHSL	Reset# high before CS# low	10			us
tRS	Reset# setup time	150			ns
tRH	Reset# hold time	150			ns
tRLRH	Reset# low pulse width	10			us
tREADY2	Reset Recovery time (except WRSR/WRCR)			30	us
	Reset Recovery time (for WRSR/WRCR)			12	ms

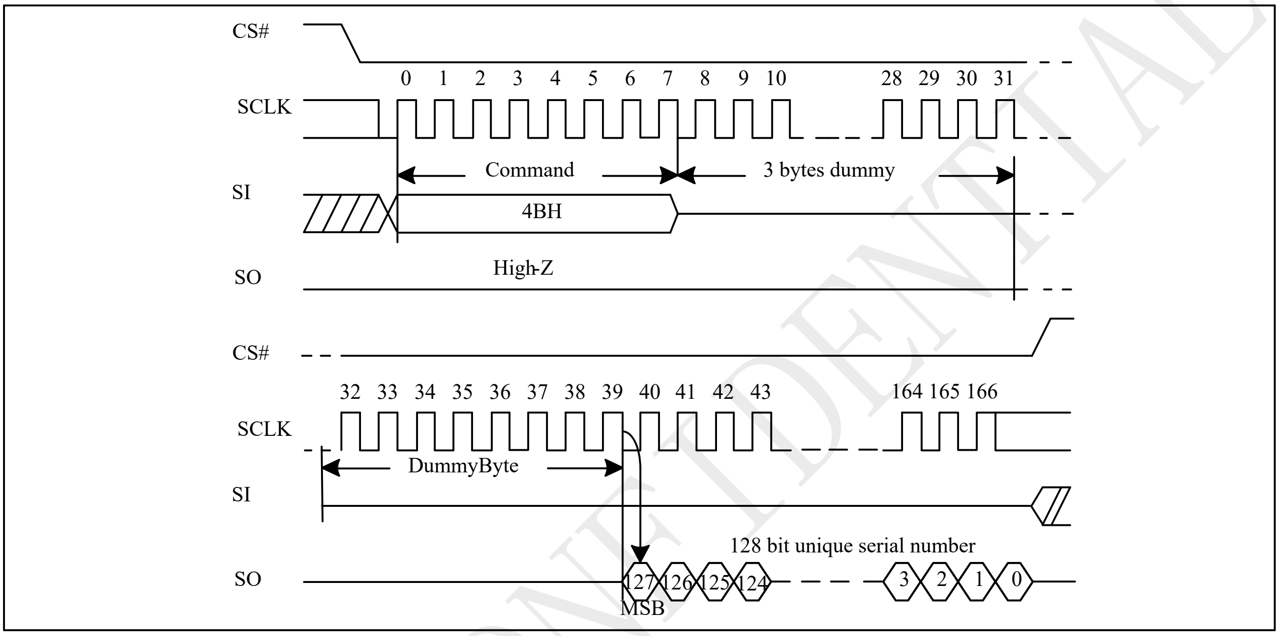
10.58 Read Unique ID (RUID)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each P25QSxx device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command →Dummy Byte1 →Dummy Byte2 →Dummy Byte3 → Dummy Byte4 → 128bit Unique ID Out → CS# goes high.

The command sequence is show below.

Figure 10-58 Read Unique ID (RUID) Sequence (Command 4B)



10.59 Read SFDP Mode (RDSFDP)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is same as FREAD: CS# goes low→ send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→ send 1 dummy byte on SI pin→ read SFDP code on SO→ to end RDSFDP operation can use CS# to high at any time during data out.

Detail SFDP data please contact Puya.

Figure 10-59 Read Serial Flash Discoverable Parameter (RDSFDP) Sequence

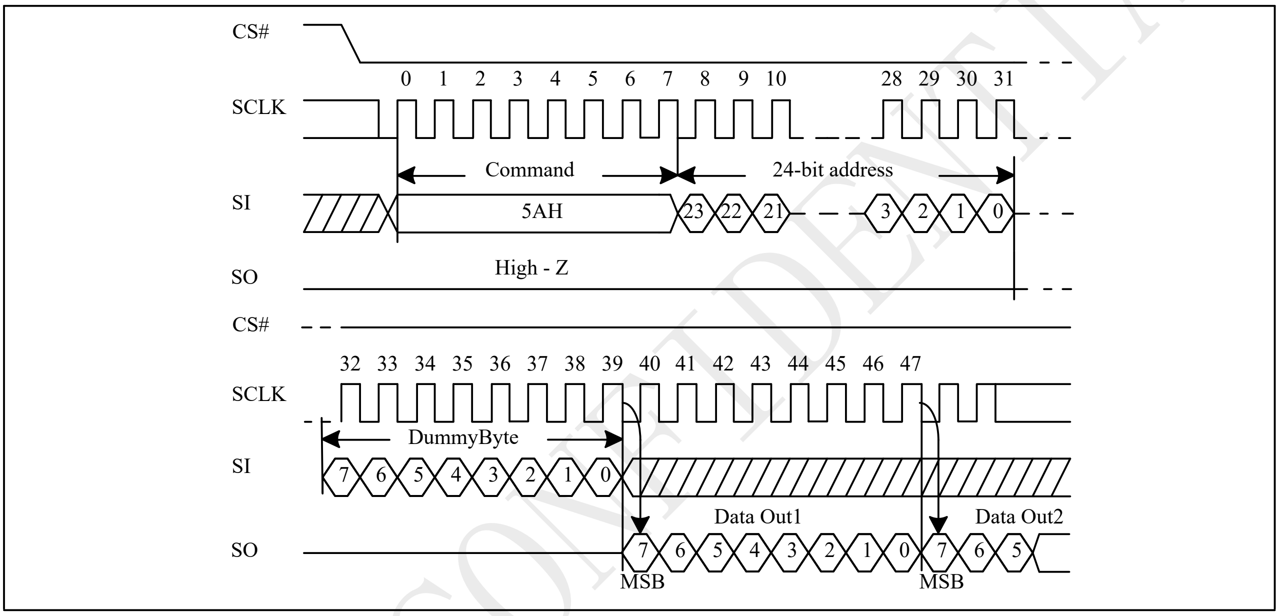
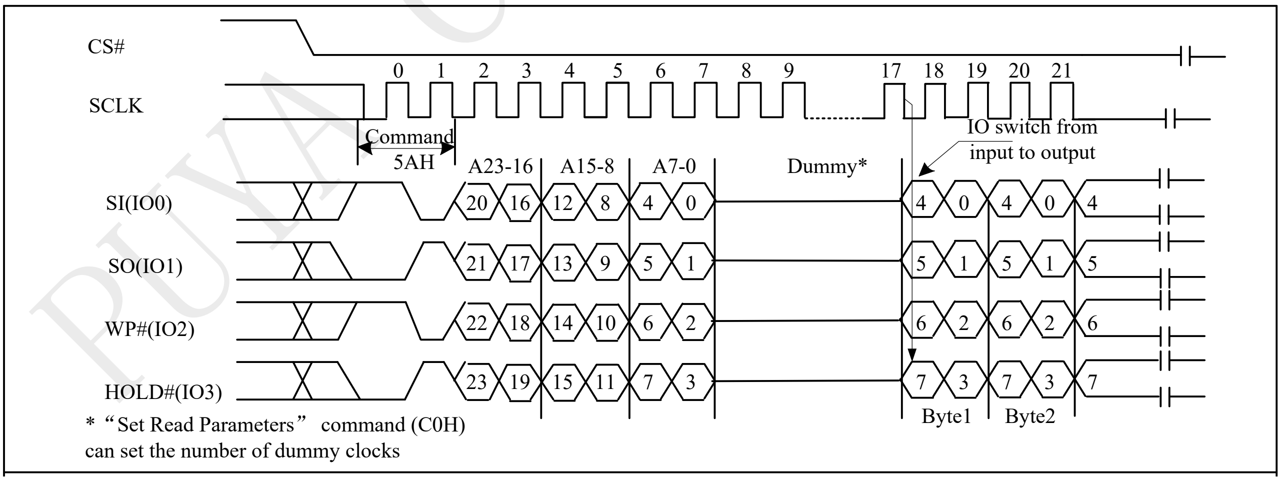


Figure 10-59a Read Serial Flash Discoverable Parameter (RDSFDP) Sequence(QPI)



11 Ordering Information

P 25 Q 16S H A - SS H - I T - x

Company Designator

P = Puya Semiconductor

Product Family

25 = SPI interface flash

Product Serial

Q = Q serial

Memory Density

16S = new version 16Mb

Operation Voltage

H = 2.3V~3.6V

Generation

A = A Version Default = blank

Package Type

SS = SOP8 150mil
SU = SOP8 208mil
NX = USON8 3x4x0.55mm
WF = WAFER
UX = USON8 3x2x0.55mm
TS = TSSOP8
WX = WSON8 6x5x0.75mm
UW = USON8 3x2x0.45mm

Plating Technology

H: RoHS Compliant Halogen free, Antimony free

Device Grade

I =- 40 ~ 85C

Packing Type

T = TUBE
R = TAPE & REEL
Y = TRAY
W = WAFER

Ordering Option

Default = blank

12 Valid Part Numbers and Top Marking

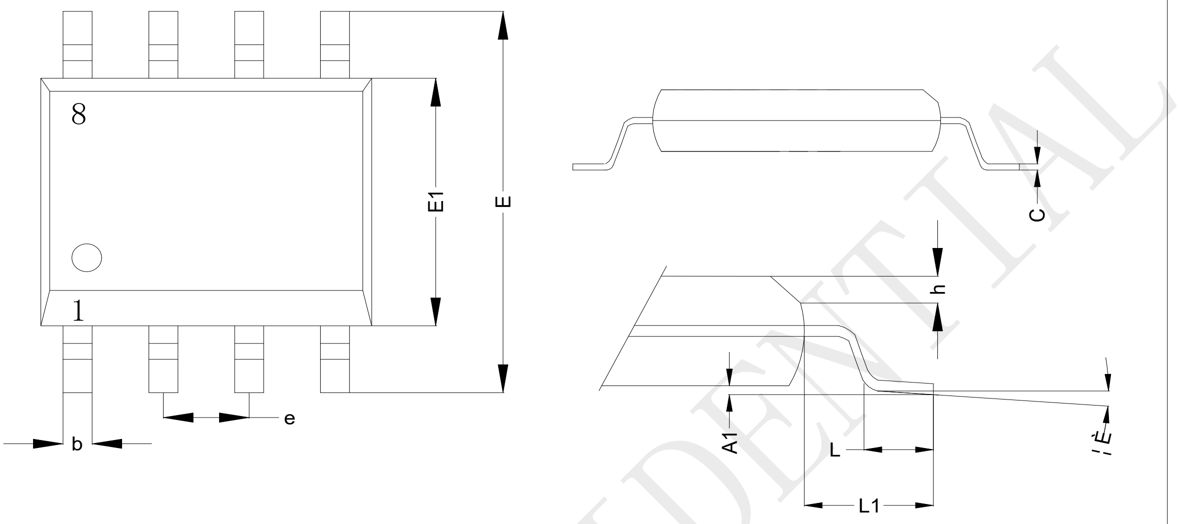
The following table provides the valid part numbers for the P25Q16SH Flash Memory. Please contact PUYA for specific availability by density and package type. PUYA Flash memories use a 15-digit Product Number for ordering.

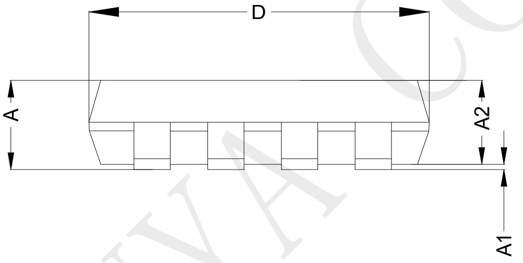
Package Type	Product Number	Density	Top Side Marking	Temp.	Packing Type
SS SOP8 150mil	P25Q16SH-SSH-IT	16M-bit	P25Q16SH xxxxxxx	85C	Tube
SS SOP8 150mil	P25Q16SH-SSH-IR	16M-bit	P25Q16SH xxxxxxx	85C	Reel
SU SOP8 208mil	P25Q16SH-SUH-IT	16M-bit	P25Q16SH xxxxxxx	85C	Tube
SU SOP8 208mil	P25Q16SH-SUH-IR	16M-bit	P25Q16SH xxxxxxx	85C	Reel
TS TSSOP8	P25Q16SH-TSH-IT	16M-bit	P25Q16SH xxxxxxx	85C	Reel
TS TSSOP8	P25Q16SH-TSH-IR	16M-bit	P25Q16SH xxxxxxx	85C	Reel
UX USON8 3x2x0.55mm	P25Q16SH-UXH-IR	16M-bit	PQ16S Hxxx	85C	Reel
NX* USON8 3x4mm	P25Q16SH-NXH-IR	16M-bit	PQ16S Hxxx	85C	Reel
WX* WSON8 6x5mm	P25Q16SH-WXH-IR	16M-bit	P25Q16SH xxxxxxx	85C	Reel
UW* USON8 3x2x0.45mm	P25Q16SH-UWH-IR	16M-bit	PQ16S Hxxx	85C	Reel

Note：The package marked with "*", if necessary, please contact Puya sales.

13 Package Information

13.1 8-Lead SOP(150mil)





Common Dimensions

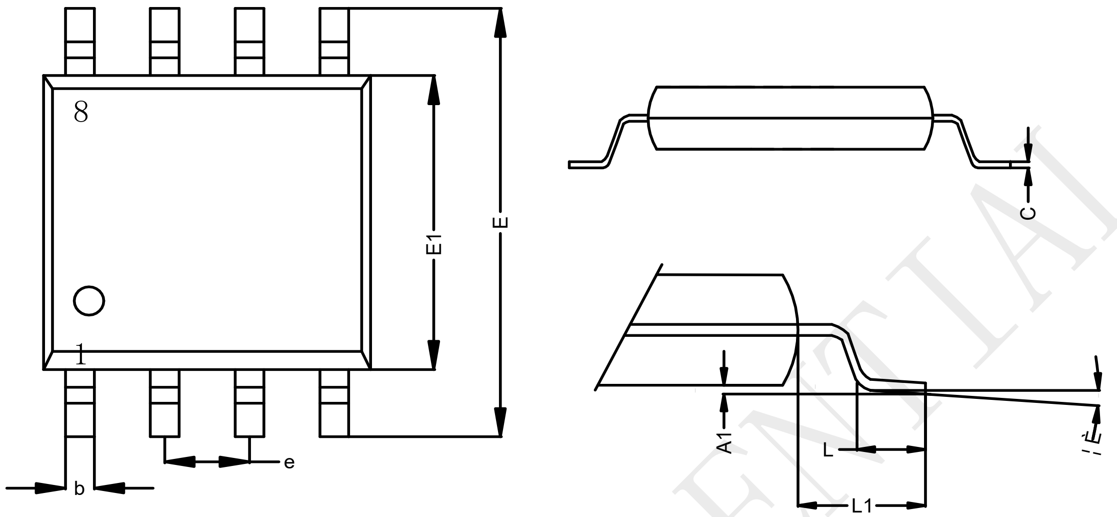
(Unit of Measure=millimeters)

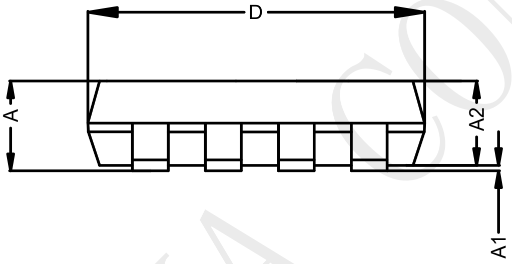
Symbol	Min	Typ	Max
A	1.350	-	1.750
A1	0.100	-	0.250
A2	1.250	-	-
b	0.310	-	0.510
c	0.170	-	0.250
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	-	1.270	-
L	0.400	-	1.270
L1	-	1.050	-
¦È	0	-	8¡ã
h	0.25	-	0.50

Note： 1. Dimensions are not to scale

PUYA	TITLE Puya SOP8（150mil）POD	DRAWING NO. QRPD-0004	REV 1.1

13.2 8-Lead SOP(208mil)





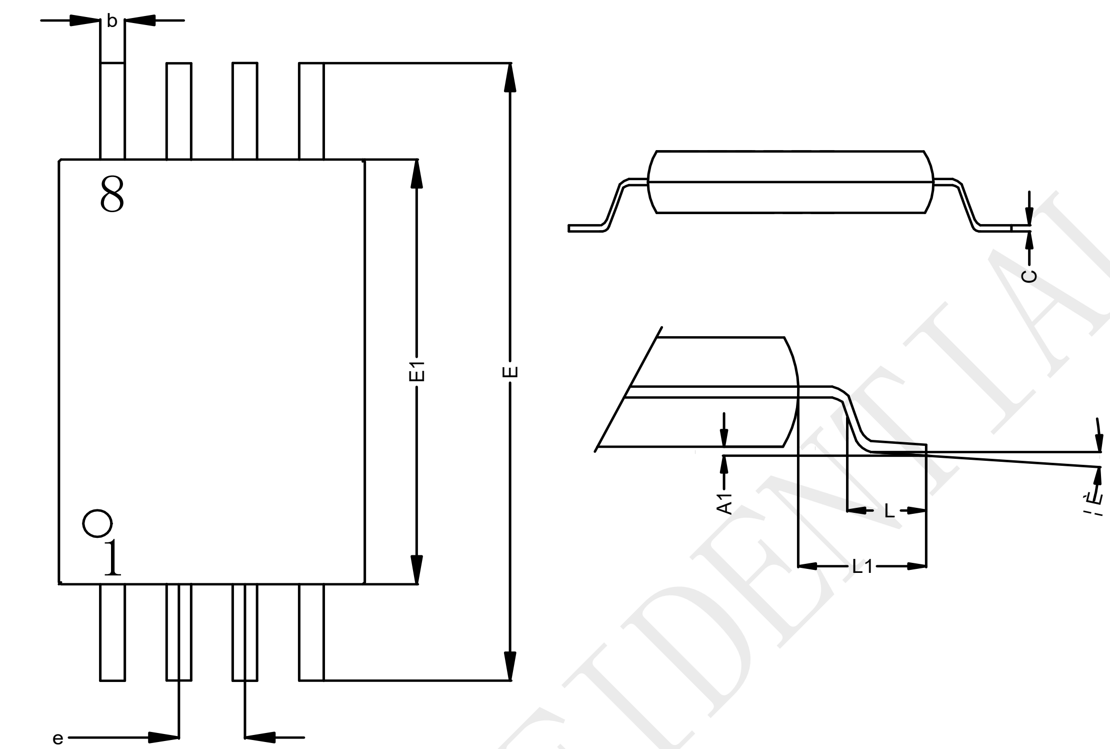
Common Dimensions
(Unit of Measure=millimeters)

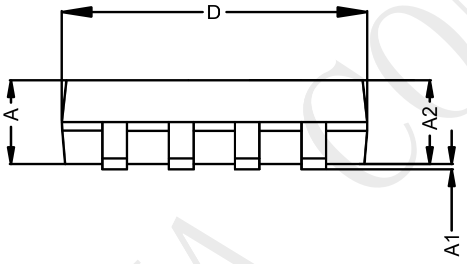
Symbol	Min	Typ	Max
A	-	-	2.150
A1	0.050	-	0.250
A2	1.700	-	1.900
b	0.310	-	0.510
c	0.150	-	0.250
D	5.130	5.230	5.330
E	7.800	7.900	8.000
E1	5.180	5.280	5.380
e	-	1.270	-
L	0.500	-	0.800
L1	-	1.310	-
¦È	0	-	8¡ã

Note：1. Dimensions are not to scale

PUYA	TITLE Puya SOP8(208MIL) POD	DRAWING NO. QRPD-0005	REV 1.0

13.3 8-Lead TSSOP





Common Dimensions

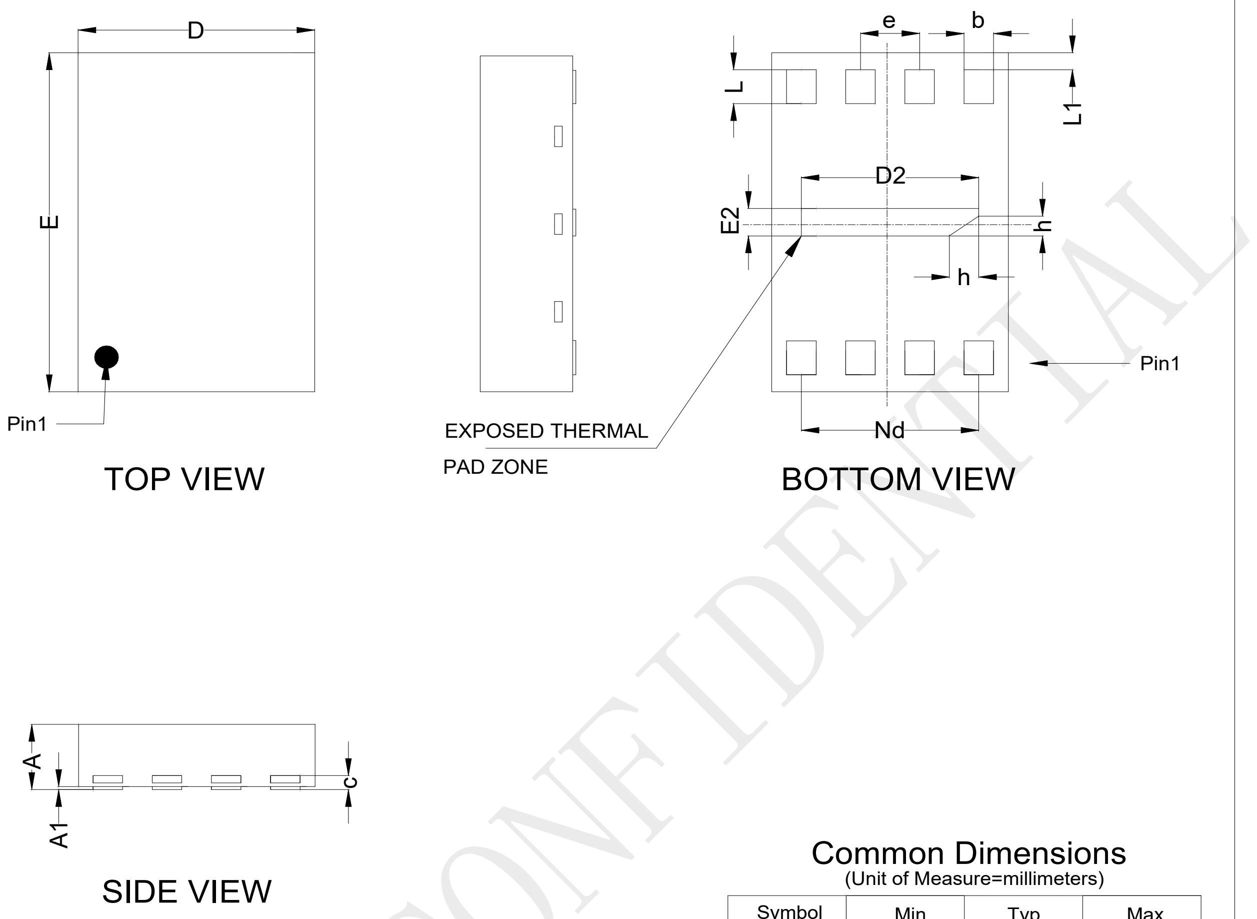
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	1.000	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	2.900	3.000	3.100
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e	-	0.650	-
L	0.450	-	0.750
L1	-	1.000	-
¦È	0	-	8¡ã

Note： 1. Dimensions are not to scale

PUYA	TITLE PUYA TSSOP8 POD	DRAWING NO. QRPD-0019	REV 1.0

13.4 8-Pad USON(3x2x0.55mm)



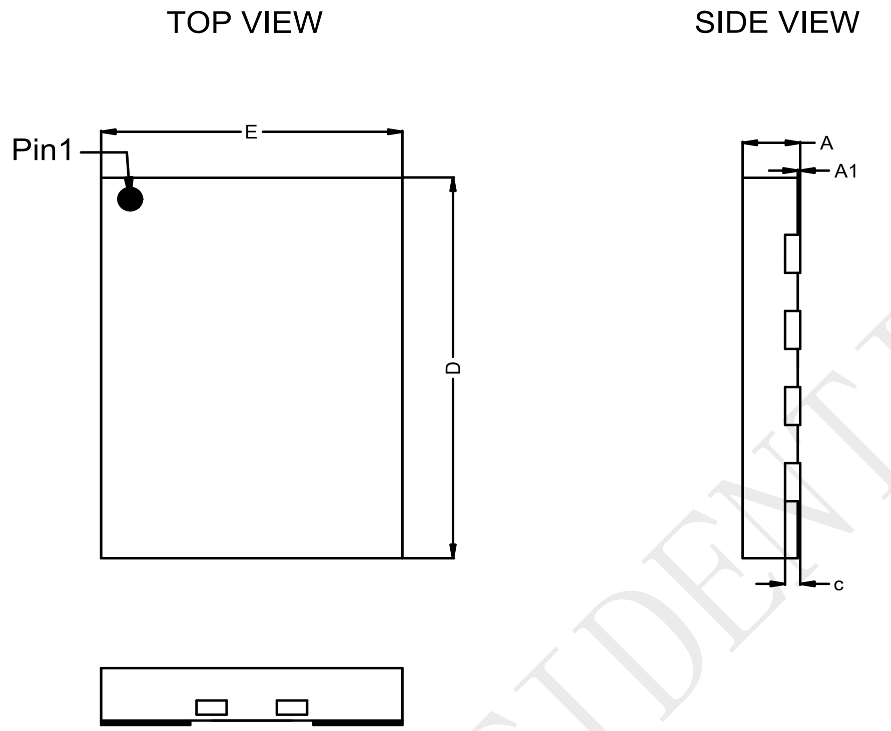
Common Dimensions
(Unit of Measure=millimeters)

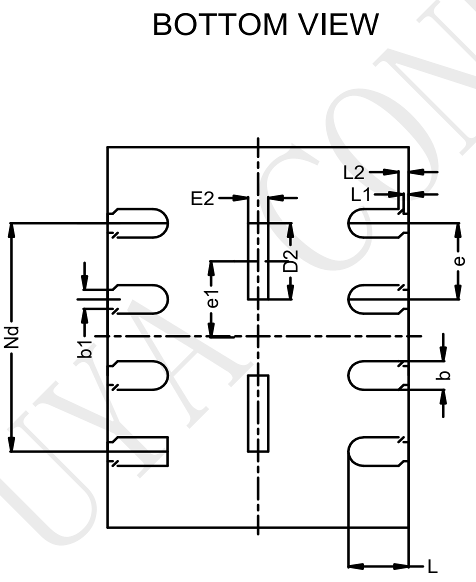
Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	2.90	3.00	3.10
E2	0.10	0.20	0.30
e	0.50BSC		
L	0.30	0.35	0.40
h	0.05	0.15	0.25
Nd		1.50BSC	
L1	0.05	0.10	0.15
c	0.10	0.15	0.20

Note：1. Dimensions are not to scale

PUYA	TITLE Puya USON8L 2x3x0.55-0.5PITCH POD	DRAWING NO. QRPD-0009	REV 1.0

13.5 8-Pad USON(3x4x0.55mm)





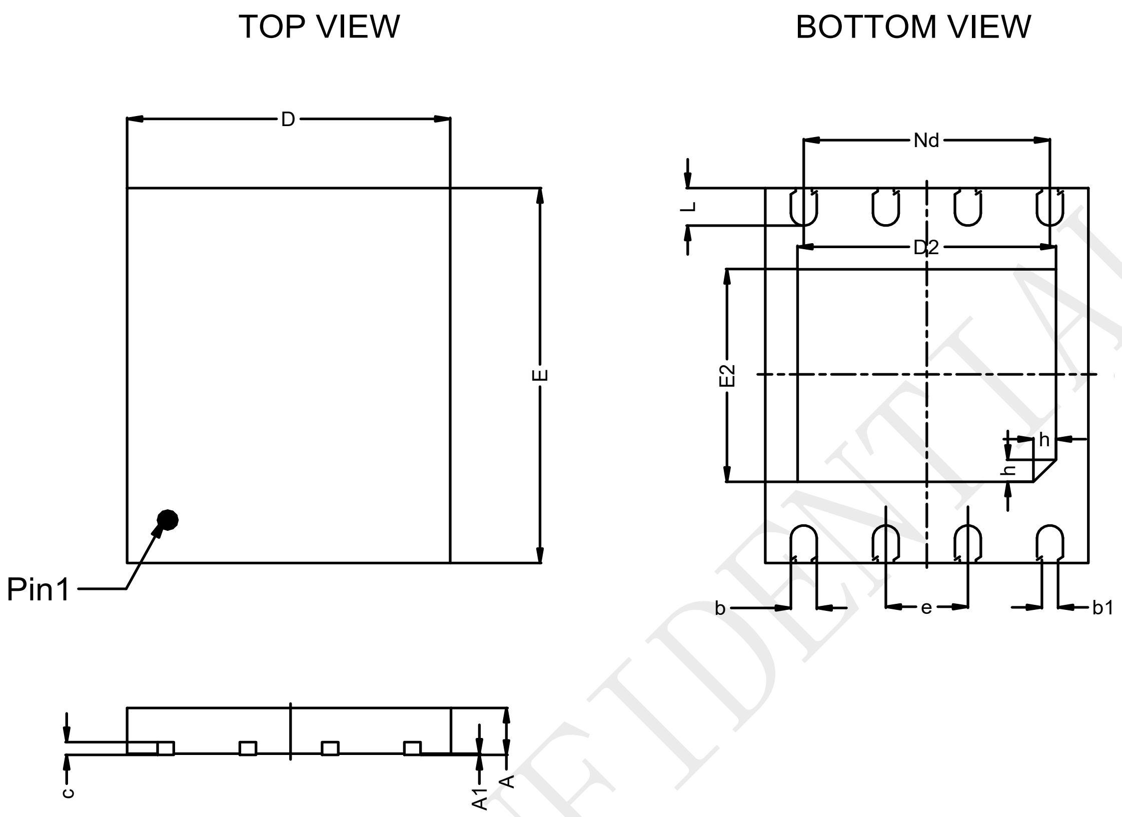
Common Dimensions
(Unit of Measure=millimeters)

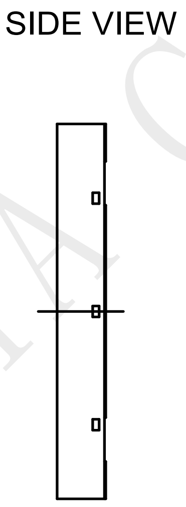
Symbol	Min	Typ	Max
A	0.500	0.550	0.600
A1	0.000	0.020	0.050
b	0.250	0.300	0.350
D	3.900	4.000	4.100
D2	0.700	0.800	0.900
E	2.900	3.000	3.100
E2	0.100	0.200	0.300
e	-	0.800BCS	-
L	0.550	0.600	0.650
c	0.100	0.150	0.200
Nd	-	2.400BCS	-
L1		0.050REF	
b1		0.200REF	
L2		0.100REF	
e1	-	0.800BSC	-

Note： 1. Dimensions are not to scale

PUYA	TITLE Puya USON8L 4x3x0.55-0.8PITCH POD	DRAWING NO. QRPD-0012	REV 1.0

13.6 8-Pad WSON(6x5x0.75mm)





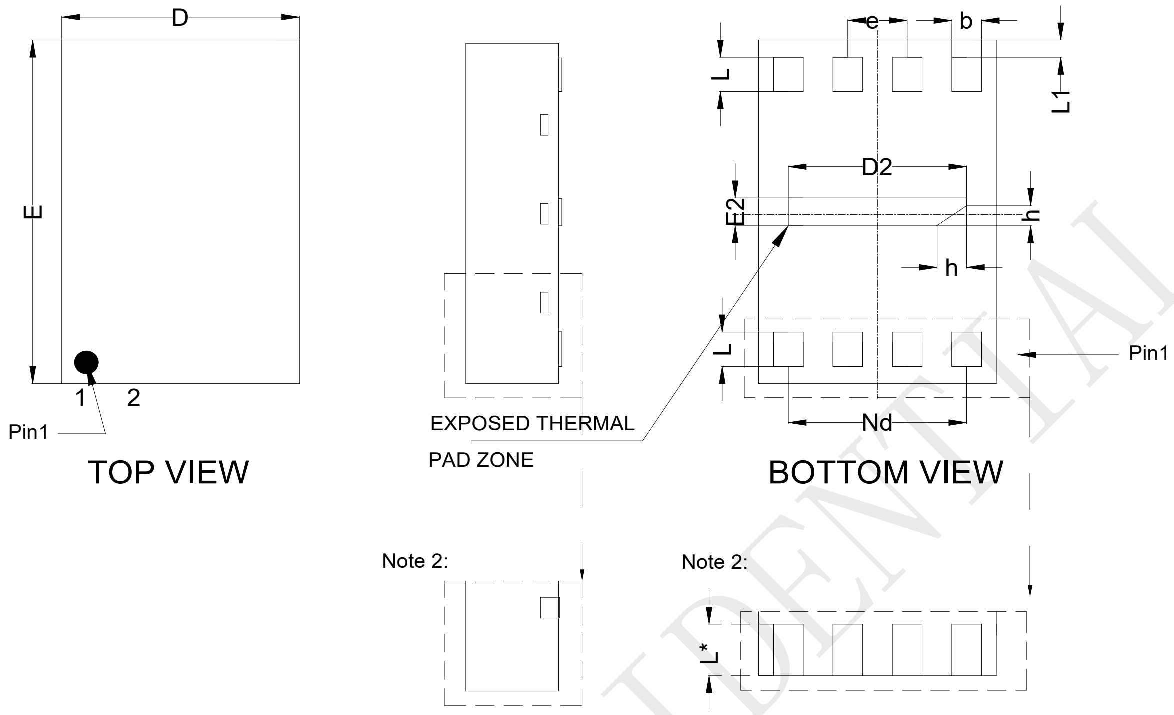
Common Dimensions
(Unit of Measure=millimeters)

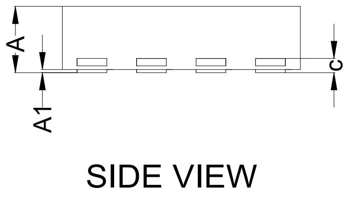
Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.350	0.400	0.450
D	4.900	5.000	5.100
D2	3.900	4.000	4.100
E	5.900	6.000	6.100
E2	3.300	3.400	3.500
e	-	1.27BSC	-
L	0.550	0.600	0.650
c	0.180	0.203	0.250
Nd	-	3.81BSC	-
b1	0.250REF		
h	0.300	0.350	0.400

Note：1. Dimensions are not to scale

PUYA	TITLE Puya WSON8L 6x5X0.75-1.27PITCH POD	DRAWING NO. QRPD-0015	REV 1.0

13.7 8-Pad USON(3x2x0.45mm)





Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.400	0.450	0.500
A1	0.000	0.020	0.050
b	0.180	0.250	0.300
D	1.900	2.000	2.100
D2	1.550	1.600	1.650
E	2.900	3.000	3.100
E2	0.150	0.200	0.250
e	0.500BSC		
L	0.300	0.350	0.400
L*	0.400	0.450	0.500
h	0.050	0.100	0.150
Nd	1.500BSC		
L1	0.050	0.100	0.150
c	0.100	0.150	0.200

Note：1. Dimensions are not to scale
2.Have two lead shape can be compatible with each other

PUYA	TITLE Puya USON8L 2x3x0.45-0.5PITCH POD	DRAWING NO. QRPD-0011	REV 1.1

14 Revision History

Rev.	Date	Description	Note
0.1	2018-08-21	V0.1 datasheet	-
0.2	2019-04-03	Add ordering option "D" for 01H command Add MPM mode 1024 byte Add 9E Buffer clear command Change SUS2(SR10) to EP_FAIL bit at SR1 Change SUS1(SR15) at SR1 to show program & erase suspend Add Valid Part Number	-
1.0	2019-08-05	Update product name to P25Q16SH from P25QS16H Update part AC/DC parameter Change security register size to 1024Bytes Update Acceptable Commands List when suspend	-
1.1	2020-04-30	Update T_{ERS} and T_{PRS} Minimum value	-
1.2	2020-10-20	Update DC Data and Update memory type.	-
1.3	2021-01-20	Add Clock Frequency for WREAD instructions P94 Add RESET Timing Update fSCLK Description	-
1.4	2021-09-26	Update AC parameters	-
1.5	2022-10-26	Update Ultra Low Power Consumption Add VIL Min and VIH Max value Update Absolute Maximum Ratings Update all POD	-
1.6	2023-05-30	Update tReady Max and Min value Update WRSR description Update SS(SOP8 150mil) POD	-
1.7	2024-04-10	Correct type error SLCK->SCLK Move the location of Figure 5-3 Maximum Overshoot Waveform Update ordering information(16MB->16Mb) delete size marking (150mil SOP POD) Update format: delete date and PUYA logo at the homepage; delete directory; update IMPORTANT NOTICE and delete PUYA logo at last page; add PUYA logo in the header	-
1.8	2024-09-24	1.Update AC parameters 2.Delete duplicate description for Max Read Freq 3.Correct timing chart typo 4.Delete SFDP table 5.Update default Drive Strength 6.Add UW(USON8 3x2x0.45mm) package type 7.Update the POD of UX(USON8 3x2x0.55mm)package type	-

1.9	2025-01-06	1.Correct timing chart typo 2.Update RESET timing	-

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