CCD207-40
Back-illuminated 2-Phase IMO Series Electron-multiplying CCD Sensor

FEATURES

- Nominally 1632 x 1608 pixels each 16 µm square
- Full frame operation
- Two-phase Inverted Mode Operation
- Multiplication gain
- Back-illuminated
- Low-noise output circuits

INTRODUCTION

The CCD207-40 is a full frame sensor in the L3VisionTM range of products from e2v Technologies. This device uses a novel output amplifier circuit that is capable of operating at an equivalent output noise of less than one electron at pixel rates of over 15 MHz. The sensor converts photons to charge in the image area during the integration period, then transfers this charge into the readout register. Following transfer through the readout register, the charge is multiplied in the gain register before conversion to a voltage by an output amplifier. The sensor can also operate in inverted mode to suppress dark current, as this is now the dominant noise source (even at short integration times). This makes the sensor well suited to high readout rate imaging, particularly when the focal plane irradiance is low.

The CCD207-40 has 1632(H) x 1608(V) elements. Each element is 16 µm square. The image section is designed to operate in 2-phase mode, in order to achieve the highest parallel transfer frequency.

The CCD207-40 has two different output circuits. There is a large-signal (LS) higher-speed type output at the end of the gain register for when multiplication gain is employed, and a high-responsivity (HR) type output at the end of the normal register for normal CCD operation. Either amplifier can be powered-down by disconnecting the output drain bias (with the reset drain still biased and the reset gate held at dc high or low, or clocked as normal). Operation of the high gain mode is controlled by adjustment of the multiplication phase amplitude RØ2HV.

All the bond pads are at the bottom of the chip. Shielded elements are provided for dark reference purposes and for some positional tolerance in aligning a back-face light-shield

GENERAL DATA

Format

Active Image area	26.11mm x 25.73 mm
Active pixels	1632 (H) x 1608 (V)
Pixel size	16 x 16 µm
Total elements per line	1648
Number of output amplifiers	2
Fill factor	100%
Additional dark reference columns	16 +16
Additional over scan rows	4

Package (ceramic)

Overall dimensions	48.5mm x 37.0mm
Number of pins	38
Inter-pin spacing	1.78 mm

Package shown in Fig. 16.

ORDERING INFORMATION

Part number CCD207-40-G-XYZ

Where G is the grade and XYZ is the build type.

e.g. XYZ = C32 for a mid-band coating with shield for dark reference pixels

XYZ = G48 for uncoated, no shield for dark reference pixels.

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TYPICAL PERFORMANCE SPECIFICATIONS

- Device performance will be within the limits specified by Min and Max below, when operated at the recommended voltages, and unless specified otherwise at 3 MHz pixel rate.
- Parameters are given at 243 K.
- Where parameters are different in the normal and high gain mode, both are given.

PARAMETER	UNIT	MIN	TYPICAL	MAX
Output amplifier responsivity, HR amplifier (normal mode) (see note 1)	μV/e-	4.4	5.2	6.0
Output amplifier responsivity, LS amplifier (normal mode) (see note 1)	μV/e-	0.8	1.1	1.4
Multiplication register gain, LS amplifier (high gain mode) (see notes 2 and 3)	-	1	1000	2000
Peak signal - 2-phase IMO	e-/pixel	100k	130k	–
Charge handling capacity of readout register (see note 4)	e-/pixel	350k	400k	
Charge handling capacity of multiplication register (see note 4)	e-/pixel	–	800k	–
Charge handling capacity of HR amplifier (see note 5)	e-	–	300k	–
Charge handling capacity of LS amplifier (see note 5)	e-	–	1.3M	–
Readout noise at 50 kHz with CDS, HR amplifier (normal mode) (see note 5)	e- rms		3.5	–
Readout noise at 1 MHz with CDS, HR amplifier (normal mode) (see note 5)	e- rms	–	7.0	–
Amplifier reset noise (without CDS), HR amplifier (normal mode)(see note 5)	e- rms	–	50	–
Readout noise at 10 MHz with CDS, LS amplifier (normal mode)(see note 5)	e- rms	–	37	–
Amplifier reset noise (without CDS), LS amplifier (normal mode)(see note 5)	e- rms	–	100	–
Readout noise at 10 MHz (high gain mode) (see note 5)	e- rms	–	–	< 1
Pixel Rate Limit (settling to 1%), HR amplifier (see notes 5 and 6)	MHz	–	–	3
Pixel Rate Limit (settling to 5%), HR amplifier (see notes 5 and 6)	MHz	–	–	4.5
Pixel Rate Limit (settling to 1%), LS amplifier (see note 5 and 6)	MHz	–	–	13
Pixel Rate Limit (settling to 5%), LS amplifier (see note 5, 6 and 7)	MHz	–	–	20
Parallel transfer frequency Limit (see note 5)	kHz	–	–	40
Photo Response Non Uniformity (650nm broadband) (note 8)	%		3	
Dark signal @ 293 K (see note 9)	e-/pix/s	–	400	1600
Dark signal non-uniformity (DSNU) at 293 K (see note 10)	e-/pix/s	–	90	–
Excess noise factor (see note 11)			√2	
Charge Transfer Efficiency (see note 12) Parallel Serial	 % %		 99.9995 99.9995	

NOTES

1. All tests are at a pixel rate of 1MHz, except the noise test.
2. The variation of gain with Rϕ2HV at different temperatures is shown in Fig. 1.
3. Some increase of Rϕ2HV may be required throughout life to maintain gain performance. Adjustment of Rϕ2HV should be limited to the maximum specified under Operating Conditions.
4. When multiplication gain is used and clock timings optimized, a linear response of output signal with input signal of better than 3% is achieved for output signals up to 400 ke- typically.
5. These values are inferred by design.
6. The quoted maximum frequencies assume a 20pF load and correlated double sampling.
7. This max pixel rate limit refers to that set by the output amplifier. The multiplication register has only been assessed up to 15MHz. Operation up to 20MHz cannot be guaranteed
8. Photo Response Non-Uniformity (PRNU) is defined as the local 1σ variation in photo response to flat field illumination. Any pixels classed as dark defects at high light level are omitted from the analysis.
9. The quoted dark signal has the usual temperature dependence for inverted mode operation. There will also be a component generated during readout through the register, with non-inverted mode temperature dependence. Clock induced charge is only weakly temperature dependent, is independent of integration time, and depends on the operating biases and timings employed. It is typically 0.05 e- / pixel/frame at T = - 55 °C. For more information, refer to the technical note "Dark Signal and Clock-Induced Charge in L3Vision™ CCD Sensors
10. DSNU is defined as the 1σ variation of the dark signal.
11. The excess noise factor is defined as the factor by which the multiplication process increases the shot noise on the image when multiplication gain is used.

12. CTE is the fraction of charge stored in a CCD element that is transferred to the adjacent element by a single clock cycle. The charge not transferred remains in the original element, possibly in trapping states and may possibly be released into later elements. The value of CTE is not constant but varies with signal size, temperature and clock frequency.

DEVICE COSMETIC PERFORMANCE

- Grade 1 devices are supplied to the blemish specification shown below.
- Incorrect biasing of the device may result in spurious dark or white blemishes appearing. These will be eliminated if the biases are adjusted.

TEST CONDITIONS

- Devices run at 1 MHz readout rate in 2-phase inverted mode
- Device temperature 253K.

Bright Defect in Darkness	A Bright Defect in Darkness is defined as any pixel whose mean response in darkness exceeds 100 times the specification for maximum dark signal at the test temperature. This corresponds to a response of 280 electrons/pixel/second at the -20°C test temperature.
Bright Column in Darkness	A Bright Column in Darkness is defined as 9 or more consecutive pixels in any column, whose mean response in darkness exceeds 10 times the specification for the maximum dark signal at the test temperature. This corresponds to a response of 28 electrons/pixel/second at the -20°C test temperature.
Dark Defect	A Dark Defect at high light level is defined as any pixel whose mean photo response is less than 80% of the local mean at a signal level of approximately 50% of image full well capacity.
Dark Column at high light level	A Dark Column at high light level is defined as any column containing 9 or more (not necessarily consecutive) dark defects at high light level.

Type of Defect	**Grade 1 CCD207-40**
Bright Defects in Darkness	≤80
Dark Defects at High Light Level	≤80
Dark Columns at High Light Level	≤4 (Total)
Bright Columns in Darkness	

Figure 1: TYPICAL VARIATION OF MULTIPLICATION GAIN WITH Rϕ2HV AT DIFFERENT TEMPERATURES

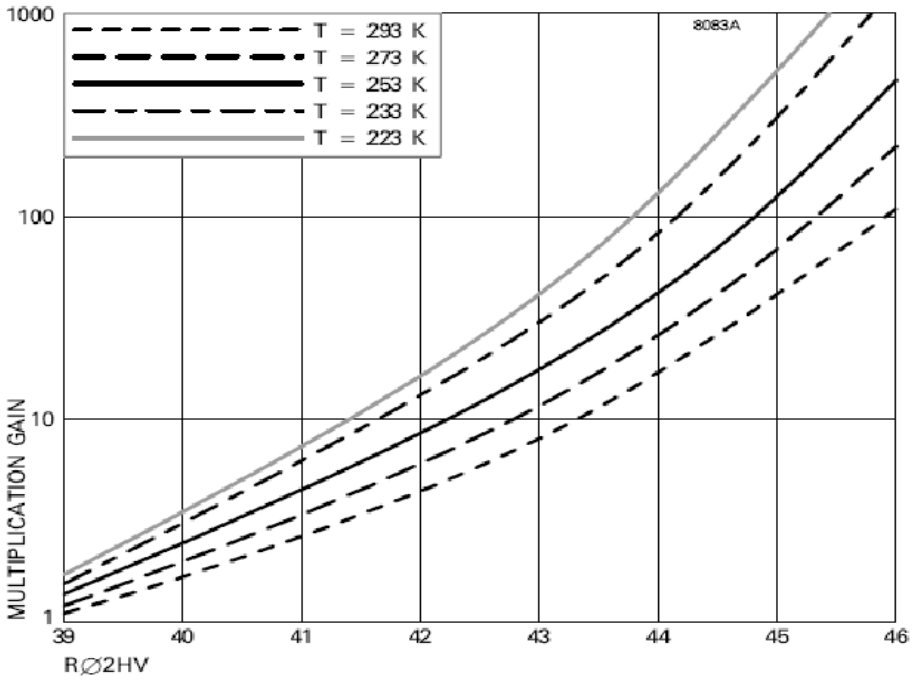


Figure 2: TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE

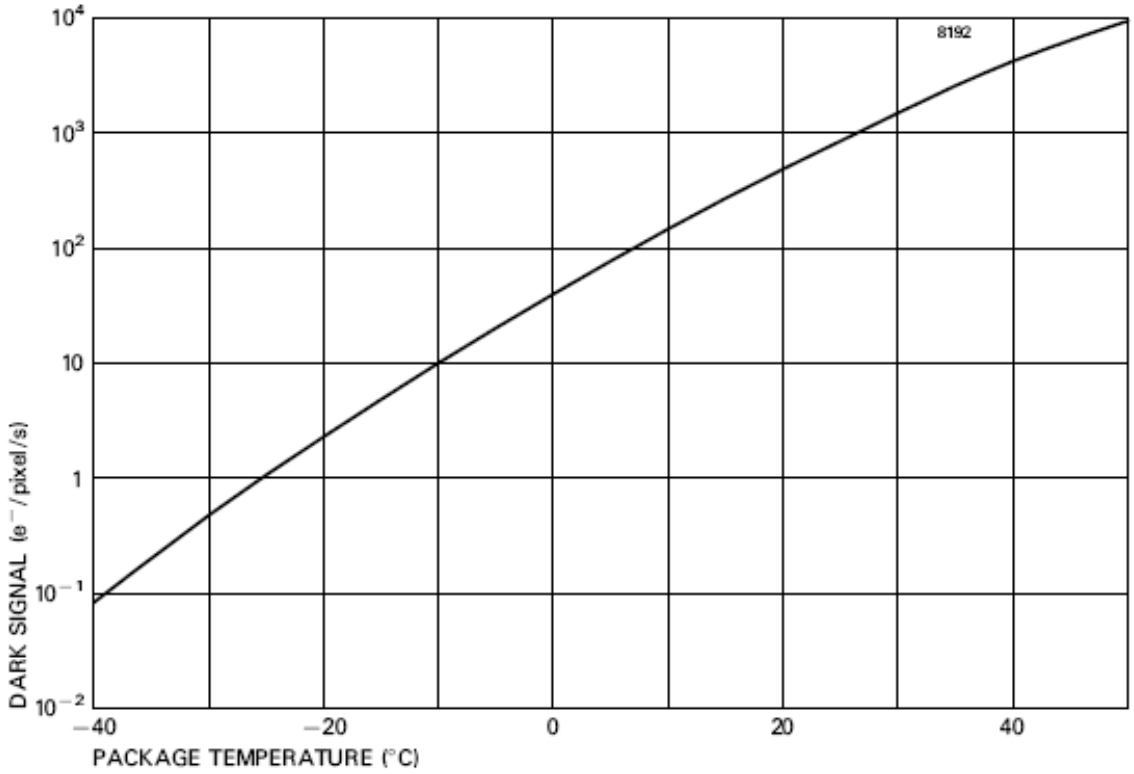
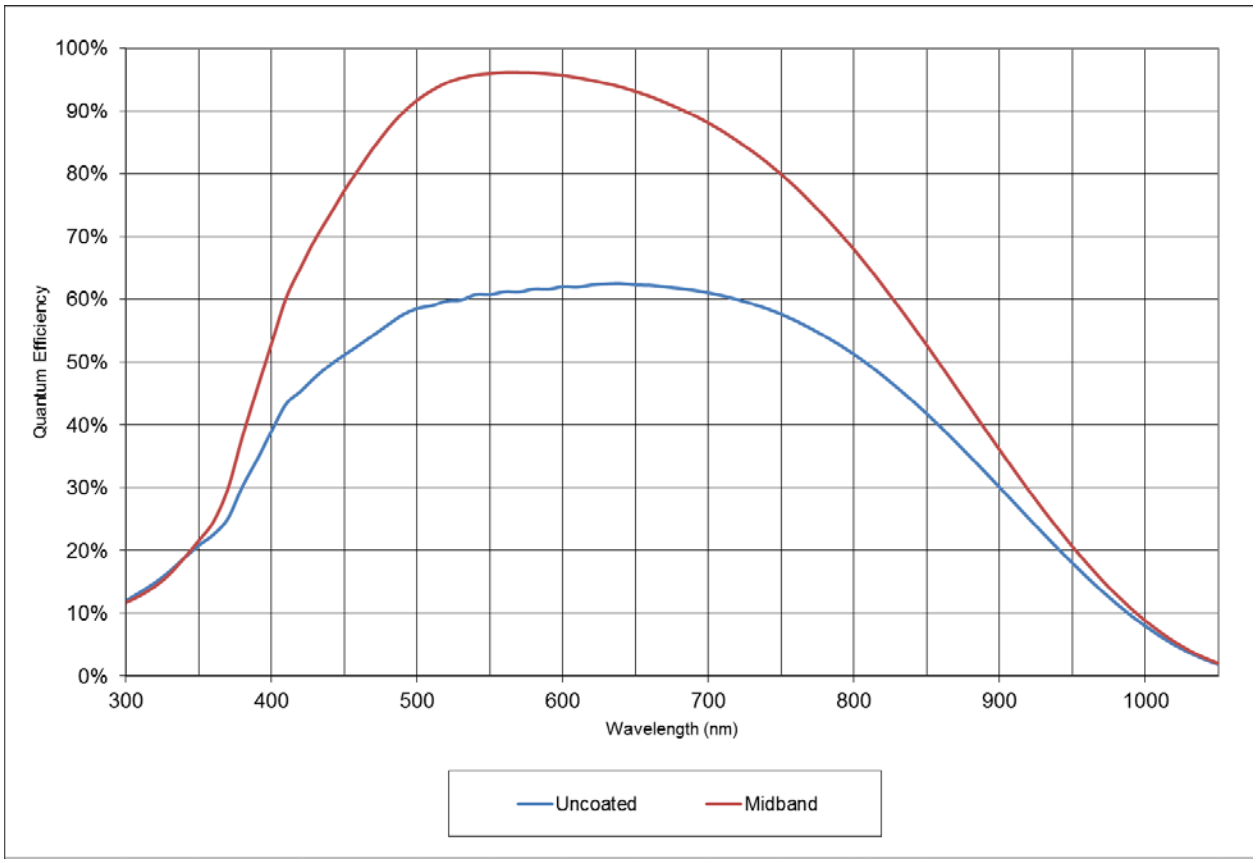


Figure 3: TYPICAL SPECTRAL RESPONSE (no window, T = -20°C)



ESD HANDLING PROCEDURES

CCD sensors, in common with most high performance IC devices, are static sensitive. In certain cases a static electricity discharge may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench.
- Operator wearing a grounded wrist strap.
- All receiving socket pins to be positively grounded.
- Unattended CCD's should not be left out of their conducting foam or socket.

All devices are provided with internal protection circuits to most
gate electrodes but not to the other pins.
Evidence of incorrect handling will terminate the warranty.

EXPOSURE TO RADIATION

Exposure to radiation may irreversibly damage the device and result in degradation of performance. Users wishing to operate the device in a radiation environment are advised to consult e2v technologies.

POWER UP / POWER DOWN

When powering the device up or down, it is critical that any specified maximum rating is not exceeded. Specifically, the voltage for the amplifier and dump drains must never be taken negative with respect to the substrate. Hence, if the substrate is to be operated at a positive voltage (e.g. to minimize dark current) then the drive electronics should have a switch-on sequence which powers up all the drains to their positive voltages before the substrate voltage starts to increase from zero. Similarly, for powering down, the substrate must be taken to zero voltage before the drains.

It is also important to ensure that excess currents do not flow in the OS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased dc coupled preamplifier

Connections, Typical Voltages and Absolute Maximum ratings

PIN	CONNECTION	DESCRIPTION	Clock Amplitude or DC Level (V) see Note 13 Min	Typ	Max	MAX RATING with respect to VSS (V)
1	SS	Substrate	0	+4.5	+7	N/A
2	RDL	Reset Drain	+15	+18	+20	- 0.3 to +25
3	ODL	Output Drain (LS Amplifier)	25	+30	+32	- 0.3 to +32
4	OSH	Output Source (HR Amplifier)	See notes 15, 16 & 17			- 0.3 to +25
5	OSL	Output Source (LS Amplifier)				- 0.3 to +25
6	OGH	Output Gate	+1	+3	+5	±20
7	ϕR	Reset Pulse High	(note14)	+11	(note14)	±20
		Reset Pulse Low	–	0	–	
8	Rϕ3	Register Clock High	+8	+10	+13	±20
		Register Clock Low	–	0	–	
9	Rϕ1	Register Clock High	+8	+10	+13	±20
		Register Clock Low	–	0	–	
10	Rϕ2HV	Multiplication Register Clock Hi	+8	+40	+48 (note 3)	- 20 to +48
		Multiplication Register Clock Lo	0	+4	+5	
11	Rϕ2	Register Clock High	+8	+10	+13	±20
		Register Clock Low	–	0	–	
12	RϕDC	Multiplication Register DC Bias	+1	+3.5	+5	±20
13	N / C		–	–	–	N/A
14	OGL	Output Gate	+1	+3	+5	±20
15	N / C		–	–	–	N/A
16	N / C		–	–	–	N/A
17	ODH	Output Drain (HR Amplifier)	+25	+29	+32	- 0.3 to +32
18	RDH	Reset Drain	+15	+18	+20	- 0.3 to +25
19	SS	Substrate	0	+4.5	+7	N/A
20	SS	Substrate	0	+4.5	+7	N/A
21	N / C		–	–	–	N/A
22	N / C		–	–	–	N/A
23	N / C		–	–	–	N/A
24	N / C		–	–	–	N/A
25	IG	Isolation Gate	-	-5	0	±20
26	DG	Dump Gate High	+7	+12	+13	±20
		Dump Gate Low	–	0	–	
27	Iϕ3	Image Clock High	+5	+7	+9	±20
		Image Clock Low	-6	-5	-4	
28	Iϕ1	Image Clock High	+5	+7	+9	±20
		Image Clock Low	-6	-5	-4	
29	SS	Substrate	0	+4.5	+7	N/A
30	Iϕ2	Image Clock High	+5	+7	+9	±20
		Image Clock Low	-6	-5	-4	
31	Iϕ4	Image Clock High	+5	+7	+9	±20
		Image Clock Low	-6	-5	-4	
32	DD	Dump Drain	+20	+24	25	- 0.3 to +25
33	ABD	Anti-blooming Drain	+10	+18	+20	- 0.3 to +25
34	N / C		–	–	–	N/A
35	N / C		–	–	–	N/A
36	N / C		–	–	–	N/A
37	N / C		–	–	–	N/A
38	SS	Substrate	0	+4.5	+7	N/A

NOTES

13. All operating voltages are with respect to readout clock low level (nominally 0V). To ensure correct device operation, the drive circuitry must be designed so that any value in the range Min to Max can be set.
14. ϕR high level may be adjusted in common with Rϕ 1,2,3.
15. The current through these pins must not exceed 20mA. Permanent damage may result if OS experiences short circuit conditions, even momentarily. Do not connect to a voltage supply, but use a current source or external load : HR amplifier: ~5mA or ~5kohm, LS amplifier: ~7.5mA or ~3k3ohm.
16. The quiescent voltage on OS will be ~6-8 volts above the reset drain voltage and is typically 24V. The dc restoration circuitry is activated by an internal connection from the last parallel transfer phase (IØ4). The on-chip amplifier power dissipation is approximately 30 mW for the HR amplifier and 50 mW for the LS amplifier.
17. Between the two amplifiers, common connections are made to the reset gates (ϕR), reset drains (RD) and output gates (OG).

Maximum voltages between pairs of pins:

PIN	CONNECTION	PIN	CONNECTION	MIN(V)	MAX(V)
19	Rϕ2HV	18	RϕDC	-20	+48
19	Rϕ2HV	27	Rϕ3	-20	+48
Maximum Output transistor current 20mA					

Output Amplifiers

Parameter	CCD207-40	Unit
Output Impedance, HR amplifier	400	Ω
Output Impedance, LS amplifier	350	Ω
External Load, HR amplifier	5 mA or 5kΩ	
External Load, LS amplifier	7.5 mA or 3k3Ω	

DRIVE PULSE WAVEFORM SPECIFICATION

The device is of a 4-phase construction, designed to operate in 2-phase inverted mode. This is achieved by applying common timings to phases Iϕ and Iϕ2, and phases Iϕ3 and Iϕ4 of the image section. Suggested timing diagrams are shown in Figs. 4 – 12. Factory tests are performed at 1MHz pixel rates. Parameters shown in the table are for nominal rates up to 15MHz

The following are suggested pulse rise and fall times.

CLOCK PULSE	TYPICAL RISE TIME t (ns)	TYPICAL FALL TIME t (ns)	TYPICAL PULSE OVERLAP
Iϕ1	140 < t < 200	140 < t < 200	@90% points
Rϕ1	10	10	@70% points
Rϕ2	10	10	@70% points
Rϕ3	10	10	@70% points
Rϕ2HV	25	25	see note 18
Rϕ2HV	Sine	Sine	Sinusoid- high on falling edge of Rϕ1

NOTES

18. Register clock pulses are as shown in Figs. 5 and 6.
19. An example clocking scheme is shown in Fig. 5. Rϕ2HV can also be operated with a normal clock pulse, as shown in Fig. 6. The requirement for successful clocking is that Rϕ2HV reaches its maximum amplitude before Rϕ1 goes low.

ELECTRICAL INTERFACE CHARACTERISTICS

ELECTRODE CAPACITANCES AT MID CLOCK LEVELS

Connection	Capacitance to SS	Inter-phase Capacitances	Total Capacitance	Resistance	τp = RC
IØ1	8.8 nF	7.2 nF	23.2 nF	~22 Ω	~ 510ns
IØ2	14.8 nF	7.2 nF	29.2 nF	~17 Ω	~ 510ns
IØ3	8.8 nF	7.2 nF	23.2 nF	~22 Ω	~ 510ns
IØ4	14.8 nF	7.2 nF	29.2 nF	~17 Ω	~ 510ns

	Min	Typ	Max	Unit
Row Shift Period (2-phase)	25	50		µs
IØ & SØ Pulse overlap		1.5		µs

Connection	Capacitance to SS	Inter-phase Capacitances	Total Capacitance	Units
ELECTRODE CAPACITANCES AT MID CLOCK LEVELS				
RØ1	80		213	pF
RØ2	56		151	pF
RØ3	104		201	pF
RØDC	48		66	pF
RØ2HV	14		30	pF
RØ1-RØ2		63		pF
RØ1-RØ3		65		pF
RØ2-RØ3		32		pF
RØ1-RØDC		5		pF
RØ3-RØ2HV		3		pF
RØ2HV-RØDC		13		pF
SERIES RESISTANCES				
Connection	Approximate Total Series Resistance			
Rϕ1	8			Ω
Rϕ2	8			Ω
Rϕ3	8			Ω
Rϕ2HV	8			Ω

Figure 4: CLOCKING SCHEME FOR 2-PHASE INVERTED MODE OPERATION

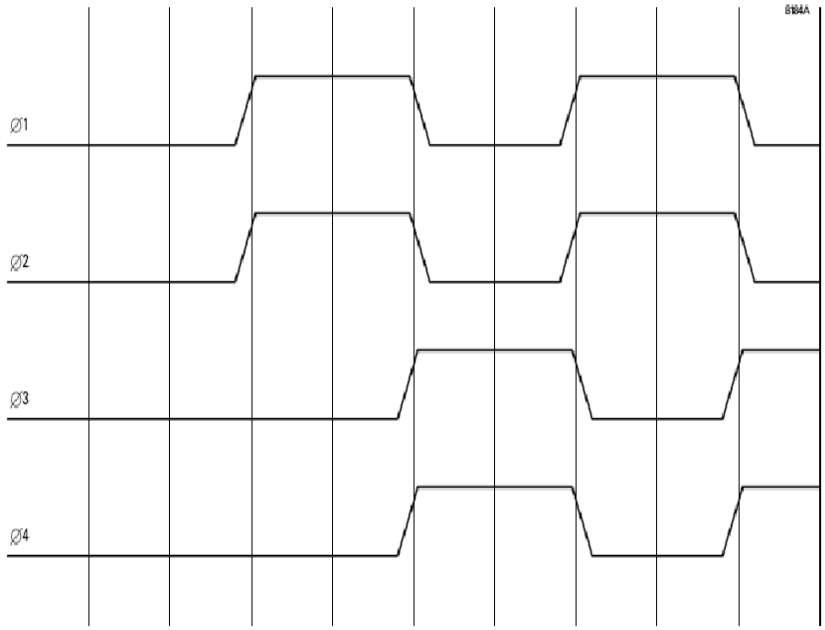


Figure 5: CLOCKING SCHEME FOR MULTIPLICATION GAIN (sinusoidal RØ2HV pulse)

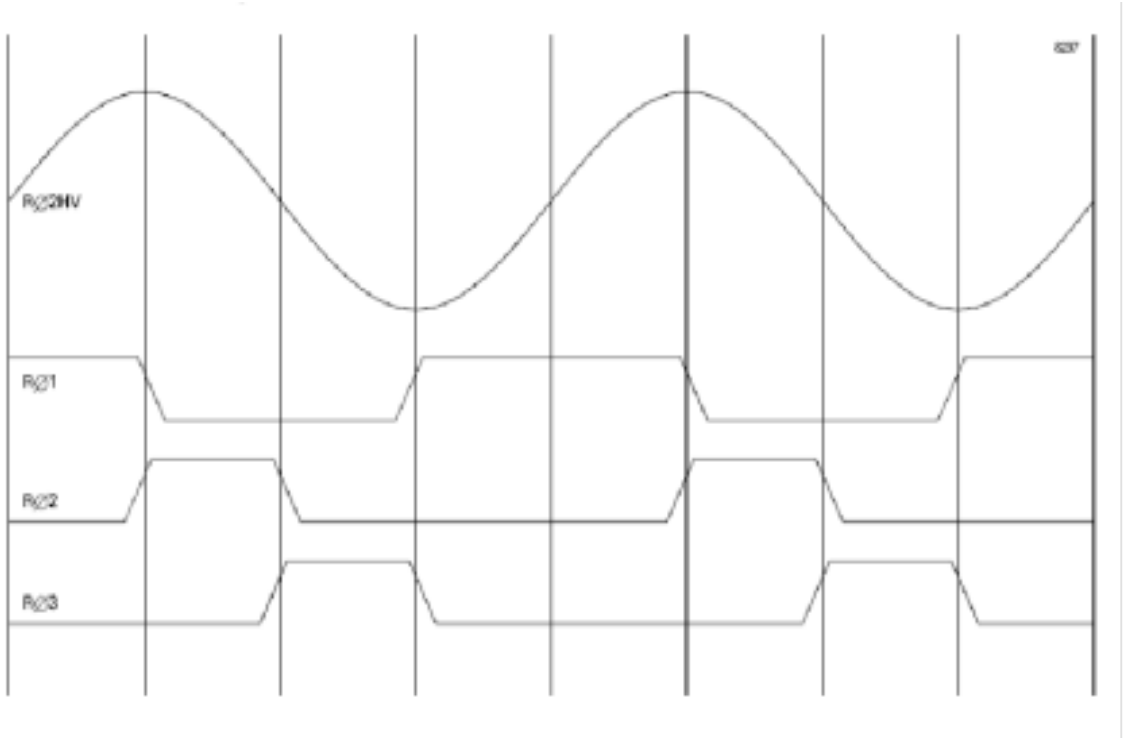


Figure 6: CLOCKING SCHEME FOR MULTIPLICATION GAIN

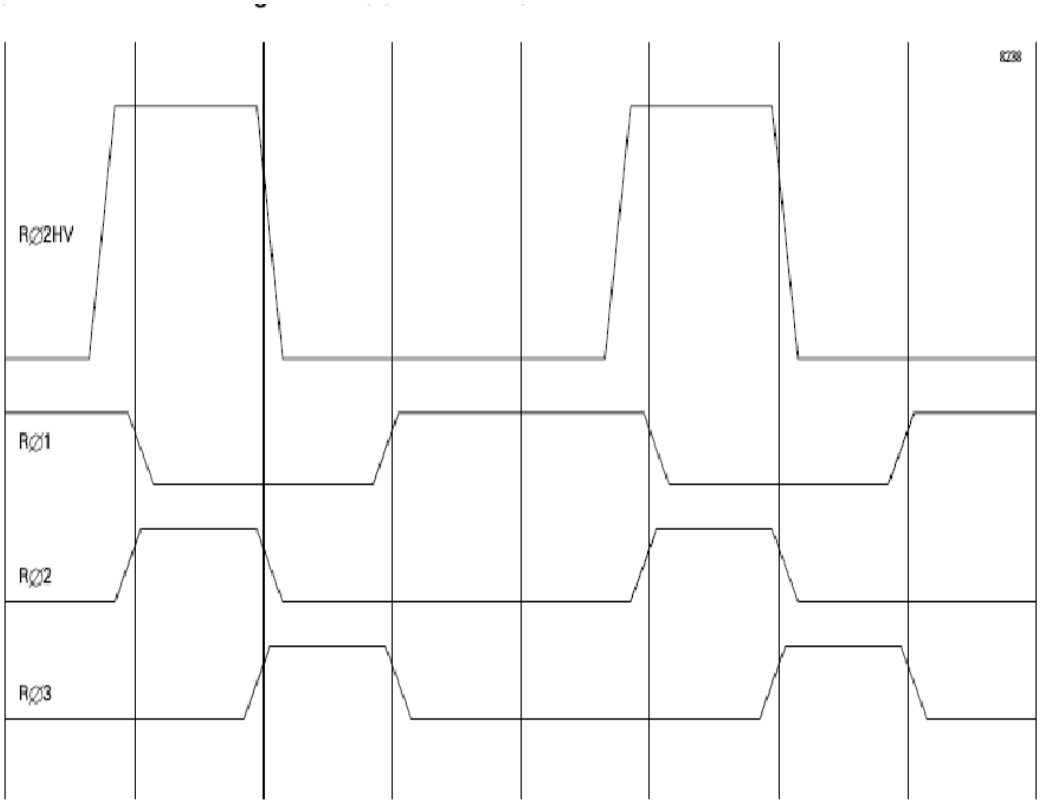
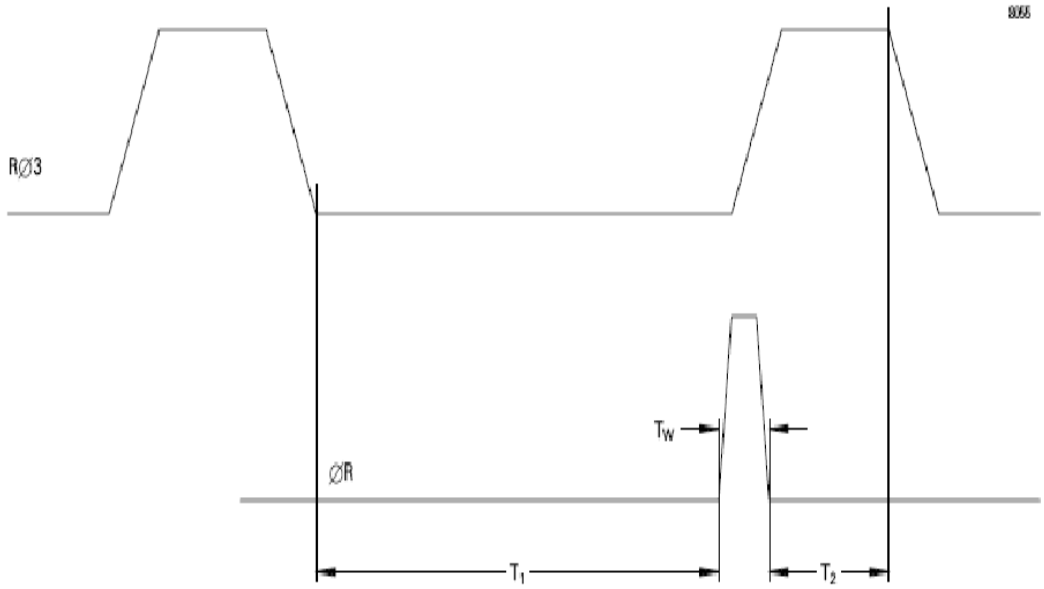


Figure 7: RESET PULSE



T_W = 10 ns typical
T_1 = output valid
T_2 > 0 ns

Figure 8: PULSE AND OUTPUT TIMING

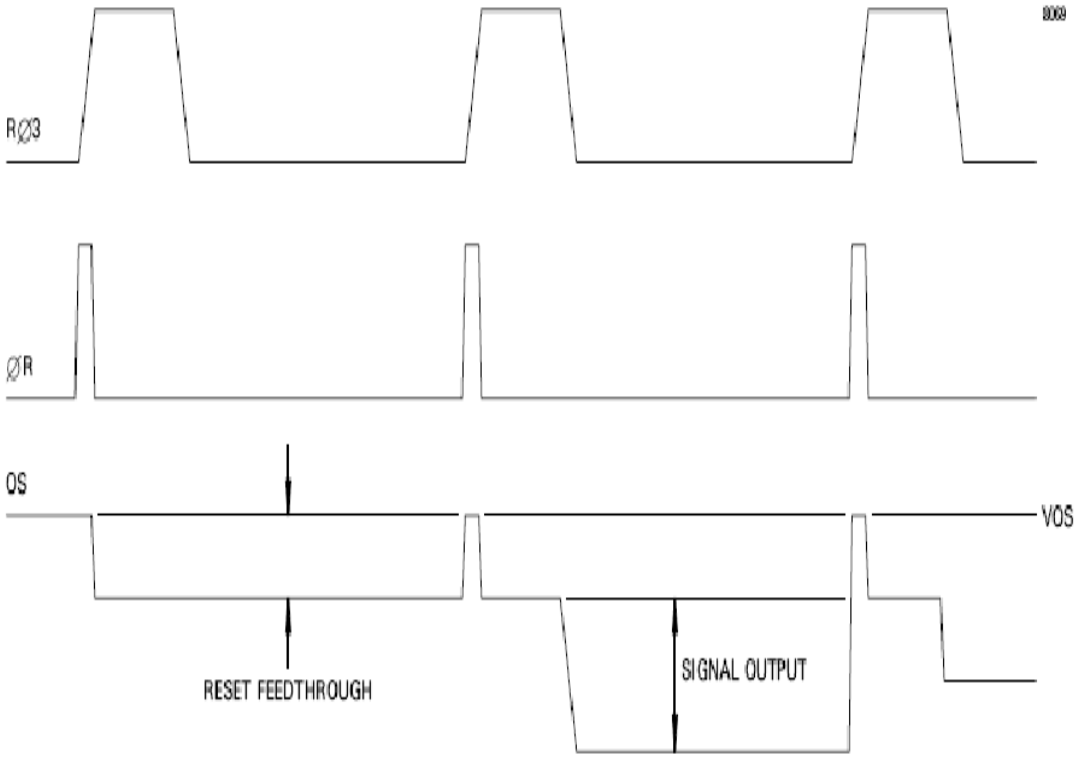
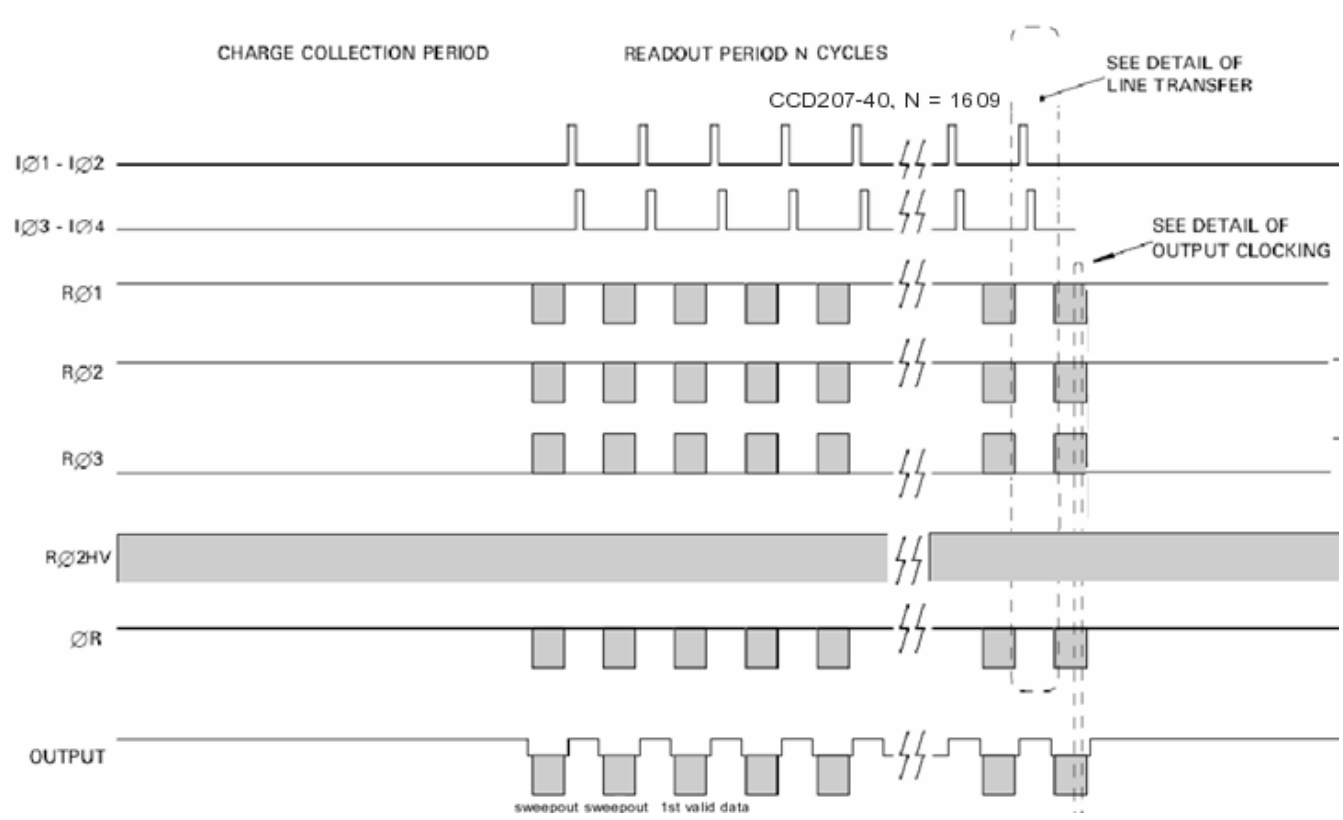


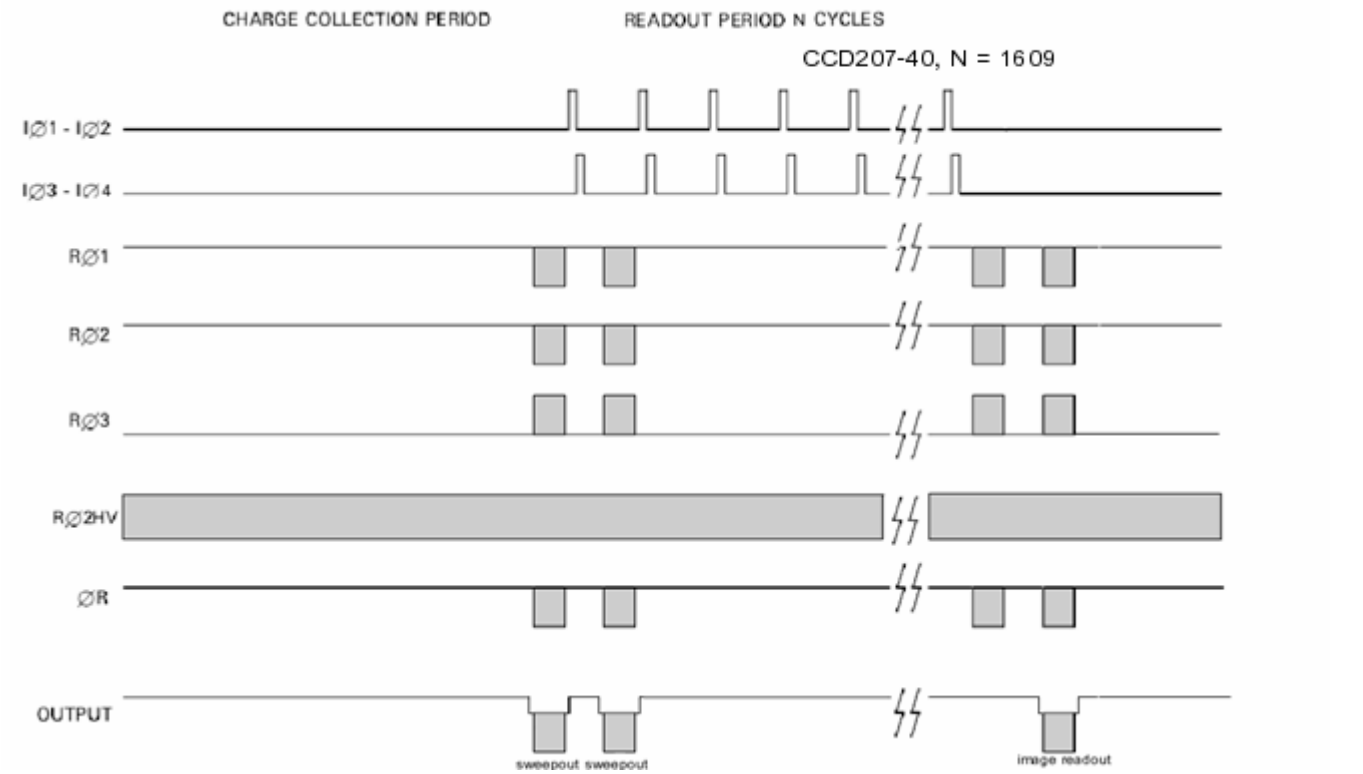
Figure 9: EXAMPLE FRAME TIMING DIAGRAM



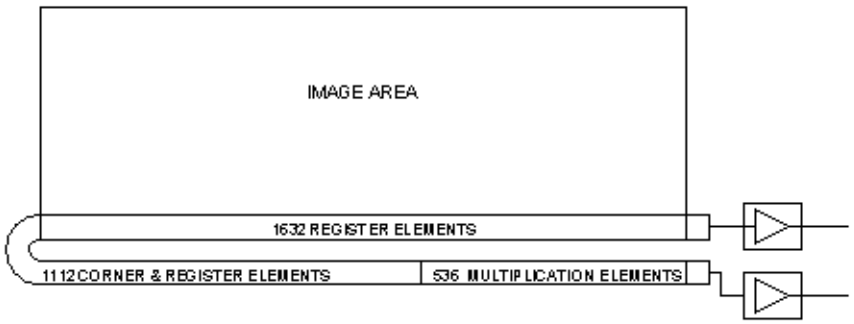
NOTES

20. For lowest noise, it is preferable to switch off the RØ2HV clock during long integration periods. Particular care is needed in the design of HV clock buffers when feedback circuitry is employed to achieve amplitude control. If the sequence of clock pulses is interrupted, the circuit design must ensure that the amplitude of the first few pulses after clocking re-starts is not excessive. If in doubt, the RØ2HV clock should remain continuous as shown.

Figure 10: EXAMPLE FRAME TIMING DIAGRAM, Full Vertical Binning, Readout Through L3 Port

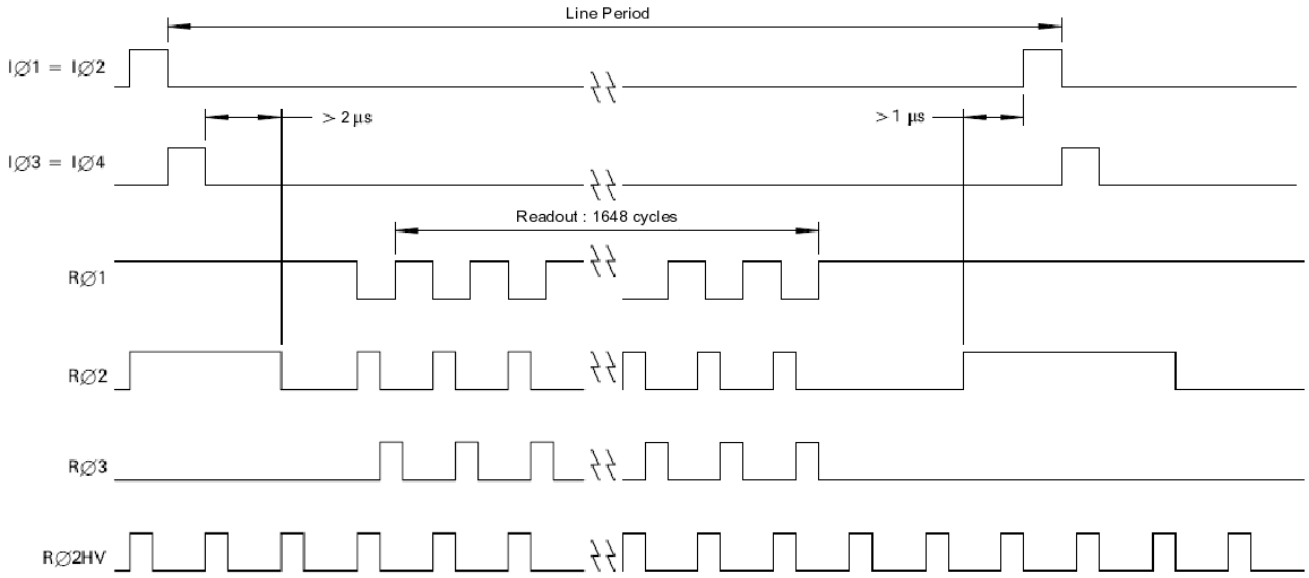


This clocking scheme illustrates the pipeline delay inherent in the device when multiplication gain is employed. This is a consequence of the path that charge packets must take in passing from the image area to the readout node. A total of (1632 + 1112 + 536+16) pixel clock cycles are required before the last pixel following a particular line transfer is read out. This is exactly two line readout cycles, each consisting of 1648 pixel cycles.



The clocking scheme can be further explained by referring to each of the RØ burst in the diagram. RØ burst1 is to clear the register. It reads out the elements adjacent to the port, and shifts the elements adjacent to the image area into the pipeline, leaving space for a fresh set, which is transferred by the first line transfer. The second RØ burst reads the rest of the charge clear pixels and clears the pipeline. Subsequent line transfers transfer the signal charge resulting from the integration time into the first 1632 register elements, resulting in 100% vertical binning. RØ burst3 shifts these elements into the pipeline. RØ burst4 reads the binned image out.

Figure 11: EXAMPLE LINE TIMING DIAGRAM (Operation through OSL / LS Port - see note)



NOTES

21. To operate through the OSH output amplifier, the RØ 1 and RØ 2 waveforms should be interchanged.

Figure 12: OPERATION OF THE DUMP GATE TO DUMP n LINES OF UNWANTED DATA FROM THE STANDARD REGISTER

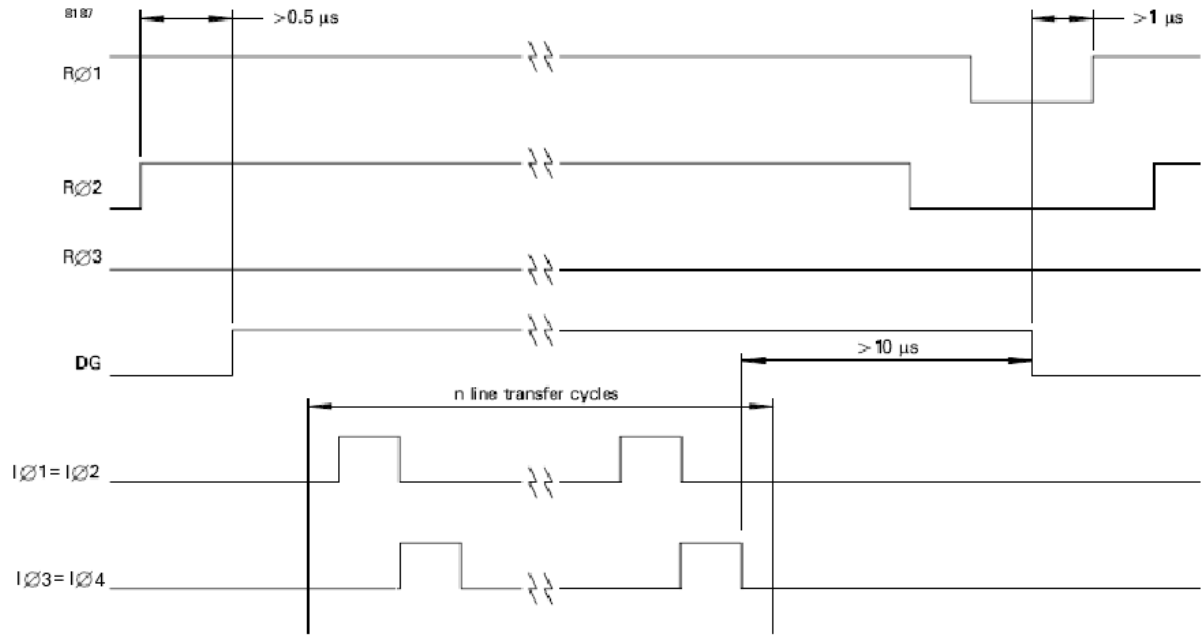


Figure 13: OUTPUT CIRCUIT SCHEMATIC (OSL and OSH Amplifiers)

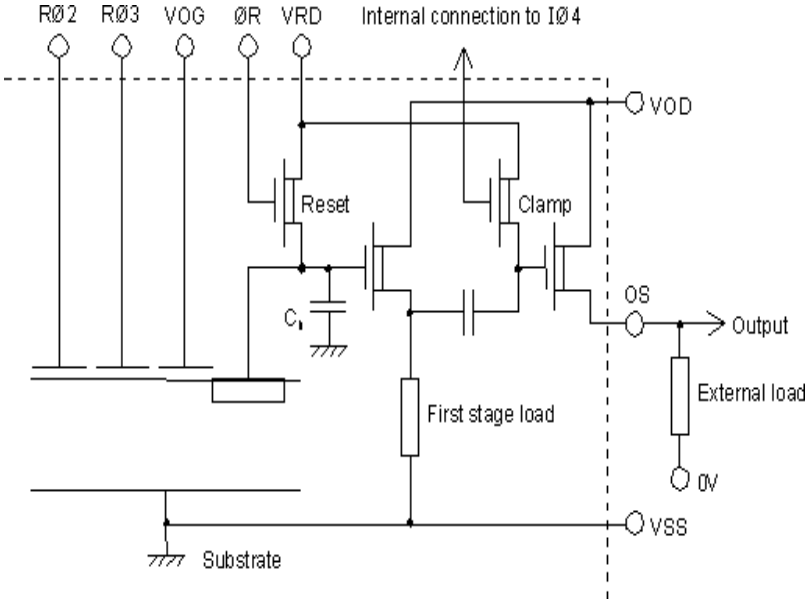


Figure 14: SCHEMATIC CHIP DIAGRAM (for C32 build type)

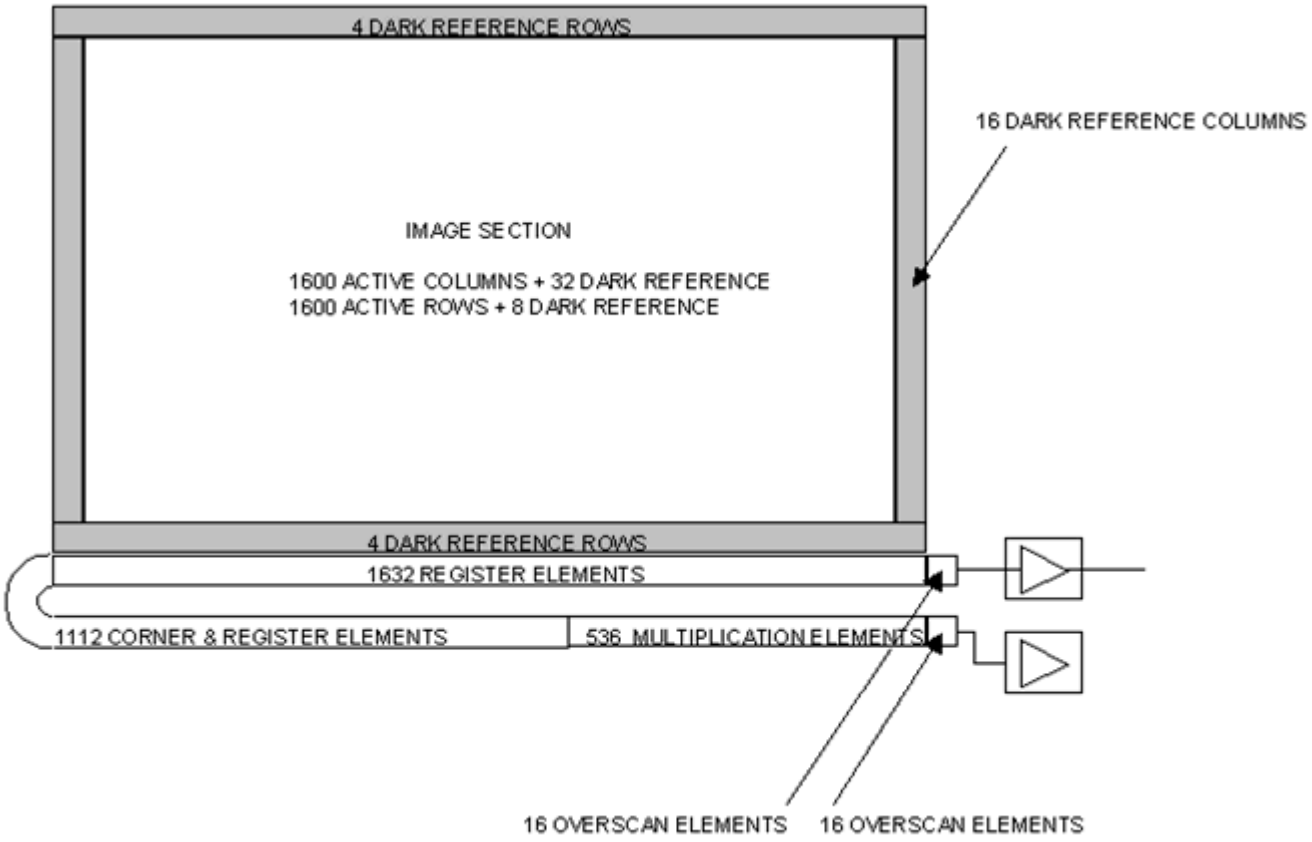
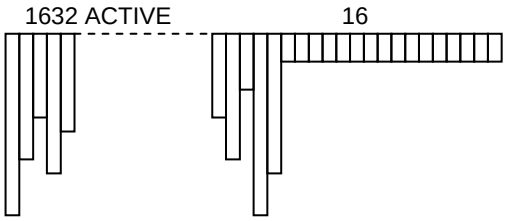
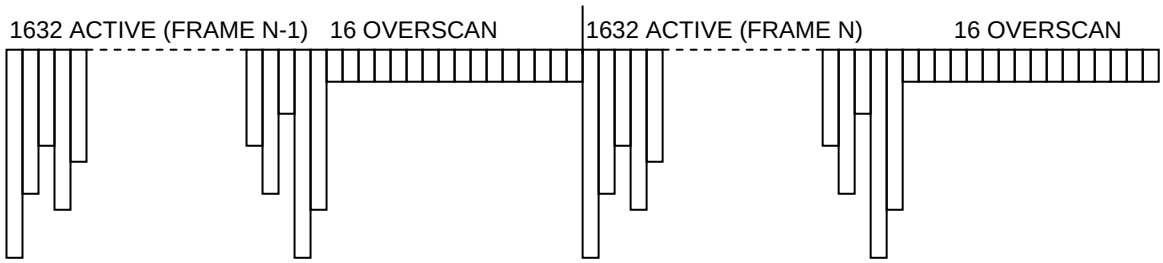


Figure 15: LINE OUTPUT FORMAT (for Example Line Timing Figure 11)

Read Out Through Conventional (HR) Port



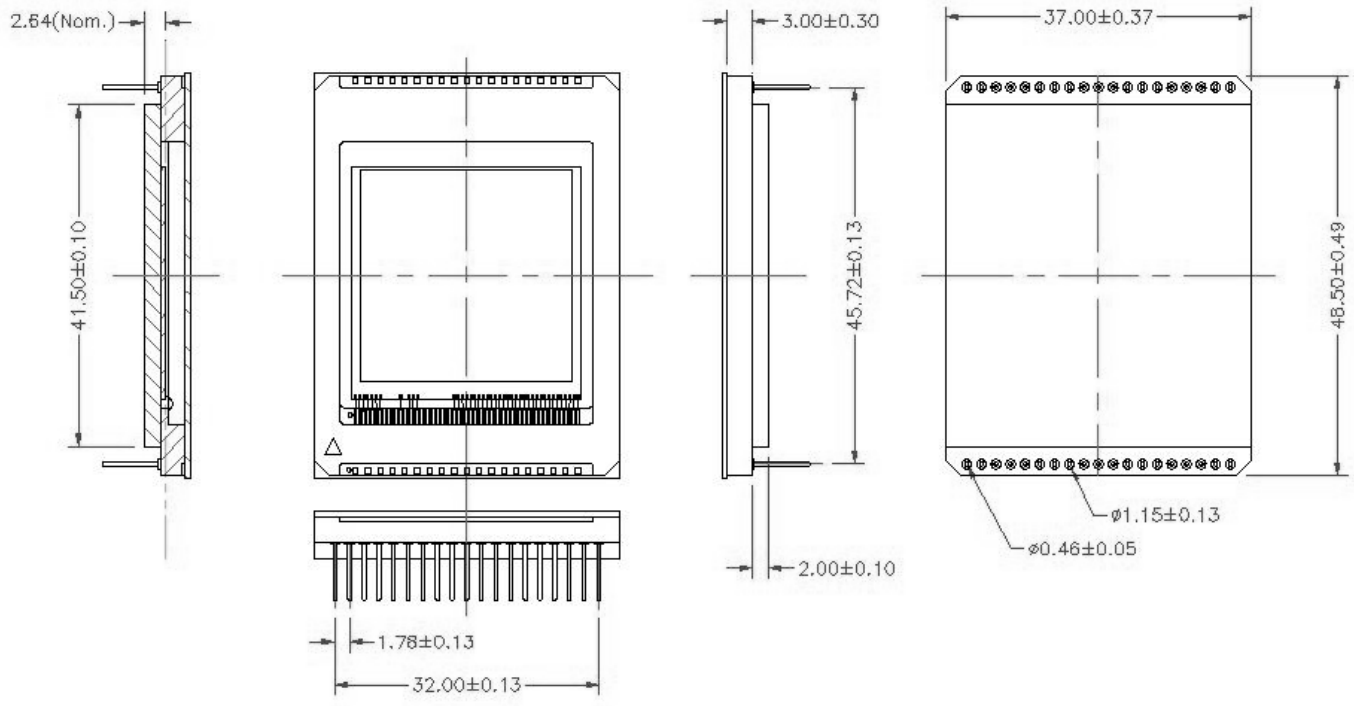
Read Out Through L3 (LS) Port (after two frame flush)



NOTES

22. the first and last elements of both the overscan and active groups should not be used for critical measurements

Figure 16: CCD207-40 PACKAGE OUTLINE



The device is mounted in an aluminium oxide ceramic package with a temporary window. In addition to the traditional DIL pins, external bond pads will be available for the user to connect via wire bonds. However, e2v can give no guarantees as to the reliability of the customer applied wire bonds

Operating Conditions

Devices are tested at -20°C, but may be operated at -100°C
Maximum cooling rate: 5°C per min

Intended for low light level use
Do not operate at high light level for extended periods