HT32F61630
Datasheet

32-Bit Arm® Cortex®-M0+ Li-Battery Protection Microcontroller, up to 32 KB Flash and 2 KB SRAM with 500 ksps ADC, UART, SPI, I²C, SCTM, BFTM, LEDC, RTC and WDT

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1 General Description

The Holtek HT32F61630 device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer and including advanced debug support.

The device operates at a frequency of up to 16 MHz to obtain maximum efficiency. It provides up to 32 KB of embedded Flash memory for code/data storage and 2 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I^2C, UART, SPI, SCTM, BFTM, LEDC, RTC, WDT and SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The device also includes an accumulative cell voltage monitor, a high accuracy voltage regulator, two discharge N-type MOSFET gate-drivers and a charge N-type MOSFET gate-driver which are provided for 3 to 8 cell Li-ion rechargeable battery applications. The accumulative cell voltage monitor is used to monitor an accumulative voltage from 1 to N and output the divide-by-N voltage to the analog multiplexer with a ±0.5 % divided ratio accuracy which can then be connected the VOUT pin to the one of the integrated A/D converter channel for measurement. The device can directly drive external power N-type MOSFETs to control charge and discharge by charge and discharge gate-drivers. The integrated battery balance circuitry provides a cell balance current without the need of external transistors.

The above features ensure that the device is suitable for use in a wide range of applications, especially in areas such as handheld instruments, electronically controlled tools, handheld hair dryers, handheld vacuum cleaners and other handheld devices.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 16 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- Up to 32 KB on-chip Flash memory for instruction/data and options storage
- 2 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor access and debug access share the single external interface to external AHB peripherals. The processor accesses take priority over debug accesses. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the device, including code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions for the embedded on-chip Flash Memory. The word programming/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor
  - Power On Reset / Power Down Reset – POR / PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32.768 kHz crystal oscillator
- Internal 16 MHz RC oscillator trimmed to ±1 % accuracy at 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), an HSE clock monitor, clock pre-scalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from the HSI, HSE, LSI or LSE. The Watchdog Timer and Real-Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management Control Unit – PWRCU

- V_{DD} power supply: 2.5 V ~ 5.5 V
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- V_{DD} and V_{CORE} power domains
- Three power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides many types of power saving modes such as Sleep, Deep-Sleep1 and Deep-Sleep2 mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

Accumulative Cell Voltage Monitor

- Accumulative Cell Voltage Monitor 8-to-1 Analog Multiplexer with divided ratio accuracy: (1/n ± 0.5 %)
- Cell Charging Balance Switches
- Two Discharge N-type MOSFET Gate-Drivers
- Single Charge N-type MOSFET Gate-Driver
- Sleep Mode with 0.1 μA ultra-low standby current
- Direct High Voltage Wake-up function

External Interrupt/Event Controller – EXTI

- Up to 8 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 8 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 500 ksps conversion rate
- Up to 6 external analog input channels

A 12-bit multi-channel Analog to Digital Converter is integrated in the device. There are multiplexed channels, which include up to 6 external analog signal channels and 2 internal channels which can be measured. There are two conversion modes to convert an analog signal to digital data. The A/D conversion can be operated in one shot and continuous conversion mode.

The internal voltage reference generator (VREF) which can provide a stable ADC reference positive voltage (ADCREFP) and the Band gap of VREF is internally connected to the ADC internal input channel. The precise voltage of the V_{REF} is individually measured for each part by Holtek during production test.

I/O Ports – GPIO

- Up to 22 GPIOs
- Port A, B, C are mapped as 8-line EXTI interrupts
- Almost all I/O pins have configurable output driving current

There are up to 22 General Purpose I/O pins for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

Single-Channel Timer – SCTM

- 16-bit auto-reload up-counter
- One channel for each timer
- 8-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 256 to generate the counter clock frequency
- One input Capture function
- Two compare Match Output
- PWM waveform generation with Edge-aligned counting Mode
- Single Pulse Mode Output

The Single Channel Timer Module, SCTM, consists of one 16-bit up-counter, one 16-bit Capture / Compare Register (CCR), one 16-bit Counter Reload Register (CRR) and several control / status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as PWM outputs.

Basic Function Timer – BFTM

- 16-bit compare match up-counter – no I/O control
- One shot mode – counter stops counting when compare match occurs
- Repetitive mode – counter restarts when compare match occurs

The Basic Function Timer Module, BFTM, is a simple 16-bit up-counting counter designed to measure time intervals and generate one shots or generate repetitive interrupts. The BFTM can operate in two functional modes, repetitive and one shot modes. In the repetitive mode, the counter will restart at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down-counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit down-counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter before it reaches a delta value. It means that the counter reload must occur when the Watchdog timer value has a value within a limited window using a specific method. The Watchdog Timer counter can be stopped when the processor is in the debug mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog Timer configuration.

Real-Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real-Time Clock, RTC, circuitry includes the APB interface, a 24-bit up-counter, a control register, a prescaler, a compare register and a status register. The RTC circuits are located in the V_{CORE} power domain. The RTC counter is used as a wakeup timer to generate a system resume or interrupt signal from the MCU power saving mode.

Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Supports 7-bit addressing mode and general call addressing
- Supports two 7-bit slave addresses

The I^2C module is an internal circuit allowing communication with an external I^2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I^2C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I^2C bus is a bidirectional data line between the master and slave devices and is used for data transmission and reception.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- Programmable data frame length up to 8 bits
- FIFO Depth: 4 levels

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, among which are serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamlined data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

LED Controller – LEDC

- Supports 8-segment digital displays up to 4
- Supports 8-segment digital displays with common anode or common cathode
- Support frame interrupt
- Three clock sources: LSI, LSE and PCLK
- The LED light on/off times can be controlled using the dead time setting

The LED controller is used to drive 8-segment digital displays. These device can driver 8-segment digital displays up to 4. Users can flexibly configure the pin position and number of the COMs according to the digital displays in the application. In a complete frame period, the enabled COMs will be scanned from the lower to the higher. Taking an example of where four 8-segment LEDs are used and where COM0, COM1, COM2 and COM3 are enabled. Here COM0, COM1, COM2 and the COM3 will be scanned successively in this sequence within a complete frame period. The scanning time of each COM port is equal to 1/4 frame, which is subdivided into the dead time duty and the COM duty. Users can adjust the dead time duty to change the LED brightness.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watch points

Package and Operation Temperature

- 48-pin LQFP-EP package
- Operation temperature range: -40 °C to 85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F61630
Main Flash (KB)		31
Option Bytes Flash (KB)		1
SRAM (KB)		2
Timers	SCTM	3
	BFTM	1
	WDT	1
	RTC	1
Communication	SPI	1
	UART	2
	I^2C	1
EXTI		8
12-bit ADC		1
Number of channels		Max.6 Channels
GPIO		Up to 22
LEDC		Up to 4 × 8-segment
CPU frequency		Up to 16 MHz
Operating voltage		2.5 V ~ 5.5 V
Operating temperature		-40 °C ~ 85 °C
Package		48-pin LQFP-EP

Block Diagram

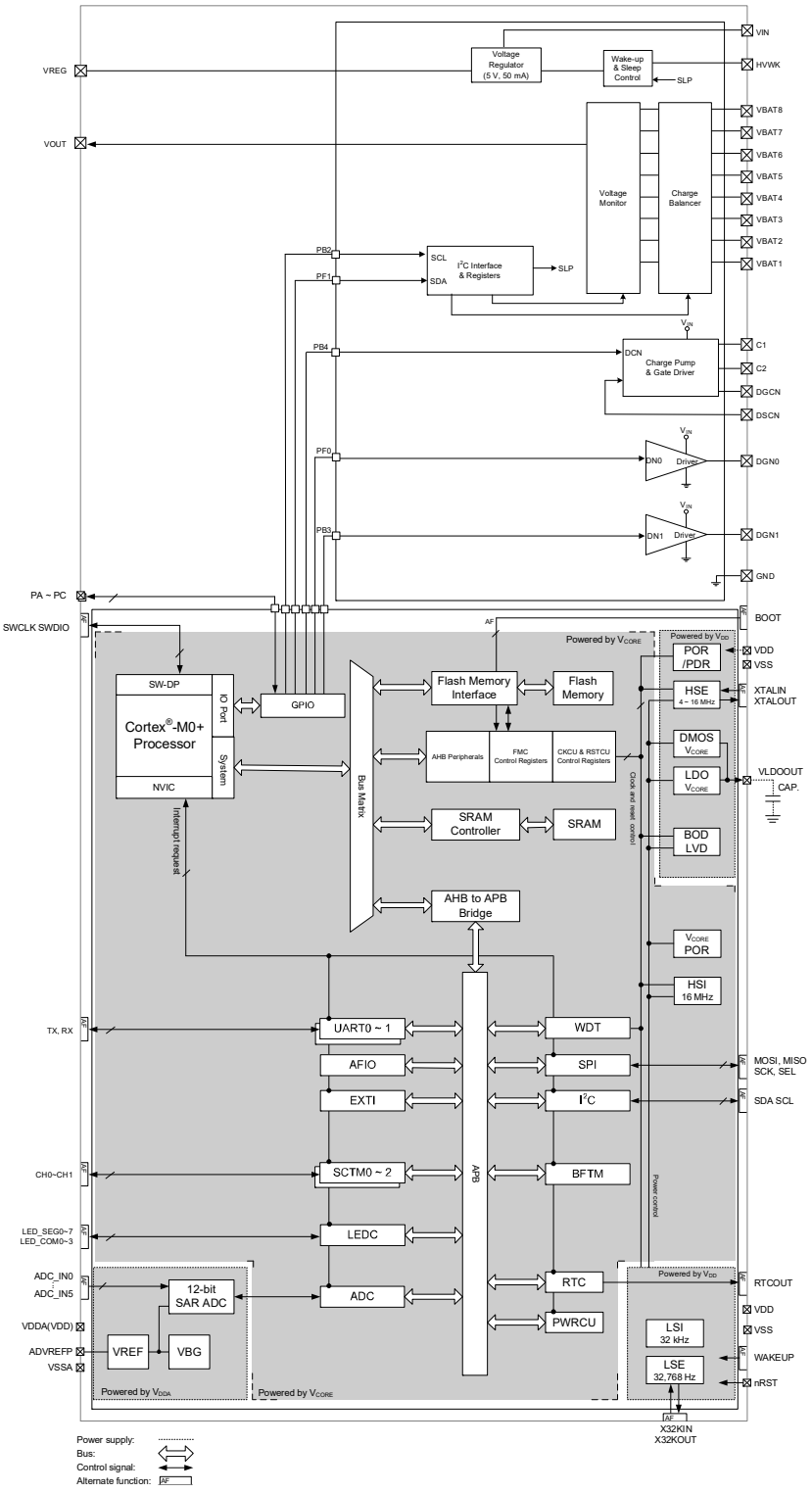


Figure 1. Block Diagram

Memory Map

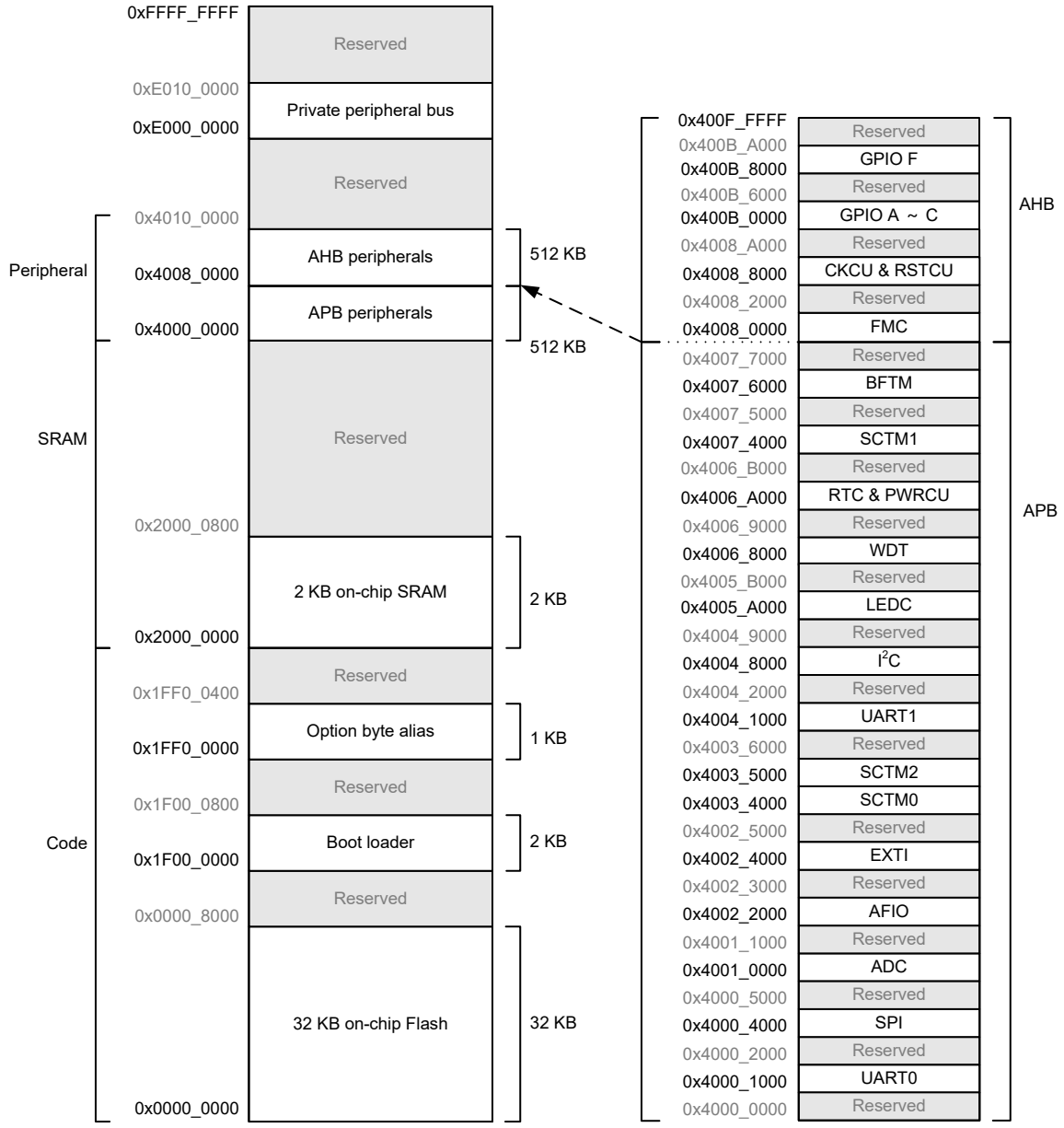


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	Reserved	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4003_5FFF	SCTM2	
0x4003_6000	0x4004_0FFF	Reserved	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C	
0x4004_9000	0x4005_9FFF	Reserved	
0x4005_A000	0x4005_AFFF	LEDC	
0x4005_B000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM	
0x4007_7000	0x4007_FFFF	Reserved	
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIO A	
0x400B_2000	0x400B_3FFF	GPIO B	
0x400B_4000	0x400B_5FFF	GPIO C	
0x400B_6000	0x400B_7FFF	Reserved	
0x400B_8000	0x400B_9FFF	GPIO F	
0x400B_A000	0x400F_FFFF	Reserved	

Clock Structure

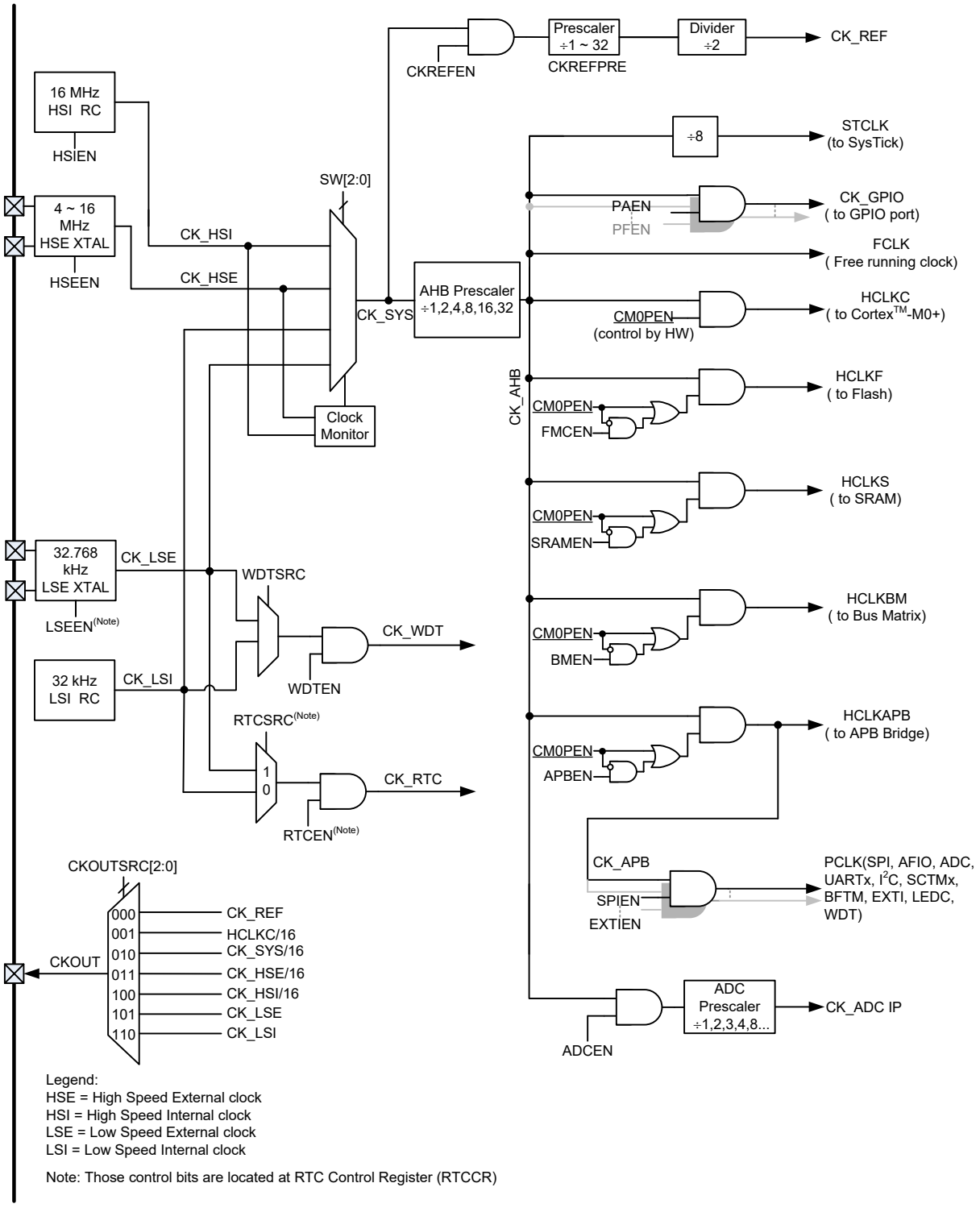


Figure 3. Clock Structure

4 Accumulative Cell Voltage Monitor

The Accumulative Cell Voltage Monitor is designed to monitor an accumulative voltage from 1 to N and outputs the divide-by-N voltage to the analog multiplexer. Each divided accumulative cell voltage from pin VBATn can be observed sequentially and measured by using the internal A/D converter, which is only required to externally connect the VOUT pin to the one of the internal A/D converter channels.

The Accumulative Cell Voltage Monitor can directly drive the MCU controlled power N-type MOSFETs to control charge and discharge by charge and discharge gate-drivers. The integrated battery balance circuitry provides a cell balance current without the need of external transistors.

An integrated regulator provides a 5 V supply to the MCU with a 50 mA driving current capability and which has ±1 % accuracy. The voltage regulator, cell voltage monitor and gate-drivers are shut down with an ultra-low standby current of 0.1 μA when the device is in the Sleep mode. When the HVWK pin is triggered by a voltage greater than its threshold, the device will return to the standby state.

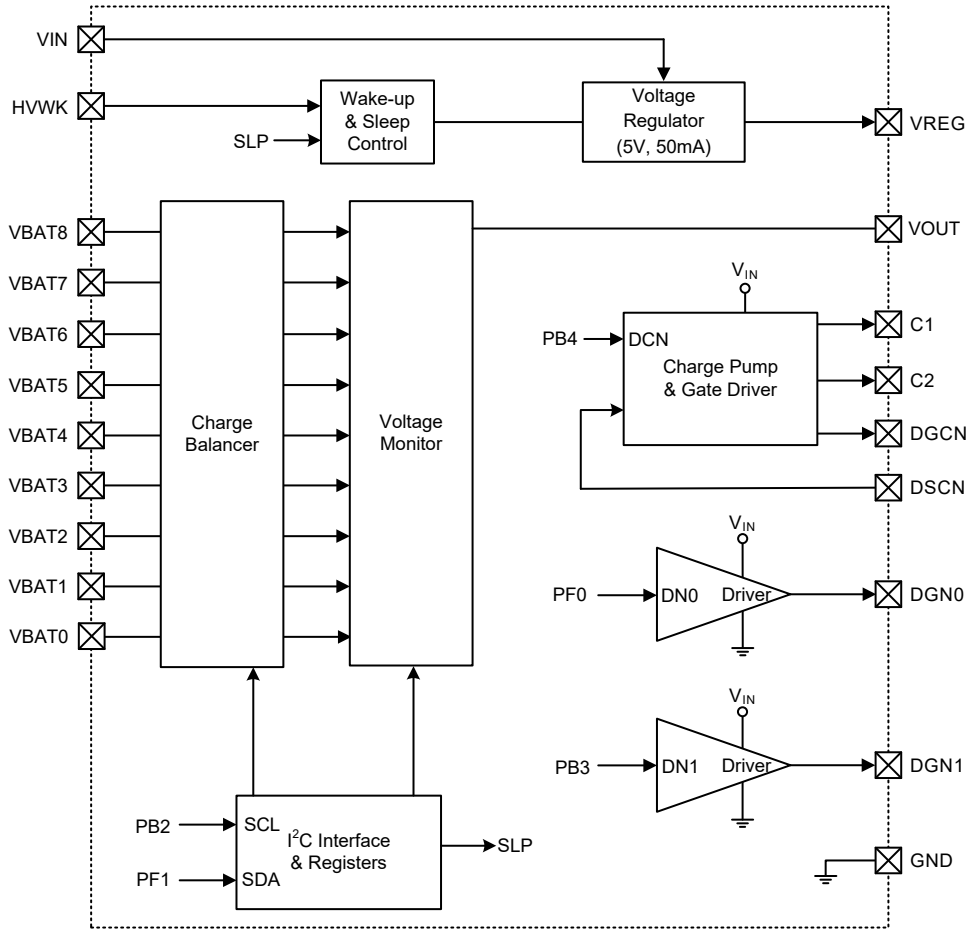


Figure 4. Accumulative Cell Voltage Monitor Block Diagram

I²C Serial Interface Functional Description

The Accumulative cell voltage monitor includes an I²C serial interface. The I²C bus is used for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are open-drain structure and two pull-high resistors are required. When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open-drain or open-collector to implement the Wired-AND function. Data transfer is initiated only when the bus is not busy.

Data Validity

The data on the SDA line must be stable during the clock high period. The high or low state of the data line can only change when the clock signal on the SCL line is low.

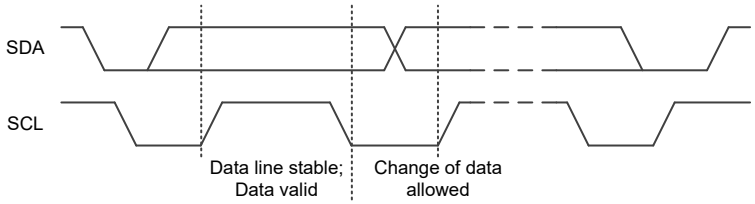


Figure 5. Data Validity

START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START (S).
- A low to high transition on the SDA line while SCL is high defines a STOP (P).
- START and STOP are always generated by the master. The bus is considered to be busy after the START. The bus is considered to be free again a certain time after the STOP.
- The bus remains busy if a Repeated START (Sr) is generated instead of a STOP. In the respect, the START and Repeated START are functionally identical.

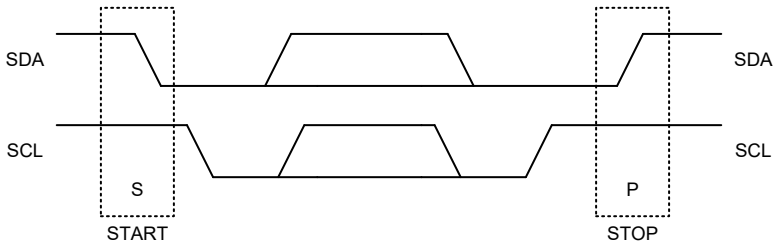


Figure 6. START and STOP Conditions

Byte Format

Every byte placed on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.

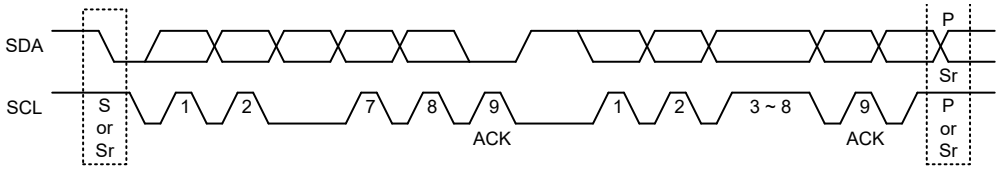


Figure 7. Byte Format

Acknowledge

- Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level placed on the bus by the receiver, the master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an acknowledge (ACK) after the reception of each byte.
- The device that provides an acknowledge must pull down the SDA line during the acknowledge clock pulse so that it remains at a stable low level during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge (NACK) bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse so as to not acknowledge. The master will generate a STOP or a Repeated START.

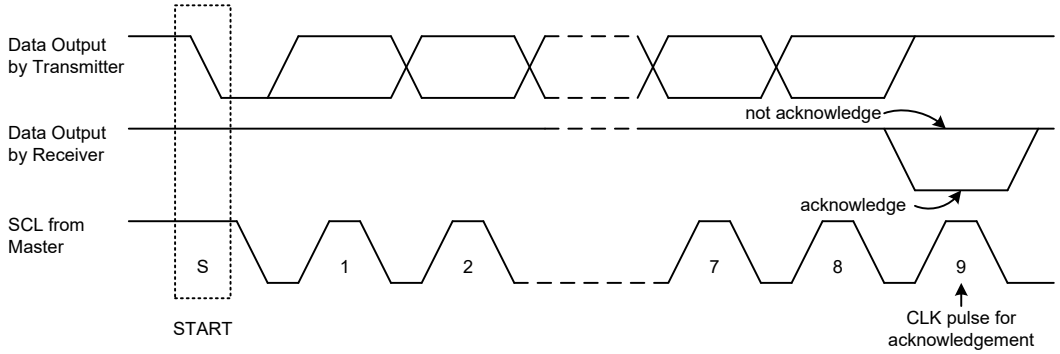


Figure 8. Acknowledge

I²C Time-out Control

In order to reduce the I²C lockup problem due to reception of erroneous clock sources, a time-out function is provided. The I²C time-out function starts timing for the specified I²C time-out period (t_{OUT}) when receiving START (S) from I²C bus. The timer is reset by every falling edge of SCL and gets interrupted when receiving STOP (P). If the next falling edge of SCL or STOP (P) does not appear throughout the I²C time-out period (t_{OUT}), the SDA and SCL are set to their default states at the end of timing and meanwhile the registers remains unchanged. The I²C time-out period can be specified to 32 ms or 64 ms by Trim-fuse selection.

Write Operation

An I²C write operation combines a START bit, a Slave address with a Write bit, a Register command byte, a Data byte and a STOP bit.

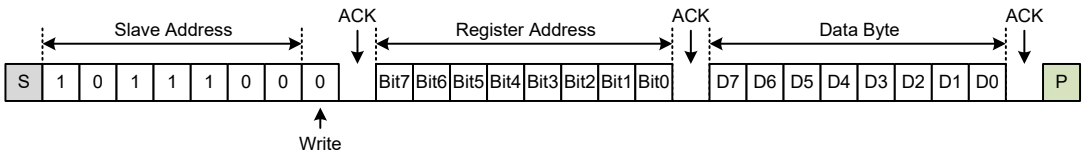


Figure 9. Write Operation Format

Read Sequence

The complete read mode consists of two stages. For the 1st stage, write the Register Address Byte to the device. For the 2nd stage, reads out the Data Byte from the device. The following diagram shows the complete read format.

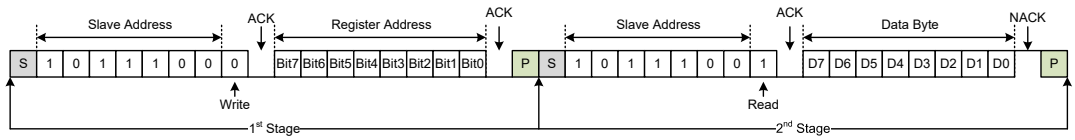


Figure 10. Read Sequence Format

Slave Address

- The slave address byte is the first byte received following the START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines whether a read or write operation is to be performed. When the R/W bit is "1", then a read operation is selected. When the R/W bit is "0", it selects a write operation.
- The slave address of the device is "1011100". When an address byte is sent, the device compares the first seven bits after the START condition. If matched, the device outputs an Acknowledge on the SDA line.

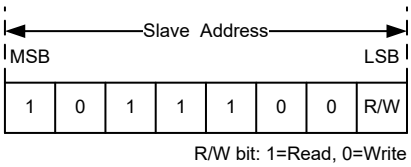


Figure 11. Slave Address Format

I²C Register Map

The I²C register map is listed below.

Address	Acronym	Access Type	Value after POR	Register Description
00H	REG00	R/W	0000 0000	Sleep and Voltage monitor
01H	REG01	R/W	0000 0000	Charge balance

• Sleep and Voltage Monitor Register

Bit	7	6	5	4	3	2	1	0
Name	SLP	EXT_WK	EN_S	Reserved	Reserved	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **SLP**: Sleep mode enable control
0: Stay in normal operation
1: Start Sleep procedure
At the state of EXT_WK = "1", SLP is reset to "0" and keep the "0" state until EXT_WK is cleared to "0". The Sleep command from I²C master is ignored during the state of EXT_WK = "1".

Bit 6 **EXT_WK**: External wake-up event status
0: Denotes that external wake-up event does not exist
1: Denotes that external wake-up event exists or is written by MCU
(1) When the voltage applied on HVWK pin remains higher than V_{WKTH} over 10 μs, the EXT_WK will be set to "1" and the SLP will be reset to "0". The EXT_WK is cleared to "0" immediately when the voltage applied on HVWK pin is less than 1.5 V.
(2) The EXT_WK can be written as "1" by MCU for the purpose of sending a wake-up signal. The EXT_WK and SLP have to be written as "0" through the I²C interface after the EXT_WK is set to "1" by MCU, otherwise the external wake-up event on HVWK pin cannot be recognized and the follow-up Sleep command will be failed.
(3) Writing both EXT_WK and SLP as "1" is not permitted for avoiding unpredictable status.
(4) Reading EXT_WK reveals the external wake-up even status of the HVWK pin only.

Bit 5 **EN_S**: Voltage monitor function enable control
0: Voltage monitor function is disabled, V_{OUT} = 0 V
1: Voltage monitor function is enabled, $V_{OUT} = V_{BATn}/n$

Bit 4~3 Reserved bits

Bit 2~0 **B2~B0**: 8-to-1 analog multiplexer selection bits (MSB: B2, LSB: B0)
Control B2~B0 to select which accumulative cell voltage to be output to VOUT.

EN_S	B2	B1	B0	V_{OUT} (V)
0	—	—	—	0
1	0	0	0	V_{BAT1} × 1/1
1	0	0	1	V_{BAT2} × 1/2
1	0	1	0	V_{BAT3} × 1/3
1	0	1	1	V_{BAT4} × 1/4
1	1	0	0	V_{BAT5} × 1/5
1	1	0	1	V_{BAT6} × 1/6
1	1	1	0	V_{BAT7} × 1/7
1	1	1	1	V_{BAT8} × 1/8

- **Charge Balance Register**

Bit	7	6	5	4	3	2	1	0
Name	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **CB8**: Enable control of the charge balance switch between VBAT8 and VBAT7
0: Balance switch OFF
1: Balance switch ON

Bit 6 **CB7**: Enable control of the charge balance switch between VBAT7 and VBAT6
0: Balance switch OFF
1: Balance switch ON

Bit 5 **CB6**: Enable control of the charge balance switch between VBAT6 and VBAT5
0: Balance switch OFF
1: Balance switch ON

Bit 4 **CB5**: Enable control of the charge balance switch between VBAT5 and VBAT4
0: Balance switch OFF
1: Balance switch ON

Bit 3 **CB4**: Enable control of the charge balance switch between VBAT4 and VBAT3
0: Balance switch OFF
1: Balance switch ON

Bit 2 **CB3**: Enable control of the charge balance switch between VBAT3 and VBAT2
0: Balance switch OFF
1: Balance switch ON

Bit 1 **CB2**: Enable control of the charge balance switch between VBAT2 and VBAT1
0: Balance switch OFF
1: Balance switch ON

Bit 0 **CB1**: Enable control of the charge balance switch between VBAT1 and GND
0: Balance switch OFF
1: Balance switch ON

Accumulative Cell Voltage Monitor Functional Description

The accumulative cell voltage monitor consists of high voltage switches, voltage dividers and an 8-to-1 analog multiplexer as shown in the following diagram. The high voltage switches are implemented using an anti-reverse current topology which provides isolation between the output voltage and the unselected VBATn.

EN_S, B2, B1 and B0 are four control bits from I²C interface and are used to control the P-type MOSFET S1 ~ S8 only if EN_S = "1". The control truth table is shown below. This produces an accumulative cell voltage, V_{BATn}, divided by "n" on VOUT. This accurate ±0.5% voltage divided ratio is designed to minimize any mismatch errors.

Table 3. Accumulative Cell Voltage Monitor Truth Table

EN_S	B2	B1	B0	S8	S7	S6	S5	S4	S3	S2	S1	V_{OUT} (V)
0	X	X	X	1	1	1	1	1	1	1	1	0
1	0	0	0	1	1	1	1	1	1	1	0	V_{BAT1} × 1/1
1	0	0	1	1	1	1	1	1	1	0	1	V_{BAT2} × 1/2
1	0	1	0	1	1	1	1	1	0	1	1	V_{BAT3} × 1/3
1	0	1	1	1	1	1	1	0	1	1	1	V_{BAT4} × 1/4
1	1	0	0	1	1	1	0	1	1	1	1	V_{BAT5} × 1/5
1	1	0	1	1	1	0	1	1	1	1	1	V_{BAT6} × 1/6
1	1	1	0	1	0	1	1	1	1	1	1	V_{BAT7} × 1/7
1	1	1	1	0	1	1	1	1	1	1	1	V_{BAT8} × 1/8

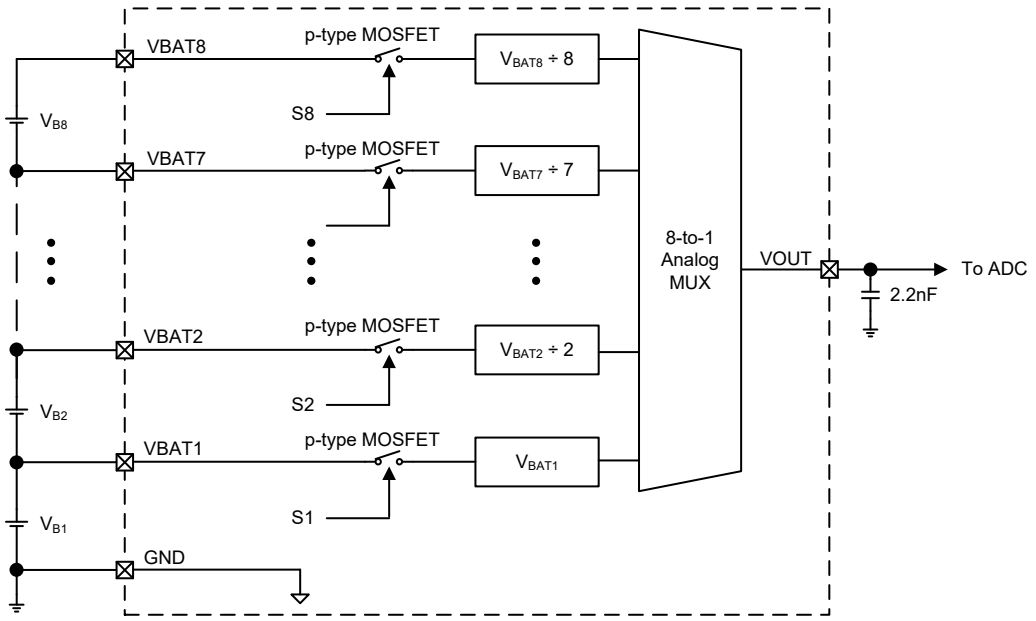


Figure 12. Accumulative Cell Voltage Monitor Functional Block

Charge Balance Functional Description

Multiple channels of charge balance switch can be turned on by MCU via I²C interface. The register address of charge balance function is 01H, and the Bit 7 ~ Bit 0 of Data byte correspond to the charge balance switch of each channel from CB8 to CB1, respectively. More than one switch can be turned on at the same time, **but side-by-side cell balancing switches are recommended not to be turned on simultaneously to ensure equal balance current between each channel**. After receiving a turn on command, the charge balance switch remains turned on until it is turned off by a "0" data or getting a command of SLP bit = "1". The typical charge balance current is 10 mA when the battery cell voltage is 4.2 V and the external series resistance is 100 Ω, and the balance current can be adjusted by series resistors R1 ~ R8. **Note that for the reason of keeping voltage monitor accuracy, do not proceed voltage monitor while charge balance is activated**.

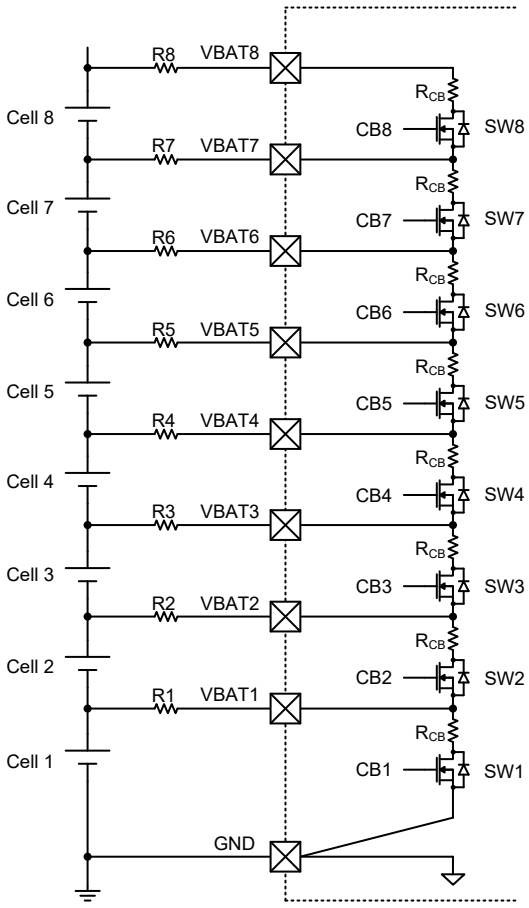


Figure 13. Charge Balance Functional Circuit Diagram

Table 4. Balance Switch ON/OFF

CB1	CB2	CB3	CB4	CB5	CB6	CB7	CB8	Balance Switch ON/OFF
1	0	0	0	0	0	0	0	SW1 ON, others OFF
0	1	0	0	0	0	0	0	SW2 ON, others OFF
0	0	1	0	0	0	0	0	SW3 ON, others OFF
0	0	0	1	0	0	0	0	SW4 ON, others OFF
0	0	0	0	1	0	0	0	SW5 ON, others OFF
0	0	0	0	0	1	0	0	SW6 ON, others OFF
0	0	0	0	0	0	1	0	SW7 ON, others OFF
0	0	0	0	0	0	0	1	SW8 ON, others OFF

Note: More than one switch can be turned on in the same time.

Discharge N-type MOSFET Gate-drive Functional Description

Two discharge NMOS gate-drivers DGN0 and DGN1 are fabricated in the Accumulative Cell Voltage Monitor as discharge switch controllers. The output voltage of DGN0 and DGN1 are both clamped at 12 V. A 430 kΩ pull-down resistor is integrated in the discharge gate control input pins DN0 and DN1. The gate-driver capability of DGN0 is better than that of DGN1, therefore it is recommended to apply DGN0 on primary loading path and DGN1 on secondary loading path. While operating in the Standby or Sleep mode, the DGN0 and DGN1 are pulled down by 5 Ω and 8.5 Ω respectively. The control logic and output status of DGN0 and DGN1 in each state are listed in the following table.

Table 5. DGN0 Control Logic and Output Status

SLP	DN0	V(DGN0, GND)	Note
0	Floating	0	Pulled low to GND by 5 Ω.
0	0	0	
0	1	V_Z	Normal operation.
1	Floating	0	Pulled low to GND by 5 Ω.
1	0	0	

Table 6. DGN1 Control Logic and Output Status

SLP	DN1	V(DGN1, GND)	Note
0	Floating	0	Pulled low to GND by 8.5 Ω.
0	0	0	
0	1	V_Z	Normal operation.
1	Floating	0	Pulled low to GND by 8.5 Ω.
1	0	0	

Charge N-type MOSFET Gate-drive Functional Description

A charge NMOS gate-drive DGCN is provided as a charge switch controller. A charge pump circuit is fabricated to provide 12 V between the gate and source node of charge NMOS. A 430 kΩ pull-down resistor is integrated in the control input pin DCN. The control logic of DCN and output status of DGCN and DSCN in each state are listed in the following table.

Table 7. DCN Control Logic, DGCN and DSCN Output Status

SLP	DCN	V(DGCN, DSCN)	Note
0	Floating	0	DGCN and DSCN pulled low to GND by 50 Ω respectively. DGCN pulled low to DSCN by 90 Ω.
0	0	0	
0	1	V_Z	Normal operation.
1	Floating	0	DGCN and DSCN pulled low to GND by 830 Ω respectively. DGCN pulled low to DSCN by 1.65 kΩ.
1	0	0	

Sleep Mode Functional Description

It is important not to confuse this Sleep mode with the Sleep mode, which is described in the "Power Management – PWRCU" section of this datasheet.

EXT_WK represents the external wake-up event status. EXT_WK = "0" means that high voltage applied on the HVWK pin is not detected, on the contrary EXT_WK = "1" denotes that wake-up event is happening such as charger connecting or power switch on. When receiving a sleep command from I²C master at EXT_WK = "0", the SLP bit is set to "1" and the Accumulative Cell Voltage Monitor enters the Sleep mode. During the Sleep mode, all outputs are shut down and the capacitor of VREG is discharged through internal discharge resistor. The pre-regulator and high voltage wake-up circuit are the only blocks that are still working in the Sleep mode and operate with an ultra-low standby current of 0.1 μA (typical).

When EXT_WK = "1", the SLP will be cleared to "0" and the sleep command from I²C master will be abandoned until EXT_WK is cleared to "0".

Table 8. Enter / Exit Sleep Mode

EXT_WK Status	SLP Status
0	According to I²C master command or POR default.
1	0

Wake up from Sleep Mode Functional Description

The HVWK pin can be used for detecting charger plugged-in, switch turned on, or load connected events. When the Accumulative Cell Voltage Monitor is under the Sleep mode, if the HVWK pin is triggered by a pulse with requiring at least 5.5 V voltage and 1ms width, the output of VREG will resume and the whole Accumulative Cell Voltage Monitor is ready for normal operation. The reference timing diagram of entering the Sleep mode and waked up is listed below.

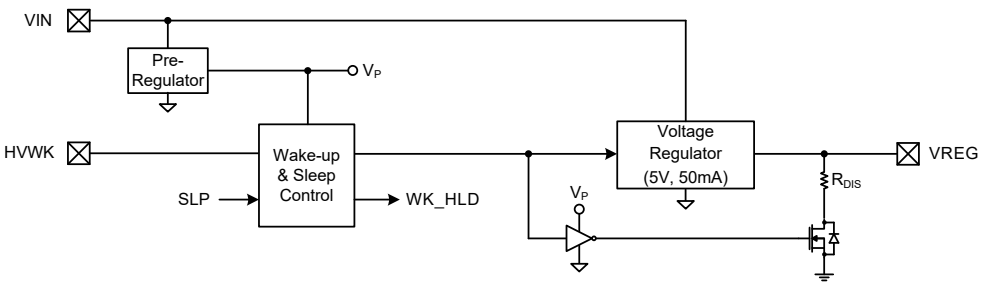


Figure 14. Wake up from Sleep Mode Functional Block Diagram

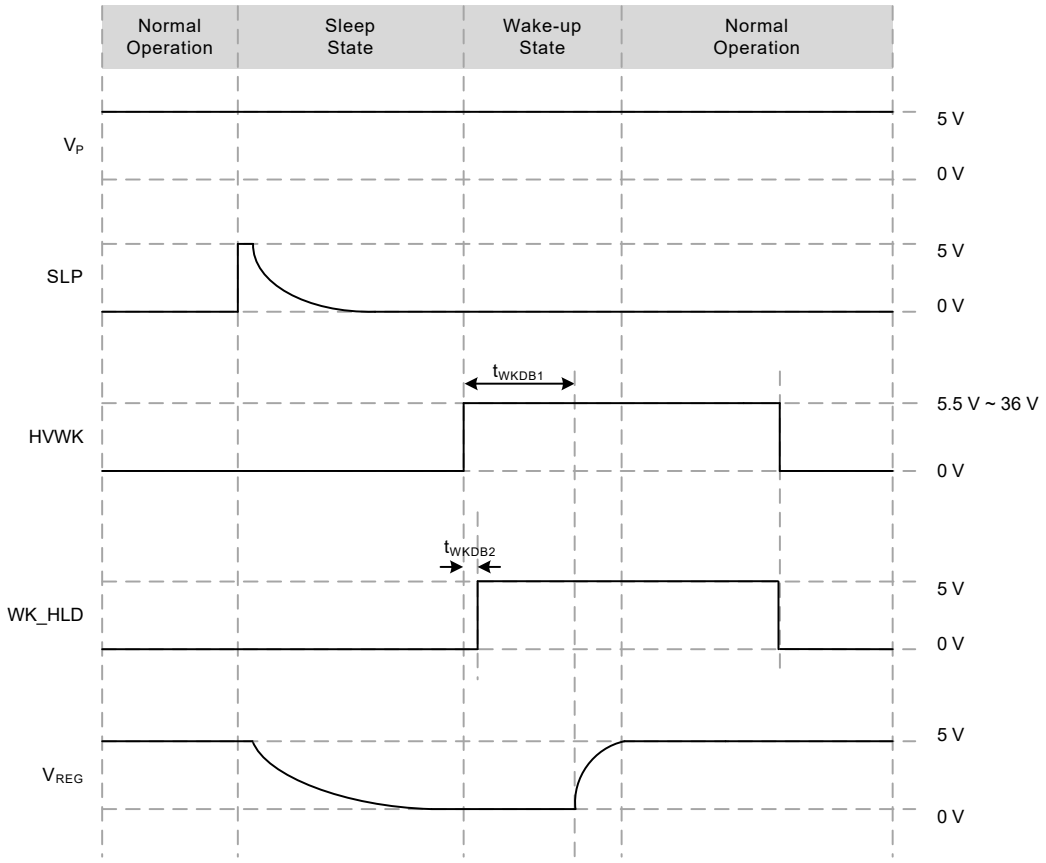


Figure 15. Entering the Sleep Mode and Waked up Reference Timing Diagram

Charge NMOS Switch Configuration

Due to the internal pull down MOS switch between DSCN and GND, the recommended Charge NMOS switch configuration is back-to-back or single NMOS in series with a diode in order to avoid the DSCN pin draining current from battery.

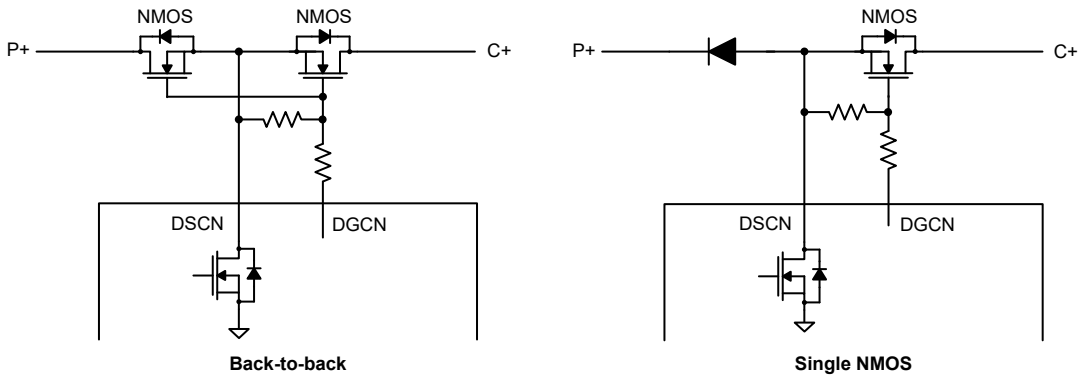


Figure 16. Charge NMOS Switch Configuration

VIN, VREG, VOUT Capacitors

The VIN input capacitor C1 and VREG output capacitor C2 are 4.7 μF for better input noise filtering and output load transient behavior. A recommended 2.2 nF noise filtering capacitor should be connected between VOUT and GND terminals. Note that higher noise capacitance value of C3 will lower the acceptable scan frequency.

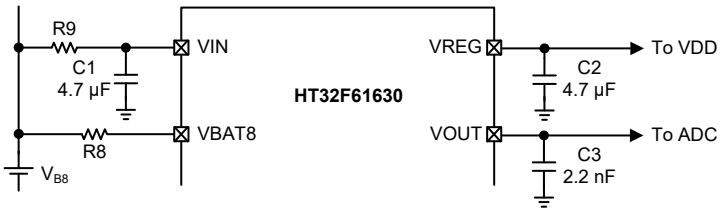


Figure 17. VIN, VREG, VOUT Capacitors Configuration

VIN Filter Recommendation

The input capacitor C1 for VIN is used for lowering the input voltage ripple while the battery is supplying a highly inductive load in PWM mode. The recommanded value of VIN input capacitor C1 is 4.7 μF. The input resistor R9 of VIN is able to reduce the inrush current during battery assembly, and also it shares the heat on chip while VREG outputs a large current in normal operation mode. The recommanded value for VIN input resistor R9 differs from different battery cell number applications. The recommended resistance values of VIN input resistor R9 with different battery cell numbers and the corresponding VREG maximum output current are listed in the following table.

Table 9. VIN Input Resistor R9 Recommended Resistance Values

Battery Cell Number	VIN Recommended Resistor (R9)	VREG Maximum Output Current
3 S	15 Ω	50 mA
4 S	43 Ω	50 mA
5 S	110 Ω	40 mA
6 S	220 Ω	35 mA
7 S	330 Ω	30 mA
8 S	430 Ω	30 mA

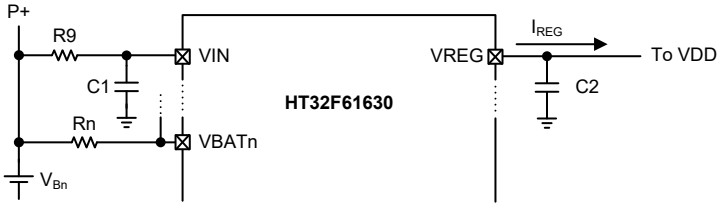


Figure 18. VIN Filter Circuit Diagram

It is necessary to select an appropriate package for VIN filter resistor (R9) in order to prevent it being damaged from overheated. The maximum power on R9 is easily calculated by:

$$P_{R9.MAX} = (I_{REG})^2 \times R9$$

where I_{REG} is the maximum VREG output current, R9 is the resistance value of VIN filter resistor (R9).

It is recommended to choose the resistor package that its maximum rated power is greater than twice the $P_{R9.MAX}$.

VBATn Protection and Balance Resistor Selection

The VBATn series resistors R1~R8 not only suppress inrush and noise spikes applied to I/O pins, they affect charge balance current as well. Larger resistance of R1 ~ R8 provide better protection to VBATn and other I/O pins, but they lower the charge balance current instead. The charge balance current of each channel is configured by internal balance resistance and external series resistors. Because the balance current of Cell 1 flows out through the GND pin, the balance current of Cell 1 is greater than that of other cells. Considering inrush spike protection to I/O pins and noise reduction of voltage monitor, the recommended typical values of resistor R1 ~ R8 are 100 Ω, and the charge balancing current is 11mA while the voltage of battery cell is 4.2 V. If larger balancing current is needed, the recommended minimum values of the R1 ~ R8 resistors are 30 Ω which provide 25 mA while the voltage of battery cell is 4.2 V. To ensure the internal balance circuit works properly, the minimum battery cell voltage to start the balance function is 3 V. The recommended VBATn series resistances and their related charge balancing current are listed in the following table.

Table 10. VBATn Protection and Balance Resistor Selection

Resistance of R1 ~ R8	Typical Balancing Current (@ V_{Bn} = 4.2 V)	Note
30 Ω	25 mA	Minimum value of resistors R1 ~ R8
51 Ω	18 mA	—
100 Ω	11 mA	—
150 Ω	8.4 mA	—

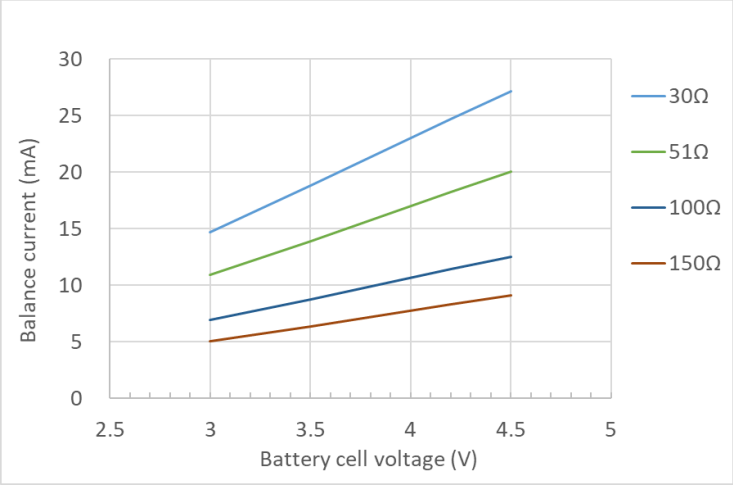


Figure 19. Balance Current VS Battery Cell Voltage

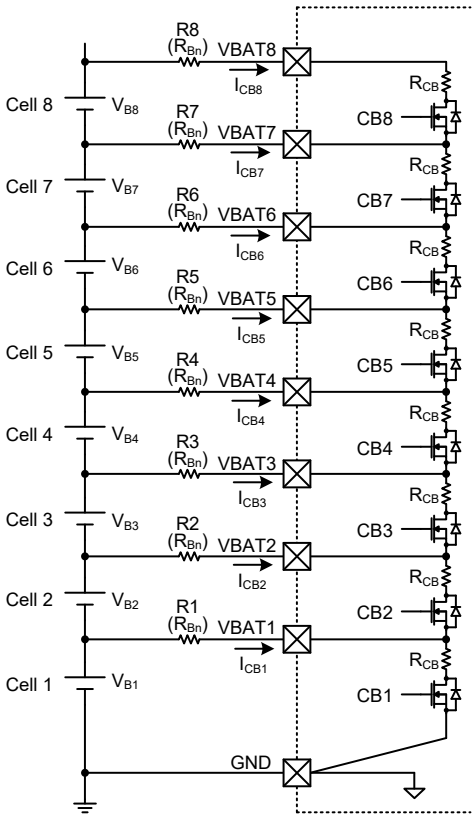


Figure 20. VBATn Protection and Charge Balance Function Circuit Diagram

Charger and Switch Status Detection

The High-voltage wake-up (HVWK) function is capable of detecting charger plugged in or load switched on. The recommended HVWK external circuit is listed below. When a charger is plugged in or load switch is on, the voltage of HVWK is triggered to be larger than V_{WKTH} and set EXT_WK bit as "1". After the charger or switch is removed or turned off, the EXT_WK bit is reset to "0". An MCU can acquire the charger or switch status by reading the EXT_WK bit through the I^2C interface. Therefore, by the means of reading the EXT_WK bit status, additional charger or switch detection circuit for MCU are not necessary. The circuit below is a typical application for high-voltage wake-up function, charger plugged-in detection and charger voltage detection.

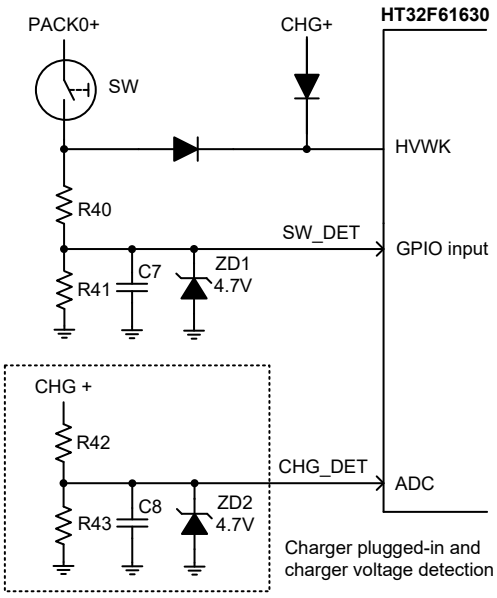


Figure 21. Charger and Switch Status Detection Circuit Diagram

Cell Voltage Monitor Scan Frequency

The VOUT pin can output the accumulative cell voltage and be connected to one of the internal A/D converter channels for monitoring battery voltage status. The timing diagrams of cell voltage monitor scanning for 5S and 8S applications are shown below. The VOUT pin starts to charge the VOUT capacitor from 0V to the selected cell voltage while the EN_S is set to "1". In order to ensure MCU A/D conversion accuracy, the A/D conversion procedure has to wait before the VOUT capacitor is fully charged. The suggested minimum waiting time is 5ms after the EN_S is set to "1" or cell voltage monitor channel switched. It is recommended that the maximum scan frequency for accumulative cell voltage monitoring is less than 100 Hz and that EN_S = "0" when the voltage scanning procedure has finished for power saving purposes.

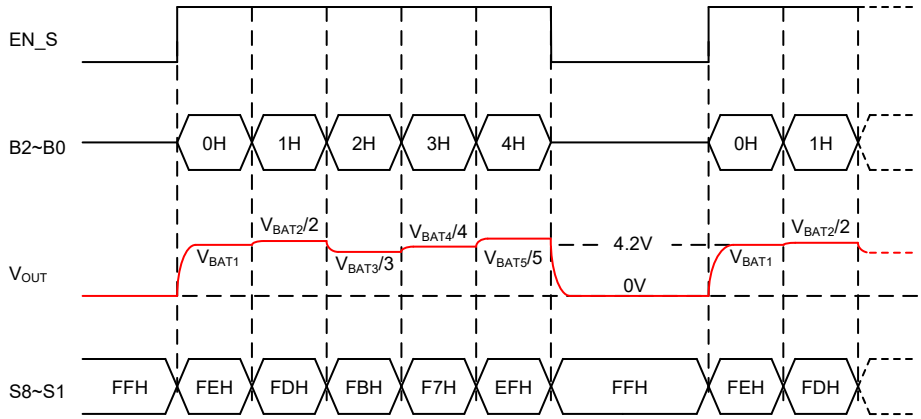


Figure 22. 5 S Battery Monitoring Timing

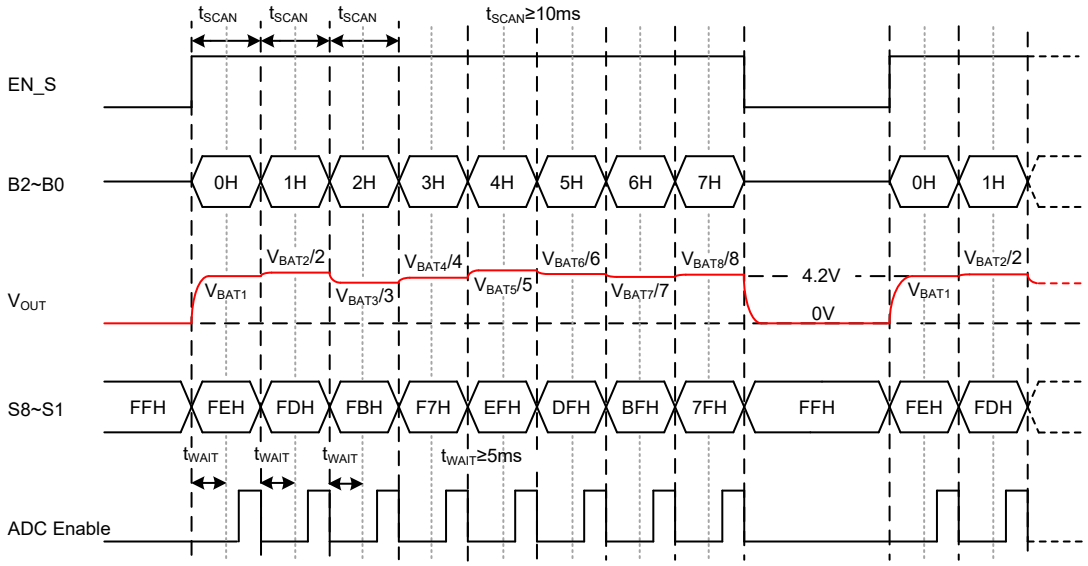


Figure 23. 8 S Battery Monitoring Timing

Voltage Spike Suppression Method

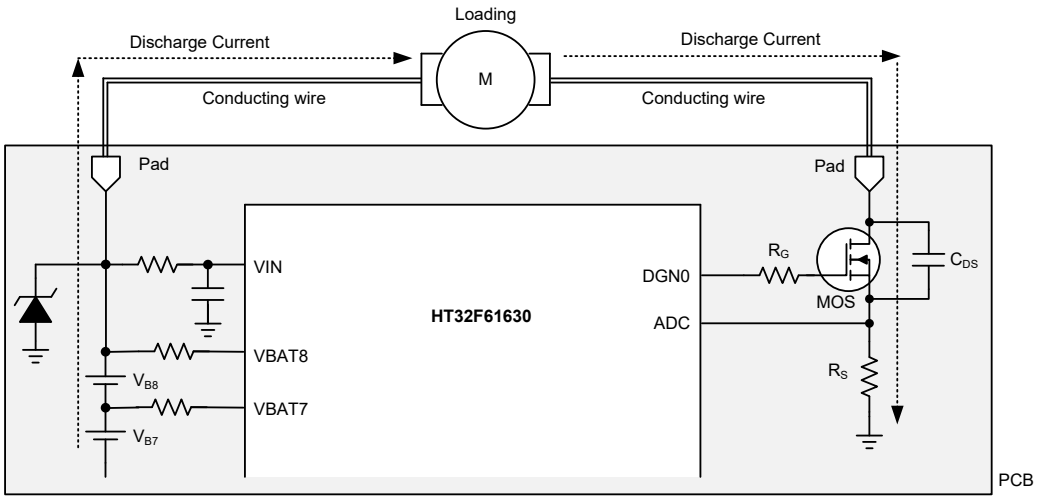


Figure 24. Simplified Typical BMS System Discharge Path Diagram

Most battery-management systems would monitor charge and discharge current to prevent over-current damage. Due to the parasitic inductance on conducting wires and PCB layout connections, large voltage spike may occurs while the MOS rapidly shuts down the charge or discharge current, and this spike may damage the device VBATn or VIN pins. Any voltage spike on the VBATn and VIN pins should not over the limitation in Absolute Maximum Ratings, which is 48 V. Four recommended measures listed below would help to reduce the voltage spike.

1. Make the external conducting wire and PCB layout connections as short as possible where large charge or discharge current flows.
2. Adjust the slew rate of MOS switch with the gate resistor R_G. Turn off the MOS with slower slew rate for lower voltage spike, and the tradeoff is a slower protection response time.
3. Add a capacitor (C_{DS}) between drain and source node of the MOS switch as shown above. The recommended capacitance is 0.1μF to 0.22 μF.
4. Add a Zener diode between the highest voltage potential node of battery cells and GND.

PCB Layout Considerations

The following component placement and layout guidelines are suggested for the sake of noise reduction and voltage spike suppression.

1. The VIN filter capacitor must be close to VIN pin.
2. The VREG regulation and noise filter capacitor must be close to VREG pin.
3. The tracks where large current would flow through should be wide and short to suppress the voltage spike at the time when external NMOS switch change its ON/OFF state.
4. Minimize VBAT1 ~ VBAT8 signal trace length to reduce parasitic inductance and capacitance and improve measure accuracy.

Thermal Considerations

The maximum power dissipation depends upon the thermal resistance of the IC package, PCB layout, rate of surrounding airflow and difference between the junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA} \text{ (W)}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of IC package.

For maximum operating rating conditions, the maximum junction temperature is 125 °C. However, it is recommended that the maximum junction temperature does not exceed 125 °C during normal operation to maintain high reliability. The de-rating curve of the maximum power dissipation is show below:

$$P_{D(MAX)} = (125\ °C - 25\ °C) / (50\ °C/W) = 2\ W$$

For a fixed $T_{J(MAX)}$ of 125 °C, the maximum power dissipation depends upon the operating ambient temperature and the package's thermal resistance, θ_{JA}. The de-rating curve below shows the effect of rising ambient temperature on the maximum recommended power dissipation.

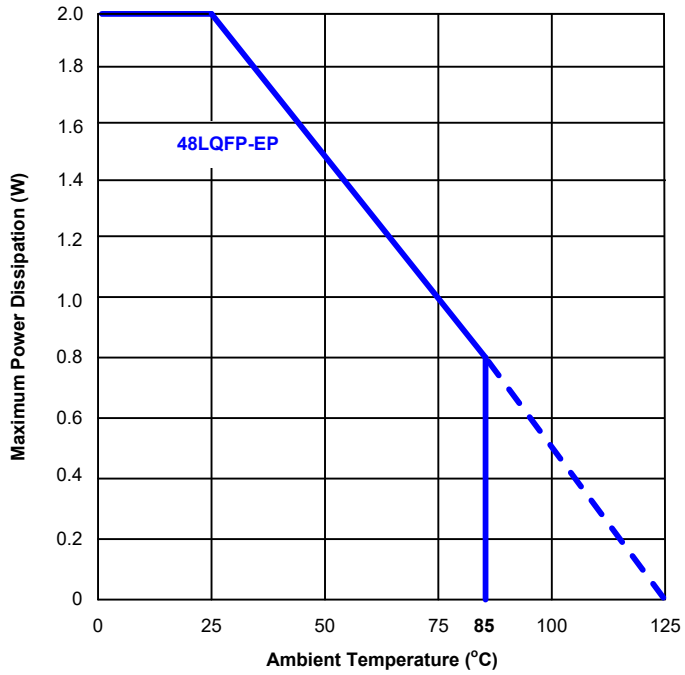


Figure 25. Maximum Power Dissipation VS Ambient Temperature

5 Pin Assignment

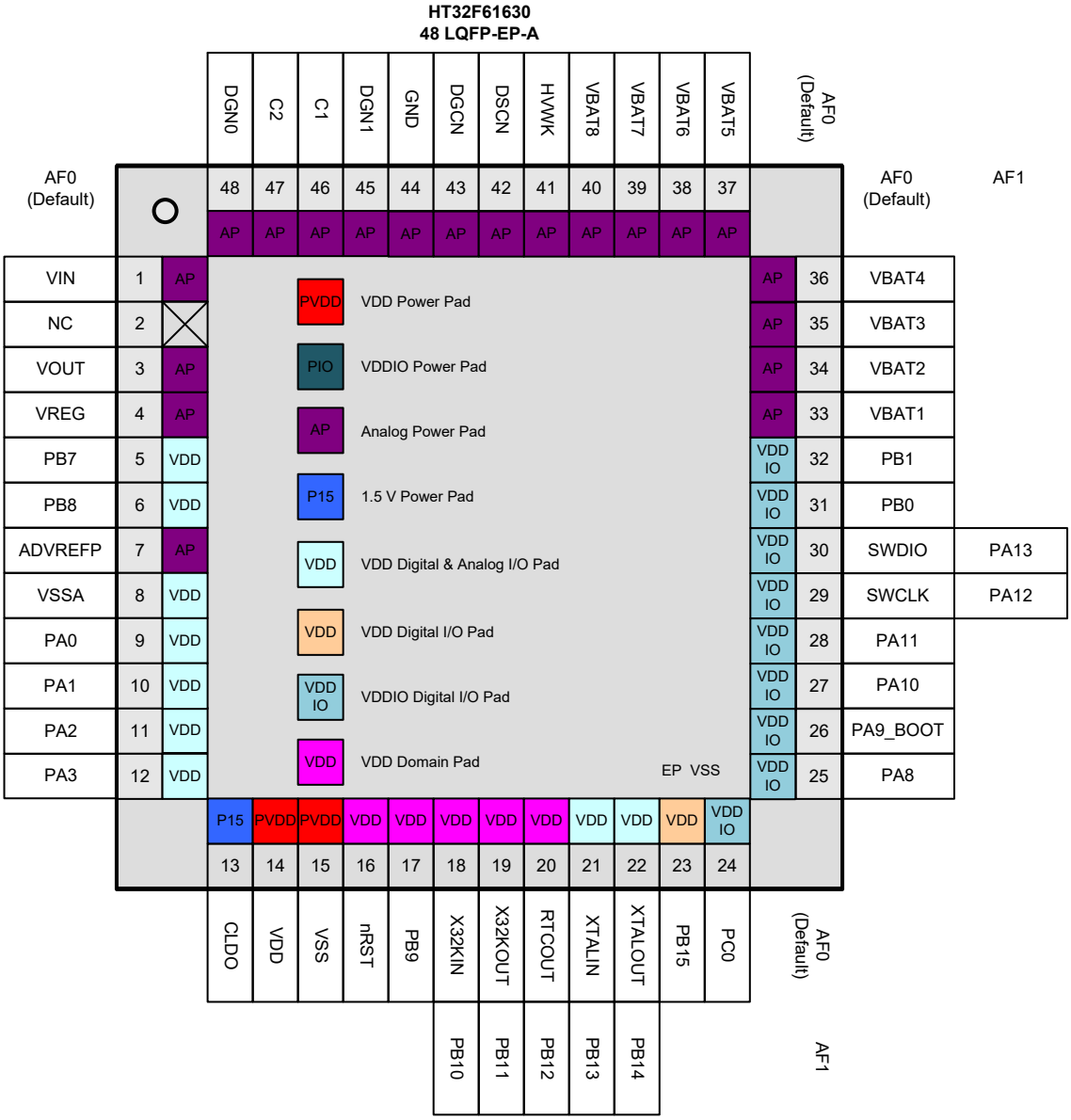


Figure 26. 48 pin LQFP-EP Pin Assignment

Table 11. Pin Assignment

Package	Alternate Function Mapping							
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
48 LQFP-EP	System Default	System Other	ADC	LEDC	SCTM	SPI	UART	I2C
9	PA0	VBG	ADC_IN2	LED_SEG0	SCTM1_CH0	SPI_SCK		I2C_SCL
10	PA1		ADC_IN3	LED_SEG1	SCTM1_CH1	SPI_MOSI		I2C_SDA
11	PA2		ADC_IN4	LED_SEG2		SPI_MISO	UR0_TX	
12	PA3		ADC_IN5	LED_SEG3		SPI_SEL	UR0_RX	
13	CLDO							
14	VDD							
15, EP(Note)	VSS							
16	nRST							
17	PB9	PB9 / WAKEUP1			SCTM0_CH0			
18	X32KIN	PB10		LED_SEG4	SCTM1_CH1	SPI_SEL	UR1_TX	
19	X32KOUT	PB11		LED_SEG5	SCTM1_CH0	SPI_SCK	UR1_RX	
20	RTCOUT	PB12 / WAKEUP0			SCTM0_CH1	SPI_MISO		
21	XTALIN	PB13		LED_SEG6	SCTM2_CH0		UR0_TX	I2C_SCL
22	XTALOUT	PB14		LED_SEG7	SCTM2_CH1		UR0_RX	I2C_SDA
23	PB15					SPI_SEL		I2C_SCL
24	PC0			LED_OM0	SCTM1_CH1	SPI_SCK		I2C_SDA
25	PA8			LED_OM1	SCTM2_CH1		UR0_TX	
26	PA9_BOOT	CKOUT			SCTM1_CH0	SPI_MOSI		
27	PA10			LED_OM2	SCTM0_CH0	SPI_MOSI	UR0_RX	
28	PA11			LED_OM3	SCTM0_CH1	SPI_MISO		
29	SWCLK	PA12						
30	SWDIO	PA13						
31	PB0			LED_SEG0	SCTM2_CH0	SPI_MOSI	UR0_TX	I2C_SCL
32	PB1			LED_SEG1	SCTM2_CH1	SPI_MISO	UR0_RX	I2C_SDA
33	VBAT1							
34	VBAT2							
35	VBAT3							
36	VBAT4							
37	VBAT5							
38	VBAT6							
39	VBAT7							
40	VBAT8							
41	HVWK							
42	DSCN							
43	DGCN							
44	GND							

Package	Alternate Function Mapping							
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
48 LQFP-EP	System Default	System Other	ADC	LEDC	SCTM	SPI	UART	I2C
45	DGN1							
46	C1							
47	C2							
48	DGN0							
1	VIN							
2	NC							
3	VOUT							
4	VREG							
5	PB7		ADC_IN0	LED_SEG4	SCTM0_CH0	SPI_MISO	UR0_TX	I2C_SCL
6	PB8		ADC_IN1	LED_SEG5	SCTM0_CH1	SPI_SEL	UR0_RX	I2C_SDA
7	ADVREFP							
8	VSSA							

Note: The EP VSS is internally connected to the VSS of pin number 15 and externally connected to the GND pin.
The EP means the Exposed Pad of the LQFP-EP package.

Table 12. Pin Description

Pin Number	Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
48 LQFP-EP					Default Function (AF0)
9	PA0	AI/O	5V	4/8/12/16 mA	PA0
10	PA1	AI/O	5V	4/8/12/16 mA	PA1
11	PA2	AI/O	5V	4/8/12/16 mA	PA2, this pin provides a UART_TX function in the Boot loader mode.
12	PA3	AI/O	5V	4/8/12/16 mA	PA3, this pin provides a UART_RX function in the Boot loader mode.
13	CLDO	P	—	—	Core power LDO output It must be connected a 2.2 μF capacitor as close as possible between this pin and VSS.
14	VDD	P	—	—	Voltage for digital I/O
15, EP	VSS	P	—	—	Ground reference for digital I/O
16	nRST(3)	I	5V_PU	—	External reset pin
17	PB9(3)	I/O (V_{DD})	5V	4/8/12/16 mA	PB9
18	PB10(3)	AI/O (V_{DD})	5V	4/8/12/16 mA	X32KIN
19	PB11(3)	AI/O (V_{DD})	5V	4/8/12/16 mA	X32KOUT
20	PB12(3)	I/O (V_{DD})	5V	4/8/12/16 mA	RTCOUT
21	PB13	AI/O	5V	4/8/12/16 mA	XTALIN
22	PB14	AI/O	5V	4/8/12/16 mA	XTALOUT
23	PB15	I/O	5V	4/8/12/16 mA	PB15
24	PC0	I/O (V_{DD})	5V	4/8/12/16 mA	PC0
25	PA8	I/O (V_{DD})	5V	4/8/12/16 mA	PA8
26	PA9	I/O (V_{DD})	5V_PU	4/8/12/16 mA	PA9_BOOT
27	PA10	I/O (V_{DD})	5V	4/8/12/16 mA	PA10
28	PA11	I/O (V_{DD})	5V	4/8/12/16 mA	PA11
29	PA12	I/O (V_{DD})	5V_PU	4/8/12/16 mA	SWCLK
30	PA13	I/O (V_{DD})	5V_PU	4/8/12/16 mA	SWDIO
31	PB0	I/O (V_{DD})	5V	4/8/12/16 mA	PB0
32	PB1	I/O (V_{DD})	5V	4/8/12/16 mA	PB1

Pin Number	Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
48 LQFP-EP					Default Function (AF0)
33	VBAT1	AI	—	—	Battery cell 1 positive terminal and battery cell 2 negative terminal
34	VBAT2	AI	—	—	Battery cell 2 positive terminal and battery cell 3 negative terminal
35	VBAT3	AI	—	—	Battery cell 3 positive terminal and battery cell 4 negative terminal
36	VBAT4	AI	—	—	Battery cell 4 positive terminal and battery cell 5 negative terminal
37	VBAT5	AI	—	—	Battery cell 5 positive terminal and battery cell 6 negative terminal
38	VBAT6	AI	—	—	Battery cell 6 positive terminal and battery cell 7 negative terminal
39	VBAT7	AI	—	—	Battery cell 7 positive terminal and battery cell 8 negative terminal
40	VBAT8	AI	—	—	Battery cell 8 positive terminal
41	HVWK	AI	—	—	High voltage wake-up function sense and trigger pin
42	DSCN	AO	—	—	Charge pump reference voltage input. Connect to charge N-type MOSFET source pin
43	DGCN	AO	—	—	Gate-driver output for driving charge N-type MOSFET with 12 V clamped from DGCN to DSCN
44	GND	P	—	—	Accumulative cell voltage monitor ground terminal
45	DGN1	AO	—	—	Gate-driver output 1 for driving discharge N-type MOSFET. Recommended for applying on secondary loading path
46	C1	AI	—	—	Charge pump capacitor for DGCN. Connect an capacitor between C1 and C2
47	C2	AI	—	—	Charge pump capacitor for DGCN. Connect an capacitor between C1 and C2
48	DGN0	AO	—	—	Gate-driver output 0 for driving discharge N-type MOSFET. Recommended for applying on primary loading path
1	VIN	P	—	—	Regulator input supply voltage. Connect to the top VBATn
2	NC	—	—	—	No connected
3	VOUT	AO	—	—	VOUT is 8 to 1 analog multiplexer output. It is necessary to connect a 2.2 nF capacitor to GND
4	VREG	P	—	—	Regulator 5 V / 50 mA output. Connect a 4.7 μF capacitor typically
5	PB7	AI/O	5V	4/8/12/16 mA	PB7
6	PB8	AI/O	5V	4/8/12/16 mA	PB8
7	ADVREFP	P	—	—	Positive reference voltage for the ADC
8	VSSA	P	—	—	Ground reference for the ADC

Note: 1. I = input, O = output, A = Analog port, P = Power Supply, V_{DD} = V_{DD} Power, EP = Exposed Pad.

2. 5V = 5 V operation I/O type, PU = Pull-up.
3. These pins are located at the V_{DD} power domain.

Internal Connection Signal Lines

The MCU generated signals such as the SCTM0 channel output and SCTM1 channel output have been internally connected to the Accumulative Cell Voltage Monitor input for control purpose. Note that the PB2 ~ PB4 and PF0 ~ PF1 lines, which are internally connected to the accumulative cell voltage monitor SCL, DN1, DCN, DN0 and SDA inputs respectively. These output levels are used to control the operation of the Accumulative Cell Voltage Monitor. It is necessary to ensure that the PB2 ~ PB4 and PF0 ~ PF1 are selected as output types. The connections are listed in the following table and the related control registers should be configured correctly using application program.

Table 13. Internal Connection Signal Lines

MCU Signal Name	Accumulative Cell Voltage Monitor Signal Name	Description
PB4	DCN	Gate-driver DGCN control input(Note). The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function.
PB3/SCTM0_CH0 (SCTM0)	DN1	Gate-driver DGN1 control input(Note). If the SCTM0_CH0 output is used, the MCU AFIO setting should be AF4 to select the SCTM pin function.
PB2	SCL	Accumulative cell voltage monitor I^2C serial clock line. The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function.
PF1	SDA	Accumulative cell voltage monitor I^2C serial data line. The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function.
PF0/SCTM1_CH0 (SCTM1)	DN0	Gate-driver DGN0 control input(Note). If the SCTM1_CH0 output is used, the MCU AFIO setting should be AF4 to select the SCTM pin function.

Note: Internal pull down with 430 kΩ.

6 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 14. Absolute Maximum Ratings

Parameter	Value	Unit
V_{DD}	(Vss - 0.3) ~ (Vss + 5.5)	V
V_{DDIO}	(Vss - 0.3) ~ (Vss + 5.5)	V
Input Voltage	(Vss - 0.3) ~ (V_{DD} + 0.3)	V
T_A	-40 ~ 85	°C
T_{STG}	-60 ~ 150	°C
T_J	< 125	°C
P_D	< 500	mW
VIN, DSCN, HVWK, C2	-0.3 ~ 48	V
DGCN, C1	-0.3 ~ 60	V
DGN0, DGN1	-0.3 ~ 18	V
V_{REG}, V_{OUT}, V_{BAT1}	-0.3 ~ 5.5	V
$\Delta[V_{BATi} \sim V_{BAT(i-1)}]$, i = 8 ~ 2	-0.3 ~ 5.5	V
Electrostatic Discharge Voltage (Human Body Model)	-2000 ~ 2000	V

Recommended DC Operating Conditions

Table 15. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	2.5	5.0	5.5	V
$V_{ADVREFP}$	ADC Positive Reference Voltage	—	2.5	5.0	5.5	V

Note: The $V_{ADVREFP}$ power voltage needs below or equal to the V_{DD} power voltage.

Recommended Operating Range

Table 16. Recommended Operating Range

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Regulator Input Voltage	—	7.5	—	36	V
T_A	Operating Temperature Range	—	-40	—	85	°C

Note: Recommended Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specified performance limits

On-Chip LDO Voltage Regulator Characteristics

Table 17. LDO Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 2.5 V Regulator input @ I_{LDO} = 12 mA and voltage variant = ±5 %, After trimming	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.5 V Regulator input @ V_{LDO} = 1.5 V	—	12	15	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

Power Consumption

Table 18. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	f_{HCLK}	Conditions		Typ.	Max @ T_A		Unit
						25 °C	85 °C	
I_{DD}	Supply Current (Run Mode)	16 MHz	V_{DD} = 5 V HSI = 16 MHz	All peripherals enabled	3.35	3.60	—	mA
				All peripherals disabled	2.75	2.95	—	
		8 MHz	V_{DD} = 5 V HSI = 16 MHz	All peripherals enabled	1.88	2.02	—	
				All peripherals disabled	1.57	1.69	—	
		32 kHz	V_{DD} = 5 V LSI = 32 kHz LDO in LCM Mode	All peripherals enabled	26.39	32.72	—	μA
				All peripherals disabled	25.13	31.42	—	
	Supply Current (Sleep Mode)	16 MHz	V_{DD} = 5 V HSI = 16 MHz	All peripherals enabled	1.16	1.24	—	mA
				All peripherals disabled	0.44	0.48	—	
		8 MHz	V_{DD} = 5 V HSI = 16 MHz	All peripherals enabled	0.77	0.83	—	
				All peripherals disabled	0.41	0.45	—	
	Supply Current (Deep-Sleep-1 Mode)	—	V_{DD} = 5 V, HSI/HSE clock off, LDO in LCM Mode, LSE off, LSI on, RTC on		20.27	26.39	—	μA
	Supply Current (Deep-Sleep-2 Mode)	—	V_{DD} = 5 V, HSI/HSE clock off, LDO off, DMOS on, LSE off, LSI on, RTC on		3.45	5.14	—	μA

Note: 1. HSE means high speed external oscillator. HSI means 16 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means Real-Time clock.
4. Code = while (1) { 208 NOP } executed in Flash.

Reset and Supply Monitor Characteristics

Table 19. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	2.22	2.35	2.48	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})		2.12	2.2	2.33	V
$V_{PORHYST}$	POR Hysteresis	—	—	150	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 5.0 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO will be turned off.

Table 20. LVD / BOD Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	After factory-trimmed, V_{DD} falling edge		2.37	2.45	2.53	V
V_{LVD}	Voltage of Low Voltage Detection	V_{DD} falling edge	LVDS = 000	2.57	2.65	2.73	V
			LVDS = 001	2.77	2.85	2.93	V
			LVDS = 010	2.97	3.05	3.13	V
			LVDS = 011	3.17	3.25	3.33	V
			LVDS = 100	3.37	3.45	3.53	V
			LVDS = 101	4.15	4.25	4.35	V
			LVDS = 110	4.35	4.45	4.55	V
			LVDS = 111	4.55	4.65	4.75	V
$V_{LVDHTST}$	LVD Hysteresis	V_{DD} = 5.0 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 5.0 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 5.0 V	—	—	—	—	ms
I_{DDLVD}	Operation Current (2)	V_{DD} = 5.0 V	—	—	10	20	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Bandgap current is not included.
3. LVDS field is in the PWRCU LVDCSR register.

External Clock Characteristics

Table 21. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{HSE}	HSE Frequency	V_{DD} = 2.5 V ~ 5.0 V	4	—	16	MHz
C_L	Load Capacitance	V_{DD} = 5.0 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	12	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT pins	V_{DD} = 5.0 V	—	0.5	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 5.0 V, C_L = 12 pF @ 16 MHz, HSEDR = 0	—	—	110	Ω
		V_{DD} = 2.5 V, C_L = 12 pF @ 16 MHz, HSEDR = 1				
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 5.0 V, R_{ESR} = 100 Ω, C_L = 12 pF @ 8 MHz, HSEDR = 0	—	0.85	—	mA
		V_{DD} = 5.0 V, R_{ESR} = 25 Ω, C_L = 12 pF @ 16 MHz, HSEDR = 1	—	3.0	—	
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 5.0 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 5.0 V	—	—	4	ms

Table 22. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{CK_LSE}	LSE Frequency	V_{DD} = 2.5 V ~ 5.5 V	—	32.768	—	kHz
R_F	Internal feedback resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 5.0 V	30	—	TBD	kΩ
C_L	Recommended load capacitances	V_{DD} = 5.0 V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, $C_L \geq$ 7 pF, V_{DD} = 2.5 V ~ 5.5 V, T_A = -40 °C ~ 85 °C	—	3.3	6.3	μA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, C_L < 7 pF, V_{DD} = 2.5 V ~ 5.5 V, T_A = -40 °C ~ 85 °C	—	1.8	3.3	μA
	Power Down Current	—	—	—	0.01	μA
t_{SULSE}	LSE Oscillator Startup Time (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, V_{DD} = 2.5 V ~ 5.5 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace length as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent the crosstalk adverse effects.

Internal Clock Characteristics

Table 23. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{HSI}	HSI Frequency	V_{DD} = 5 V @ 25 °C	—	16	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 2.5 V ~ 5.5 V T_A = 25 °C	-1	—	1	%
		V_{DD} = 2.5 V ~ 5.5 V T_A = -25 °C ~ 85 °C	-2.5	—	2	%
		V_{DD} = 2.5 V ~ 5.5 V T_A = -40 °C ~ 85 °C	-4	—	3	%
Duty	Duty Cycle	f_{HSI} = 16 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{HSI} = 16 MHz @ V_{DD} = 2.5 V ~ 5.5 V	—	—	140	μA
	Power Down Current		—	—	0.01	μA
T_{SUHSI}	HSI Oscillator Startup Time	f_{HSI} = 16 MHz	—	—	20	μs

Table 24. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{LSI}	LSI Frequency	V_{DD} = 5.0 V, T_A = -40 °C ~ 85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	V_{DD} = 5.0 V, with factory-trimmed	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 5.0 V	—	0.5	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 5.0 V	—	—	100	μs

Memory Characteristics

Table 25. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program / Erase Cycles before Failure (Endurance)	T_A = -40 °C ~ 85 °C	20	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 85 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 85 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 85 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 85 °C	10	—	—	ms

I/O Port Characteristics

Table 26. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	5.0 V I/O	$V_I = V_{SS}$, On-chip pull-up resister disabled	—	—	3	μA
		Reset pin		—	—	3	μA
I_{IH}	High Level Input Current	5.0 V I/O	$V_I = V_{DD}$, On-chip pull-down resister disabled	—	—	3	μA
		Reset pin		—	—	3	μA
V_{IL}	Low Level Input Voltage	5.0 V I/O		-0.5	—	V_{DD} × 0.35	V
		Reset pin		-0.5	—	V_{DD} × 0.35	V
V_{IH}	High Level Input Voltage	5.0 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.5	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.5	V
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	5.0 V I/O		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	mV
I_{OL}	Low Level Output Current (GPIO Sink Current)	5.0 V I/O 4 mA drive, V_{OL} = 0.6 V		4	—	—	mA
		5.0 V I/O 8 mA drive, V_{OL} = 0.6 V		8	—	—	mA
		5.0 V I/O 12 mA drive, V_{OL} = 0.6 V		12	—	—	mA
		5.0 V I/O 16 mA drive, V_{OL} = 0.6 V		16	—	—	mA
I_{OH}	High Level Output Current (GPIO Source Current)	5.0 V I/O 4 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		—	4	—	mA
		5.0 V I/O 8 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		—	8	—	mA
		5.0 V I/O 12 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		—	12	—	mA
		5.0 V I/O 16 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		—	16	—	mA
V_{OL}	Low Level Output Voltage	5.0 V 4 mA drive I/O, I_{OL} = 4 mA		—	—	0.6	V
		5.0 V 8 mA drive I/O, I_{OL} = 8 mA		—	—	0.6	V
		5.0 V 12 mA drive I/O, I_{OL} = 12 mA		—	—	0.6	V
		5.0 V 16 mA drive I/O, I_{OL} = 16 mA		—	—	0.6	V
V_{OH}	High Level Output Voltage	5.0 V 4 mA drive I/O, I_{OH} = 4 mA		V_{DD} - 0.6	—	—	V
		5.0 V 8 mA drive I/O, I_{OH} = 8 mA		V_{DD} - 0.6	—	—	V
		5.0 V 12 mA drive I/O, I_{OH} = 12 mA		V_{DD} - 0.6	—	—	V
		5.0 V 16 mA drive I/O, I_{OH} = 16 mA		V_{DD} - 0.6	—	—	V
R_{PU}	Internal Pull-up Resistor	V_{DD} = 5.0 V		—	50	—	kΩ
R_{PD}	Internal Pull-down Resistor	V_{DD} = 5.0 V		—	50	—	kΩ

ADC Characteristics

Table 27. ADC Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.5	5.0	5.5	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Positive Reference Voltage	—	—	—	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 5.0 V, 500 ksps	—	1.4	1.5	mA
I_{ADC_DN}	Power Down Current Consumption	V_{DDA} = 5.0 V	—	—	0.1	μA
f_{ADC}	A/D Converter Clock Frequency	—	0.7	—	8	MHz
f_S	Sampling Rate	—	50	—	500	ksps
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	ADST [7:0] = 2	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	4	—	pF
t_{SU}	Startup Time	—	—	—	1	μs
N	Resolution	—	—	12	—	Bits
INL	Integral Non-linearity Error	f_S = 500 ksps, V_{DDA} = 5.0 V	—	±2	±5	LSB
DNL	Differential Non-linearity Error	f_S = 500 ksps, V_{DDA} = 5.0 V	—	±1	—	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

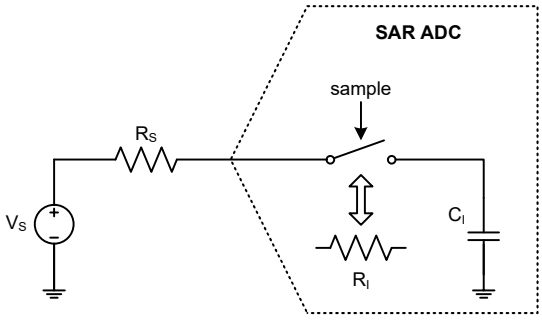


Figure 27. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF+}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

Internal Reference Voltage Characteristics

Table 28. Internal Reference Voltage Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—		2.8	—	5.5	V
V_{REF}	Internal Reference Voltage after Factory Trimming @ T_A = 25 °C	V_{DDA} ≥ 2.8 V	VREFSEL[1:0] = 00	2.44	2.50	2.56	V
		V_{DDA} ≥ 3.3 V	VREFSEL[1:0] = 01	2.92	3.00	3.08	
		V_{DDA} ≥ 4.3 V	VREFSEL[1:0] = 10	3.90	4.00	4.10	
		V_{DDA} ≥ 4.8 V	VREFSEL[1:0] = 11	4.39	4.50	4.61	
ACC_{VREF}	Reference Voltage Accuracy after Trimming	V_{DDA} = 2.8 V ~ 5.5 V, V_{REF} = 2.5 V, T_A = -40 °C ~ 85 °C		-2	—	+2	%
t_{STABLE}	Reference Voltage Stable Time	—		—	—	100	ms
t_{SREFV}	ADC Sampling Time when Reading Reference Voltage	—		10	—	—	μs
I_{DD}	Operating Current	—		—	50	70	μA
I_{DDPWD}	Power Down Current	—		—	—	0.01	μA

Note: 1. Data based on characterization results only, not tested in production.
2. The trimming bits of the internal reference voltage are 7-bit resolution.

SCTM Characteristics

Table 29. SCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for SCTM	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Signal Frequency on Channel	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	Bits

Accumulative Cell Voltage Monitor Electrical Characteristics

Table 30. Accumulative Cell Voltage Monitor Electrical Characteristics

V_{IN}=36V, C_{VREG}=4.7μF, C_{VOUT}=2.2nF, T_A=25°C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply and Input						
V_{IN}	Supply Voltage	—	7.5	—	36.0	V
$I_{IN(VM\_ACT)}$	Supply Current When Voltage Monitor is Activated	EN_S = 1	6	11	16	μA
$I_{IN(STB)}$	Supply Current – Standby	B2 = B1 = B0 = EN_S = 0, V_{DN0} = V_{DN1} = V_{DCN} = 0 V	—	3.5	6.0	μA
$I_{IN(STB\_DSG)}$	VIN Supply Current When DGN0 is Activated	B2 = B1 = B0 = EN_S = 0, V_{DN0} = 5 V, V_{DN1} = V_{DCN} = 0 V	—	35	42	μA
I_{SLP}	Standby Current in SLEEP Mode	V_{SLP} = 5 V, V_{HVWK} = 0 V	—	0.1	0.2	μA
Voltage Regulator						
V_{REG}	Regulator Output Voltage	I_{LOAD} = 10 mA	4.95	5.00	5.05	V
I_{REG}	Regulator Maximum Output Current	V_{IN} = 7.5 V, T_A = -40 °C ~ 85 °C	50	—	—	mA
ΔV_{REG}	Load Regulation	I_{LOAD} = 0 mA ~ 50 mA	—	30	80	mV
$\Delta V_{REG}/(V_{REG}\times\Delta V_{IN})$	Line Regulation	V_{IN} = 7.5 V ~ 36 V, I_{LOAD} = 10 mA	—	0.02	—	%/V
$\Delta V_{REG}/(V_{REG}\times\Delta T_A)$	Temperature Coefficient	I_{LOAD} = 1 mA, T_A = -40 °C ~ 85 °C	—	±100	—	ppm /°C
R_{DIS}	VREG Discharge Resistance	SLP = 1, V_{REG} = 1 V, I_{REG1} denotes VREG input current at V_{REG} = 1 V, R_{DIS} = V_{REG}/I_{REG1}	—	85	—	Ω
Charge Balancer						
R_{CB}	Charge Balance Resistance	V_{Bi} = 4.5 V (i = 1 ~ 8), VBATn series resistors = 0 Ω	55	85	115	Ω
		V_{Bi} = 2.5 V (i = 1 ~ 8), VBATn series resistors = 0 Ω	80	120	160	Ω
High Voltage Wake-Up						
V_{WKTH}	HVWK Trigger Threshold Voltage	—	4.5	5.5	6.5	V
t_{WKDB1}	HVWK Trigger Debounce Time	—	1	—	—	ms
I_{WK}	HVWK Input Current	V_{HVWK} = 36 V	—	50	—	μA
Accumulative Cell Voltage Monitor						
V_{Bi}	Cell Voltage	i = 1 ~ 8	2.5	—	4.5	V
$V_{B(MIN)}$	Input Voltage between VBATi and VBAT(i-1) for Charge Balance and Voltage Monitor	—	1.5	—	—	V
$I_{Bi(PWR)}$	Cell Input Leakage Current When V_{IN} is Powered	V_{BATi} = 5 V × i, EN_S = 0, V_{IN} = V_{BAT8}, i = 1 ~ 8	-0.1	—	0.1	μA
$I_{Bi(ACT)}$	Cell Input Current When Voltage Monitoring	V_{Bi} = 4.5 V, EN_S = 1, V_{IN} = 36 V, i = 1 ~ 8	19	24	35	μA
R	Divided Resistance	—	140	200	260	kΩ

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$Ratio8_{(NORM)}$	VBAT8 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT8} = 20 V ~ 36 V, B2 ~ B0 = 0b111	0.995	1	1.005	V/V
		V_{BAT8} = 20 V ~ 36 V, B2 ~ B0 = 0b111, T_A = -40 °C ~ 85 °C	0.99	1	1.01	V/V
$Ratio7_{(NORM)}$	VBAT7 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT7} = 17.5 V ~ 31.5 V, B2 ~ B0 = 0b110	0.995	1	1.005	V/V
		V_{BAT7} = 17.5 V ~ 31.5 V, B2 ~ B0 = 0b110, T_A = -40 °C ~ 85 °C	0.99	1	1.01	V/V
$Ratio6_{(NORM)}$	VBAT6 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT6} = 15 V ~ 27 V, B2 ~ B0 = 0b101	0.995	1	1.005	V/V
		V_{BAT6} = 15 V ~ 27 V, B2 ~ B0 = 0b101, T_A = -40 °C ~ 85 °C	0.99	1	1.01	V/V
$Ratio5_{(NORM)}$	VBAT5 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT5} = 12.5 V ~ 22.5 V, B2 ~ B0 = 0b100	0.995	1	1.005	V/V
		V_{BAT5} = 12.5 V ~ 22.5 V, B2 ~ B0 = 0b100, T_A = -40 °C ~ 85 °C	0.99	1	1.01	V/V
$Ratio4_{(NORM)}$	VBAT4 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT4} = 10 V ~ 18 V, B2 ~ B0 = 0b011	0.995	1	1.005	V/V
		V_{BAT4} = 10 V ~ 18 V, B2 ~ B0 = 0b011, T_A = -40 °C ~ 85 °C	0.99	1	1.01	V/V
$Ratio3_{(NORM)}$	VBAT3 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT3} = 7.5 V ~ 13.5 V, B2 ~ B0 = 0b010	0.995	1	1.005	V/V
		V_{BAT3} = 7.5 V ~ 13.5 V, B2 ~ B0 = 0b010, T_A = -40 °C ~ 85 °C	0.99	1	1.01	V/V
$Ratio2_{(NORM)}$	VBAT2 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT2} = 5 V ~ 9 V, B2 ~ B0 = 0b001	0.995	1	1.005	V/V
		V_{BAT2} = 5 V ~ 9 V, B2 ~ B0 = 0b001, T_A = -40 °C ~ 85 °C	0.99	1	1.01	V/V
$Ratio1_{(NORM)}$	VBAT1 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT1} = 2.5 V ~ 4.5 V, B2 ~ B0 = 0b000	0.995	1	1.005	V/V
		V_{BAT1} = 2.5 V ~ 4.5 V, B2 ~ B0 = 0b000, T_A = -40 °C ~ 85 °C	0.99	1	1.01	V/V
f_{MAX}	Voltage Monitor Channel to Channel Scan Frequency	C_{VOUT} = 2.2 nF	—	—	100	Hz
Gate-drivers						
V_Z	DGNx Clamp Voltage	V_{DN0} = V_{DN1} = 5 V, V_{IN} > 13 V	10	12	16	V
		V_{DN0} = V_{DN1} = 5 V, V_{IN} ≤ 13 V	—	V_{IN}-0.7	—	V
	V(DGCN,DSCN) Clamp Voltage	V_{DCN} = 5 V, V_{IN} > 15 V	10	12	16	V
		V_{DCN} = 5 V, V_{IN} ≤ 15 V	—	V_{IN}-3.2	—	V
t_{r0}	DGN0 Rising Time	C_{DGN0} = 15 nF	—	0.5	1.0	µs
t_{f0}	DGN0 Falling Time	C_{DGN0} = 15 nF	—	0.5	1.0	µs
t_{PD_HL0}	DGN0 Falling Propagation Delay Time	C_{DGN0} = 15 nF	—	0.5	1.0	µs
t_{MM0}	DGN0 Delay Time Mismatch	C_{DGN0} = 15 nF, t_{MM0} = $\lvert t_{PD\_LH0}-t_{PD\_HL0}\rvert$	—	0.5	1.0	µs
$I_{SOURCE0}$	DGN0 Source Current	C_{DGN0} = 1 µF, peak current at DN0 rising edge (0 → 1)	—	850	—	mA
I_{SINK0}	DGN0 Sink Current	C_{DGN0} = 1 µF, peak current at DN0 falling edge (1 → 0)	—	400	—	mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PWM0}	DGN0 PWM Frequency	C_{DGN0} = 15 nF	—	—	10	kHz
t_{r1}	DGN1 Rising Time	C_{DGN1} = 15 nF	—	1.2	2.5	μs
t_{f1}	DGN1 Falling Time	C_{DGN1} = 15 nF	—	1.2	2.5	μs
t_{PD_HL1}	DGN1 Falling Propagation Delay Time	C_{DGN1} =15 nF	—	1.2	2.5	μs
t_{MM1}	DGN1 Delay Time Mismatch	C_{DGN1} = 15 nF, $t_{MM1} = \lvert t_{PD\_LH1} - t_{PD\_HL1} \rvert$	—	1.2	2.5	μs
$I_{SOURCE1}$	DGN1 Source Current	C_{DGN1} = 1 μF, peak current at DN1 rising edge (0 → 1)	—	350	—	mA
I_{SINK1}	DGN1 Sink Current	C_{DGN1} = 1 μF, peak current at DN1 falling edge (1 → 0)	—	180	—	mA
f_{PWM1}	DGN1 PWM Frequency	C_{DGN1} = 15 nF	—	—	2	kHz
f_{CP}	Charge Pump Switching Frequency	External capacitor is 22 nF between C1 and C2	—	150	—	kHz
t_{rC}	Rising Time of The Voltage Difference between DGCN and DSCN	$C_{DGCN-DSCN}$ = 15 nF, V_{IN} = 36 V	—	500	—	μs
t_{fC}	Falling Time of The Voltage Difference between DGCN and DSCN	$C_{DGCN-DSCN}$ = 15 nF, V_{IN} = 36 V	—	5	10	μs
R_{PD}	DN0, DN1, DCN Pull-Down Resistance	—	—	430	—	kΩ
$R_{PL\_SLP\_G}$	DGCN Pull-Low Resistance in Sleep Mode	SLP = 1, resistance between DGCN and GND	—	830	—	Ω
$R_{PL\_SLP\_S}$	DSCN Pull-Low Resistance in Sleep Mode	SLP = 1, resistance between DSCN and GND	—	830	—	Ω
$R_{PL\_SLP\_GS}$	DGCN to DSCN Pull-Low Resistance in Sleep Mode	SLP = 1, resistance between DGCN and DSCN	—	1.65	—	kΩ
$R_{PL\_STB\_G}$	DGCN Pull-Low Resistance in Standby Mode	SLP = 0, V_{DCN} = 0 V, resistance between DGCN and GND	—	50	—	Ω
$R_{PL\_STB\_S}$	DSCN Pull-Low Resistance in Standby Mode	SLP = 0, V_{DCN} = 0 V, resistance between DSCN and GND	—	50	—	Ω
$R_{PL\_STB\_GS}$	DGCN to DSCN Pull-Low Resistance in Standby Mode	SLP = 0, V_{DCN} = 0 V, resistance between DGCN and DSCN	—	90	—	Ω
$R_{PL\_S\_0}$	DGN0 Pull-Low Resistance in Sleep and Standby Mode	V_{DN0} = 0 V, SLP = 0 or 1, resistance between DGN0 and GND	—	5	—	Ω
$R_{PL\_S\_1}$	DGN1 Pull-Low Resistance in Sleep and Standby Mode	V_{DN1} = 0 V, SLP = 0 or 1, resistance between DGN1 and GND	—	8.5	—	Ω

Accumulative Cell Voltage Monitor I²C Interface Electrical Characteristics

Table 31. Accumulative Cell Voltage Monitor I²C Interface Electrical Characteristics

V_{IN} = 36 V, T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	Clock Frequency	—	—	—	400	kHz
t_{BMF}	Bus Free Time	Bus free time between STOP and START	1.3	—	—	μs
$t_{HD:STA}$	START Hold Time	After this period, the first clock pulse is generated	0.6	—	—	μs
t_{LOW}	SCL Low Time	—	1.3	—	—	μs
t_{HIGH}	SCL High Time	—	0.6	—	—	μs
$t_{SU:STA}$	START Setup Time	Only relevant for Repeated START	0.6	—	—	μs
$t_{HD:DAT}$	Data Hold Time	—	0	—	—	ns
$t_{SU:DAT}$	Data Setup Time	—	100	—	—	ns
t_{R_I2C}	Rising Time	SDA and SCL (Note)	—	—	0.3	μs
t_{F_I2C}	Falling Time	SDA and SCL (Note)	—	—	0.3	μs
$t_{SU:STO}$	STOP Setup Time	—	0.6	—	—	μs
t_{AA}	Output Valid from Clock	—	—	—	0.9	μs
t_{SP}	Input Filter Time Constant	SDA and SCL noise suppression time	—	—	20	ns
t_{OUT}	I²C Time Out	Trimming selection 1 (default setting)	—	32	—	ms
		Trimming selection 2	—	64	—	ms

Note: These parameters are periodically sampled but not 100% tested.

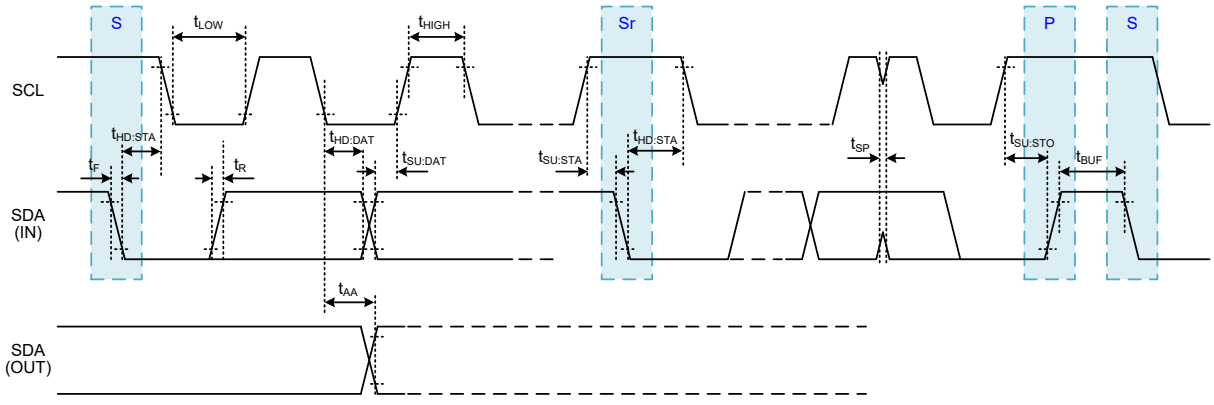


Figure 28. Accumulative Cell Voltage Monitor I²C Interface Timing Diagrams

I²C Characteristics

Table 32. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time (5)	0	—	0	—	0	—	ns
	SDA Data Hold Time (6)	—	1.6	—	0.475	—	0.25	μs
$t_{VD(SDA)}$	SDA Data Valid Time	—	1.6	—	0.475	—	0.25	μs
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast plus mode, the peripheral clock frequency must be higher than 16 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 0 and SEQFILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 1 and SEQFILTER = 00.

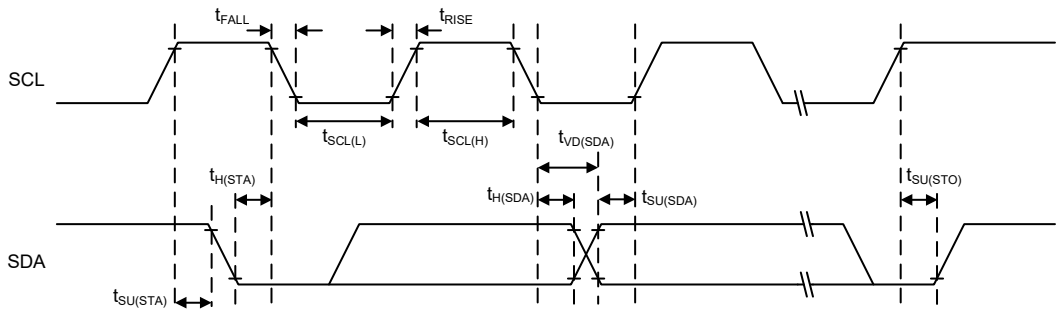


Figure 29. I²C Timing Diagram

SPI Characteristics

Table 33. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	Master mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2$ - 2	—	$t_{SCK}/2$ + 1	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	Slave mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	3 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

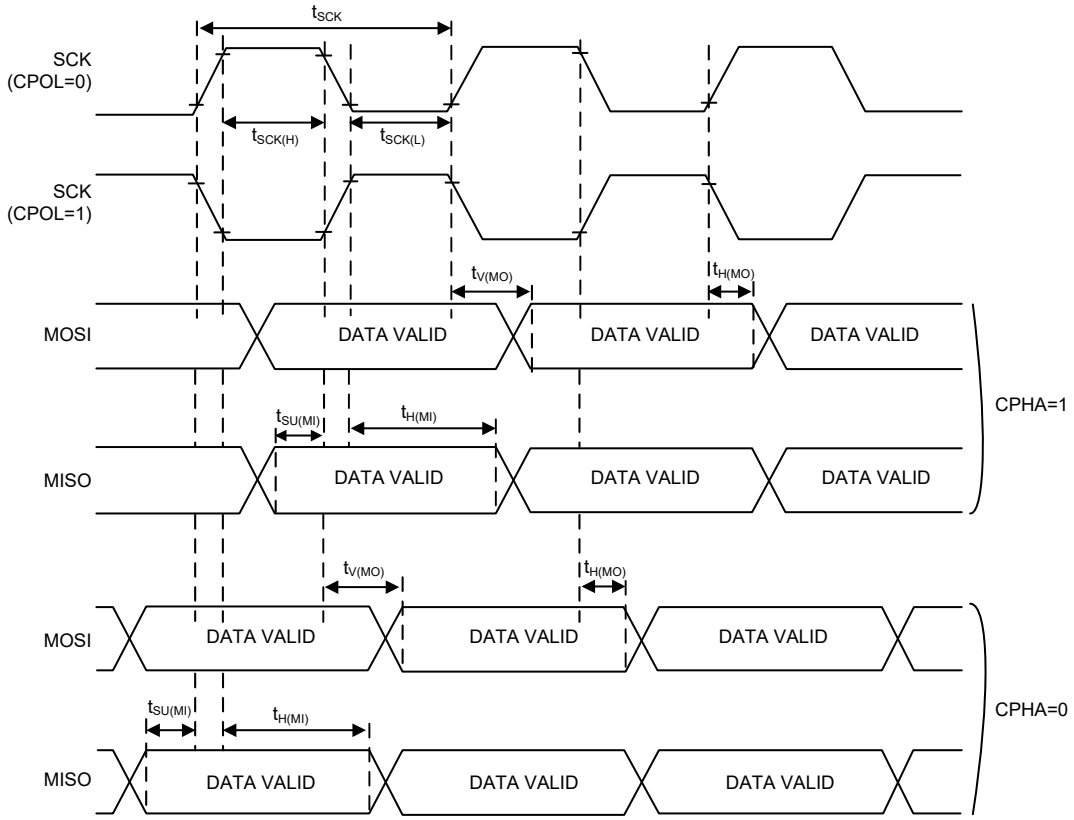


Figure 30. SPI Timing Diagram – SPI Master Mode

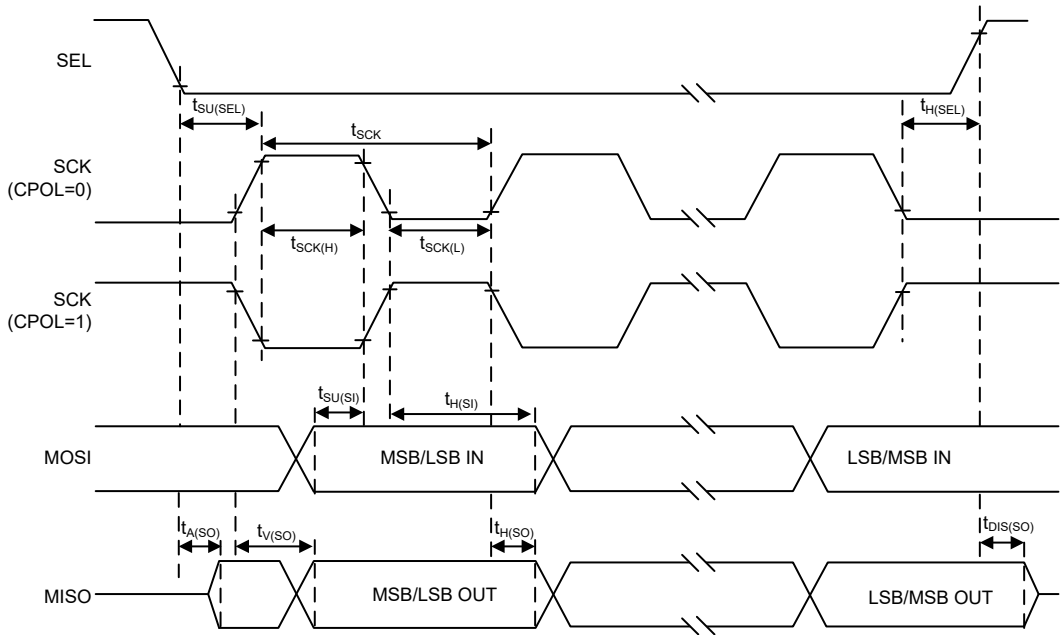


Figure 31. SPI Timing Diagram – SPI Slave Mode with CPHA = 1

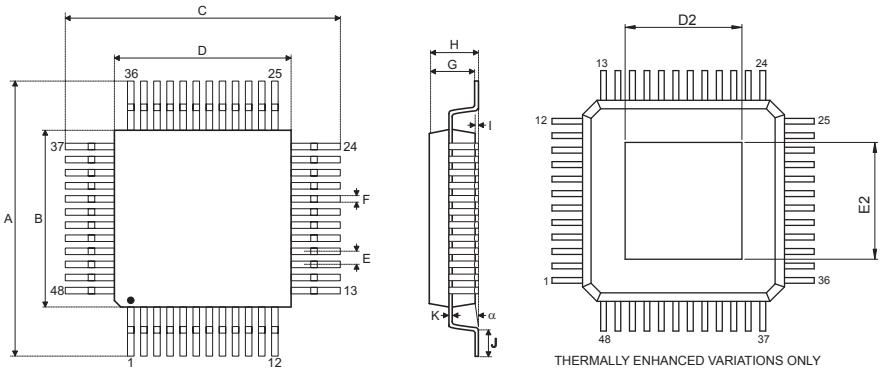
7 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

48-pin LQFP-EP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
D2	0.170	—	0.211
E2	0.170	—	0.211
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.50 BSC	—
D2	4.31	—	5.36
E2	4.31	—	5.36
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°