

Dual Channel Digital Audio System with EQ and Frequency DRC Control

General Description

The RT9114C is a high efficiency, I²S-input, stereo channel audio power amplifier delivering 2x20W into 8Ω BTL speaker loads. It can deliver over 90% power efficiency and eliminate the need for heat-sink.

The built-in anti-pop functions can reduce the speaker's pop noise under all kind of scenarios. Built-in protection circuits can provide over-temperature, over-current, over-voltage, and under-voltage protections and report error status.

The RT9114C is an I²S device receiving all clocks from external sources with wide input sampling rate from 8kHz to 96kHz. A fully programmable data path routes these channels to the internal speaker drivers. Besides, the RT9114C also supports the master mode if an external MCLK is ready.

The RT9114C features three band DRC and flexible multi-band biquads for anti-clipping, power limiting, and speaker equalization.

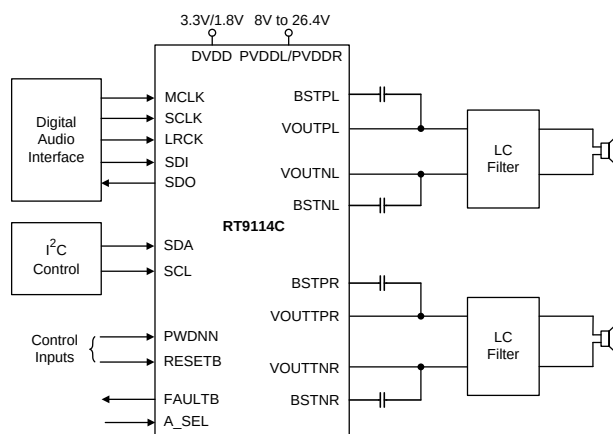
Features

- **Wide Input Supply Range** : 8V to 26.4V
- **2x20W** at into 8Ω BTL at 20V
- **2x9W** at into 8Ω BTL at 12V
- **Support Stereo/PBTL/Mono Output**
- **Sampling Frequency** from 8kHz to 96kHz with **Auto Detection**
- **Support Master and Slave I²S Interface**
- **MCLK-Less** with **Clock Auto Detection**
- **Built-In Anti-Pop Function**
- **Support SDO** for **Acoustic Echo Cancellation**
- **> 24 Programmable Biquads**
- **Programmable Coefficients** for **DRC Filters** and **Supporting Multi-Compression Ratios** with **post DRC**
- **Built-In DC Blocking Filters**
- **Protection Features** : **UVLO, OVP, OCP, OTP** and **DCP**
- **Filter-Less Application**
- **VQFN-28L Thermally-Enhanced Package**
- **RoHS Compliant** and **Halogen Free**

Applications

- LCD-TV
- Monitors
- Home Audio
- Amusement Equipment

Simplified Application Circuit



Ordering Information

RT9114C□□

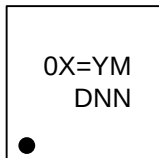
- Package Type
QV : VQFN-28L 4x5 (V-Type)
- Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

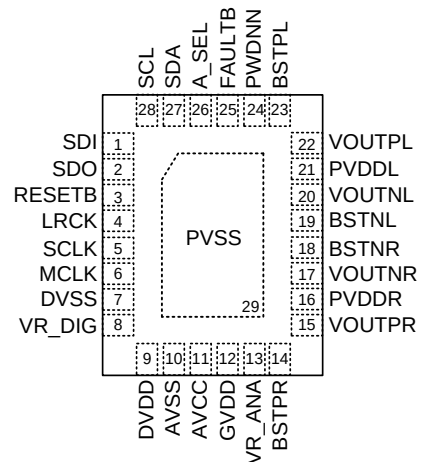
Marking Information



0X= : Product Code
YMDNN : Date Code

Pin Configuration

(TOP VIEW)



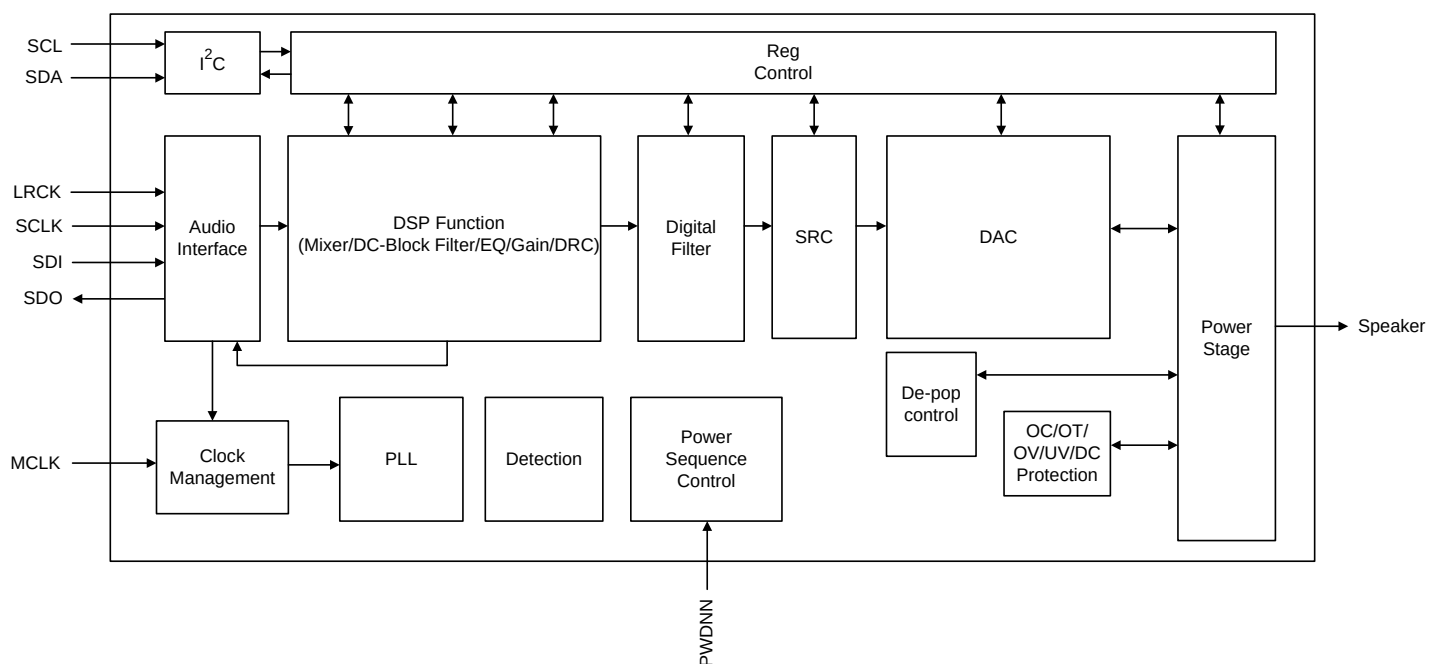
VQFN-28L 4x5

Functional Pin Description

Pin No.	Pin Name	IO	Pin Function
1	SDI	DI	I ² S data input.
2	SDO	DO	I ² S data output.
3	RESETB	DI	Reset, low active.
4	LRCK	DI/O	I ² S L/R clock input.
5	SCLK	DI/O	I ² S bit clock input.
6	MCLK	DI	Master clock input.
7	DVSS	P	Ground for digital circuits.
8	VR_DIG	P	1.8V digital supply voltage generated by internal LDO.
9	DVDD	P	3.3V/1.8V power supply for I/O and.
10	AVSS	P	Ground for analog circuits.
11	AVCC	P	26.4V power supply for analog circuits.
12	GVDD	P	Internal power supply generated by LDO.
13	VR_ANA	P	Analog reference voltage.
14	BSTPR	P	Bootstrap supply for VOUTPR.
15	VOUTPR	AO	Positive output of RCH.
16	PVDDR	P	26.4V power supply for RCH.
17	VOUTNR	AO	Negative output of RCH.
18	BSTNR	P	Bootstrap supply of VOUTNR.
19	BSTNL	P	Bootstrap supply of VOUTNL.

Pin No.	Pin Name	IO	Pin Function
20	VOUTNL	AO	Negative output of LCH.
21	PVDDL	P	26.4V power supply for LCH.
22	VOUTPL	AO	Positive output of LCH.
23	BSTPL	P	Bootstrap supply for VOUTPL.
24	PWDNN	DI	Power down pin, low active.
25	FAULTB	DO	Fault indicator (low active).
26	A_SEL	DI	Slave address selection
27	SDA	DIO	I ² C data input/output.
28	SCL	DI	I ² C clock input.
29 (Exposed Pad)	PVSS	P	Ground. The exposed pad must be connected to GND and well soldered to a large PCB copper area for maximum power dissipation.

Functional Block Diagram



Operation

Error Reporting

The FAULTB pin is error report output pin. Any fault will pull FAULTB to low. This pin is open-drain configuration, need pull-up resistor.

Clock Detection

The RT9114C can accept SCLK to be as 32fs, 48fs and 64fs and support only a 1xfS LRCK. The internal oscillator will check MCLK or SCLK input constantly. If clock is lost, the RT9114C will mute and shutdown the power stage automatically.

Volume Control

The RT9114C have master volume MS_VOL and each channel volume CH1_VOL, CH2_VOL control. The step of each volume is 0.0625dB per step, from 24dB to mute. CH1 and CH2 also have each mute control, CH1_MUTE and CH2_MUTE.

Built-In Anti-POP Function

An internal soft-start function controls the Duty ramp-up rate of the output PWM voltage to minimize the POP noise during start-up. Similarly, when power shut-down, the duty also ramp-down to eliminate the POP noise. This function also acts when the PWDNN pin turns-ON/OFF.

Over-Current Protection

The RT9114C provides OCP function to prevent the device from damages during overload or short-circuit conditions. The current are detected by an internal sensing circuit. Once overload happens, the OCP function is designed to operate the latch mode.

Under-Voltage Protection

The RT9114C monitors the voltage on PVDD voltage threshold. When the voltage on PVDDL/R pin falls below the under-voltage threshold, 6.5V (typ.), the UVP circuit turns off the output immediately. Or the latch mode can be configured to use.

Over-Voltage Protection

The RT9114C monitors the voltage on PVDD voltage threshold. When the voltage on PVDDL/R pin rise behind the over-voltage threshold, 30V, the OVP circuit turns off the output immediately and operates in cycle by cycle auto-recovery mode. Or the latch mode can be configured to use.

Over-Temperature Protection

The over-temperature protection function will turn off the power MOSFET when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 30°C, the regulator will automatically resume operation. Or the latch mode can be configured to use.

Absolute Maximum Ratings (Note 1)

Supply Voltage, AVCC, PVDDL, PVDDR	-----	-0.3V to 32V
Supply Voltage, DVDD	-----	-0.3V to 3.6V
Speaker Amplifier Output Voltage, VOUTXX	-----	-0.3V to 32V
BSTXX to PVSS DC	-----	-0.3V to 37V
SCL, SDA	-----	-0.3V to 6V
LRCK, SCLK, SDI, MCLK, PWDNN, A_SEL, RESETB	-----	-0.3V to DVDD + 0.3V
GND to PVSS	-----	-0.3V to 0.3V
VOUTPR, VOUTNR, VOUTPL, VOUTNL	-----	-10V to 37V (Note 5)
Power Dissipation, P _D @ T _A = 25°C		
VQFN-28L 4x5	-----	4.56W
Package Thermal Resistance (Note 2)		
VQFN-28L 4x5, θ_{JA}	-----	27.4°C/W
VQFN-28L 4x5, θ_{JC}	-----	1.7°C/W
Lead Temperature (Soldering, 10sec.)	-----	260°C
Junction Temperature	-----	150°C
Storage Temperature Range	-----	-65°C to 150°C
ESD Susceptibility (Note 3)		
HBM (Human Body Model)	-----	2kV

Recommended Operating Conditions (Note 4)

Supply Input Voltage, DVDD	-----	3.0V to 3.6V
Supply Input Voltage (For 1.8V I/O), DVDD, VR_DIG	-----	1.62V to 1.98V
Supply Input Voltage, PVDDL, PVDDR, AVCC	-----	8V to 26.4V
Supply Input Voltage, PVDDL, PVDDR	-----	8V to 26.4V
Ambient Temperature Range	-----	-40°C to 85°C
Junction Temperature Range	-----	-40°C to 150°C

Electrical Characteristics

(PVDD = 12V, DVDD = 3.3V, R_L = 8Ω, BTLx2, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
PWDNN, A_SEL, RESETB	V _{IH} : High-Level-Input Voltage	V _{IH}		DVDD x0.7	--	--	V
	V _{IL} : Low-Level-Input Voltage	V _{IL}		--	--	DVDD x0.3	
FAULTB	V _{OL} : Low-Level-Output Voltage	V _{OL}	I _{PULLUP} = 3mA	--	--	0.4	V
DVDD Quiescent Current (Normal Mode)		I _{Q_D}	PWDNN = 3.3V, 0dBFS input, for DVDD, no load, no LC filter	--	10	15	mA
			PWDNN = 3.3V, switch 50% duty for DVDD, no load, no LC filter	--	8	12	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
DVDD Shutdown Current	I _{SD_D}	PVDNN = 0.8V, for DVDD, no load, no LC filter		--	--	1	mA
PVDD Quiescent Current (Normal Mode)	I _{Q_P}	PVDNN = 3.3V, switch 50% duty for PVDD, no load, no LC filter		--	25	40	mA
PVDD Shutdown Current	I _{SD_P}	PVDNN = 0.8V, no load for PVDD, no load, no LC filter		--	--	2	mA
Drain-Source On-State Resistance	R _{DS(ON)}	PVDD = 12V, I _O = 500mA, T _J = 25°C	High-side	--	150	--	mΩ
			Low-side	--	130	--	
GVDD		1mA		--	5	--	V
VR_ANA				--	5	--	V
Speaker Gain variation	ΔA _V (SPK_AMP)			-0.5	--	0.5	dB
Startup Time from S/W Shutdown	t _{ON}			--	75	--	ms
Shut Down Time from Enable	t _{OFF}			--	60	--	ms
PWM Switching Frequency				300	--	500	kHz
RMS Output Power BD Modulation	P _O	THD + N = 10%, 8Ω	PVDD = 21V	--	30.3	--	W
			PVDD = 18V	--	22.8	--	
			PVDD = 12V	--	10.2	--	
		THD + N = 1%, 8Ω	PVDD = 21V	--	25.4	--	
			PVDD = 18V	--	19	--	
			PVDD = 12V	--	8.5	--	
		THD + N = 10%, 6Ω	PVDD = 18V	--	28	--	
			PVDD = 12V	--	13.1	--	
		THD + N = 1%, 6Ω	PVDD = 18V	--	23.4	--	
			PVDD = 12V	--	10.9	--	
Total Harmonic Distortion + Noise	THD+N	P _O = 1W (BTL)		--	0.03	0.1	%
Output Integrated Noise	V _n	20Hz to 20kHz, A-weighted		--	100	200	μV
Output Offset Voltage	V _{OS}			--	--	20	mV
Cross-Talk (Non Shielding Choke)	X _{TALK}	Output power = 1W		--	-75	--	dB
Cross-Talk (With full Shielding Choke)	X _{TALK}	Output power = 1W, 1KHz		--	-100	--	dB
Signal-to-Noise Ratio	SNR	THD + N ≤ 1%		--	100	--	dB
Power Supply Rejection Ratio	PSRR	1kHz, 200mV		--	-70	--	dB
Dynamic Range	DR	Input level = -60dBFS		--	100	--	dB
Efficiency	η	Output Power = 10W+10W		--	90	--	%
Over-Temperature Protection	OTP	Guaranteed by design		150	160	175	°C
Thermal Hysteresis				--	30	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Over-Current Protection	OCP		5	6.3	7.5	A
PVDDL/PVDDR Over-Voltage	OVP		29.5	30	30.9	V
PVDDL/PVDDR Under-Voltage	UVP		6	6.5	7	V
Minimum Load Impedance		Inductor = 22 μ H, PVDD < 16V	3.6	--	--	Ω
		Inductor = 22 μ H, PVDD = 24V	5.4	--	--	
		Inductor = 10 μ H, PVDD < 16V	3.6	--	--	
		Inductor = 10 μ H, PVDD = 20V	5.3	--	--	
		Inductor = 10 μ H, PVDD = 24V	7	--	--	

I²C Interface Electrical Characteristics

Pull-Down Current	I _{FO2}	(Note 6)	--	2	--	μ A
Digital Output Low (SDA)	V _{OL}	I _{PULLUP} = 3mA	--	--	0.4	V
Clock Operating Frequency	f _{SCL}		--	--	400	kHz
Bus Free Time Between Stop and Start Condition	t _{BUF}		1.3	--	--	μ s
Hold Time After (Repeated) Start Condition	t _{HD,STA}		0.6	--	--	μ s
Repeated Start Condition Setup Time	t _{SU,STA}		0.6	--	--	μ s
Stop Condition Time	t _{SU,STD}		0.6	--	--	μ s
Data Hold Time	t _{HD,DAT (OUT)}		225	--	--	ns
Input Data Hold Time	t _{HD,DAT (IN)}		0	--	900	ns
Data Setup Time	t _{SU,DAT}		100	--	--	ns
Clock Low Period	t _{LOW}		1.3	--	--	μ s
Clock High Period	t _{HIGH}		0.6	--	--	μ s
Clock Data Fall Time	t _F		20	--	300	ns
Clock Data Rise Time	t _R		20	--	300	ns
Spike Suppression Time	t _{SP}		--	--	20	ns

Slave Mode I²S Interface Electrical Characteristics (3.3V I/O)

High-Level Input Voltage		V _{IH}		2	--	--	V
Low- Level Input Voltage		V _{IL}		--	--	0.8	V
SDOUT	VOH : High-Level Output Voltage	V _{OH}		--	3.3	--	V
	VOL : Low-Level Output Voltage	V _{OL}		--	--	0.4	

Slave Mode I²S Interface Electrical Characteristics (1.8V I/O)

High-Level Input Voltage		V _{IH}		1.3	--	--	V
Low- Level Input Voltage		V _{IL}		--	--	0.5	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
SDOUT	VOH : High-Level Output Voltage	V _{OH}		--	1.8	--	V
	VOL : Low-Level Output Voltage	V _{OL}		--	--	0.2	
Frequency		f _{SCLKIN}		1.024	--	12.288	MHz
Setup Time, LRCK to SCLK Rising Edge		t _{su1}		10	--	--	ns
Hold Time, LRCK from SCLK Rising Edge		t _{h1}		10	--	--	ns
Setup Time, SDIN to SCLK Rising Edge		t _{su2}		10	--	--	ns
Hold Time, SDIN from SCLK Rising Edge		t _{h2}		10	--	--	ns
Rise/Fall Time for SCLK/LRCK		t _r /t _f		--	--	8	ns
I ² S Duty Cycle for Rising		%		40	--	60	%

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is measured at the top of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

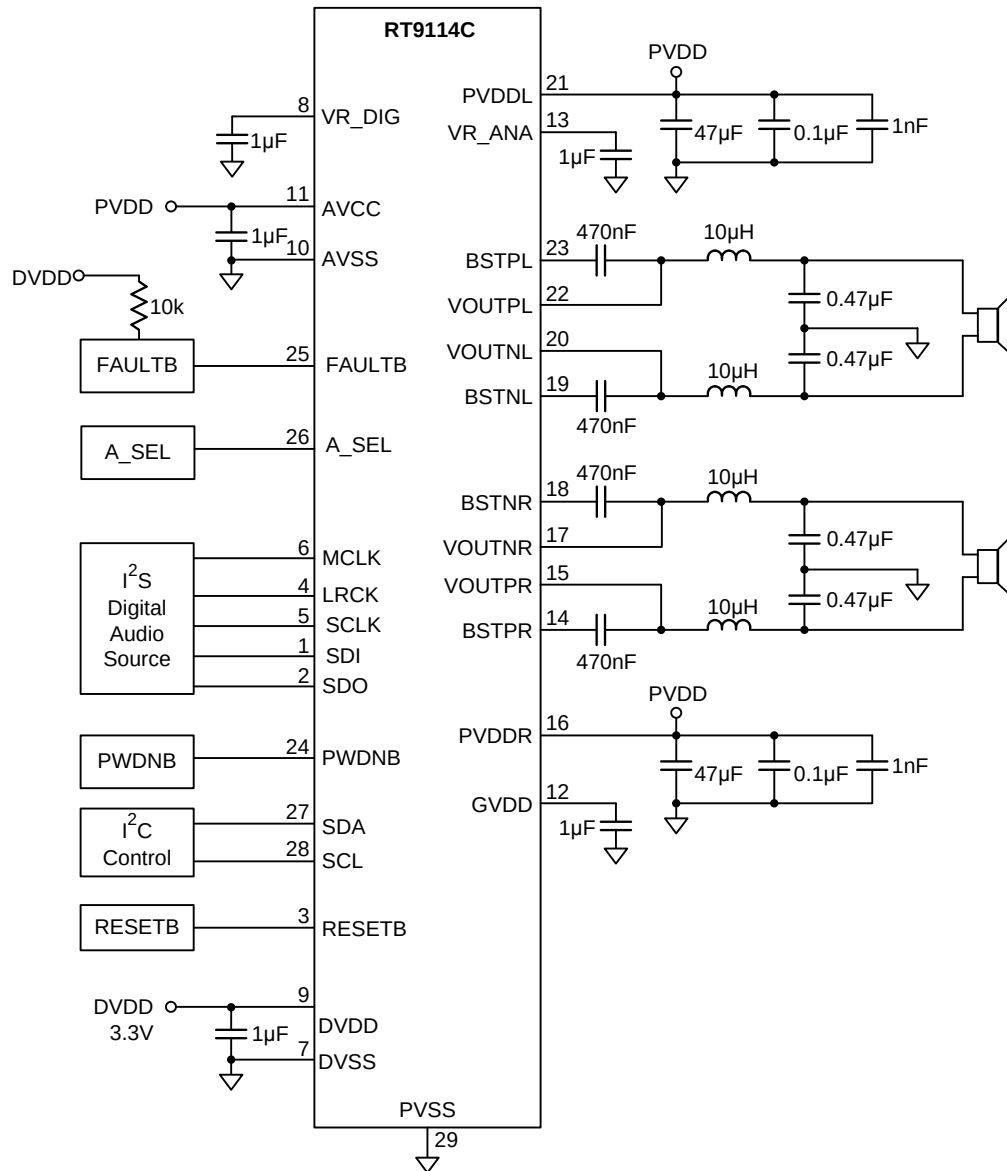
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. The switching terminal should be used within AC peak limits. Overshoot and undershoot must be less than 100ns.

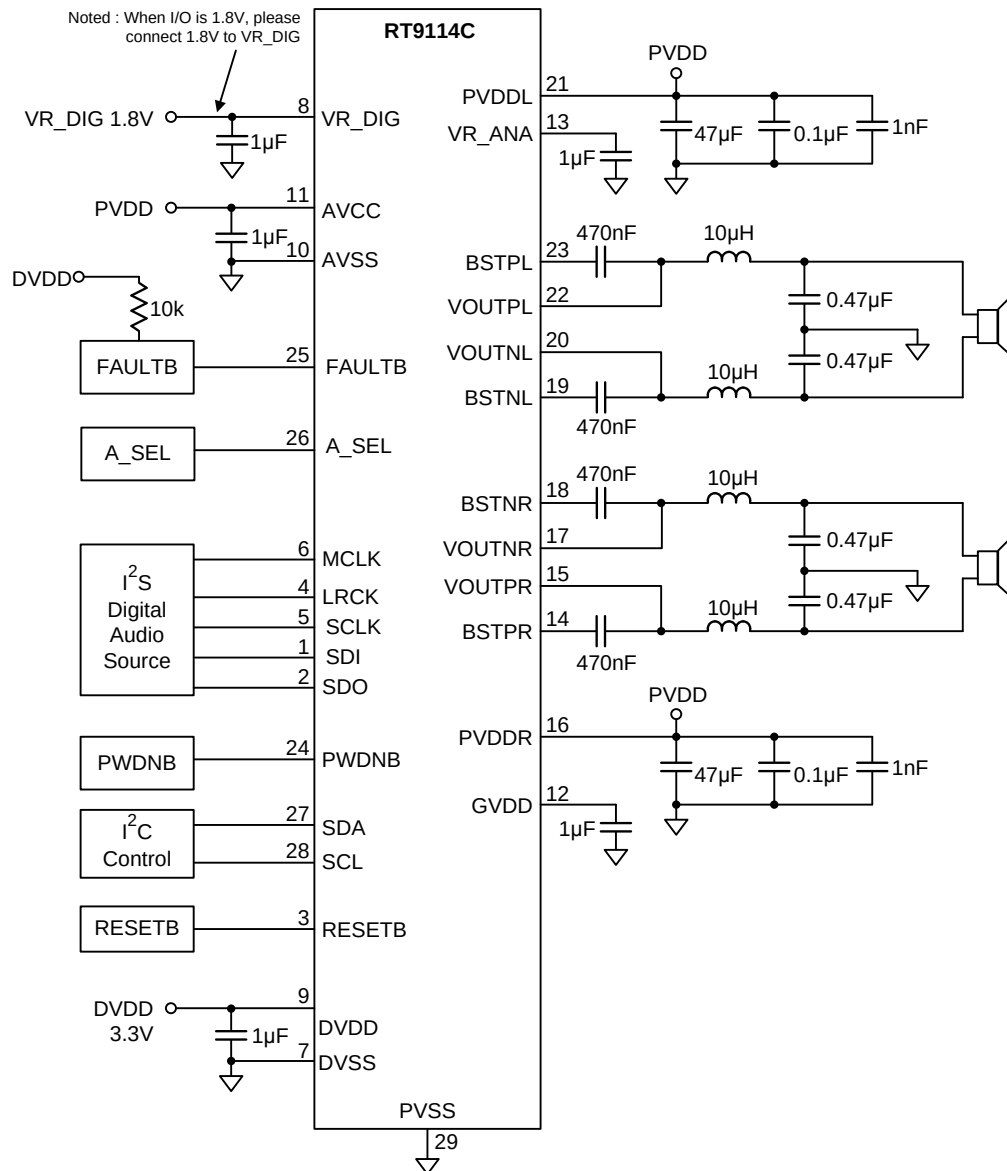
Note 6. The capability of the receiver to pull down the SDA line when during the acknowledge clock pulse.

Typical Application Circuit

3.3V I/O Application



1.8V I/O Application



Timing Diagram

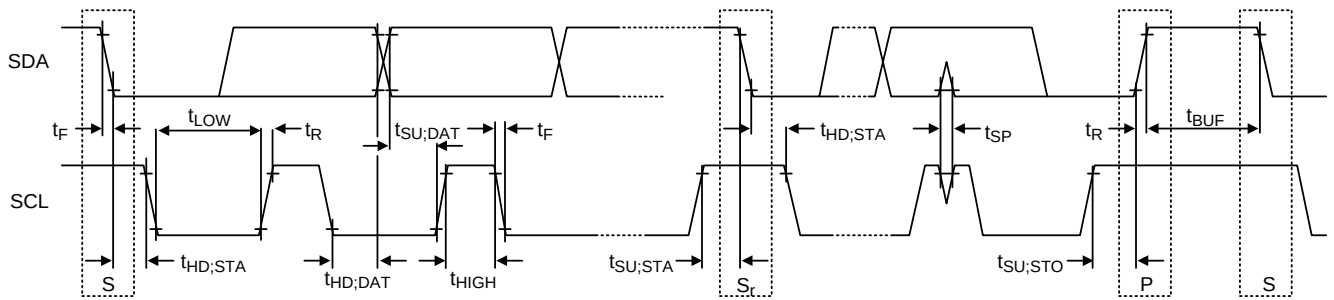


Figure 1. I²C Interface Timing Diagram

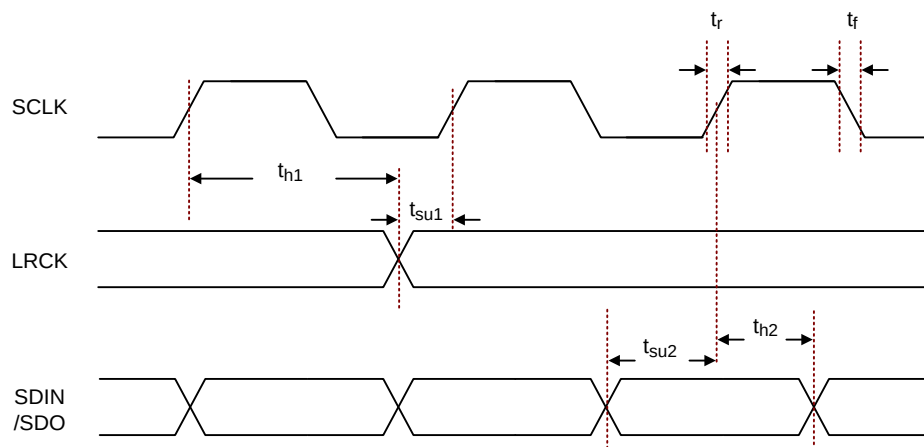
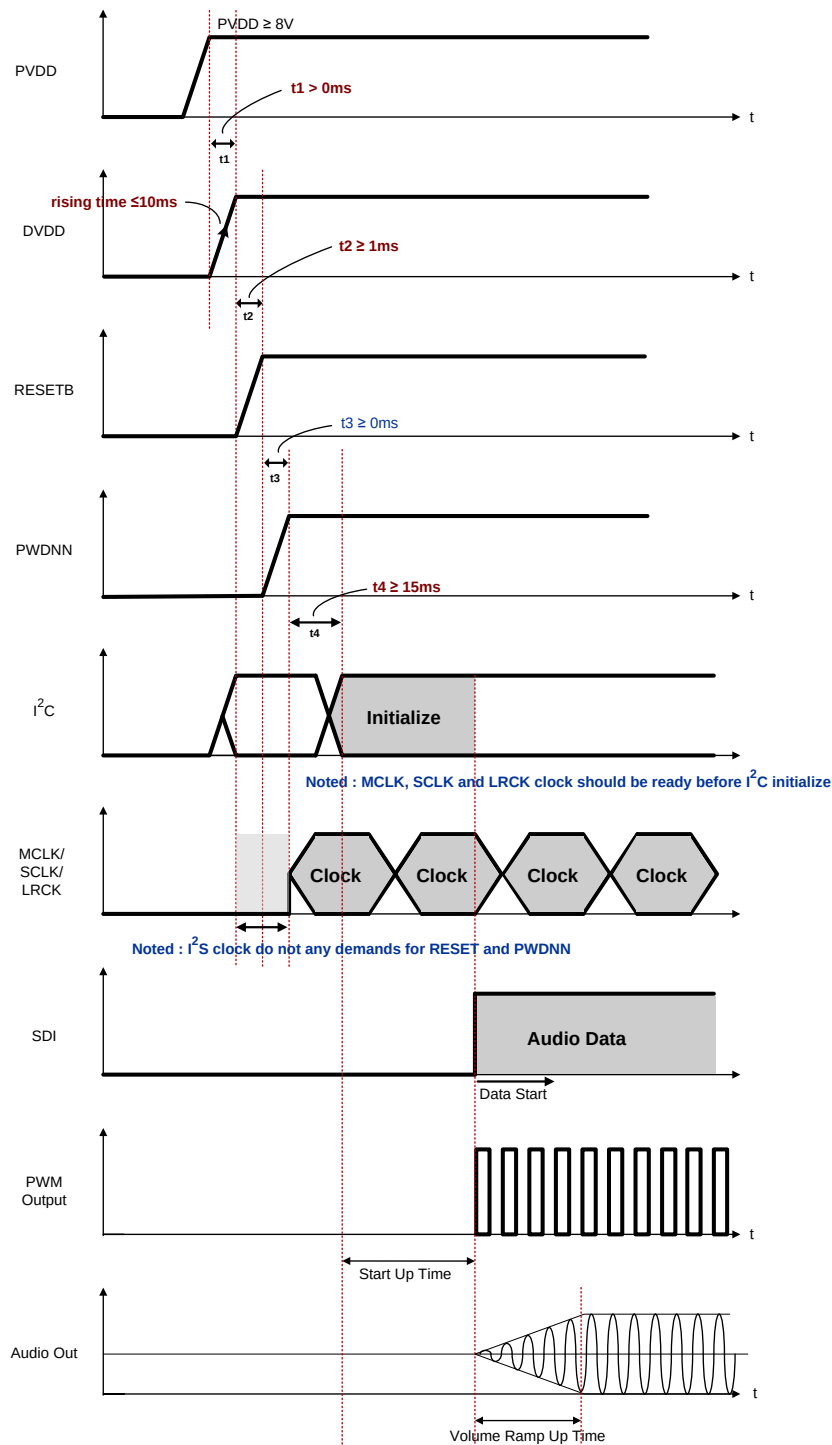


Figure 2. Timing Diagram of Slave Mode I²S Interface

Power On Timing Diagram

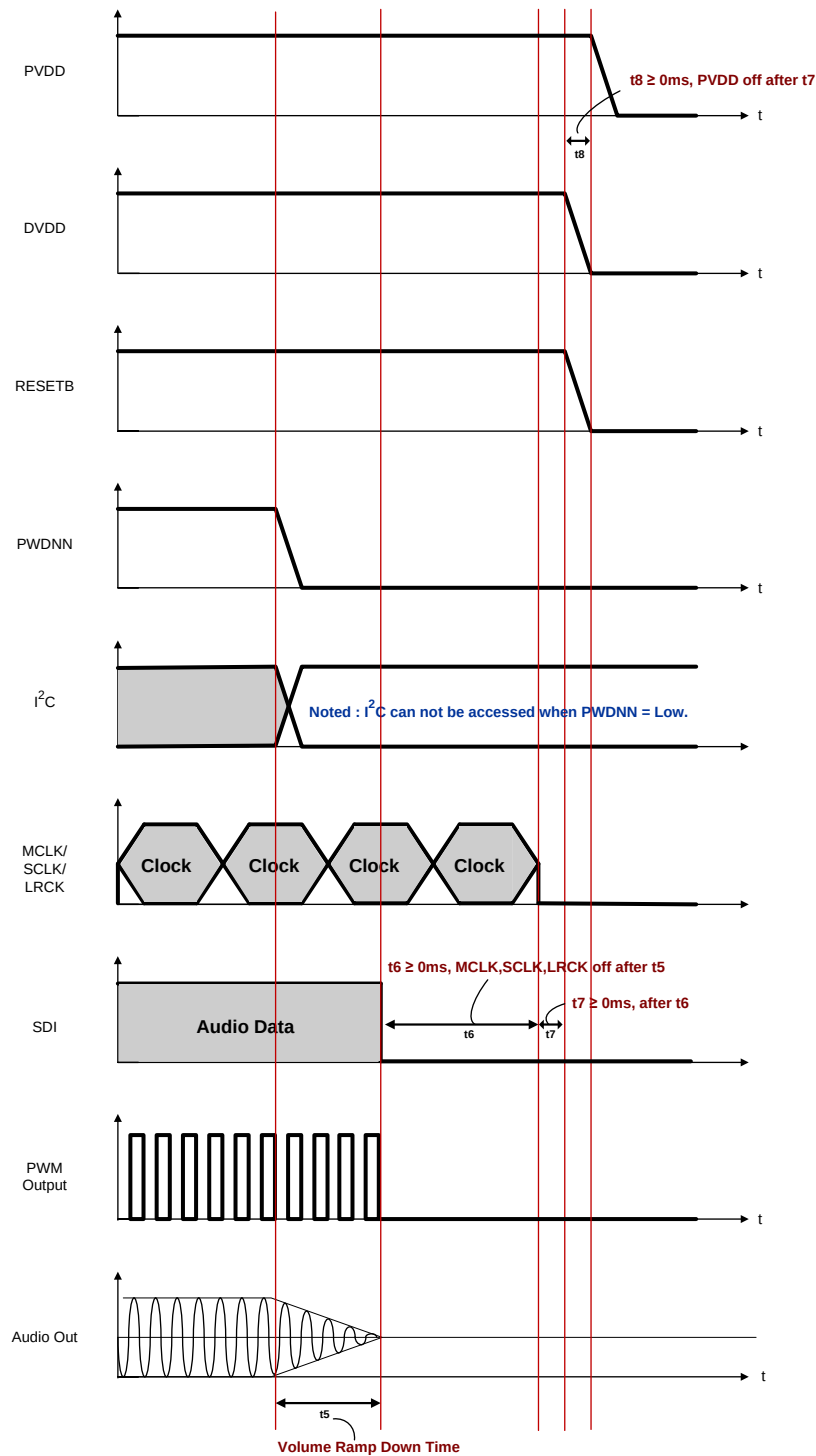


Power on Procedures:

1. Configure A_SEL pin for I²C slave address.
2. PVDD(≥ 8V) need bring up first before DVDD.
3. When power supplies are stable, the RESETB go to high and wait 1ms (t₂) at least, then the PWDNN go to high.
4. When clock (MCLK.SCLK and LRCK) are stable and PWDNN is high, set initialize via I²C and wait 15ms (t₄) at least.
5. The device is normal operation.

Figure 3. Power On Sequence

Power Off Timing Diagram



Power off Procedures:

1. Normal operation.
2. Configure the Reg [0x05h] => B[6] = b'1 or pull PWDNN pin to low
3. Wait at least t_5 (this time depends on ramp down time)
4. Turn off I²S clock.
5. Bring down DVDD and Pull RESETB pin to low.
6. Bring down PVDD.
7. The device enters shutdown mode and powered off.

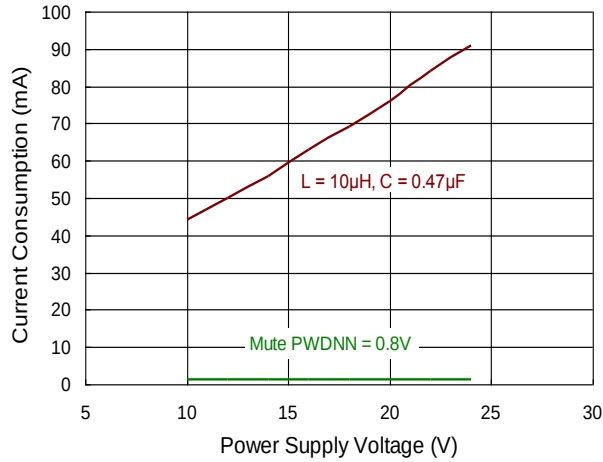
Figure 4. Power Off Sequence

Initial Sequence

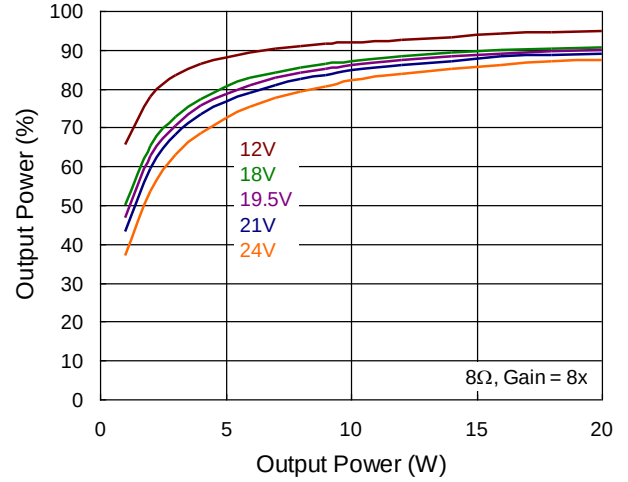
Sequence	reg_addr	reg_size	reg_value	Description	
1	0x80	1	0x80	SW reset, can be removed if hardware reset is already applied	Initial setting
2	0x07	2	0x01, 0x80	Master volume = 0dB	
3	0x62	4	0x00, 0x00, 0x00, 0xA0	Post IDF gain setting = 2dB (Depends on application)	
4	0x1A	1	0x41	Class D gain setting = 5x gain (Depends on application)	
5	0x05	1	0x02	Amp turn on	Amp turn on

Typical Operating Characteristics

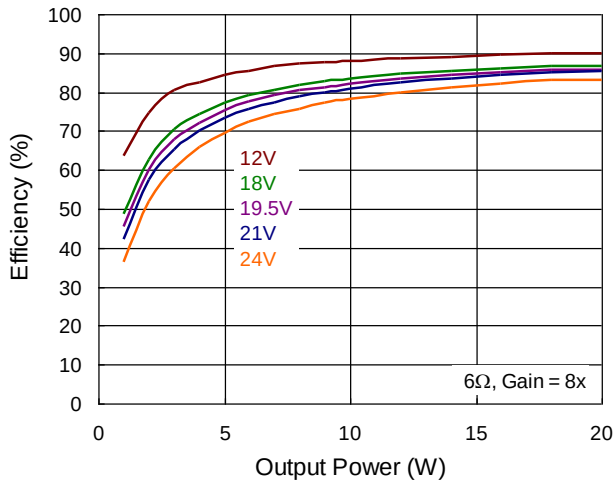
Current Consumption vs. Power Supply Voltage



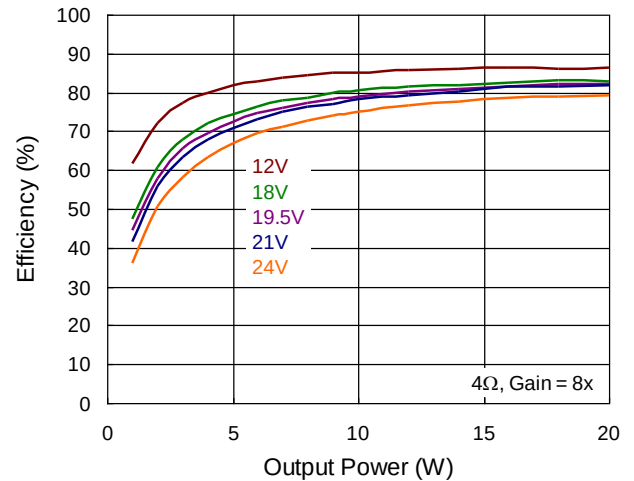
Efficiency vs. Output Power



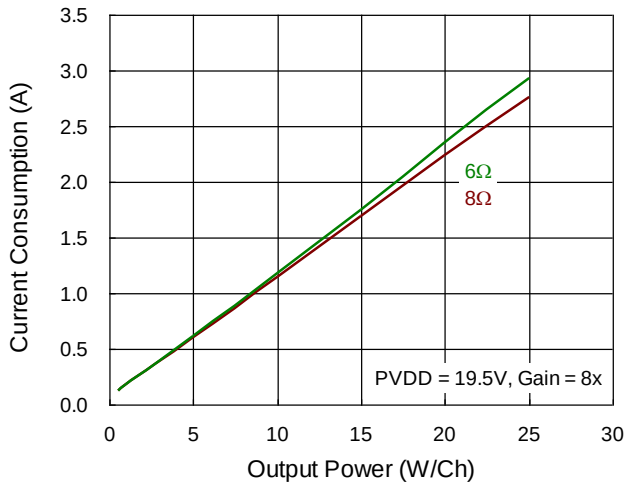
Efficiency vs. Output Power



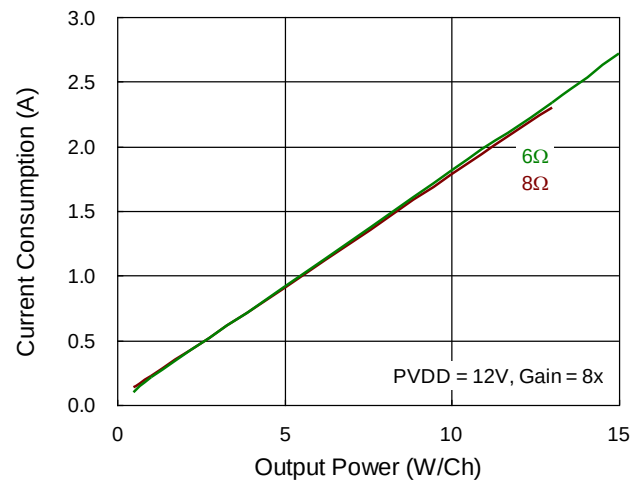
Efficiency vs. Output Power



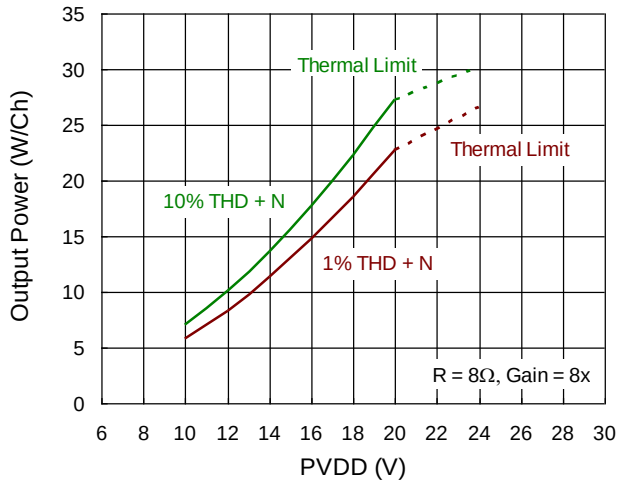
Current Consumption vs. Output Power



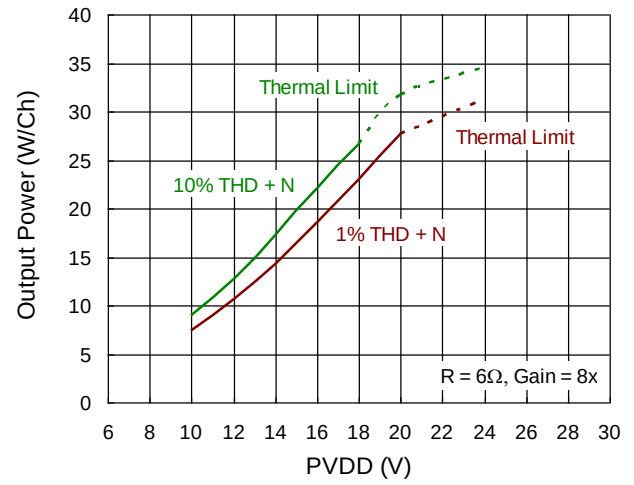
Current Consumption vs. Output Power



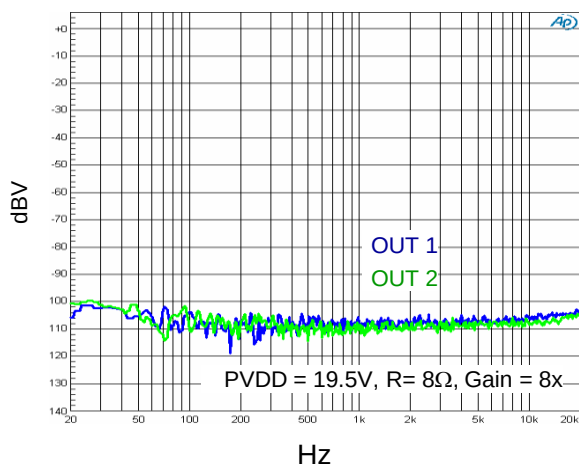
Output Power vs. PVDD



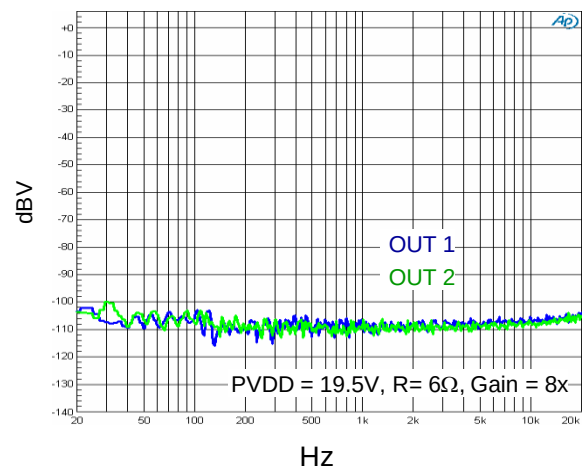
Output Power vs. PVDD



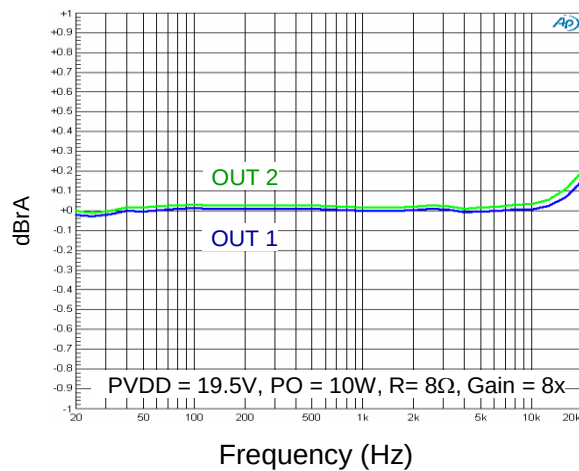
FFT of Output Noise



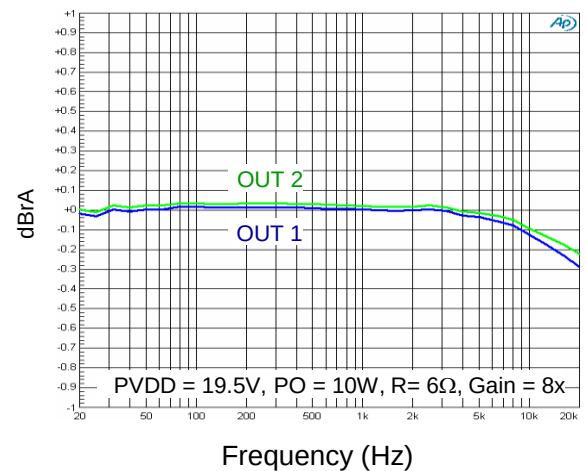
FFT of Output Noise



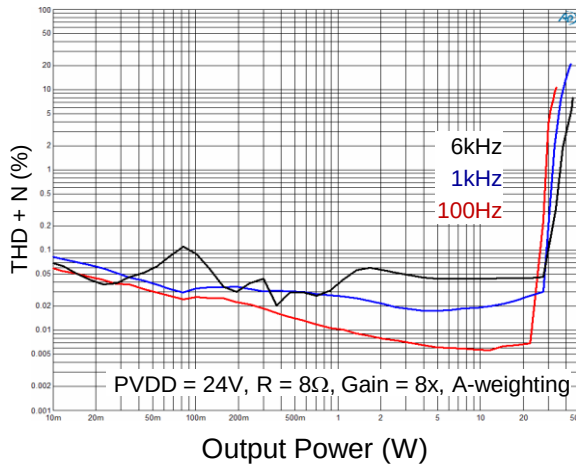
Output Level vs. Frequency



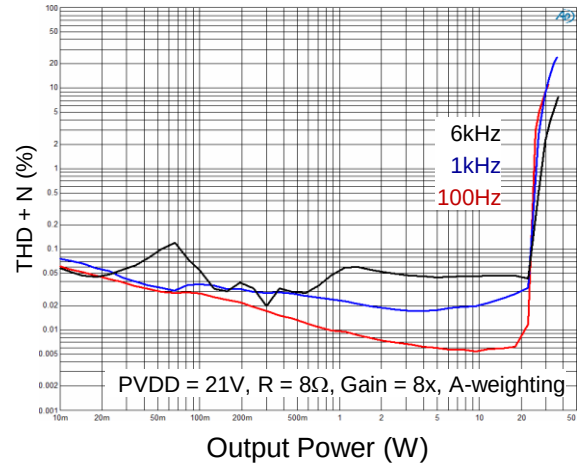
Output Level vs. Frequency



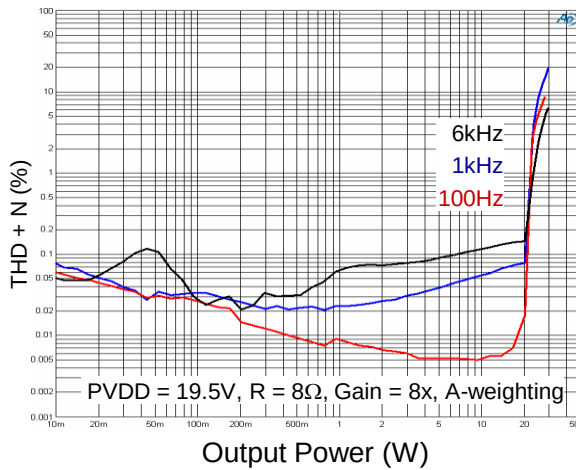
THD + N vs. Output Power



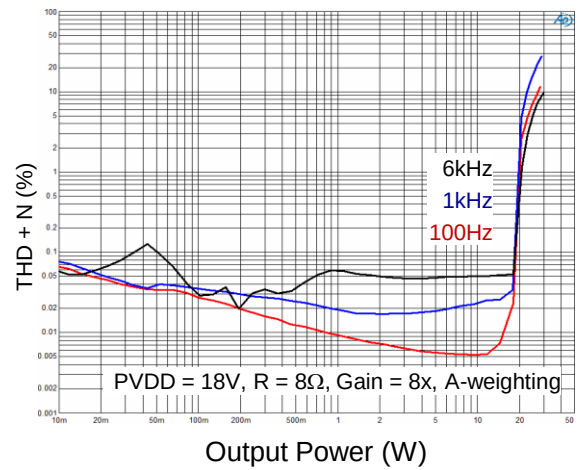
THD + N vs. Output Power



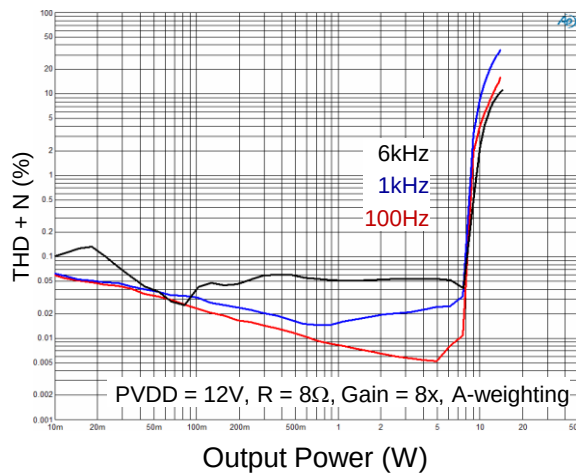
THD + N vs. Output Power



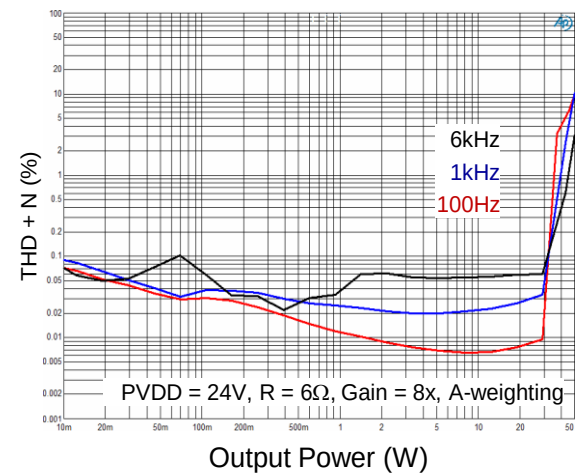
THD + N vs. Output Power



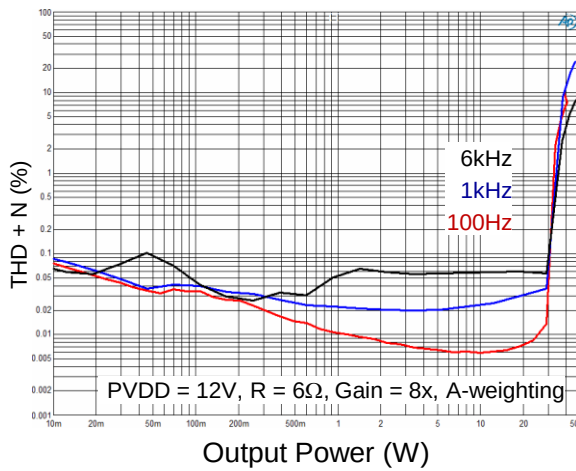
THD + N vs. Output Power



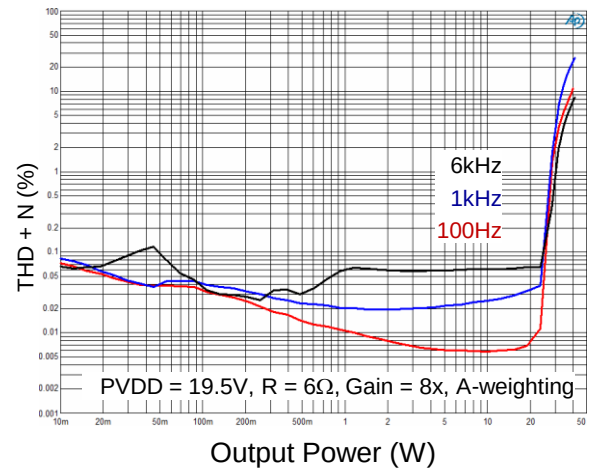
THD + N vs. Output Power



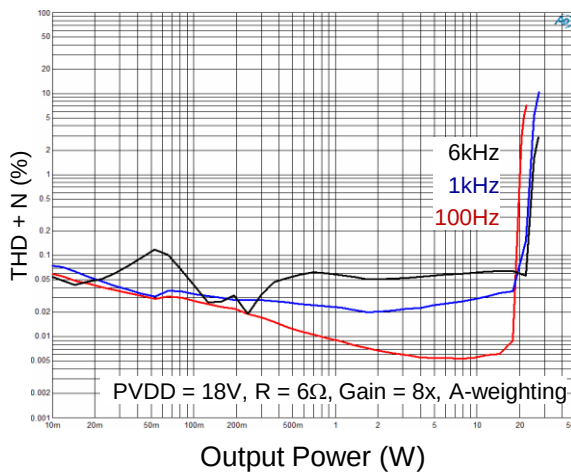
THD + N vs. Output Power



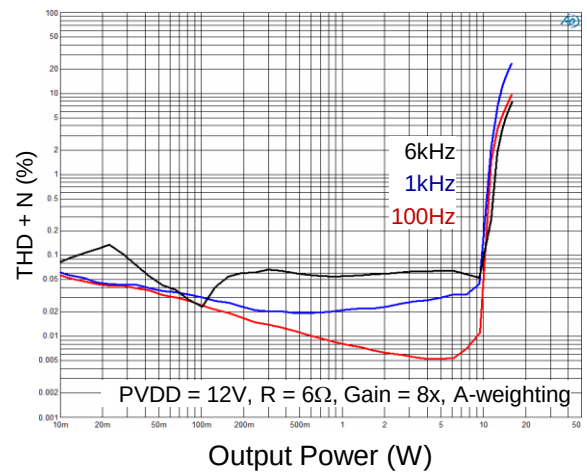
THD + N vs. Output Power



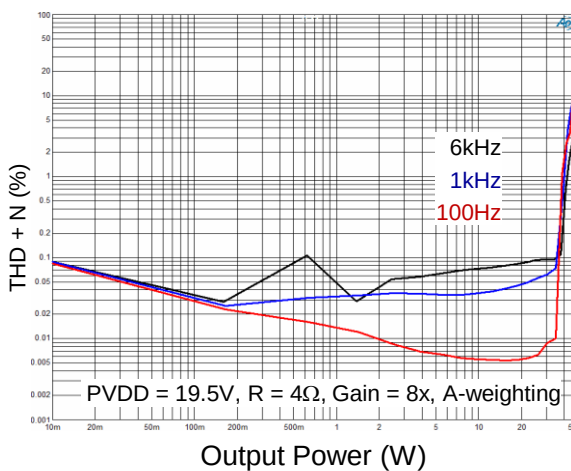
THD + N vs. Output Power



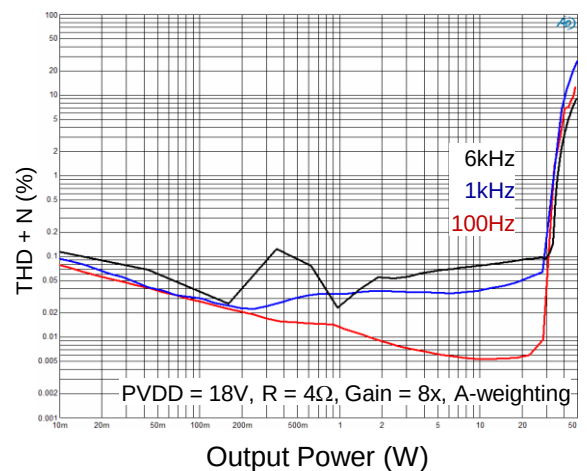
THD + N vs. Output Power



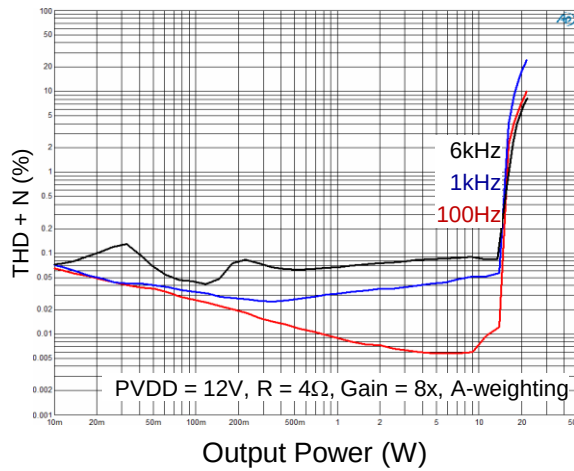
THD + N vs. Output Power



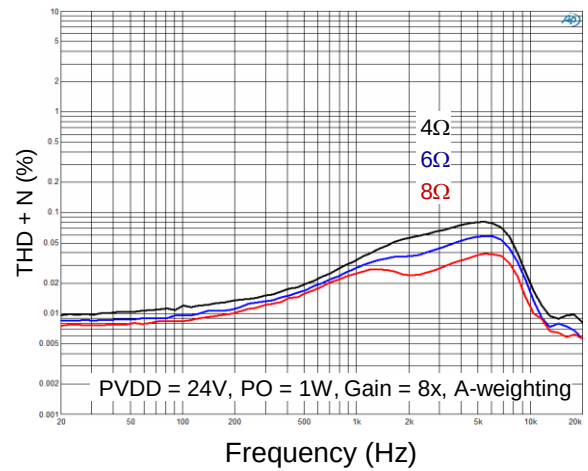
THD + N vs. Output Power



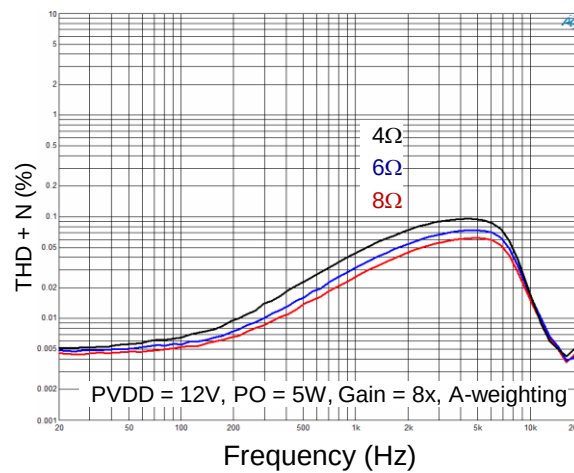
THD + N vs. Output Power



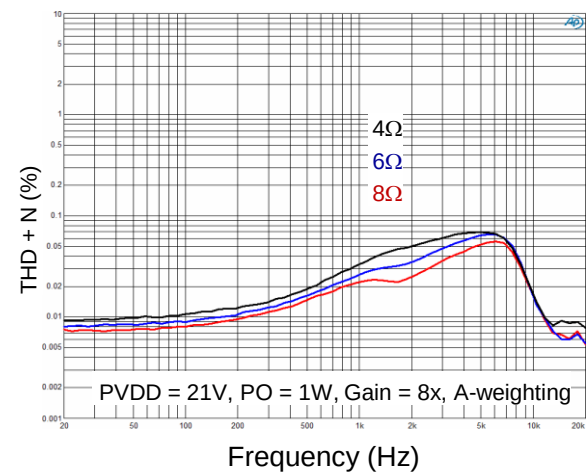
THD + N vs. Frequency



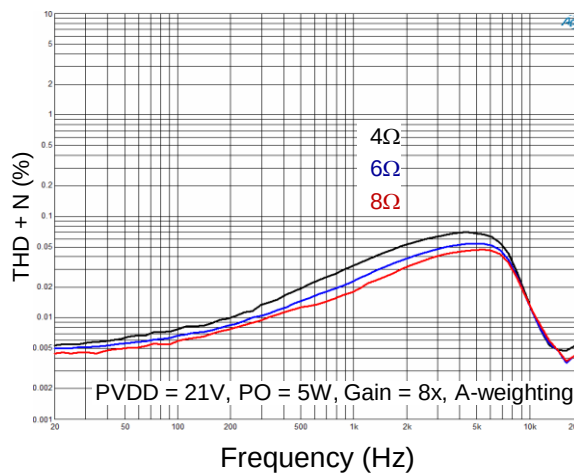
THD + N vs. Frequency



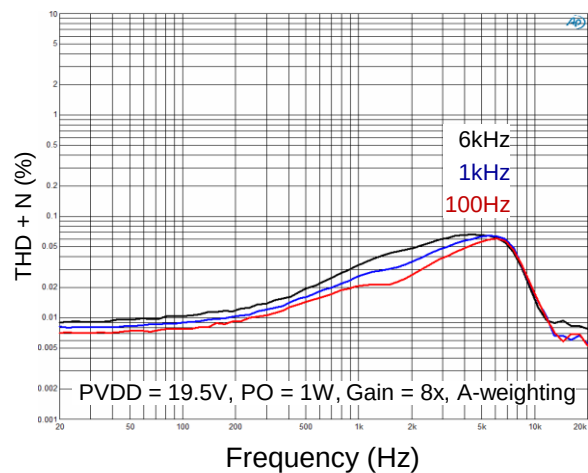
THD + N vs. Frequency



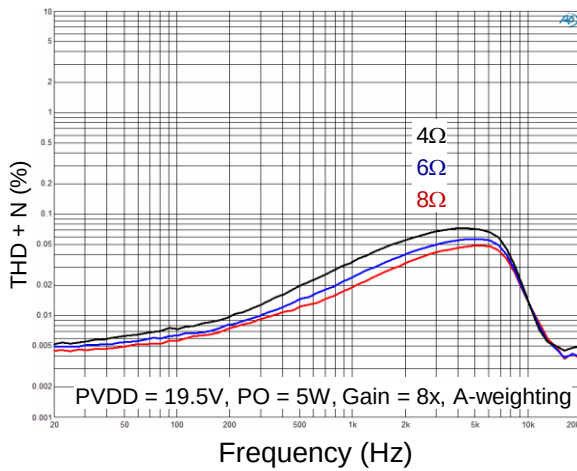
THD + N vs. Frequency



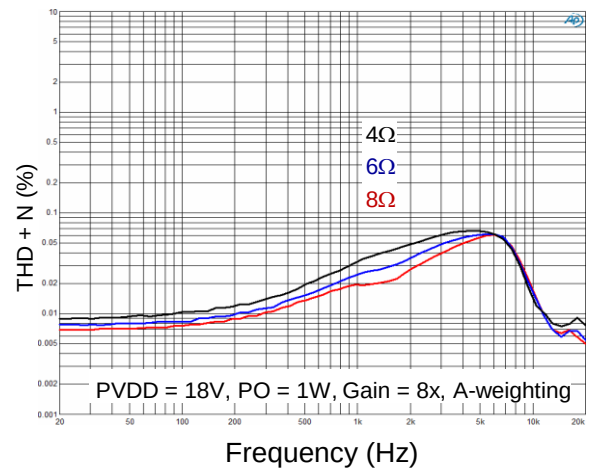
THD + N vs. Frequency



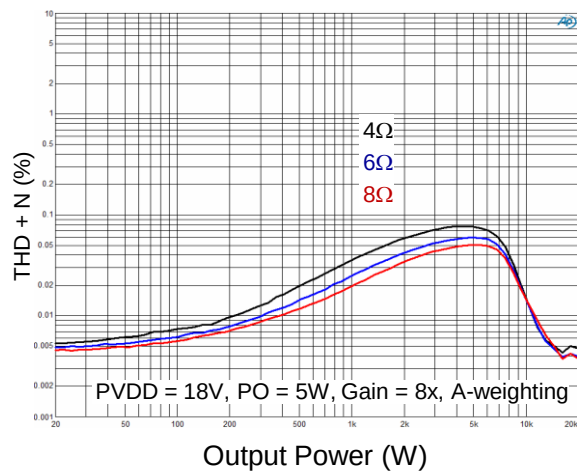
THD + N vs. Frequency



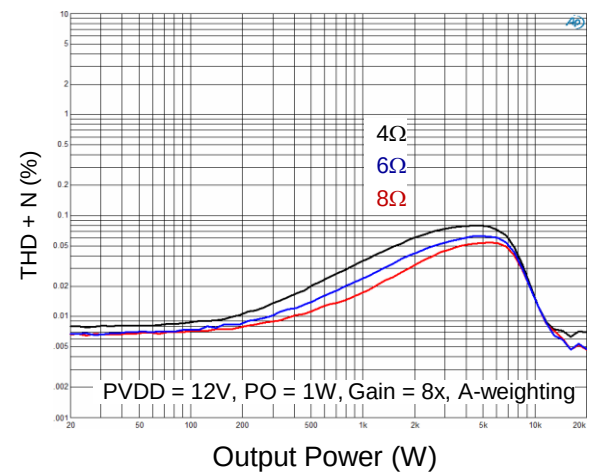
THD + N vs. Frequency



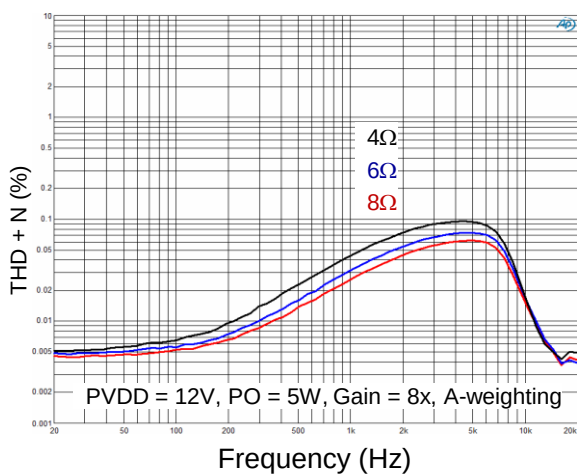
THD + N vs. Frequency



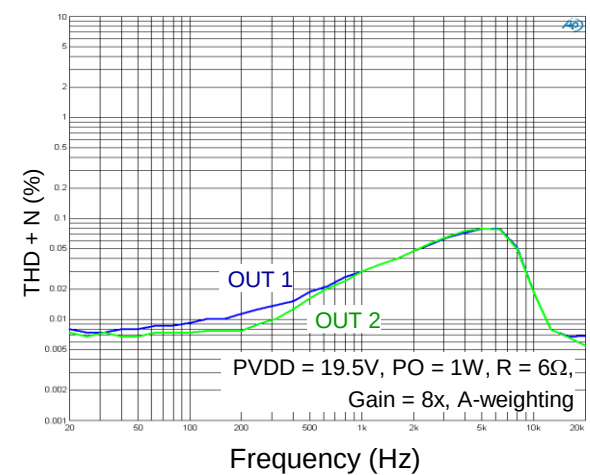
THD + N vs. Frequency

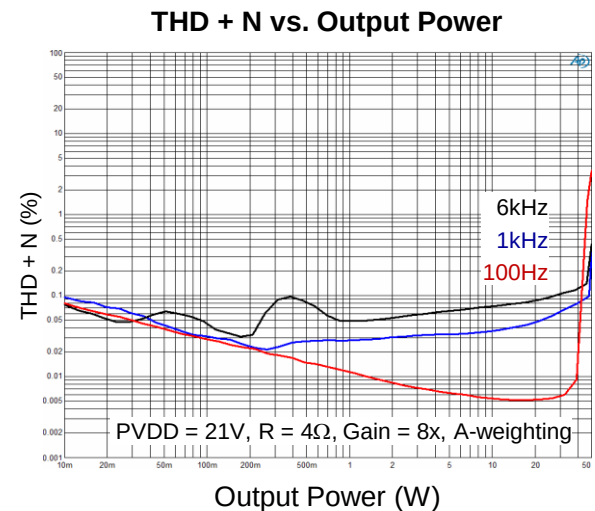
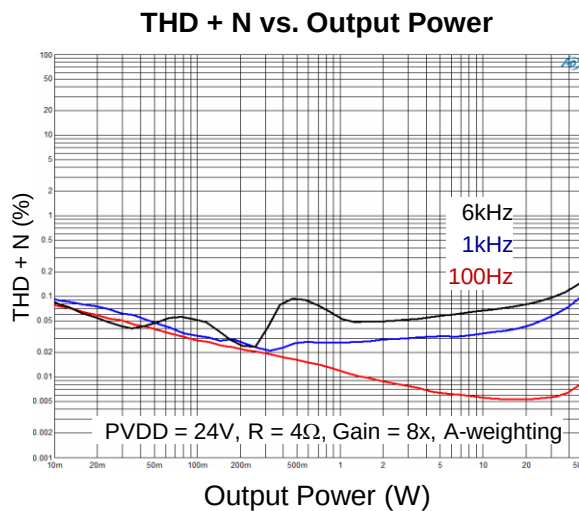
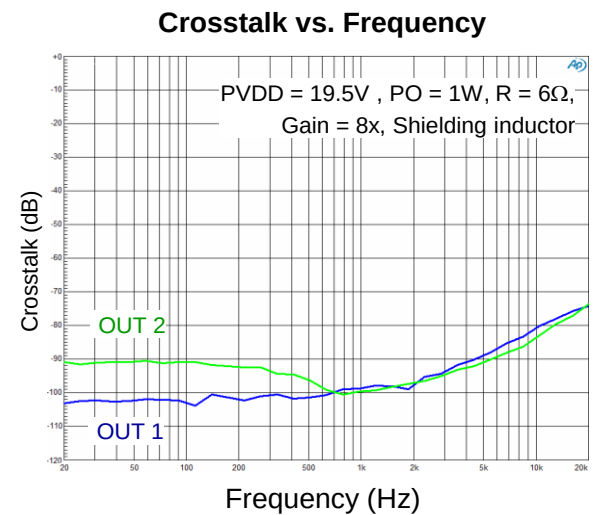
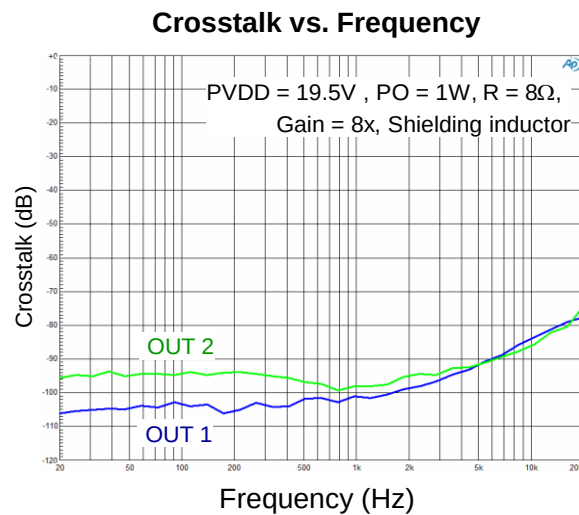
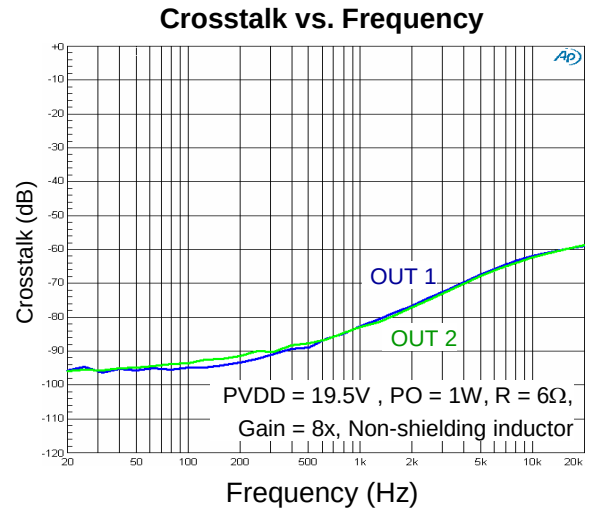
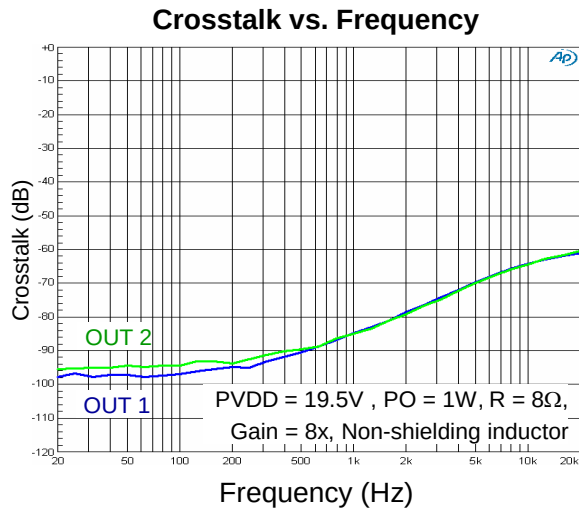


THD + N vs. Frequency

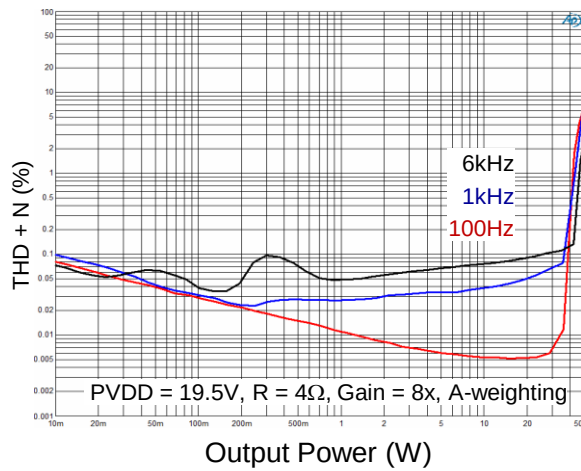


THD + N vs. Frequency

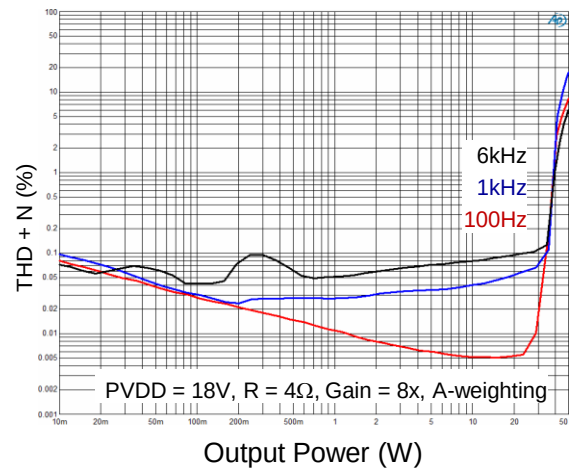




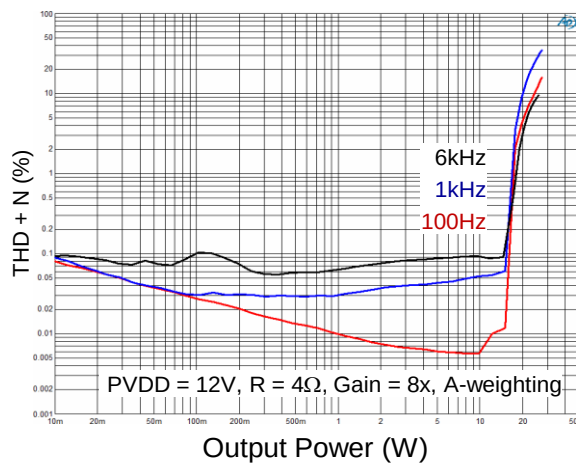
THD + N vs. Output Power



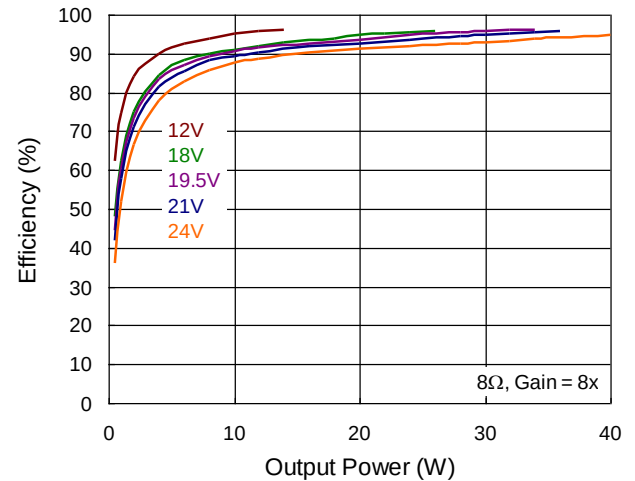
THD + N vs. Output Power



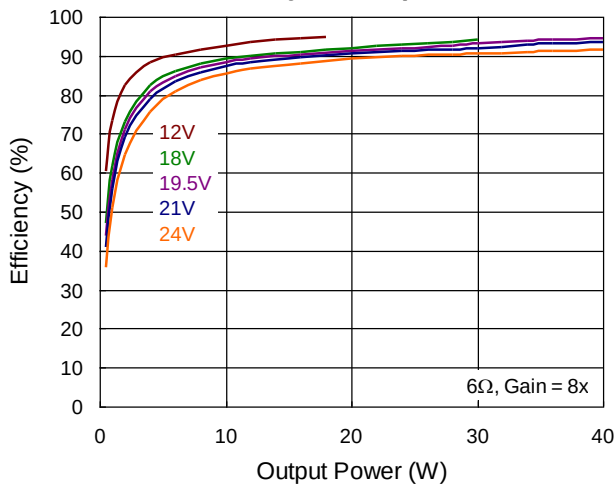
THD + N vs. Output Power



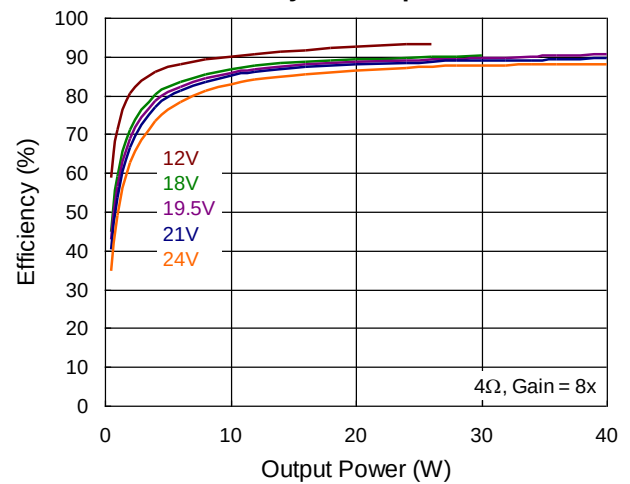
Efficiency vs. Output Power



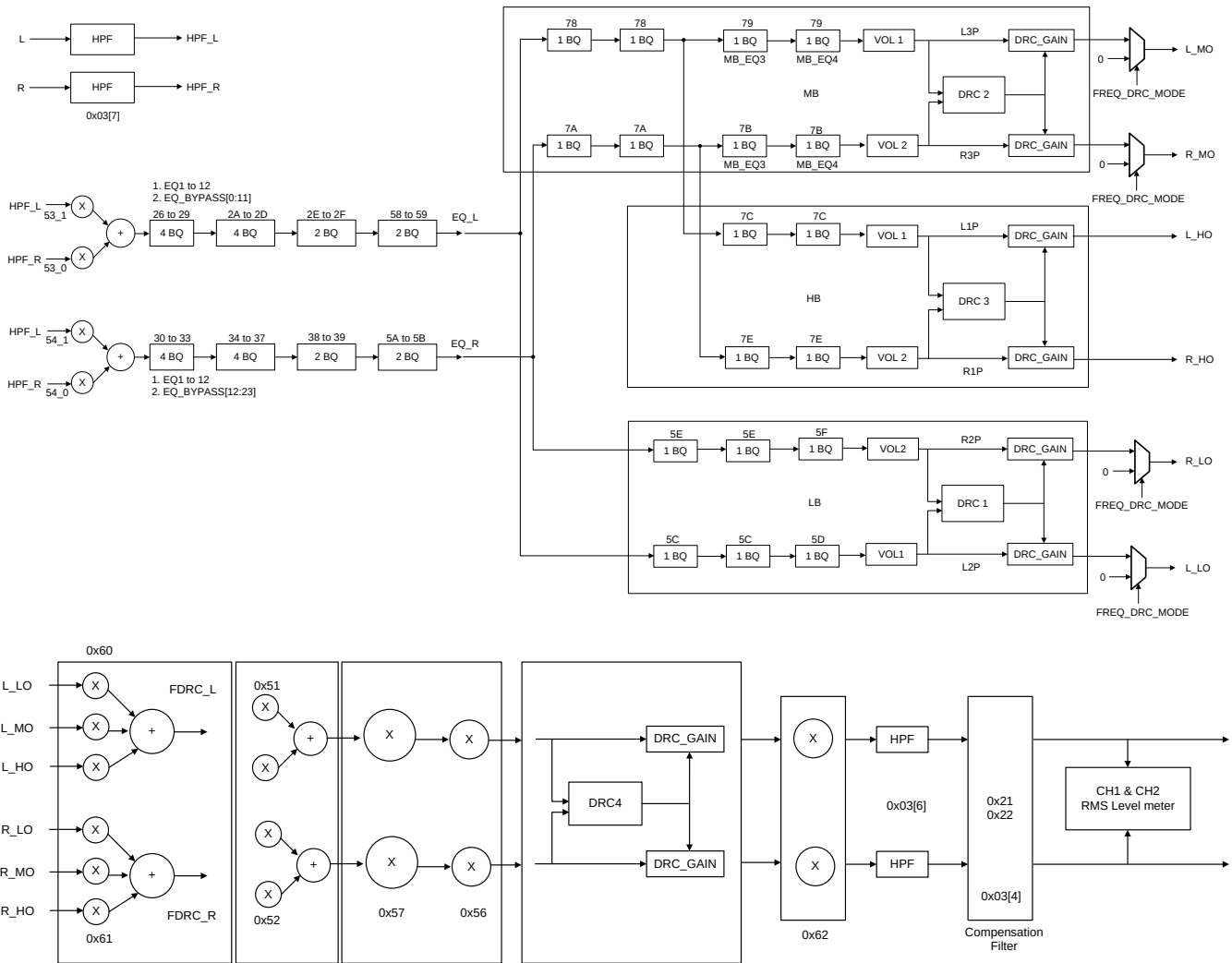
Efficiency vs. Output Power



Efficiency vs. Output Power



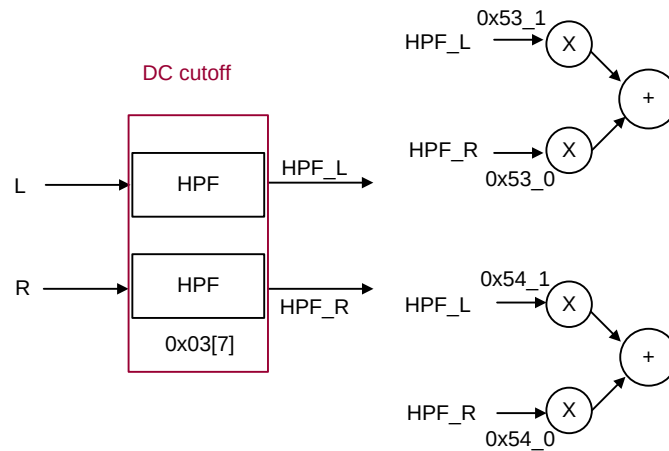
Signal Path



Input High Pass Filter

Block Diagram & Description

→ There are DC-Cut filter for each output filter. The cut off frequency is 1.5Hz

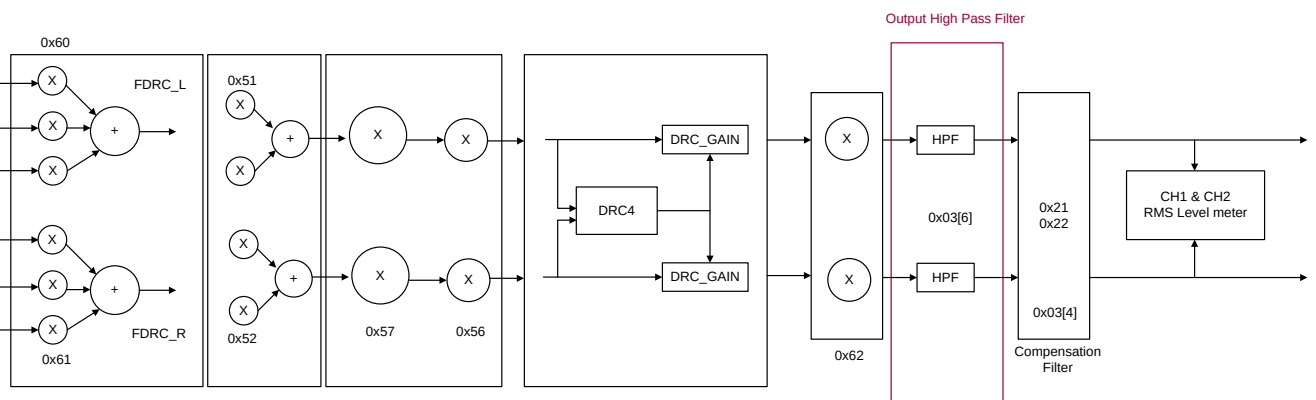


Address	BITS	Name	Description
0x03	7	HPF_EN	1 : Input high pass filter enable 0 : Input high pass filter disable

Output High Pass Filter

Block Diagram & Description

→ There are DC-Cut filter for each output filter. The cut off frequency is 1.5Hz



Address	BITS	Name	Description
0x03	6	HPF_POS_EN	1 : Post high pass filter enable 0 : Post high pass filter disable

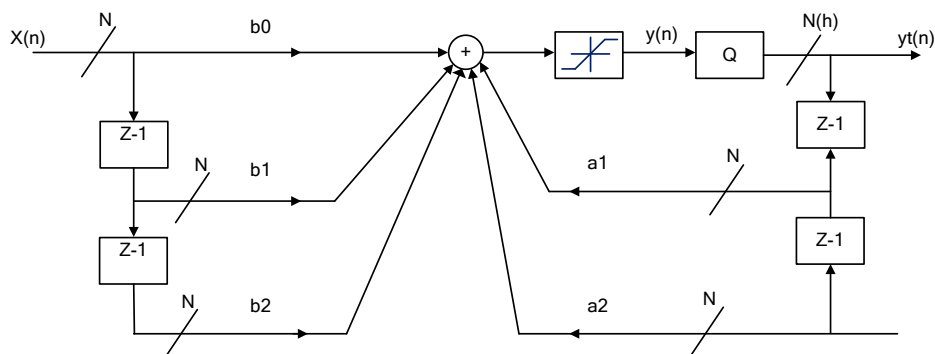
EQ

Block Diagram & Description

→ There are 12 bands of Bi-Quad filter for each channel. 26 bits coefficient for each parameter. If multi-band DRC is disabled, the max band is 14 bands. EQ_BYPASS can bypass the EQ path in signal path. Each EQ band has own disable bit.

EQ parameter : $b_0/b_1/b_2/a_1/a_2$

Update coefficient after writing 5 coefficients



Address	BITS	Name	Description
0x26	159:128	CH1_bq_1_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH1_bq_1_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH1_bq_1_b2	u[31:26], b2[25:0] u : Unused
	63:32	CH1_bq_1_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH1_bq_1_a2	u[31:26], a2[25:0] u : Unused

...

Address	BITS	Name	Description
0x2F	159:128	CH1_bq_10_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH1_bq_10_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH1_bq_10_b2	u[31:26], b2[25:0] u : Unused
	63:32	CH1_bq_10_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH1_bq_10_a2	u[31:26], a2[25:0] u : Unused

Address	BITS	Name	Description
0x58	159:128	CH1_bq_11_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH1_bq_11_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH1_bq_11_b2	u[31:26], b2[25:0] u : Unused
	63:32	CH1_bq_11_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH1_bq_11_a2	u[31:26], a2[25:0] u : Unused

Address	BITS	Name	Description
0x59	159:128	CH1_bq_12_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH1_bq_12_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH1_bq_12_b2	u[31:26], b2[25:0] u : Unused
	63:32	CH1_bq_12_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH1_bq_12_a2	u[31:26], a2[25:0] u : Unused

Address	BITS	Name	Description
0x30	159:128	CH2_bq_1_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH2_bq_1_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH2_bq_1_b2	u[31:26], b2[25:0] u : Unused
	63:32	CH2_bq_1_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH2_bq_1_a2	u[31:26], a2[25:0] u : Unused

⋮

Address	BITS	Name	Description
0x39	159:128	CH2_bq_10_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH2_bq_10_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH2_bq_10_b2	u[31:26], b2[25:0] u : Unused

	63:32	CH2_bq_10_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH2_bq_10_a2	u[31:26], a2[25:0] u : Unused

Address	BITS	Name	Description
0x5A	159:128	CH2_bq_11_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH2_bq_11_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH2_bq_11_b2	u[31:26], b2[25:0] u : Unused
	63:32	CH2_bq_11_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH2_bq_11_a2	u[31:26], a2[25:0] u : Unused

Address	BITS	Name	Description
0x5B	159:128	CH2_bq_12_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH2_bq_12_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH2_bq_12_b2	u[31:26], b2[25:0] u : Unused
	63:32	CH2_bq_12_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH2_bq_12_a2	u[31:26], a2[25:0] u : Unused

EQ Link

Block Diagram & Description

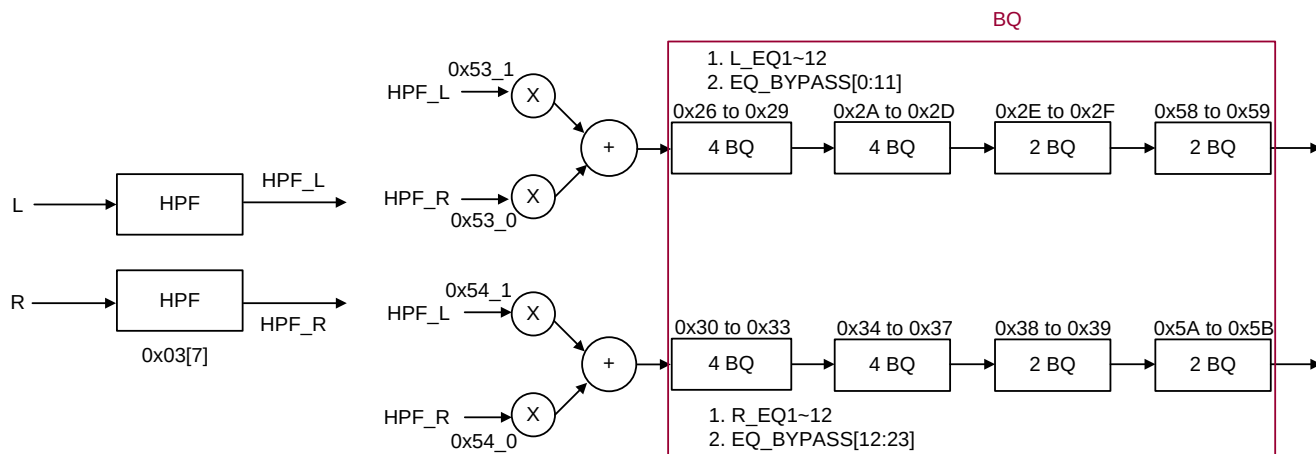
→Link L/R channel EQ parameter automatically, and using the same parameter

→0x46 b08 to b19 is mapping to CH1_bq_1 to CH1_bq_12

→0x46 b20 to b31 is mapping to CH2_bq_1 to CH2_bq_12

→L channel EQ Bypass for EQ1 to 12 is [0:11]

→R channel EQ Bypass for EQ1 to 12 is [12:23]



Address	BITS	Name	Description
0x46	5	EQ_LINK	0 : L/R Can be written independently →Adjust separate channel EQ. 1 : L and R are ganged for EQ biquads; a write to left-channel BQ is also written to right-channel BQ. (0x26–0x2F is ganged to 0x30–0x39. Also 0x58–0x59 is ganged to 0x5A–0x5B) →When link, two channel EQ will be the same.

EQ Gain Boost

Address	BITS	Name	Description
0xC3	7:0	EQ_L_GAIN_BOOST_1_8	Control L channel bq1 to bq8 gain boost →The high/low shelf filter, it can boost up to 24dB
0xC4	7:0	EQ_R_GAIN_BOOST_1_8	Control R channel bq1 to bq8 gain boost →The high/low shelf filter, it can boost up to 24dB
0x77	7:4	EQ_L_GAIN_BOOST_9_12	Control L channel bq9 to bq12 gain boost →The high/low shelf filter, it can boost up to 24dB
0x77	3:0	EQ_R_GAIN_BOOST_9_12	Control R channel bq9 to bq12 gain boost →The high/low shelf filter, it can boost up to 24dB

Multi-Band DRC

DRC Description	Address	Description
DRC_T : Threshold	0x40, 0x43, 0x4A, 0xA6	
DRC_K : Compress ratio	0x41, 0x44, 0x4B, 0xA7	
DRC_O : Make up gain	0x42, 0x45, 0x4C, 0xA8	
DRC_N_T : Noise gate threshold	0xA2	
Noise gate enable	0x72	

Address	BITS	Name	Description
0x72	7	DRC4_N_EN	1 : DRC4 Noise gate enable 0 : DRC4 Noise gate disable
	6	DRC3_N_EN	1 : DRC3 Noise gate enable 0 : DRC3 Noise gate disable
	5	DRC2_N_EN	1 : DRC2 Noise gate enable 0 : DRC2 Noise gate disable
	4	DRC1_N_EN	1 : DRC1 Noise gate enable 0 : DRC1 Noise gate disable

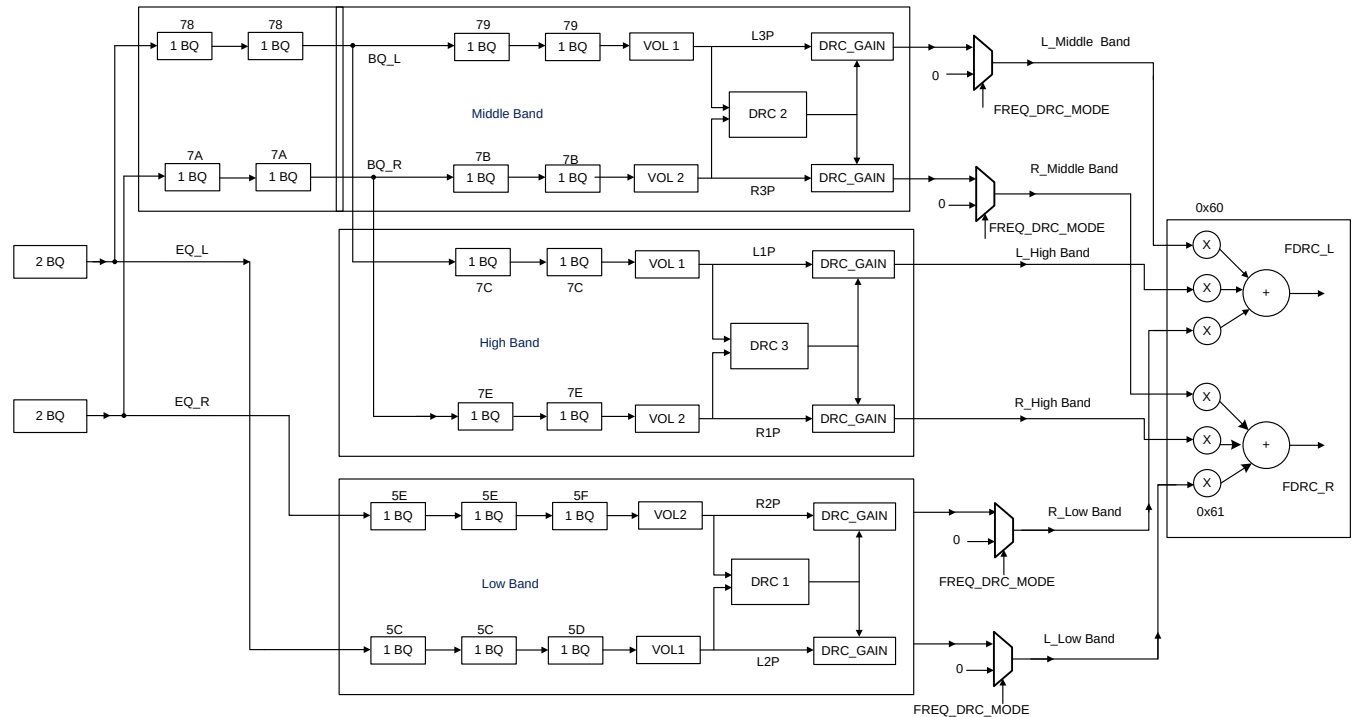
Address	BITS	Name	Description
0x40	31:0	DRC1_T[31:0]	t1[31:0], DRC1 Threshold
0x41	31:0	DRC1_K[31:0]	u[31:26], K1[25:0] DRC1 compression ratio
0x42	31:0	DRC1_O[31:0]	u[31:26], O1[25:0] DRC1 make up gain
0x43	31:0	DRC2_T[31:0]	t2[31:0], DRC2 Threshold
0x44	31:0	DRC2_K[31:0]	u[31:26], K2[25:0] DRC2 compression ratio
0x45	31:0	DRC2_O[31:0]	u[31:26], O2[25:0] DRC2 make up gain
0x4A	31:0	DRC3_T[31:0]	t3[31:0], DRC3 Threshold
0x4B	31:0	DRC3_K[31:0]	u[31:26], K3[25:0] DRC3 compression ratio
0x4C	31:0	DRC3_O[31:0]	u[31:26], O3[25:0] DRC3 make up gain
0xA6	31:0	DRC4_T[31:0]	T[31:0], DRC4 Threshold
0xA7	31:0	DRC4_K[25:0]	u[31:26], K4[25:0] DRC4 compression ratio
0xA8	31:0	DRC4_O[25:0]	u[31:26], O4[25:0] DRC4 make up gain
0xA2	31:0	DRC_N_T[31:0]	N_T[31:0] DRC1, 2, 3, 4 Noise gate of the DRC

DRC Description	Equation																								
DRC_T : Threshold DRC_N_T: Noise gate threshold	T is the threshold of the DRC_T and DRC_N_T Equation: $T = (\text{Threshold}-24)/6.0206$ (dB) Ex : $T = -4.5\text{dB}$, $(-4.5-24)/6.0206 = -4.733747$ $T_Dec = -4.733747*2^{23}= -39709551$ $T_Hex = \text{DEC2HEX}(-39709551) = 0x\text{FDA21490}$ <table><tr><th>Threshold</th><th>T_Dec</th><th>T_Hex</th></tr><tr><td>0dB</td><td>-33439622</td><td>0xFE01C079</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>-4.5dB</td><td>-39709551</td><td>0xFDA21490</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr></table>	Threshold	T_Dec	T_Hex	0dB	-33439622	0xFE01C079	.	.	.	.	.	.	-4.5dB	-39709551	0xFDA21490	.	.	.	.	.	.	.	.	.
Threshold	T_Dec	T_Hex																							
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.	.	.																							
.	.	.																							
-4.5dB	-39709551	0xFDA21490																							
.	.	.																							
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.	.	.																							
DRC_K : Compress ratio	K is the compression ratio of the DRC Equation : $K = (1/\text{Ratio}-1) + 8$, 1/Ratio is in the range of 0~1. EX : Ratio = 8 $(1/8-1) + 8 = 7.125$ $K_Dec = 7.125*2^{23} = 59768832$ $K_Hex = \text{DEC2HEX}(59768832) = 0x39000000$ <table><tr><th>Ratio</th><th>K_Dec</th><th>K_Hex</th></tr><tr><td>Full Comp</td><td>58720256</td><td>0x38000000</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>8</td><td>59768832</td><td>0x39000000</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr></table>	Ratio	K_Dec	K_Hex	Full Comp	58720256	0x38000000	.	.	.	.	.	.	8	59768832	0x39000000	.	.	.	.	.	.	.	.	.
Ratio	K_Dec	K_Hex																							
Full Comp	58720256	0x38000000																							
.	.	.																							
.	.	.																							
8	59768832	0x39000000																							
.	.	.																							
.	.	.																							
.	.	.																							
DRC_O : Make up gain	O is the offset of the DRC Equation : $O = 10^{(\text{Offset}-24)/20}$ EX : Offset = 0dB $10^{(0-24)/20} = 0.063095$ $O_Dec = 0.063095*2^{23} = 529285$ $O_Hex = \text{DEC2HEX}(529285) = 0x0081385$ <table><tr><th>Offset</th><th>O_Dec</th><th>O_Hex</th></tr><tr><td>0dB</td><td>529285</td><td>0x0081385</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>5dB</td><td>941217</td><td>0x00E5CA1</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr></table>	Offset	O_Dec	O_Hex	0dB	529285	0x0081385	.	.	.	.	.	.	5dB	941217	0x00E5CA1	.	.	.	.	.	.	.	.	.
Offset	O_Dec	O_Hex																							
0dB	529285	0x0081385																							
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.	.	.																							
5dB	941217	0x00E5CA1																							
.	.	.																							
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Bypass DRC

Block Diagram & Description

→Separate each channel of the DRC, If MB_BYPASS = 1, the output signals will be mix of HB and LB



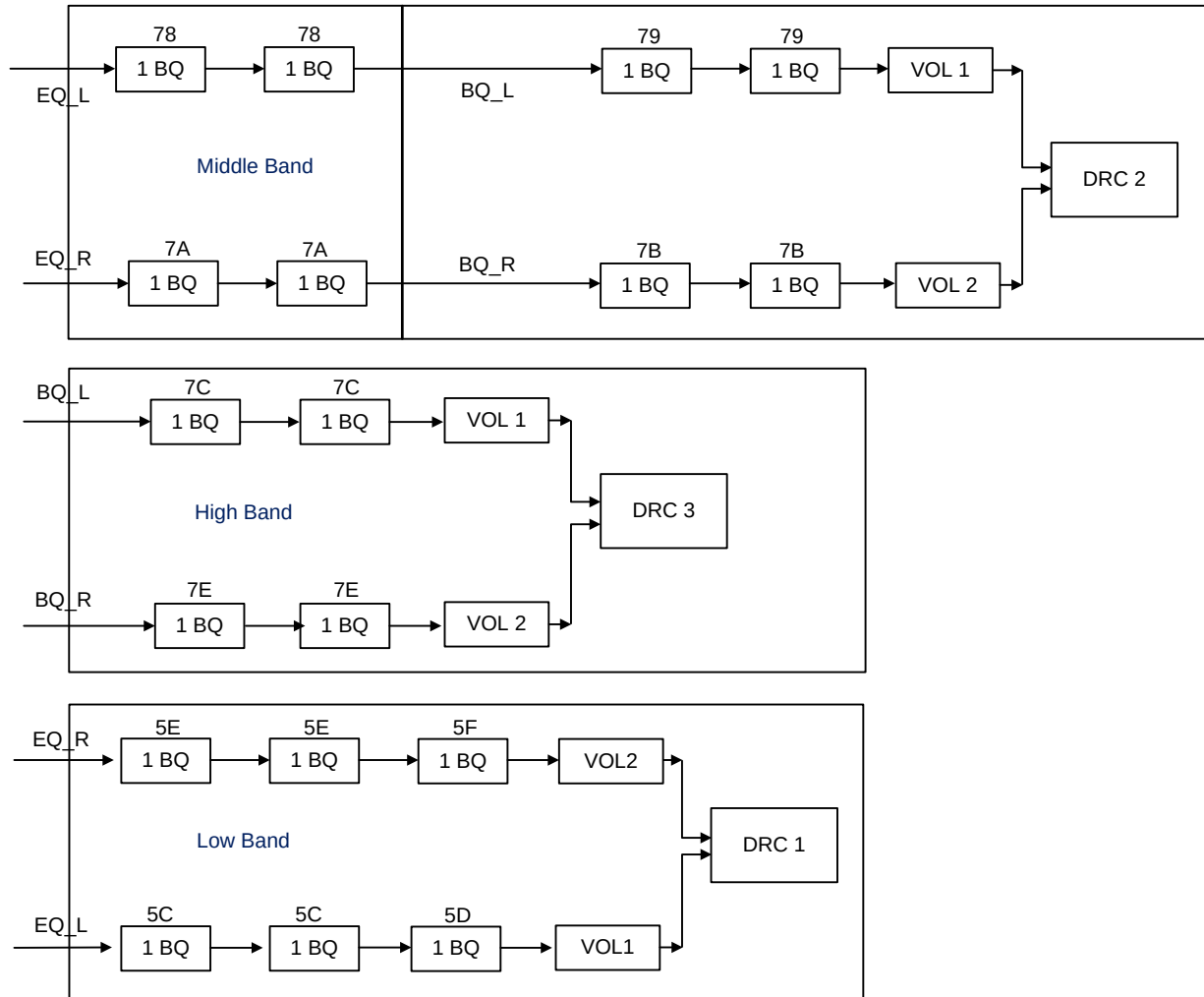
Address	BITS	Name	Description
0x46	6	DRC_EQ_LINK	0: DRC EQ L/R Can be written independently →Adjust separate channel DRC EQ. 1 : L and R are ganged for EQ biquads; a write to left-channel BQ is also written to right-channel BQ. (0x5C, 0x5D is ganged to 0x5E–0x5F. Also 0x78–0x79 is ganged to 0x7A, 0x7B, and 0x7C is ganged to 0x7E) →When link, two channel DRC EQ will be the same.
	3	DRC4_ON	DRC4 Enable 1 : Enable →Final Stage DRC enable (DRC4) 0 : Disable, →When disable, input signal is the same as output signal.
	2	DRC3_ON	DRC3 Enable 1 : Enable →DRC 3 enable (High band) 0 : Disable →When disable, input signal is the same as output signal.
	1	DRC2_ON	DRC2 Enable 1 : Enable →DRC 2 enable (Middle band) 0 : Disable →When disable, input signal is the same as output signal.
	0	DRC1_ON	DRC1 Enable 1 : Enable →DRC 1 enable (Low band) 0 : Disable →When disable, input signal is the same as output signal.
0x72	3	MB_BYPASS	0: Normal mode 1 : By pass →When bypass, the output signal is 0
	2	LB_BYPASS	0: Normal mode 1 : By pass →When bypass, the output signal is 0
	1	HB_BYPASS	0: Normal mode 1 : By pass →When bypass, the output signal is 0
	0	FREQ_DRC_MODE	0: High band only 1: Frequency DRC Mode

Multi Band DRC EQ

Block Diagram & Description

→To adjust the cut off frequency of the DRC1, 2, 3

→VOL 1= 0x08 (CH_1 Volume) + 0x07 (Master Volume), and VOL 2= 0x09 (CH_2 Volume) + 0x07 (Master Volume)



Address	BITS	Name	Description
0x5C	159:128	LB_CH1_bq_1_b0	u[31:26], b0[25:0] u : Unused
	127:96	LB_CH1_bq_1_b1	u[31:26], b1[25:0] u : Unused
	95:64	LB_CH1_bq_1_b2	u[31:26], b2[25:0] u : Unused
	63:32	LB_CH1_bq_1_a1	u[31:26], a1[25:0] u : Unused
	31:0	LB_CH1_bq_1_a2	u[31:26], a2[25:0] u : Unused

Address	BITS	Name	Description
0x5D	159:128	LB_CH1_bq_2_b0	u[31:26], b0[25:0] u : Unused
	127:96	LB_CH1_bq_2_b1	u[31:26], b1[25:0] u : Unused
	95:64	LB_CH1_bq_2_b2	u[31:26], b2[25:0] u : Unused
	63:32	LB_CH1_bq_2_a1	u[31:26], a1[25:0] u : Unused
	31:0	LB_CH1_bq_2_a2	u[31:26], a2[25:0] u : Unused

Address	BITS	Name	Description
0x5E	159:128	LB_CH2_bq_1_b0	u[31:26], b0[25:0] u : Unused
	127:96	LB_CH2_bq_1_b1	u[31:26], b1[25:0] u : Unused
	95:64	LB_CH2_bq_1_b2	u[31:26], b2[25:0] u : Unused
	63:32	LB_CH2_bq_1_a1	u[31:26], a1[25:0] u : Unused
	31:0	LB_CH2_bq_1_a2	u[31:26], a2[25:0] u : Unused

Address	BITS	Name	Description
0x5F	159:128	LB_CH2_bq_2_b0	u[31:26], b0[25:0] u : Unused
	127:96	LB_CH2_bq_2_b1	u[31:26], b1[25:0] u : Unused
	95:64	LB_CH2_bq_2_b2	u[31:26], b2[25:0] u : Unused
	63:32	LB_CH2_bq_2_a1	u[31:26], a1[25:0] u : Unused
	31:0	LB_CH2_bq_2_a2	u[31:26], a2[25:0] u : Unused

Address	BITS	Name	Description
0x78	159:128	MB_CH1_bq_1_b0	u[31:26], b0[25:0] u : Unused
	127:96	MB_CH1_bq_1_b1	u[31:26], b1[25:0] u : Unused
	95:64	MB_CH1_bq_1_b2	u[31:26], b2[25:0] u : Unused
	63:32	MB_CH1_bq_1_a1	u[31:26], a1[25:0] u : Unused

	31:0	MB_CH1_bq_1_a2	u[31:26], a2[25:0] u : Unused
--	------	----------------	----------------------------------

Address	BITS	Name	Description
0x79	159:128	MB_CH1_bq_2_b0	u[31:26], b0[25:0] u : Unused
	127:96	MB_CH1_bq_2_b1	u[31:26], b1[25:0] u : Unused
	95:64	MB_CH1_bq_2_b2	u[31:26], b2[25:0] u : Unused
	63:32	MB_CH1_bq_2_a1	u[31:26], a1[25:0] u : Unused
	31:0	MB_CH1_bq_2_a2	u[31:26], a2[25:0] u : Unused

Address	BITS	Name	Description
0x7A	159:128	MB_CH2_bq_1_b0	u[31:26], b0[25:0] u : Unused
	127:96	MB_CH2_bq_1_b1	u[31:26], b1[25:0] u : Unused
	95:64	MB_CH2_bq_1_b2	u[31:26], b2[25:0] u : Unused
	63:32	MB_CH2_bq_1_a1	u[31:26], a1[25:0] u : Unused
	31:0	MB_CH2_bq_1_a2	u[31:26], a2[25:0] u : Unused

Address	BITS	Name	Description
0x7B	159:128	MB_CH2_bq_2_b0	u[31:26], b0[25:0] u : Unused
	127:96	MB_CH2_bq_2_b1	u[31:26], b1[25:0] u : Unused
	95:64	MB_CH2_bq_2_b2	u[31:26], b2[25:0] u : Unused
	63:32	MB_CH2_bq_2_a1	u[31:26], a1[25:0] u : Unused
	31:0	MB_CH2_bq_2_a2	u[31:26], a2[25:0] u : Unused

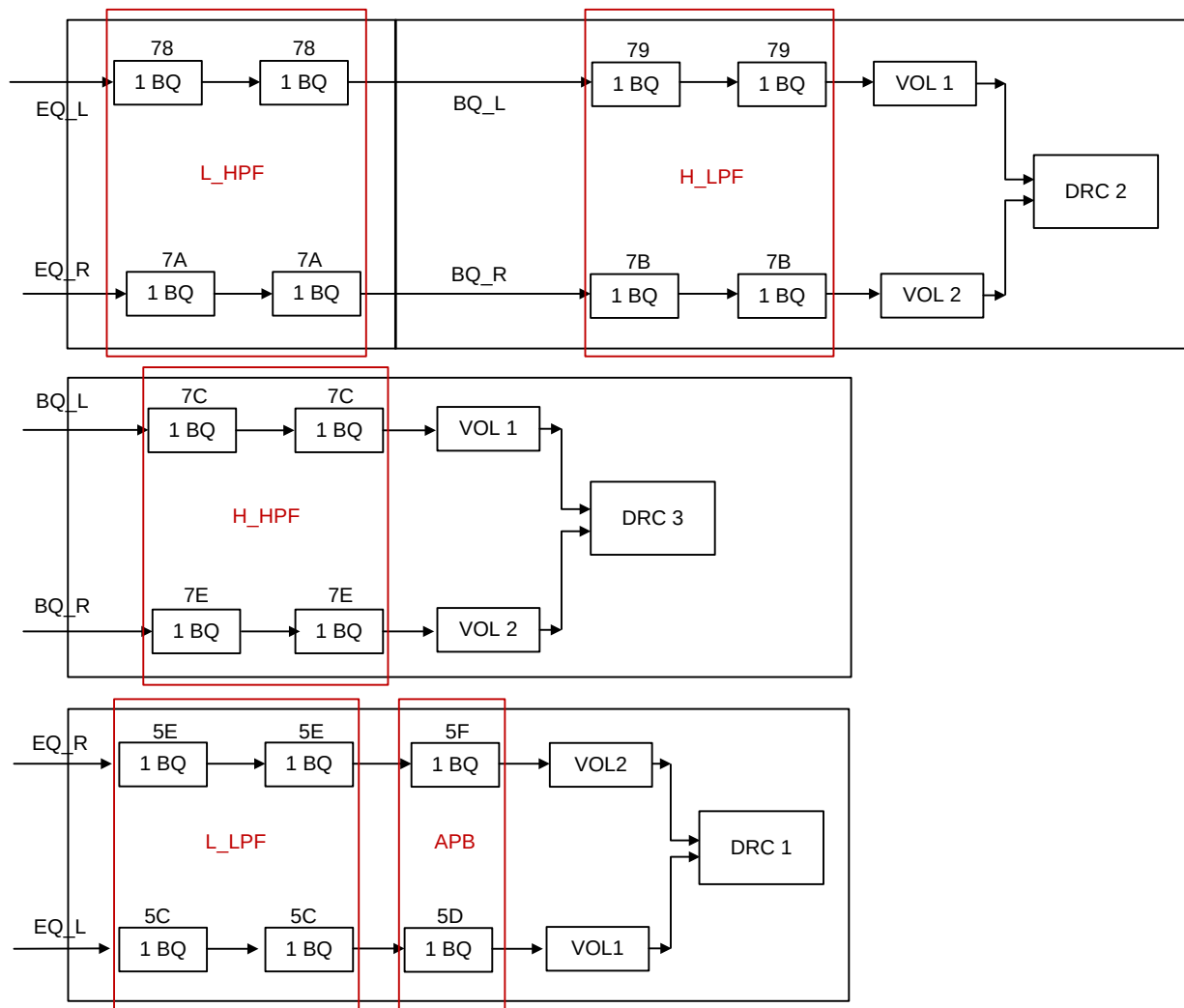
Address	BITS	Name	Description
0x7D	159:128	HB_CH1_bq_1_b0	u[31:26], b0[25:0] u : Unused
	127:96	HB_CH1_bq_1_b1	u[31:26], b1[25:0] u : Unused
	95:64	HB_CH1_bq_1_b2	u[31:26], b2[25:0] u : Unused

	63:32	HB_CH1_bq_1_a1	u[31:26], a1[25:0] u : Unused
	31:0	HB_CH1_bq_1_a2	u[31:26], a2[25:0] u : Unused

Address	BITS	Name	Description
0x7E	159:128	HB_CH2_bq_1_b0	u[31:26], b0[25:0] u : Unused
	127:96	HB_CH2_bq_1_b1	u[31:26], b1[25:0] u : Unused
	95:64	HB_CH2_bq_1_b2	u[31:26], b2[25:0] u : Unused
	63:32	HB_CH2_bq_1_a1	u[31:26], a1[25:0] u : Unused
	31:0	HB_CH2_bq_1_a2	u[31:26], a2[25:0] u : Unused

MBDRC first order setting

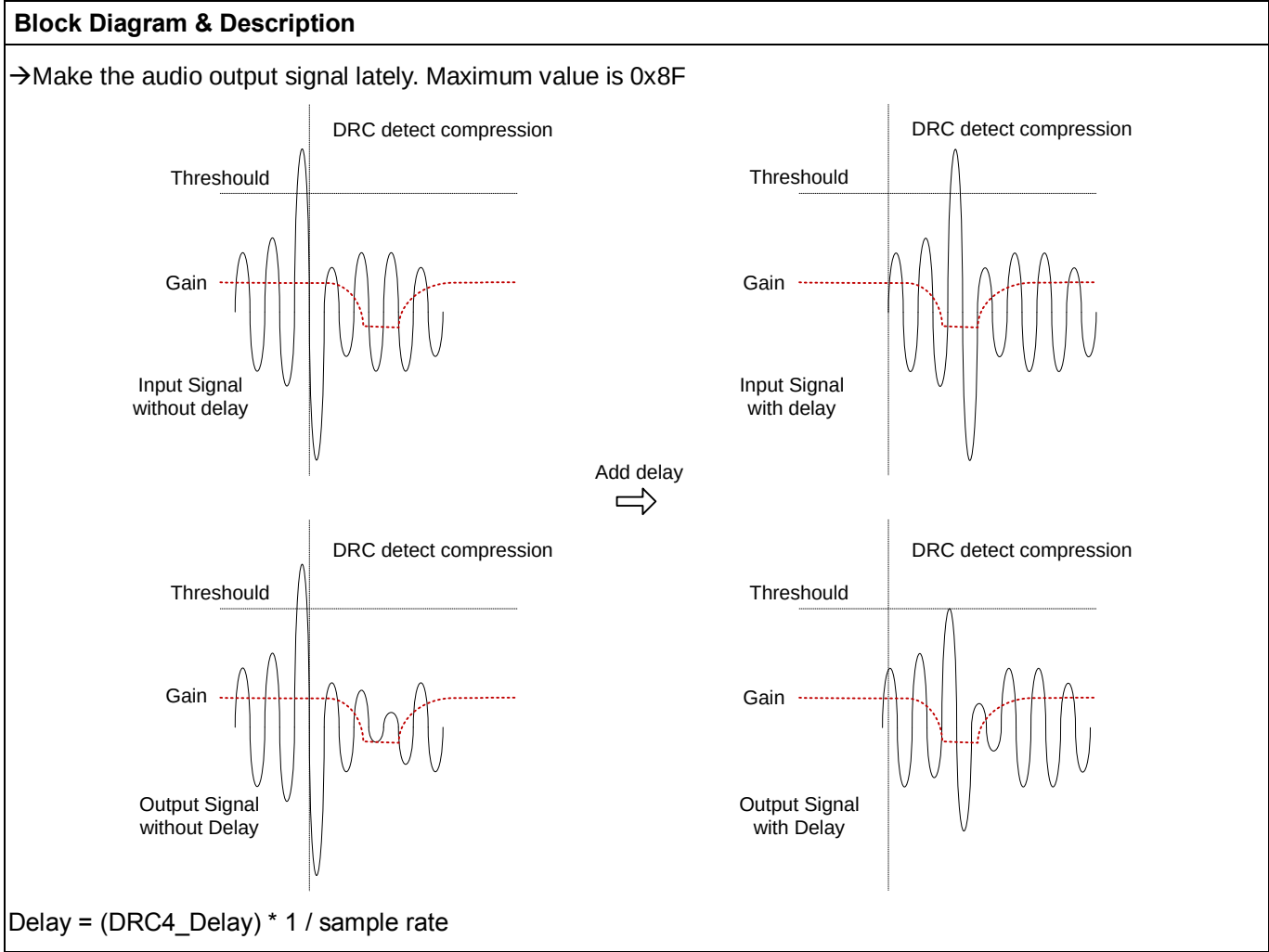
Block Diagram & Description



Address	BITS	Name	Description
0xC1	7	SKIP_BQ1_L_MBAND	(register 0x78) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped
	6	SKIP_BQ2_L_MBAND	(register 0x79) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped
	5	SKIP_BQ1_R_MBAND	(register 0x7A) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped
	4	SKIP_BQ2_R_MBAND	(register 0x7B) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped
	3	SKIP_BQ1_L_HBAND	(register 0x7C) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped
	2	SKIP_BQ1_R_HBAND	(register 0x7E) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped
	1	SKIP_BQ1_L_LBAND	(register 0x5C) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped
	0	SKIP_BQ1_R_LBAND	(register 0x5E) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped

Address	BITS	Name	Description
0xC2	4	SKIP_DRC_L_HPF	L_HPF for MB and HB DRC 0 : Normal Mode 1 : SKIP
	3	SKIP_DRC_H_LPF	H_LPF for MB DRC 0 : Normal Mode 1 : SKIP
	2	SKIP_DRC_H_HPF	H_HPF for HB DRC 0 : Normal Mode 1 : SKIP
	1	SKIP_DRC_L_LPF	L_LPF for LB DRC 0 : Normal Mode 1 : SKIP
	0	SKIP_DRC_APB	APB for LB DRC 0 : Normal Mode 1 : SKIP

DRC4 is final stage of DRC. It can be configure as the final DRC to limit the output power.



Address	BITS	Name	Description
0x0A	7:0	DRC4_DELAY[7:0]	DRC4_DELAY →The delay make the audio signal output delay →Delay = (DRC4_DELAY) * 1 / sample rate →This maximum value is 0x8F, if the setting is larger than 0x8F, it will limit at 0x8F

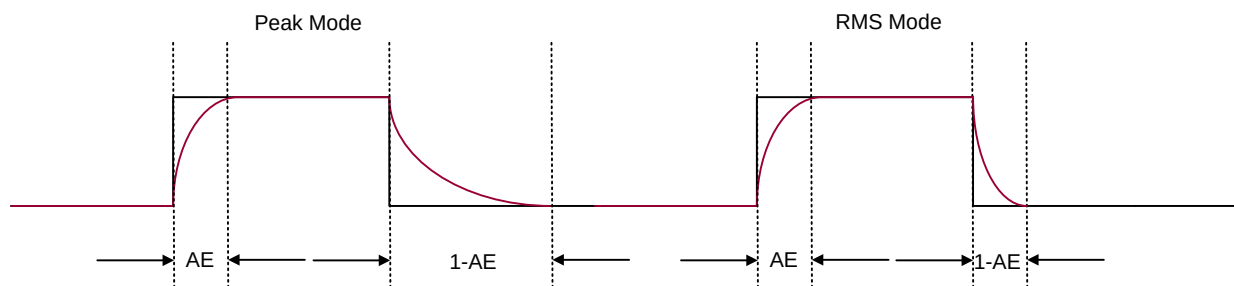
Peak Mode RMS Mode

Block Diagram & Description

→The detecting threshold using different calculated methods.

Peak mode : AE and 1-AE is independent

RMS mode : $AE + (1-AE) = 1$



Address	BITS	Name	Description
0x70	7	DRC4_PEAK	1 : Peak mode 0 : RMS mode
	6	DRC3_PEAK	1 : Peak mode 0 : RMS mode
	5	DRC2_PEAK	1 : Peak mode 0 : RMS mode
	4	DRC1_PEAK	1 : Peak mode 0 : RMS mode

DRC Timing Equation

DRC Description	Equation																					
AA/AE/AD Timing, which is 3.23 format	Equation : $AA = (1 - e^{-1/(ta*fs)}) \times 2^{23}$ ta = AA/AD/AE timing, fs = sampling rate Ex : ta = 0.1ms, fs = 48K $AA = (1 - e^{-1/(0.0001*48000)}) \times 2^{23} = 1577592$ DEC = 1577592 HEX = 0x181278 <table><tr><th>Threshold</th><th>T_Dec</th><th>T_Hex</th></tr><tr><td>0.1ms</td><td>1577592</td><td>0x181278/0067ED88</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>400ms</td><td>436</td><td>0x0001B4/007FFE4C</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr></table>	Threshold	T_Dec	T_Hex	0.1ms	1577592	0x181278/0067ED88	.	.	.	.	.	.	400ms	436	0x0001B4/007FFE4C	.	.	.	.	.	.
Threshold	T_Dec	T_Hex																				
0.1ms	1577592	0x181278/0067ED88																				
.	.	.																				
.	.	.																				
400ms	436	0x0001B4/007FFE4C																				
.	.	.																				
.	.	.																				
1-AA/1-AE/1-AD Timing	Equation: $1-AA = (0x800000 - AA \text{ timing})$ Ex : If AA = 0x000001B4 $1-AA = (0x800000 - 0x000001B4)$ HEX = 0x007FFE4C $1-AA/1-AD$, must be follow the equations $AA+(1-AA) = 1$, $AD+(1-AD) = 1$ for RMS and peak mode. For peak mode, 1-AE, must be defined by users and there is no limitation. For RMS mode, 1-AE, must be calculated and follow the equation $AE + (1-AE) = 1$.																					

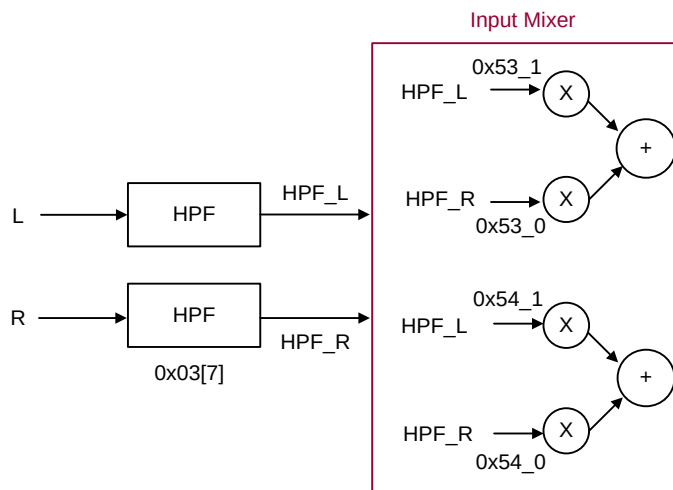
Input Mixer / Pre-Scale / Post-Scale / Output Mixer

Input Mixer, pre-scale and post-scale are also provided by the RT9114C.

Input Mixer

Block Diagram & Description

→ Input mixer range is from mute to 12dB, fixed point design, bit25 is sign bit.



→ MIX_0 is from HPF_R

→ MIX_1 is from HPF_L

Address	BITS	Name	Description
0x53	63:32	CH1_IN_MIX_1	u[31:26],mix_1[25:0] u : Unused
	31:0	CH1_IN_MIX_0	u[31:26],mix_0[25:0] u : Unused
0x54	63:32	CH2_IN_MIX_1	u[31:26],mix_1[25:0] u : Unused
	31:0	CH2_IN_MIX_0	u[31:26],mix_0[25:0] u : Unused

Input / Output / MBDRC Mixer Gain Setting

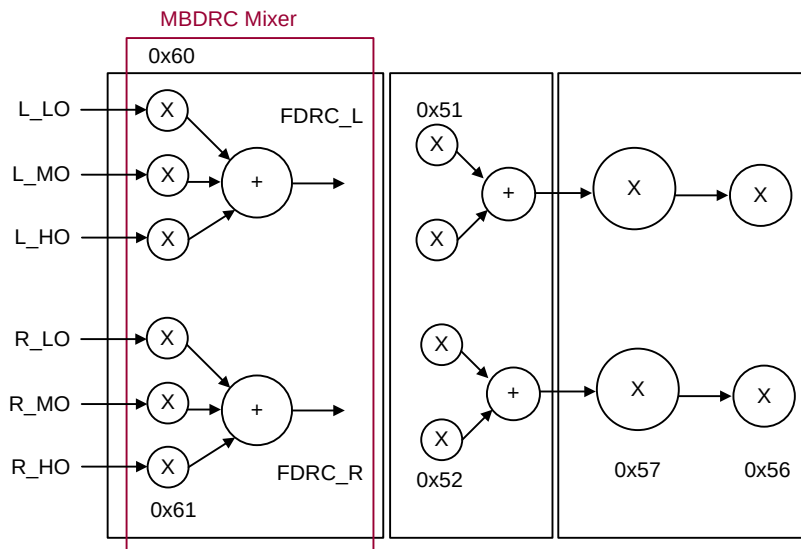
Address	BITS	Name	Equation																											
0x51, 0x52, 0x53, 0x54, 0x60, 0x61	25:0	mix_2[25:0], mix_1[25:0], mix_0[25:0]	Equation : $20\text{Log} (\text{Dec} / 8388608)$ Range : 12dB (0X1ffffff) to Mute (0x00000000) Ex : 6dB, Hex = 0x1000000 Dec = 16777216 Gain = $20\text{Log} (16777216 / 8388608) = 6\text{dB}$ <table><tr><th>Gain</th><th>Dec</th><th>Hex</th></tr><tr><td>12dB</td><td>33554431</td><td>0X1FFFFFFF</td></tr><tr><td>6dB</td><td>16777216</td><td>0X1000000</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>0</td><td>8388608</td><td>0X0800000</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr></table>	Gain	Dec	Hex	12dB	33554431	0X1FFFFFFF	6dB	16777216	0X1000000	.	.	.	.	.	.	0	8388608	0X0800000	.	.	.	.	.	.	.	.	.
Gain	Dec	Hex																												
12dB	33554431	0X1FFFFFFF																												
6dB	16777216	0X1000000																												
.	.	.																												
.	.	.																												
0	8388608	0X0800000																												
.	.	.																												
.	.	.																												
.	.	.																												

Mixer Inverse Phase Setting

Address	BITS	Name	Equation																								
0x51, 0x52, 0x53, 0x54, 0x60, 0x61	25:0	bit25 is sign bit, 3.23 format	Equation : Hex = DEC2HEX Ex : Gain = 6dB, Hex = 0x1000000 Phase Inverse : Hex = DEC2HEX (−16777216) = 0xFF000000																								
			<table><tr><th>Gain</th><th>Dec</th><th>Hex</th></tr><tr><td>12dB</td><td>−33554431</td><td>0XFE000001</td></tr><tr><td>6dB</td><td>−16777216</td><td>0XFF000000</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>0</td><td>−8388608</td><td>0XF800000</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr></table>	Gain	Dec	Hex	12dB	−33554431	0XFE000001	6dB	−16777216	0XFF000000	.	.	.	.	.	.	0	−8388608	0XF800000	.	.	.	.	.	.
			Gain	Dec	Hex																						
			12dB	−33554431	0XFE000001																						
			6dB	−16777216	0XFF000000																						
			.	.	.																						
			.	.	.																						
			0	−8388608	0XF800000																						
.	.	.																									
.	.	.																									

MBDRC Mixer

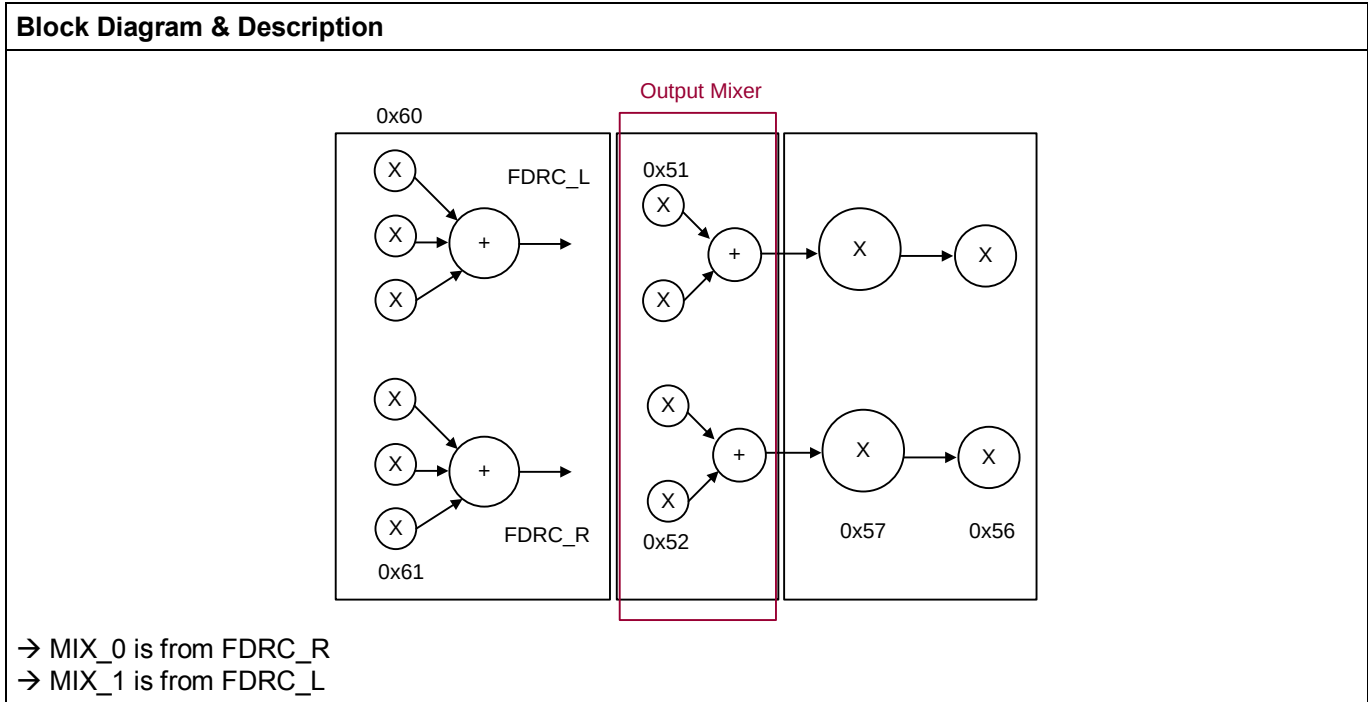
Block Diagram & Description



→ MIX_L is from LO
 → MIX_M is from MO
 → MIX_H is from HO

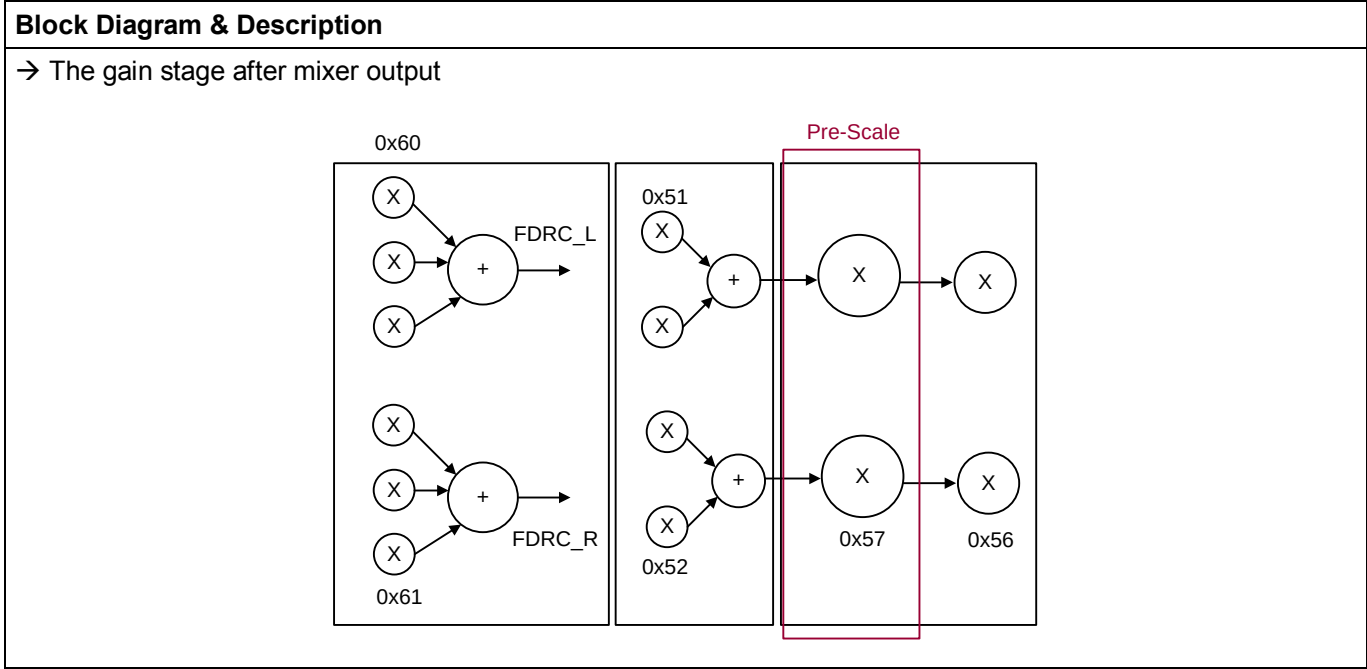
Address	BITS	Name	Description
0x60	95:64	CH1_OUT_MIX_L	u[31:26], mix_2[25:0] u : Unused
	63:32	CH1_OUT_MIX_M	u[31:26], mix_1[25:0] u : Unused
	31:0	CH1_OUT_MIX_H	u[31:26], mix_0[25:0] u : Unused
0x61	95:64	CH2_OUT_MIX_L	u[31:26], mix_2[25:0] u : Unused
	63:32	CH2_OUT_MIX_M	u[31:26], mix_1[25:0] u : Unused
	31:0	CH2_OUT_MIX_H	u[31:26], mix_0[25:0] u : Unused

Output Mixer



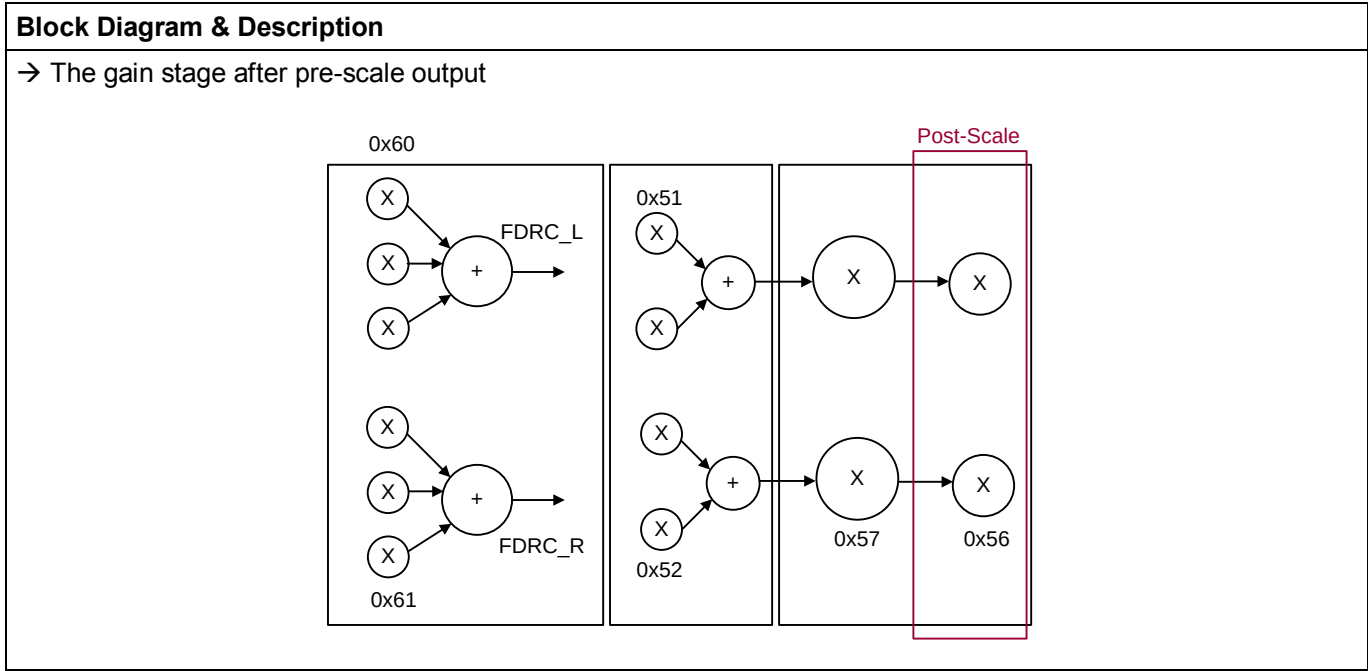
Address	BITS	Name	Description
0x51	63:32	CH1_OUT_MIX_1	u[31:26], mix_1[25:0] u : Unused
	31:0	CH1_OUT_MIX_0	u[31:26], mix_0[25:0] u : Unused
0x52	63:32	CH2_OUT_MIX_1	u[31:26], mix_1[25:0] u : Unused
	31:0	CH2_OUT_MIX_0	u[31:26], mix_0[25:0] u : Unused

Pre-scale



Address	BITS	Name	Description																											
0x57	31:0	PRE_SCALE, u[31:26], pre[25:0], 9.17 format Bit 25 is sign bit	Equation : 20Log (Dec / 131072) Range : 24dB (0X200000) to Mute (0x00000000) Ex : 24dB, Hex = 0x200000 Dec = 2097152 Gain = 20Log (2097152 / 131072) = 24dB <table><tr><th>Gain</th><th>Dec</th><th>Hex</th></tr><tr><td>24dB</td><td>2097152</td><td>0x200000</td></tr><tr><td>20dB</td><td>1310720</td><td>0X140000</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>10dB</td><td>414486</td><td>0x65316</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr></table>	Gain	Dec	Hex	24dB	2097152	0x200000	20dB	1310720	0X140000	.	.	.	.	.	.	10dB	414486	0x65316	.	.	.	.	.	.	.	.	.
Gain	Dec	Hex																												
24dB	2097152	0x200000																												
20dB	1310720	0X140000																												
.	.	.																												
.	.	.																												
10dB	414486	0x65316																												
.	.	.																												
.	.	.																												
.	.	.																												

Post-scale



Address	BITS	Name	Description																					
0x56	31:0	POST_SCALE, 3.23 format, u[31:26], post[25:0] Bit 25 is sign bit	Equation : $20\text{Log}(\text{Dec} / 8388608)$																					
			Range : 12dB (0X01ffffff) to Mute (0x00000000)																					
			Ex : 9.5dB, Hex = 0x01800000																					
			Dec = 25165824																					
			Gain = $20\text{Log}(25165824 / 8388608) = 9.5\text{dB}$																					
			<table><tr><th>Gain</th><th>Dec</th><th>Hex</th></tr><tr><td>12dB</td><td>33554431</td><td>0x01ffffff</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>6dB</td><td>16777216</td><td>0x01000000</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr></table>	Gain	Dec	Hex	12dB	33554431	0x01ffffff	.	.	.	.	.	.	6dB	16777216	0x01000000	.	.	.	.	.	.
			Gain	Dec	Hex																			
			12dB	33554431	0x01ffffff																			
.	.	.																						
.	.	.																						
6dB	16777216	0x01000000																						
.	.	.																						
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Application Information

I²C Bus Specification

The RT9114C supports the I²C protocol via the input ports SCL and SDA. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The RT9114C is always a slave device in all of its communications. It can operate at up to 400kb/s. The RT9114C I²C interface is a slave only interface.

Communication Protocol

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition. START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer. STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between the RT9114C and the bus master. During the data input, the RT9114C samples the SDA signal on the rising edge of clock SCL. For correct device operation, the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

Device Addressing

The RT9114C Support I²C Control interface. The default device address is 0011011 when A_SEL = High or 0011010 when A_SEL = Low. A_SEL will latch from the power on or software reset, then define the address depends on the low, or high.

A_SEL	Device Address
High	0011011
Low	0011010

I²C Write Control

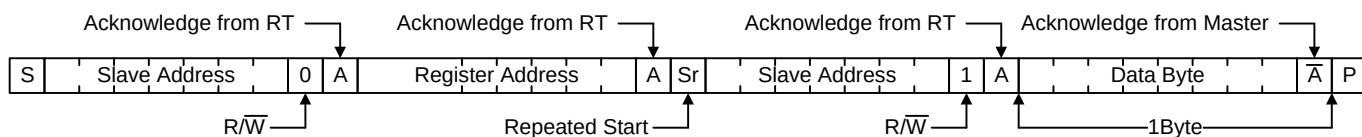
Following the START condition, the master sends a device select code with the RW bit set to 0. The RT9114C acknowledges this and the writes for the byte of internal address. After receiving the internal byte address, the RT9114C again responds with an acknowledgement.

I²C Read Control

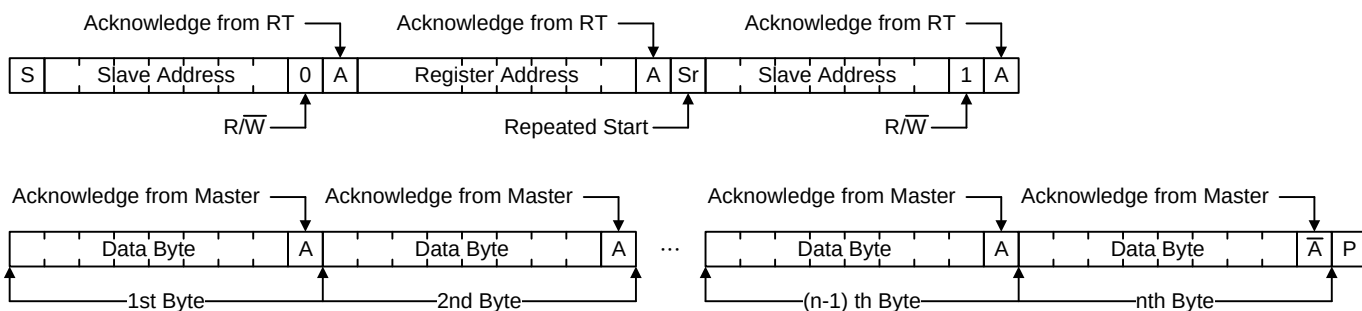
Following the START condition the master sends a device select code with the RW bit set to 1. The RT9114C acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

Read Function

■ Reading One Indexed Byte of Data from RT (With 1-Byte)

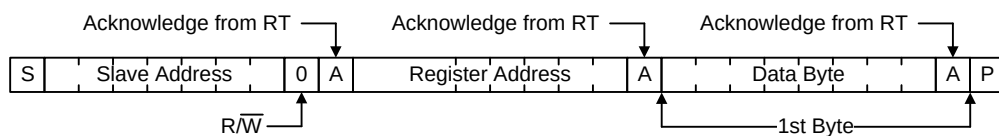


■ Reading n Indexed Words of Data from RT (With N-Byte)

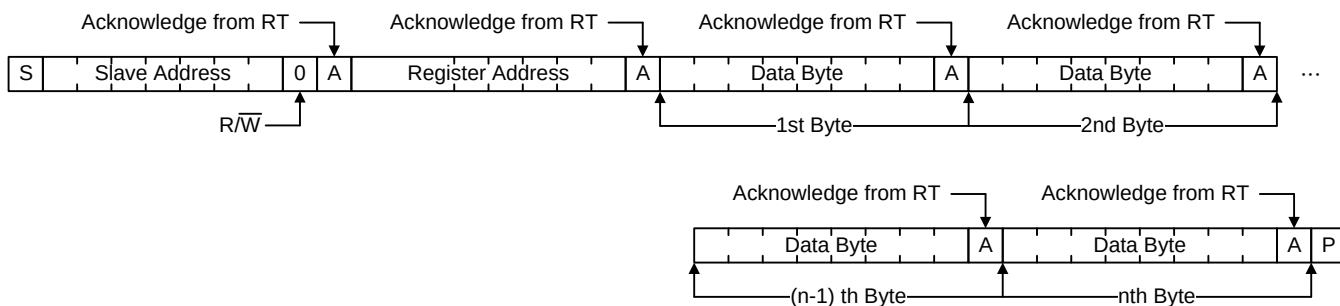


Write Function

■ Writing One Byte of Data to RT (With 1-Byte)

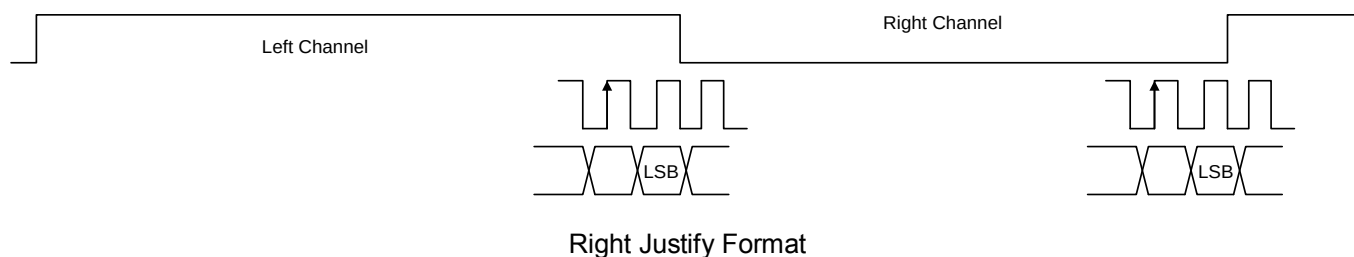
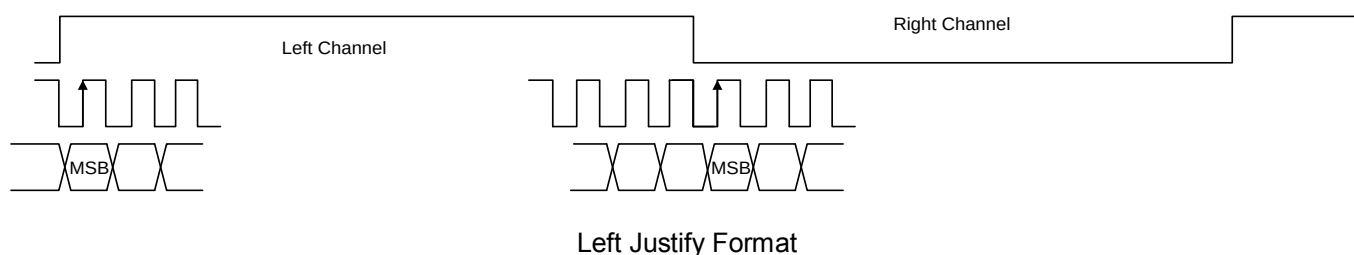
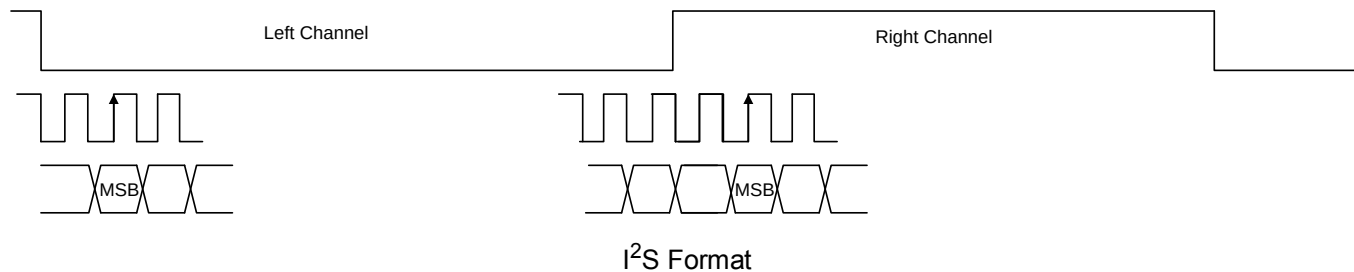


■ Writing n Bytes of Data to RT (With N-Byte)



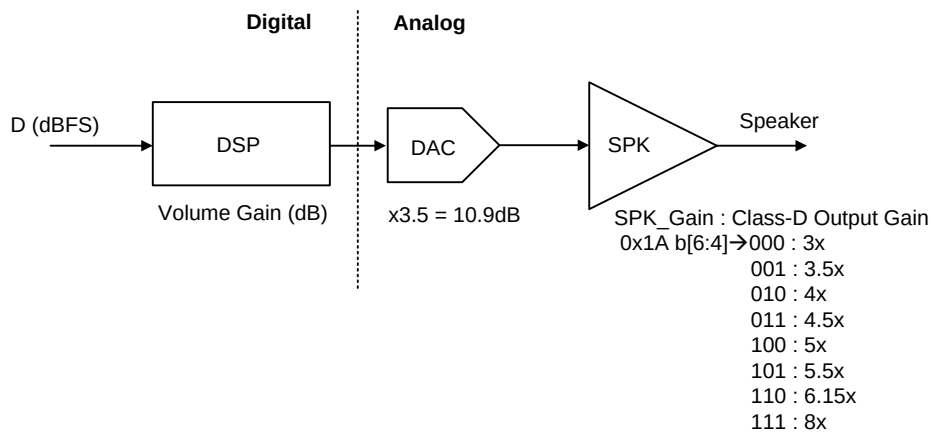
Audio Interface

The RT9114C supports three kinds of audio interface, I²S, Left justify and Right justify. Each kind of interface support 24bits, 20bits, 18bits and 16 bits format and 8~96KHz sampling rate. The timing diagram is shown below.



Address	BITS	Name	Description
0x04	3:0	AUD_MODE	0000 : 16bits Right Justify 0001 : 20bits Right Justify 0010 : 24bits Right Justify 0011 : 16bits I ² S 0100 : 20bits I ² S 0101 : 24bits I ² S 0110 : 16bits Left Justify 0111 : 20bits Left Justify 1000 : 24bits Left Justify Others : No define

Amplification Gain



Output voltage calculation formula = $10^{(D+Vol_Gain)/20} \times 3.5 \times \text{Output_Gain (Vp)}$

Speaker Gain

Address	BITS	Name	Description
0x1A	6:4	D_SPK_GAIN[2:0]	Class-D output gain, 111 = 8x, 110 = 6.15x, 101 = 5.5x, 100 = 5x, 011 = 4.5x, 010 = 4x, 001 = 3.5x, 000 = 3x

Digital gain includes Final gain, Post_IDF gain and Volume gain.

Final Gain

Address	BITS	Name	Description
0xC0	3	Final_Gain	Final gain after hard clip 0: 0dB 1: 6dB

POST_IDF Gain

Address	BITS	Name	Equation																											
0x62	7:0	POST_IDF[7:0]	Equation : 20Log (Dec / 128)																											
			Range : 6dB (0xFF) to Mute (0x00)																											
			Ex : 6dB, Hex = 0xFF																											
			Dec = 255																											
			Gain = $20\text{Log (255 / 128)} = 6\text{dB}$																											
			<table><tr><th>Gain</th><th>Dec</th><th>Hex</th></tr><tr><td>6dB</td><td>255</td><td>0xFF</td></tr><tr><td>5dB</td><td>226</td><td>0XE2</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>0dB</td><td>128</td><td>0x80</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr></table>	Gain	Dec	Hex	6dB	255	0xFF	5dB	226	0XE2	.	.	.	.	.	.	0dB	128	0x80	.	.	.	.	.	.	.	.	.
			Gain	Dec	Hex																									
			6dB	255	0xFF																									
			5dB	226	0XE2																									
.	.	.																												
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0dB	128	0x80																												
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Master Volume Gain

Address	BITS	Name	Equation		
0x07	10:0	MS_VOL[10:0]	Equation : 24dB - (Dec x 0.0625)		
			Range : 24dB (0X000) to mute (0x7ff)		
			Ex : 10dB, Hex = 0xE0		
			Dec = 224		
			Gain = 24dB - (224 x 0.0625) = 10dB		
			Gain	Dec	Hex
			24dB	0	0x00
			10dB	224	0XE0
			.	.	.
0dB	384	0x180			
.	.	.			
.	.	.			
.	.	.			

CH1 Volume Gain

Address	BITS	Name	Equation		
0x08	10:0	CH1_VOL[10:0]	Equation : 24dB - (Dec x 0.0625)		
			Range : 24dB (0X000) to mute (0x7ff)		
			Ex : 10dB, Hex = 0xE0		
			Dec = 224		
			Gain = 24dB - (224 x 0.0625) = 10dB		
			Gain	Dec	Hex
			24dB	0	0x00
			10dB	224	0XE0
			.	.	.
0dB	384	0x180			
.	.	.			
.	.	.			
.	.	.			

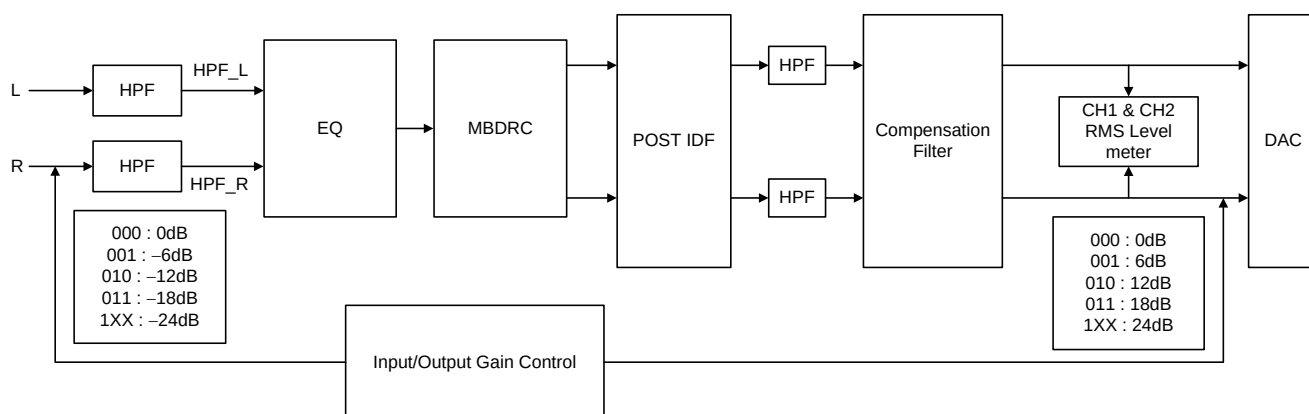
CH2 Volume Gain

Address	BITS	Name	Equation		
0x09	10:0	CH2_VOL[10:0]	Equation : 24dB - (Dec x 0.0625)		
			Range : 24dB (0X000) to mute (0x7ff)		
			Ex : 10dB, Hex = 0xE0		
			Dec = 224		
			Gain = 24dB - (224 x 0.0625) = 10dB		
			Gain	Dec	Hex
			24dB	0	0x00
			10dB	224	0XE0
			.	.	.
0dB	384	0x180			
.	.	.			
.	.	.			
.	.	.			

Input / Output gain Control

Block Diagram & Description

→For increase Dynamic range in signal processing, gain pair control decrease gain in the initial of signal path. (0dB / -6dB / -12dB / -18dB / -24dB), and at the end of signal processing, gain pair control return the decrease gain. (0dB / 6dB / 12dB / 18dB / 24dB)



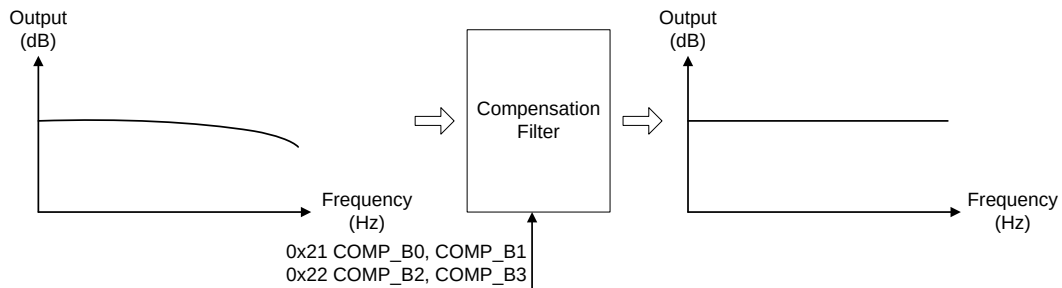
→Below table is to describe the setting to increase dynamic range during signal processing and maximum final output level is 0dB, otherwise it will clip.

GAIN_PAIR_CTRL	Dynamic range during signal processing
0dB / 0dB	24dB
-6dB / 6dB	30dB
-12dB / 12dB	36dB
-18dB / 18dB	42dB
-24dB / 24dB	48dB

Address	BITS	Name	Description
0xC0	2:0	GAIN_PAIR_CTRL	Input decrease and output increase gain control, for increasing DSP dynamic range 000 : 0dB / 0dB 001 : -6dB / 6dB 010 : -12dB / 12dB 011 : -18dB / 18dB Others : -24dB / 24dB

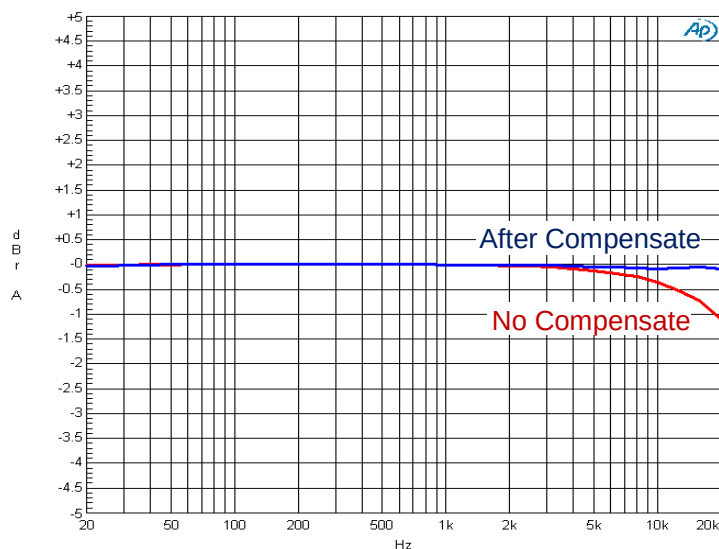
Compensate Filter

Compensation filter is purpose to compensate internal gain from DAC, this filter can also compensate the frequency response affected by LC filter, recommended setting will based on different application circuit to fit the curve.



Compensate Description	Equation
Compensate	$y[n] = B3 \cdot x[n-6] + B2 \cdot x[n-5] + B1 \cdot x[n-4] + B0 \cdot x[n-3] + B1 \cdot x[n-2] + B2 \cdot x[n-1] + B3 \cdot x[n]$ - B0, B1, B2, B3 : Compensate coefficient - N : Input signal when applied

Address	BITS	Name	Description
0x03	4	COMP_EN	1 : Compensation filter enable 0 : Compensation filter disable
0x21	31:16	COMP_B0[15:0]	Compensate B0, B1 coefficient
	15:11	Reserved	
	10:0	COMP_B1[10:0]	
0x22	31:8	Reserved	Compensate B2, B3 coefficient
	26:16	COMP_B2[10:0]	
	15:9	Reserved	
	8:0	COMP_B3[8:0]	



Volume Ramp

000 : 1 step in every sample

001 : mute → -40dB, every sample with 1 step. -40dB → 24dB, 2 sample with 1 step.

010 : mute → -40dB, 2 sample with 1 step. -40dB → 24dB, 4 sample with 1 step.

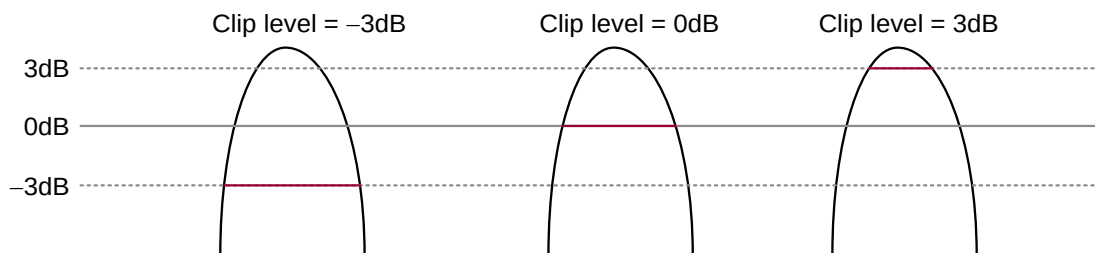
Others : mute → -40dB, 4 sample with 1 step. -40dB → 24dB, 8 sample with 1 step.

Note : 1 step = 0.0625dB, 1 sample period = 1/Fs.

Address	BITS	Name	Description
0x0C	2:0	VOL_RAMP_MODE[2:0]	000 : 1 step in every sample 001 : mute → -40dB, every sample with 1 step. -40dB → 24dB, 2 sample with 1 step. 010 : mute → -40dB, 2 sample with 1 step. -40dB → 24dB, 4 sample with 1 step. Others : mute → -40dB, 4 sample with 1 step. -40dB → 24dB, 8 sample with 1 step.

Hard Clip Function

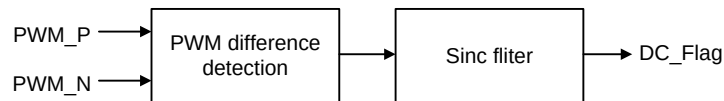
To clip the signal with different threshold, operate in time domain.



Address	BITS	Name	Description
0x62	31	HARD_CLIP_EN	1 : Enable hard clip 0 : Disable hard clip
	30	FINAL_HARD_CLIP_EN	1 : Enable final hard clip 0 : Disable final hard clip
	18:8	HARD_CLIP_TH[10:0]	Hard Clip Threshold for Hard clip & Final Hard clip 11'h000 : 24dB 11'h180 : 0dB 0.0625db per step

DC Protection Function

It is to use to protect the loudspeaker, when there are some DC exists at the output. The method is to detect DC at final stage (PWM), calculate the difference of the PWM and a sinc filter to decide the DC level. The IC will shut down when detect the DC.



Address	BITS	Name	Description
0x76	7	DC_FLAG	DC Flag report 1 : DC happen
	6	Reserved	
	5:4	DC_TH[1:0]	DC threshold for DC detection 00 : No available 01 : 12.5% 10 : 18.75% 11 : 25%
	2	DC_FREQ_SEL	Select clock frequency for DC detection 0 : Prohibited 1 : 384K
	1	DC_TIME_SEL	Detection time 0 : 342ms 1 : 684ms
	0	DC_EN	0 : DC Protection disable 1 : DC protection enable

PBTL Function

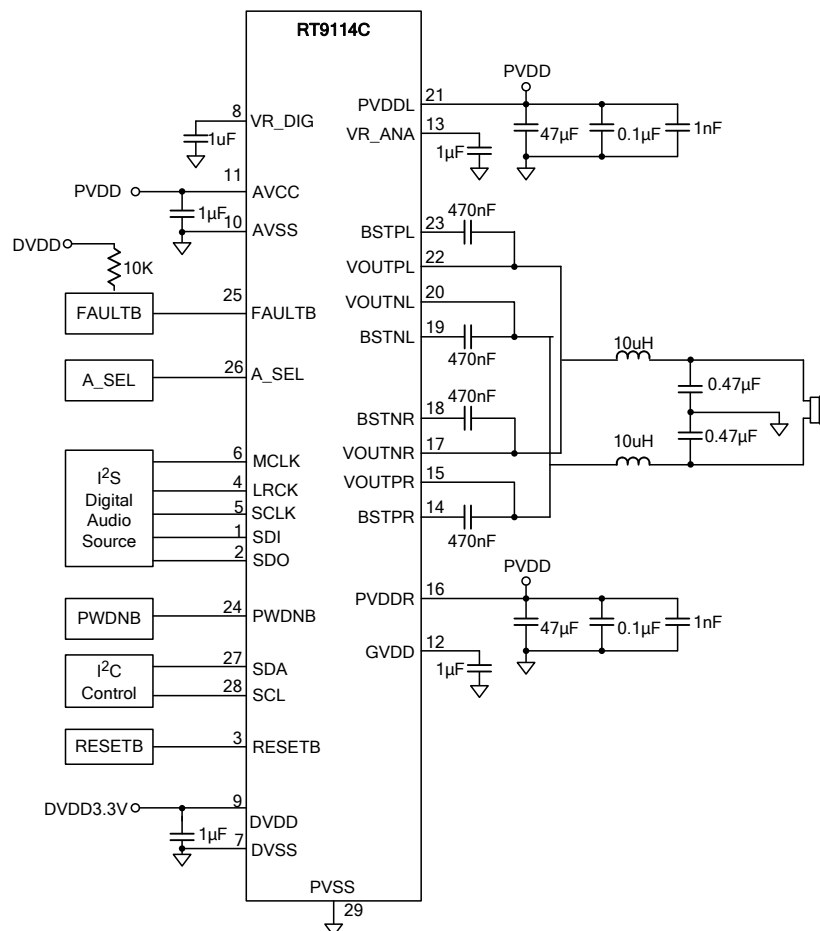
It can be configure by the hardware, also need to change the software setting of register 0x84 B[2].

The Input signal, can be configured by the input mixer of register 0x53.

Address	BITS	Name	Description
0x84	7:3	Reserved	
	2	D_PBTL	0 : BTL, 1 : PBTL
	1:0	D_NOISE_AMP[1:0]	Nosie amplitude for SSC 00 = 5kHz 01 = 10kHz 10 = 15kHz 11 = 20kHz

Address	BITS	Name	Description
0x53	63:32	CH1_IN_MIX_1	u[31:26], mix_1[25:0] u : Unused
	31:0	CH1_IN_MIX_0	u[31:26], mix_0[25:0] u : Unused

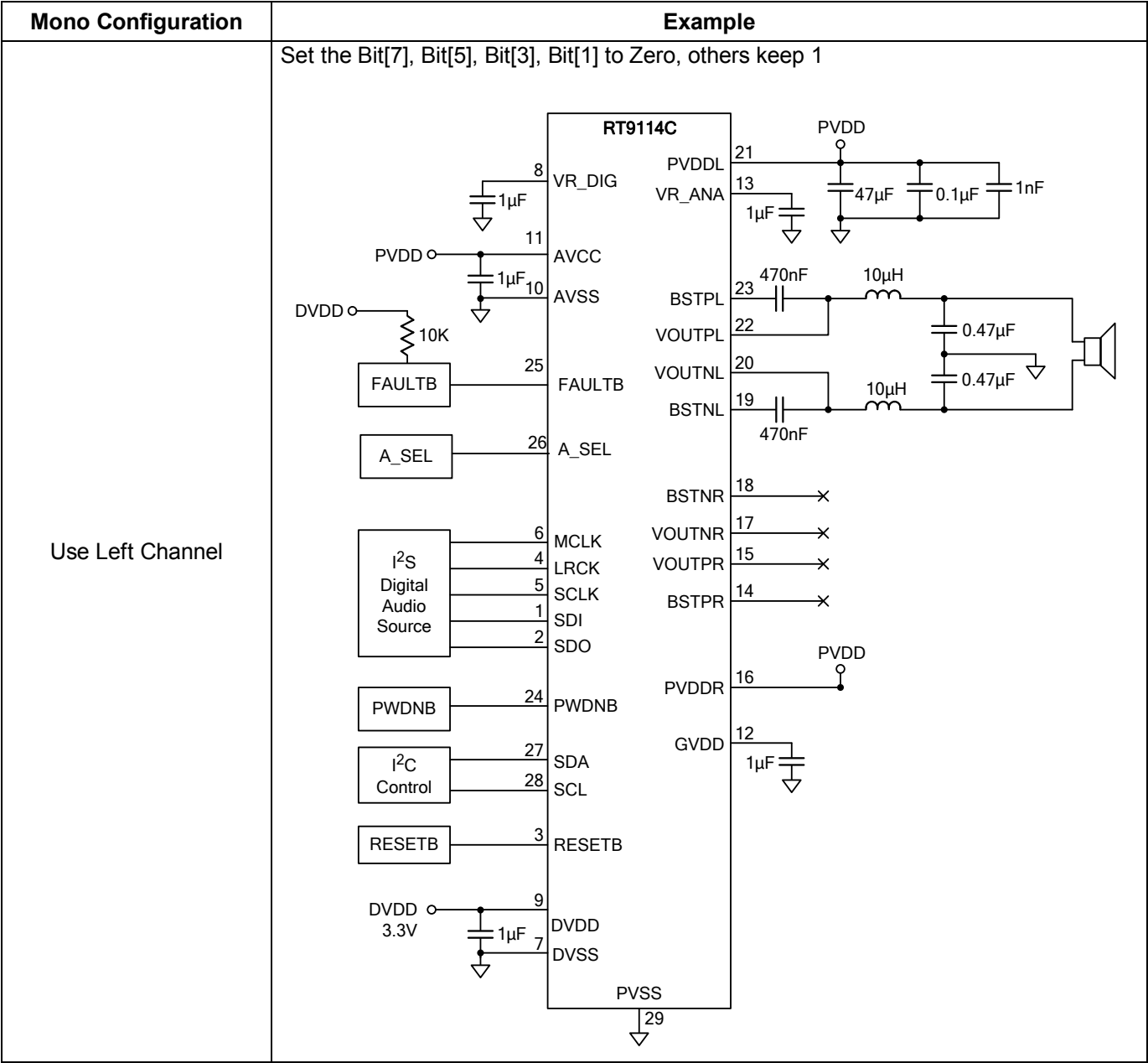
Mono PBTL Application Circuit

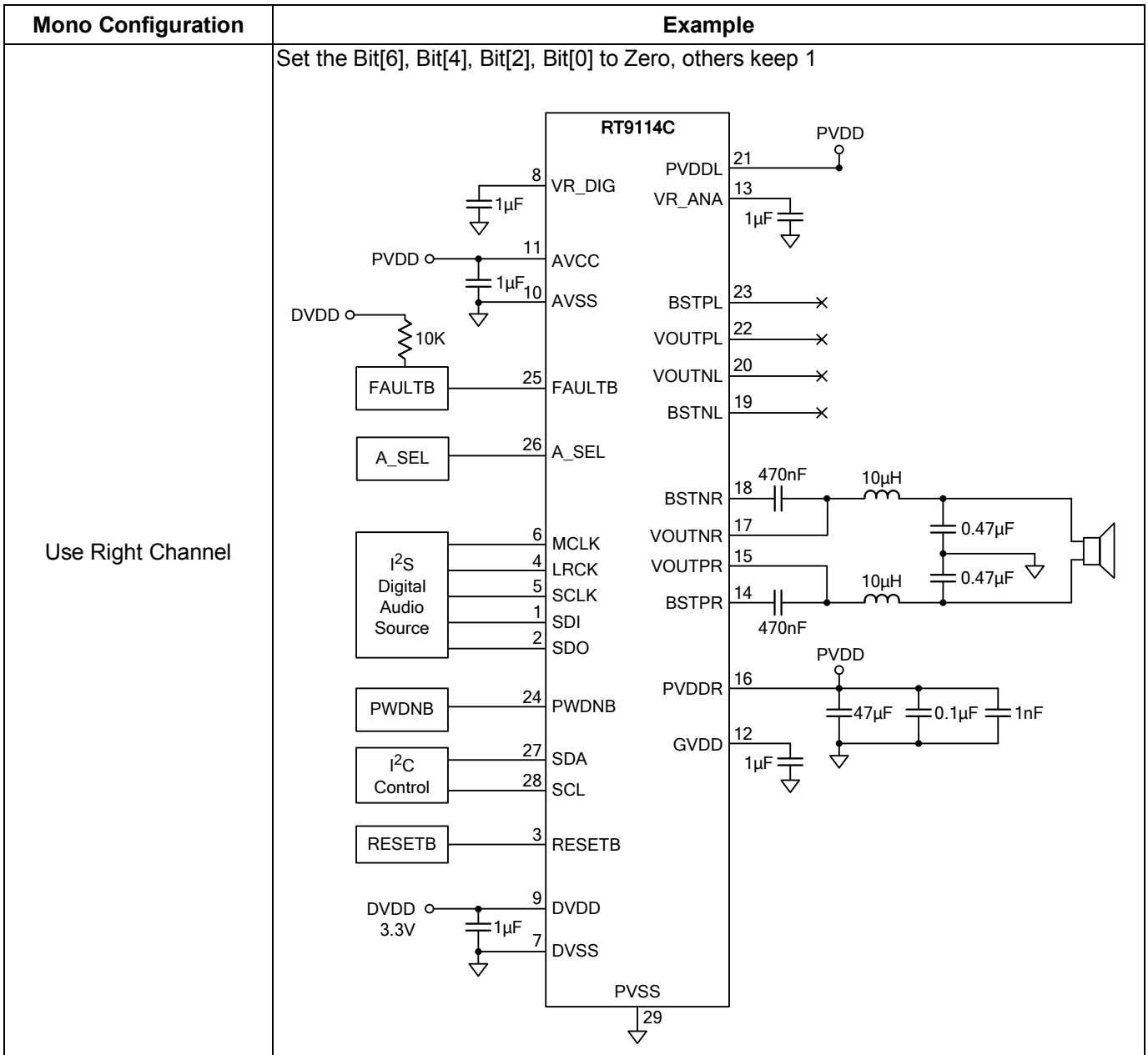


Mono Configuration

To use the mono configuration, It can be configured by register setting.

Address	BITS	Name	Description
0x14	7	D_LPFR_EN	Enable DAC RCH LPF, 0 : Disable, 1 : Enable
	6	D_LPFL_EN	Enable DAC LCH LPF, 0 : Disable, 1 : enable
	5	D_EN_RCH_PWR	RCH PWR stage enable, 0 : Disable, 1 : Enable
	4	D_EN_LCH_PWR	LCH PWR stage enable, 0 : Disable, 1 : Enable
	3	D_DAC_RCH_EN	Enable DAC_RCH, 0 : Disable, 1 : Enable
	2	D_DAC_LCH_EN	Enable DAC LCH, 0 : Disable, 1 : enable
	1	D_SPK_RCH_EN	Enable Class-D RCH SPK, 0 : Disable, 1 : Enable
	0	D_SPK_LCH_EN	Enable Class-D LCH SPK, 0 : Disable, 1 : Enable





Reference Clock Selection

Due to the coefficient of PLL can be automated selected, so the RT9114C can choose the MCLK/SCLK as the reference clock from register setting.

Address	Reference Clock	Example
0x70	MCLK	To choose the reference clock Bit[0] to 0 : Reference clock is MCLK
	SCLK	To choose the reference clock Bit[0] to 1 : Reference clock is SCLK

Protection Behavior

If the protection behavior happened, the IC will automated detect, there are some behavior as below list.

Protection	Auto recovery	Shutdown Amp	Fault pin pull low
DC Protection	No	Yes	Yes
MCLK ERROR	Depends on 0xD1 bit[6]	Yes	Yes, depends on 0xD0 bit[6]
SCLK ERROR	Depends on 0xD1 bit[5]	Yes	Yes, depends on 0xD0 bit[5]
LRCK ERROR	Depends on 0xD1 bit[4]	Yes	Yes, depends on 0xD0 bit[4]
OC ERROR	Depends on 0xD1 bit[3]	Yes	Yes, depends on 0xD0 bit[3]
OV ERROR	Depends on 0xD1 bit[2]	Yes	Yes, depends on 0xD0 bit[2]
OT ERROR	Depends on 0xD1 bit[1]	Yes	Yes, depends on 0xD0 bit[1]
UV ERROR	Depends on 0xD1 bit[0]	Yes	Yes, depends on 0xD0 bit[0]

Address	BITS	Name	Description
0xD0	6	MCLK_ERROR_mask	1 : Fault mask for 0x2 MCLK error 0 : No mask
	5	SCLK_ERROR_mask	1 : Fault mask for 0x2 SCLK error 0 : No mask
	4	LRCK_ERROR_mask	1 : Fault mask for 0x2 LRCK error 0 : No mask
	3	OC_ERROR_mask	1 : Fault mask for 0x71 OC error 0 : No mask
	2	OV_ERROR_mask	1 : Fault mask for 0x71 OV error 0 : No mask
	1	OT_ERROR_mask	1 : Fault mask for 0x71 OT error 0 : No mask
	0	UV_ERROR_mask	1 : Fault mask for 0x71 UV error 0 : No mask

Note : When mask enable, the error will report to FAULTB pin once the ERROR occurs.

Fault Behavior Type Select

If the protection behavior happened, the IC will automate detect, there are some error type can be configured as below list.

Note : if the fault behavior is set as latch, the RT9114C will recovery after initialization again.

Address	BITS	Name	Description
0xD1	6	MCLK_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch
	5	SCLK_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch
	4	LRCK_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch
	3	OC_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery (Don't set to 0, it will cause IC damage when OC fault happen.) 1 : Latch
	2	OV_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch
	1	OT_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch
	0	UV_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch

Register Map

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x00	1	I2S_FMT_RPT	7:5	R/W	SR_MODE[2:0]	Sampling rate report 000 : 32kHz 001 : Reserved 010 : 88.2/96kHz 011 : 44.1/48kHz 100 : 16kHz 101 : 22.05/24kHz 110 : 8kHz 111 : 11.025/12kHz	3'b011
			4:2	R/W	CK_MODE[2:0]	Clock mode report 000 : MCLK = 64fs 001 : MCLK = 128fs 010 : MCLK = 192fs 011 : MCLK = 256fs 100 : MCLK = 384fs 101 : MCLK = 512fs Others : Reserved	3'b011
			1:0	R/W	BCK_MODE[1:0]	BCK mode report 00 : BCK = 32fs 01 : BCK = 48fs 10 : BCK = 64fs Others : Reserved	2'b10
0x01	1	DEV_ID	7:0	R	DEVICE_ID[7:0]		8'h10
0x02	1	ERR_RPT1	7	R	MCLK_ERR	1: MCLK Error	1'b0
			6		Reserved		1'b0
			5	R	SCLK_ERR	1: SCLK error	1'b0
			4	R	LRCK_ERR	1: LRCK clock error	1'b0
			3		Reserved		1'b0
			2		Reserved		1'b0
			1		Reserved		1'b0
			0		Reserved		1'b0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x03	1	FLTR_MISC	7	R/W	HPF_EN	1 : High-pass filter enable 0 : High-pass filter disable	1'b1
			6	R/W	HPF_POS_EN	1 : Post high pass filter enable 0 : Post high pass filter disable	1'b0
			5		Reserved		1'b0
			4	R/W	COMP_EN	1 : Compensation filter enable 0 : Compensation filter disable	1'b0
			3	R/W	SR_MODE_SEL	0 : Auto detect enable 1 : Auto detect disable	1'b0
			2:1		Reserved		2'b00
			0	R/W	N/A	Prohibited	1'b0
0x04	1	I2S_FMT	7:4		Reserved		4'b0000
			3:0	R/W	AUD_MODE	0000 : 16 bits right justify 0001 : 20 bits right justify 0010 : 24 bits right justify 0011 : 16 bits I ² S 0100 : 20 bits I ² S 0101 : 24 bits I ² S 0110 : 16 bits left justify 0111 : 20 bits left justify 1000 : 24 bits left justify Others : No define	4'b0101
0x05	1	ENABLE	7		Reserved		1'b0
			6	R/W	SHUTDOWN	1 : Shutdown 0 : Amp enable	1'b1
			5:4		Reserved		2'b00
			3	R/W	N/A	Prohibited	1'b0
			2	R/W	N/A	Prohibited	1'b0
			1	R/W	N/A	Prohibited	1'b0
			0	R/W	N/A	Prohibited	1'b0
0x06	1	CH_MUTE	7:4		Reserved		4'b0000
			3	R/W	N/A	Prohibited	1'b0
			2		Reserved		1'b0
			1	R/W	CH2_MUTE	1 : CH2 soft mute 0 : CH2 non soft mute	1'b0
			0	R/W	CH1_MUTE	1 : CH1 soft mute 0 : CH1 non soft mute	1'b0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x07	2	MS_VOL	10:0	R/W	MS_VOL[10:0]	Master Volume control 11'h000 : 24dB 11'h180 : 0dB 11'h7FF : mute 0.0625dB per step	11'h7FF
0x08	2	CH1_VOL	10:0	R/W	CH1_VOL[10:0]	CH1 Volume control 11'h000 : 24dB 11'h180 : 0dB 11'h7FF : mute 0.0625dB per step	11'h180
0x09	2	CH2_VOL	10:0	R/W	CH2_VOL[10:0]	CH2 Volume control 11'h000 : 24dB 11'h180 : 0dB 11'h7FF : mute 0.0625dB per step	11'h180
0x0A	1	DRC4_DELAY	7:0	R/W	DRC4_DELAY[7:0]	→The delay make the audio signal output delay →Delay = (DRC4_DELAY) * 1 / sample rate →This maximum value is 0x8F, if the setting is larger than 0x8F, it will limit at 0x8F	8'hFF
0x0C	1	VOL_RAMP	7:6	R/W	N/A	Prohibited	2'b00
			5:4	R/W	N/A	Prohibited	2'b00
			3	R/W	SKIP_RAMP	0 : Enable volume ramp 1 : Disable	1'b0
			2:0	R/W	VOL_RAMP_MODE [2:0]	Volume slew step control 000 : 1 step in every sample 001 : mute→-40dB, every sample with 1 step. -40dB→24dB, 2 sample with 1 step. 010 : mute→-40dB, 2 sample with 1 step. -40dB→24dB, 4 sample with 1 step. Others : mute→-40dB, 4 sample with 1 step. -40dB→24dB, 8 sample with 1 step.	3'b001
0x0D	1	SDIN_SEL	7:4		Reserved		4'b0000
			3:2	R/W	CH1_SI[1:0]	00 : SDIN-L to CH1 01 : SDIN-R to CH1 1X : No data to CH1	2'b00
			1:0	R/W	CH2_SI[1:0]	00 : SDIN-L to CH2 01 : SDIN-R to CH2 1X : No data to CH2	2'b01

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x0E	1	AUTO_RCVRY	7		Reserved		1'b0
			6	R	D_UVP_PVDD_FLAG	0 : normal operation 1 : PVDD UV flag	1'b0
			5	R	D_UVP_3P3_FLAG	0 : normal operation 1 : DVDD3P3 UV flag	1'b0
			4		Reserved		1'b0
			3:0	R/W	BKD_TIME[3:0]	Power stage auto recovery time 0000 : 107ms 0010 : 299ms 0011 : 449ms 0100 : 598ms 0101 : 748ms 1000 : 1197ms 1001 : 1346ms 101X & 11XX : 1496ms	4'b0010
0x0F	1	ERR_RPT2	7	R	D_OCP_FLAG	0 : Normal operation 1 : OCP error flag	1'b0
			6	R	D_OVP_FLAG	0 : Normal operation 1 : OVP error flag	1'b0
			5	R	D_OTP_FLAG	0 : Normal operation 1 : OTP error flag	1'b0
			4	R	D_UVP_FLAG	0 : Normal operation 1 : UVP error flag	1'b0
			3:0	R	N/A	Prohibited	4'b0000
0x11	1	DAC_OPT1	7:6	R/W	N/A	Prohibited	2'b10
			5:4	R/W	N/A	Prohibited	2'b10
			3	R/W	N/A	Prohibited	1'b1
			2	R/W	N/A	Prohibited	1'b0
			1	R/W	N/A	Prohibited	1'b0
			0	R/W	N/A	Prohibited	1'b1
0x12	1	CLASS_D_OPT1	7:6	R/W	N/A	Prohibited	2'b11
			5	R/W	N/A	Prohibited	1'b0
			4	R/W	N/A	Prohibited	1'b1
			3	R/W	N/A	Prohibited	1'b1
			2	R/W	N/A	Prohibited	1'b0
			1:0		Reserved		2'b0
0x13	1	TEST_MODE	7:6	R/W	N/A	Prohibited	2'b00
			5:4	R/W	N/A	Prohibited	2'b00
			3	R/W	N/A	Prohibited	1'b0
			2	R/W	N/A	Prohibited	1'b0
			1	R/W	N/A	Prohibited	1'b1
			0	R/W	N/A	Prohibited	1'b0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x14	1	INTER_PWR_CTRL	7	R/W	D_LPFR_EN	Enable DAC RCH LPF, 0 : Disable 1 : Enable	1'b1
			6	R/W	D_LPFL_EN	Enable DAC LCH LPF, 0 : Disable 1 : Enable	1'b1
			5	R/W	D_EN_RCH_PWR	RCH PWR stage enable 0 : Disable 1 : Enable	1'b1
			4	R/W	D_EN_LCH_PWR	LCH PWR stage enable 0 : Disable 1 : Enable	1'b1
			3	R/W	D_DAC_RCH_EN	Enable DAC_RCH, 0 : Disable 1 : Enable	1'b1
			2	R/W	D_DAC_LCH_EN	Enable DAC LCH, 0 : Disable 1 : Enable	1'b1
			1	R/W	D_SPK_RCH_EN	Enable ClassD RCH SPK, 0 : Disable 1 : Enable	1'b1
			0	R/W	D_SPK_LCH_EN	Enable ClassD LCH SPK, 0 : Disable 1 : Enable	1'b1
0x15	1	OFFSET_CAL1	7	R/W	N/A	Prohibited	1'b0
			6	R/W	N/A	Prohibited	1'b1
			5	R/W	N/A	Prohibited	1'b0
			4	R/W	N/A	Prohibited	1'b0
			3	R/W	N/A	Prohibited	1'b0
			2	R/W	N/A	Prohibited	1'b0
			1	R/W	N/A	Prohibited	1'b1
			0	R/W	N/A	Prohibited	1'b0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x16	1	PWM_SS_OPT1	6	R/W	PWM_MODEWHITE	Noise select, 0 = pink noise, 1 = white noise	1'b0
			5	R/W	PWM_SELCOEF	Pink noise coefficient, 0 = 1/2 1 = 1/4 This will affect the noise amplitude for spread spectrum signal, not recommended to modify it.	1'b0
			4	R/W	PWM_NOISE_EN	Add noise to TRI_GEN, 0 = Disable 1 = Enable	1'b0
			3:2	R/W	N/A	Prohibited	2'b01
			1:0	R/W	N/A	Prohibited	2'b10
0x17	1	ANA_BIAS1	7:6	R/W	N/A	Prohibited	2'b10
			5:4	R/W	N/A	Prohibited	2'b10
			3:2	R/W	N/A	Prohibited	2'b10
			1	R/W	N/A	Prohibited	1'b0
			0	R/W	N/A	Prohibited	1'b0
0x18	1	OC_TEST_MODE	7	R/W	N/A	Prohibited	1'b0
			6	R/W	N/A	Prohibited	1'b0
			5	R/W	N/A	Prohibited	1'b0
			4	R/W	N/A	Prohibited	1'b0
			3:2	R/W	N/A	Prohibited	2'b00
			1:0	R/W	N/A	Prohibited	2'b11
0x19	1	PWM_SS_OPT2	7:6	R/W	D_FSS_AMP[1:0]	Spread spectrum frequency variation amplitude 00 = 20kHz 01 = 10 = 40kHz 11 = 60kHz	2'b01
			5:4	R/W	N/A	Prohibited	2'b01
			3:1	R/W	N/A	Prohibited	3'b010
			0	R/W	D_FSS_EN	Spread spectrum enable, 0 = Disable 1 = Enable	1'b0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x1A	1	SPK_GAIN	7		Reserved		1'b0
			6:4	R/W	D_SPK_GAIN[2:0]	Class-D output gain 111 = 8x 110 = 6.15x 101 = 5.5x 100 = 5x 011 = 4.5x 010 = 4x 001 = 3.5x 000 = 3x	3'b011
			3	R/W	N/A	Prohibited	1'b0
			2	R/W	N/A	Prohibited	1'b0
			1:0	R/W	N/A	Prohibited	2'b01
0x1B	1	PLL_CONFIG1	7:4	R/W	N/A	Prohibited	4'b1010
			3	R/W	N/A	Prohibited	1'b0
			2	R/W	N/A	Prohibited	1'b1
			1	R/W	N/A	Prohibited	1'b0
			0	R/W	N/A	Prohibited	1'b0
0x1C	1	PLL_CONFIG2	7:3	R/W	N/A	Prohibited	5'b00000
			2:0	R/W	N/A	Prohibited	3'b000
0x1D	1	PLL_CONFIG3	7:4	R/W	N/A	Prohibited	4'b0000
			3:2	R/W	N/A	Prohibited	2'b00
			1:0	R/W	N/A	Prohibited	2'b00
0x1E	1	PLL_CONFIG4	7:6		Reserved		2'b00
			5:4	R/W	N/A	Prohibited	2'b01
			3	R/W	N/A	Prohibited	1'b1
			2	R/W	N/A	Prohibited	1'b1
			1:0	R/W	N/A	Prohibited	2'b00
0x20	4	PLL_CONFIG5	31	R	N/A	Prohibited	1'b1
			30:28	R	N/A	Prohibited	3'b0
			27	R	N/A	Prohibited	1'b1
			26:23		Reserved		4'b0000
			22:16	R/W	N/A	Prohibited	7'b0001000
			15:0	R/W	N/A	Prohibited	16'h0000
0x21	4	COMP_FLTR1	31:16	R/W	COMP_B0[15:0]	Compensation filter B0 coefficient	16'h4000
			15:11		Reserved		5'b00000
			10:0	R/W	COMP_B1[10:0]	Compensation filter B1 coefficient	11'h000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x22	4	COMP_FLTR2	31:27		Reserved		5'b00000
			26:16	R/W	COMP_B2[10:0]	Compensation filter B2 coefficient	11'h000
			15:9		Reserved		7'b0000000
			8:0	R/W	COMP_B3[8:0]	Compensation filter B3 coefficient	9'h000
0x26	20	CH1_BQ1	159:128	R/W	CH1_bq_1_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH1_bq_1_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH1_bq_1_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH1_bq_1_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH1_bq_1_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x27	20	CH1_BQ2	159:128	R/W	CH1_bq_2_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH1_bq_2_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH1_bq_2_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH1_bq_2_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH1_bq_2_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x28	20	CH1_BQ3	159:128	R/W	CH1_bq_3_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH1_bq_3_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH1_bq_3_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH1_bq_3_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH1_bq_3_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x29	20	CH1_BQ4	159:128	R/W	CH1_bq_4_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH1_bq_4_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH1_bq_4_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH1_bq_4_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH1_bq_4_a2	u[31:26], a2[25:0] u : Unused	32'h00000000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x2A	20	CH1_BQ5	159:128	R/W	CH1_bq_5_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH1_bq_5_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH1_bq_5_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH1_bq_5_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH1_bq_5_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x2B	20	CH1_BQ6	159:128	R/W	CH1_bq_6_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH1_bq_6_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH1_bq_6_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH1_bq_6_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH1_bq_6_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x2C	20	CH1_BQ7	159:128	R/W	CH1_bq_7_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH1_bq_7_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH1_bq_7_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH1_bq_7_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH1_bq_7_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x2D	20	CH1_BQ8	159:128	R/W	CH1_bq_8_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH1_bq_8_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH1_bq_8_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH1_bq_8_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH1_bq_8_a2	u[31:26], a2[25:0] u : Unused	32'h00000000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x2E	20	CH1_BQ9	159:128	R/W	CH1_bq_9_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH1_bq_9_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH1_bq_9_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH1_bq_9_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH1_bq_9_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x2F	20	CH1_BQ10	159:128	R/W	CH1_bq_10_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH1_bq_10_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH1_bq_10_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH1_bq_10_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH1_bq_10_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x30	20	CH2_BQ1	159:128	R/W	CH2_bq_1_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH2_bq_1_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH2_bq_1_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH2_bq_1_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH2_bq_1_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x31	20	CH2_BQ2	159:128	R/W	CH2_bq_2_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH2_bq_2_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH2_bq_2_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH2_bq_2_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH2_bq_2_a2	u[31:26], a2[25:0] u : Unused	32'h00000000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x32	20	CH2_BQ3	159:128	R/W	CH2_bq_3_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH2_bq_3_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH2_bq_3_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH2_bq_3_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH2_bq_3_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x33	20	CH2_BQ4	159:128	R/W	CH2_bq_4_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH2_bq_4_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH2_bq_4_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH2_bq_4_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH2_bq_4_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x34	20	CH2_BQ5	159:128	R/W	CH2_bq_5_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH2_bq_5_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH2_bq_5_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH2_bq_5_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH2_bq_5_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x35	20	CH2_BQ6	159:128	R/W	CH2_bq_6_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH2_bq_6_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH2_bq_6_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH2_bq_6_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH2_bq_6_a2	u[31:26], a2[25:0] u : Unused	32'h00000000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x36	20	CH2_BQ7	159:128	R/W	CH2_bq_7_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH2_bq_7_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH2_bq_7_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH2_bq_7_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH2_bq_7_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x37	20	CH2_BQ8	159:128	R/W	CH2_bq_8_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH2_bq_8_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH2_bq_8_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH2_bq_8_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH2_bq_8_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x38	20	CH2_BQ9	159:128	R/W	CH2_bq_9_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH2_bq_9_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH2_bq_9_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH2_bq_9_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH2_bq_9_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x39	20	CH2_BQ10	159:128	R/W	CH2_bq_10_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH2_bq_10_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH2_bq_10_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH2_bq_10_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH2_bq_10_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x3A	8	DRC1_RMS_AE	63:32	R/W	DRC1 RMS AE	u[31:26], ae[25:0] u : Unused	32'h00800000
			31:0	R/W	DRC1 RMS 1-AE	u[31:26], (1-ae)[25:0] u : Unused	32'h00000000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x3B	8	DRC1_GAIN_AA	63:32	R/W	DRC1 GAIN AA	u[31:26], aa[25:0] u : Unused	32'h00800000
			31:0	R/W	DRC1 GAIN 1-AA	u[31:26], (1-aa)[25:0] u : Unused	32'h00000000
0x3C	8	DRC1_GAIN_AD	63:32	R/W	DRC1 GAIN AD	u[31:26], ad[25:0] u : Unused	32'h00800000
			31:0	R/W	DRC1 GAIN 1-AD	u[31:26], (1-ad)[25:0] u : Unused	32'h00000000
0x3D	8	DRC2_RMS_AE	63:32	R/W	DRC2 RMS AE	u[31:26], ae[25:0] u : Unused	32'h00800000
			31:0	R/W	DRC2 RMS 1-AE	u[31:26], (1-ae)[25:0] u : Unused	32'h00000000
0x3E	8	DRC2_GAIN_AA	63:32	R/W	DRC2 GAIN AA	u[31:26], aa[25:0] u : Unused	32'h00800000
			31:0	R/W	DRC2 GAIN 1-AA	u[31:26], (1-aa)[25:0] u : Unused	32'h00000000
0x3F	8	DRC2_GAIN_AD	63:32	R/W	DRC2 GAIN AD	u[31:26], ad[25:0] u : Unused	32'h00800000
			31:0	R/W	DRC2 GAIN 1-AD	u[31:26], (1-ad)[25:0] u : Unused	32'h00000000
0x40	4	DRC1_TH	31:0	R/W	DRC1_T[31:0]	T1[31:0]	32'hFDA21490
0x41	4	DRC1_RATIO	31:0	R/W	DRC1_K[31:0]	u[31:26], K1[25:0] u : Unused	32'h03842109
0x42	4	DRC1_OFFSET	31:0	R/W	DRC1_O[31:0]	u[31:26], O1[25:0] u : Unused	32'h00081385
0x43	4	DRC2_TH	31:0	R/W	DRC2_T[31:0]	T2[31:0]	32'hFDA21490
0x44	4	DRC2_RATIO	31:0	R/W	DRC2_K[31:0]	u[31:26], K2[25:0] u : Unused	32'h03842109
0x45	4	DRC2_OFFSET	31:0	R/W	DRC2_O[31:0]	u[31:26], O2[25:0] u : Unused	32'h00081385

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x46	4	EQ_DRC_EN	[31:8]	R/W	EQ_BYPASS[23:0]	EQ bypass control → This function is bypass the EQ setting	24'h000000
			7		Reserved		1'b0
			6	R/W	DRC_EQ_LINK	0 : DRC EQ L/R Can be written independently → Adjust separated channel DRC EQ. 1 : L and R are ganged for EQ bi-quads; a write to left-channel BQ is also written to right-channel BQ. (0x5C, 0x5D is ganged to 0x5E, 0x5F. Also 0x78, 0x79 is ganged to 0x7A, 0x7B, 0x7C is ganged to 0x7E) → When link, two channel DRC EQ will be the same.	1'b0
			5	R/W	EQ_LINK	0 : L/R can be written independently → Adjust separated channel EQ. 1 : L and R are ganged for EQ bi-quads; a write to left-channel BQ is also written to right-channel BQ. (0x26 – 0x2F is ganged to 0x30 – 0x39. Also 0x58 – 0x59 is ganged to 0x5A – 0x5B) → When link, two channel EQ will be the same.	1'b0
			4	R/W	EQ_DISABLE	1 : EQ disable 0 : EQ Enable	1'b0
			3	R/W	DRC4_ON	DRC4 enable 1 : Enable → Final Stage DRC enable (DRC4) 0 : Disable, → When disable, input signal is the same as output signal.	1'b0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x46	4	EQ_DRC_EN	2	R/W	DRC3_ON	DRC3 enable 1 : Enable → DRC 3 enable (High band) 0 : Disable → When disable, input signal is the same as output signal.	1'b0
			1	R/W	DRC2_ON	DRC2 enable 1 : Enable → DRC 2 enable (Middle band) 0 : Disable → When disable, input signal is the same as output signal.	1'b0
			0	R/W	DRC1_ON	DRC1 enable 1 : Enable → DRC 1 enable (Low band) 0 : Disable → When disable, input signal is the same as output signal.	1'b0
0x47	8	DRC3_RMS_AE	[63:32]	R/W	DRC3 RMS AE	u[31:26], ae[25:0] u : Unused	32'h00800000
			[31:0]	R/W	DRC3 RMS 1-AE	u[31:26], (1-ae)[25:0] u : Unused	32'h00000000
0x48	8	DRC3_GAIN_AA	[63:32]	R/W	DRC3 GAIN AA	u[31:26], aa[25:0] u : Unused	32'h00800000
			[31:0]	R/W	DRC3 GAIN 1-AA	u[31:26], (1-aa)[25:0] u : Unused	32'h00000000
0x49	8	DRC3_GAIN_AD	[63:32]	R/W	DRC3 GAIN AD	u[31:26], ad[25:0] u : Unused	32'h00800000
			[31:0]	R/W	DRC3 GAIN 1-AD	u[31:26], (1-ad)[25:0] u : Unused	32'h00000000
0x4A	4	DRC3_TH	[31:0]	R/W	DRC3_T	T3[31:0]	32'hFDA21490
0x4B	4	DRC3_RATIO	[31:0]	R/W	DRC3_K	u[31:26], K3[25:0] u : Unused	32'h03842109
0x4C	4	DRC3_OFFSET	[31:0]	R/W	DRC3_O	u[31:26], O3[25:0] u : Unused	32'h00081385
0x51	8	CH1_OUT_MIX	63:32	R/W	CH1_OUT_MIX_1	u[31:26], mix_1[25:0] u : Unused	32'h00800000
			31:0	R/W	CH1_OUT_MIX_0	u[31:26], mix_0[25:0] u : Unused	32'h00000000
0x52	8	CH2_OUT_MIX	63:32	R/W	CH2_OUT_MIX_1	u[31:26], mix_1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH2_OUT_MIX_0	u[31:26], mix_0[25:0] u : Unused	32'h00800000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x53	8	CH1_IN_MIX	63:32	R/W	CH1_IN_MIX_1	u[31:26], mix_1[25:0] u : Unused	32'h00800000
			31:0	R/W	CH1_IN_MIX_0	u[31:26], mix_0[25:0] u : Unused	32'h00000000
0x54	8	CH2_IN_MIX	63:32	R/W	CH2_IN_MIX_1	u[31:26], mix_1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH2_IN_MIX_0	u[31:26], mix_0[25:0] u : Unused	32'h00800000
0x56	4	POST_SCALE	31:0	R/W	POST_SCALE	u[31:26], post[25:0], 3.23 format u : Unused	32'h00800000
0x57	4	PRE_SCALE	31:0	R/W	PRE_SCALE	u[31:26], pre[25:0], 9.17 format u : Unused	32'h00020000
0x58	20	CH1_BQ11	159:128	R/W	CH1_bq_11_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH1_bq_11_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH1_bq_11_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH1_bq_11_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH1_bq_11_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x59	20	CH1_BQ12	159:128	R/W	CH1_bq_12_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH1_bq_12_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH1_bq_12_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH1_bq_12_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH1_bq_12_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x5A	20	CH2_BQ11	159:128	R/W	CH2_bq_11_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH2_bq_11_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH2_bq_11_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH2_bq_11_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH2_bq_11_a2	u[31:26], a2[25:0] u : Unused	32'h00000000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x5B	20	CH2_BQ12	159:128	R/W	CH2_bq_12_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	CH2_bq_12_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	CH2_bq_12_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	CH2_bq_12_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	CH2_bq_12_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x5C	20	LB_CH1_BQ1	159:128	R/W	LB_CH1_bq_1_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	LB_CH1_bq_1_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	LB_CH1_bq_1_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	LB_CH1_bq_1_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	LB_CH1_bq_1_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x5D	20	LB_CH1_BQ2	159:128	R/W	LB_CH1_bq_2_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	LB_CH1_bq_2_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	LB_CH1_bq_2_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	LB_CH1_bq_2_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	LB_CH1_bq_2_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x5E	20	LB_CH2_BQ1	159:128	R/W	LB_CH2_bq_1_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	LB_CH2_bq_1_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	LB_CH2_bq_1_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	LB_CH2_bq_1_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	LB_CH2_bq_1_a2	u[31:26], a2[25:0] u : Unused	32'h00000000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x5F	20	LB_CH2_BQ2	159:128	R/W	LB_CH2_bq_2_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	LB_CH2_bq_2_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	LB_CH2_bq_2_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	LB_CH2_bq_2_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	LB_CH2_bq_2_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x60	12	CH1_MBDRC_MIX	95:64	R/W	CH1_OUT_MIX_L	u[31:26], mix_2[25:0] u : Unused	32'h00800000
			63:32	R/W	CH1_OUT_MIX_M	u[31:26], mix_1[25:0] u : Unused	32'h00800000
			31:0	R/W	CH1_OUT_MIX_H	u[31:26], mix_0[25:0] u : Unused	32'h00800000
0x61	12	CH2_MBDRC_MIX	95:64	R/W	CH2_OUT_MIX_L	u[31:26], mix_2[25:0] u : Unused	32'h00800000
			63:32	R/W	CH2_OUT_MIX_M	u[31:26], mix_1[25:0] u : Unused	32'h00800000
			31:0	R/W	CH2_OUT_MIX_H	u[31:26], mix_0[25:0] u : Unused	32'h00800000
0x62	4	HARD_CLIP	31	R/W	N/A	Prohibited	1'b0
			30	R/W	FINAL_HARD_CLIP_EN	1 : Enable final hard clip 0 : Disable final hard clip	1'b0
			29:19		Reserved		11'h000
			18:8	R/W	HARD_CLIP_TH [10:0]	Hard clip threshold for Hard clip & Final Hard clip 11'h000 : 24dB 11'h180 : 0dB 0.0625dB per step	11'h180
			7:0	R/W	POST_IDF	u[31:8], POST_IDF[7:0] u : Unused	8'h80

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x70	1	DRC_CK_MODE	7	R/W	DRC4_PEAK	1 : Peak mode 0 : RMS mode	1'b1
			6	R/W	DRC3_PEAK	1 : Peak mode 0 : RMS mode	1'b1
			5	R/W	DRC2_PEAK	1 : Peak mode 0 : RMS mode	1'b1
			4	R/W	DRC1_PEAK	1 : Peak mode 0 : RMS mode	1'b1
			3		Reserved		1'b0
			2	R/W	dSR_DIV_SEL	0 : Auto parameter for PLL 1 : According to 0x20 setting, auto parameter is recommended	1'b0
			1	R/W	MS_EN	1 : Master mode 0 : Slave mode	1'b0
			0	R/W	dREF_SEL	0 : MCLK 1 : SCLK ps : if Master mode, PLL always reference MCLK	1'b1
0x71	1	ERR_LATCH	7:4		Reserved		4'b0000
			3	R/W	OC_ERROR	1 : OC, write 0 to clear flag	1'b0
			2	R/W	OV_ERROR	1 : OV, write 0 to clear flag	1'b0
			1	R/W	OT_ERROR	1 : OT, write 0 to clear flag	1'b0
			0	R/W	UV_ERROR	1 : UV, write 0 to clear flag	1'b0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x72	1	DRC_ENABLE	7	R/W	DRC4_N_EN	1 : DRC4 Noise gate enable 0 : DRC4 Noise gate disable	1'b0
			6	R/W	DRC3_N_EN	1 : DRC3 Noise gate enable 0 : DRC3 Noise gate disable	1'b0
			5	R/W	DRC2_N_EN	1 : DRC2 Noise gate enable 0 : DRC2 Noise gate disable	1'b0
			4	R/W	DRC1_N_EN	1 : DRC1 Noise gate enable 0 : DRC1 Noise gate disable	1'b0
			3	R/W	MB_BYPASS	0 : Normal mode 1 : ByPass →When bypass, the output signal is 0	1'b0
			2	R/W	LB_BYPASS	0 : Normal mode 1 : ByPass →When bypass, the output signal is 0	1'b0
			1	R/W	HB_BYPASS	0 : Normal mode 1 : ByPass → When bypass, the output signal is 0	1'b0
			0	R/W	FREQ_DRC_MODE	0 : High band only 1 : Frequency DRC Mode	1'b0
0x73	1	SDO_SEL	7	R/W	N/A	Prohibited	1'b1
			6:4	R/W	SDO_SEL[2:0]	001 : EQ output 010 : DRC/Mixer/Gain output 011 : Final output 100 : RMS output Other : No output	3'b000
			3:2		N/A	Prohibited	2'b11
			1:0	R/W	EQ_LINK[1:0]	Link select @ REG_46 bit 5 = 1 00 : Link ALL 01 : Link 2A to 2D and 34 to 37 10 : Link 2E to 2F and 38 to 39 & Link 58 to 59 and 5A to 5B 11 : Prohibited	2'b00

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x74	1	OC_LEVEL	7:6	R/W	N/A	Prohibited	2'b01
			5:4	R/W	N/A	Prohibited	2'b01
			3:2	R/W	N/A	Prohibited	2'b01
			1:0	R/W	N/A	Prohibited	2'b01
0x75	1	UVP_AD	7	R/W	N/A	Prohibited	1'b0
			6	R/W	N/A	Prohibited	1'b0
			5	R/W	N/A	Prohibited	1'b0
			4	R/W	N/A	Prohibited	1'b0
			3:2	R/W	N/A	Prohibited	2'b00
			1:0	R/W	N/A	Prohibited	2'b00
0x76	1	DC_PROT	7	R	DC_FLAG	DC Flag report 1 : DC happen	1'b0
			6		Reserved		1'b0
			5:4	R/W	DC_TH[1:0]	DC threshold for DC detection 00 : No available 01 : 12.5% 10 : 18.75% 11 : 25%	2'b10
			3	R/W	N/A	Prohibited	1'b0
			2	R/W	DC_FREQ_SEL	Select clock frequency for DC detection 0 : Prohibited 1 : 384k	1'b1
			1	R/W	DC_TIME_SEL	Detection time 0 : 342ms 1 : 684ms	1'b0
			0	R/W	DC_EN	1 : DC protection enable 0 : DC protection disable	1'b0
0x77	1	EQ_GAIN_BOOST1	7:4	R/W	EQ_L_GAIN_BOOST_9_12	Control L channel bq9_bq12 gain boost	4'b0000
			3:0	R/W	EQ_R_GAIN_BOOST_9_12	Control R channel bq9_bq12 gain boost	4'b0000
0x78	20	MB_CH1_BQ1	159:128	R/W	MB_CH1_bq_1_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	MB_CH1_bq_1_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	MB_CH1_bq_1_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	MB_CH1_bq_1_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	MB_CH1_bq_1_a2	u[31:26], a2[25:0] u : Unused	32'h00000000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x79	20	MB_CH1_BQ2	159:128	R/W	MB_CH1_bq_2_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	MB_CH1_bq_2_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	MB_CH1_bq_2_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	MB_CH1_bq_2_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	MB_CH1_bq_2_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x7A	20	MB_CH2_BQ1	159:128	R/W	MB_CH2_bq_1_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	MB_CH2_bq_1_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	MB_CH2_bq_1_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	MB_CH2_bq_1_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	MB_CH2_bq_1_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x7B	20	MB_CH2_BQ2	159:128	R/W	MB_CH2_bq_2_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	MB_CH2_bq_2_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	MB_CH2_bq_2_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	MB_CH2_bq_2_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	MB_CH2_bq_2_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x7C	20	HB_CH1_BQ1	159:128	R/W	HB_CH1_bq_1_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	HB_CH1_bq_1_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	HB_CH1_bq_1_b2	u[31:26], b2[25:0] u : Unused	32'h00000000
			63:32	R/W	HB_CH1_bq_1_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	HB_CH1_bq_1_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x7E	20	HB_CH2_BQ1	159:128	R/W	HB_CH2_bq_1_b0	u[31:26], b0[25:0] u : Unused	32'h00800000
			127:96	R/W	HB_CH2_bq_1_b1	u[31:26], b1[25:0] u : Unused	32'h00000000
			95:64	R/W	HB_CH2_bq_1_b2	u[31:26], b2[25:0] u : Unused	32'h00000000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
			63:32	R/W	HB_CH2_bq_1_a1	u[31:26], a1[25:0] u : Unused	32'h00000000
			31:0	R/W	HB_CH2_bq_1_a2	u[31:26], a2[25:0] u : Unused	32'h00000000
0x80	1	SW_RESET	7	W	SF_RESET	Write 1 to trigger software reset → Reset the whole chip to default value, need to wait 10ms for reset completion	1'b0
			6:0		Reserved		7'b00000000
0x81	1	PAD_DRV	7	R/W	N/A	Prohibited	1'b0
			6	R/W	N/A	Prohibited	1'b0
			5:4	R/W	N/A	Prohibited	2'b10
			3		Reserved		1'b0
			2	R/W	N/A	Prohibited	1'b1
			1:0	R/W	N/A	Prohibited	2'b00
0x82	1	SDM_OPT	7	R/W	N/A	Prohibited	1'b0
			6	R/W	N/A	Prohibited	1'b0
			5	R/W	N/A	Prohibited	1'b1
			4	R/W	N/A	Prohibited	1'b1
			3:2	R/W	N/A	Prohibited	2'b10
			1:0	R/W	N/A	Prohibited	2'b01
0x83	1	CK_TEST_MODE	7:4	R/W	N/A	Prohibited	4'b0000
			3	R/W	N/A	Prohibited	1'b0
			2	R/W	N/A	Prohibited	1'b0
			1	R/W	DIS_A_SEL_PU	Disable A_SEL pin internal pull up 1 : Disable 0 : Enable	1'b0
			0	R/W	N/A	Prohibited	1'b0
0x84	1	PBTL & SS_OPT3	7	R/W	N/A	Prohibited	1'b1
			6		Reserved		1'b0
			5	R/W	N/A	Prohibited	1'b0
			4	R/W	N/A	Prohibited	1'b1
			3	R/W	N/A	Prohibited	1'b0
			2	R/W	D_PBTL	0 : BTL 1 : PBTL	1'b0
			1:0	R/W	D_NOISE_AMP[1:0]	Noise amplitude for SSC 00 = 5kHz 01 = 10kHz 10 = 15kHz 11 = 20kHz	2'b00

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x85	1	OFFSET_CAL1_L	7:0	R/W	N/A	Prohibited	8'b01000000
0x86	1	OFFSET_CAL1_R	7:0	R/W	N/A	Prohibited	8'b01000000
0x87	1	OFFSET_RPT1_L	7:0	R	N/A	Prohibited	8'b01000000
0x88	1	OFFSET_RPT1_R	7:0	R	N/A	Prohibited	8'b01000000
0x89	1	OFFSET_RPT2_L	7:0	R	N/A	Prohibited	8'b01000000
0x8A	1	OFFSET_RPT2_R	7:0	R	N/A	Prohibited	8'b01000000
0x8D	1	BIST_RPT	4:0	R	N/A	Prohibited	5'b00000
0x8E	1	BIST_EN	7:4		Reserved		4'b0
			3	R	N/A	Prohibited	1'b0
			2	R	N/A	Prohibited	1'b0
			1	R	N/A	Prohibited	1'b0
			0	R/W	N/A	Prohibited	1'b0
0x8F	1	SCAN_MODE	7:0	R/W	N/A	Prohibited	8'b0
0xA2	4	DRC_NG_TH	31:0	R/W	DRC_N_T[31:0]	N_T[31:0] → DRC Noise Gate Threshold	32'hF5B3B7C6
0xA6	4	DRC4_TH	31:0	R/W	DRC4_T[31:0]	T[31:0]	32'hFDA21490
0xA7	4	DRC4_RATIO	31:0	R/W	DRC4_K[25:0]	u[31:26], K4[25:0] u : Unused	32'h03842109
0xA8	4	DRC4_OFFSET	31:0	R/W	DRC4_O[25:0]	u[31:26], O4[25:0] u : Unused	32'h00081385
0xAC	8	DRC4_AE	63:0	R/W	DRC4 RMS AE[25:0]	u[31:26], ae[25:0] u : Unused	32'h00800000
			31:0	R/W	DRC4 RMS 1-AE[25:0]	u[31:26], (1-ae)[25:0] u : Unused	32'h00000000
0xAD	8	DRC4_AA	63:0	R/W	DRC4 GAIN AA[25:0]	u[31:26], aa[25:0] u : Unused	32'h00800000
			31:0	R/W	DRC4 GAIN 1-AA[25:0]	u[31:26], (1-aa)[25:0] u : Unused	32'h00000000
0xAE	8	DRC4_AD	63:0	R/W	DRC4 GAIN AD[25:0]	u[31:26], ad[25:0] u : Unused	32'h00800000
			31:0	R/W	DRC4 GAIN 1-AD[25:0]	u[31:26], (1-ad)[25:0] u : Unused	32'h00000000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xAF	8	OUT_LEVEL_A	63:0	R/W	PWM_LEVEL RMS AE[25:0]	u[31:26], rms[25:0] u : Unused	32'h00800000
			31:0	R/W	PWM_LEVEL RMS 1-AE[25:0]	u[31:26], (1-rms)[25:0] u : Unused →Formula is the same as AE /1 - AE, need to follow the AE + 1 - AE = 1 for both RMS and peak mode	32'h00000000
0xC0	1	GAIN_OPT	7:4		Reserved		4'b0000
			3	R/W	Final_Gain	Final gain after Hard clip 0 : 0dB 1 : 6dB	1'b0
			2:0	R/W	GAIN_PAIR_CTRL	input decrease and output increase gain control, for increase DSP dynamic range 000 : 0dB/0dB 001 : -6dB/6dB 010 : -12dB/12dB 011 : -18dB/18dB Others : -24dB/24dB	3'b000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xC1	1	SKIP_BQ1	7	R/W	SKIP_BQ1_L_MBAND	(register 0x78) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped	1'b0
			6	R/W	SKIP_BQ2_L_MBAND	(register 0x79) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped	1'b0
			5	R/W	SKIP_BQ1_R_MBAND	(register 0x7A) 0: Coefficients applied to 2 identical BQ stages 1: Coefficients applied to 1 stage only, 1 is skipped	1'b0
			4	R/W	SKIP_BQ2_R_MBAND	(register 0x7B) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped	1'b0
			3	R/W	SKIP_BQ1_L_HBAND	(register 0x7C) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped	1'b0
			2	R/W	SKIP_BQ1_R_HBAND	(register 0x7E) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped	1'b0
			1	R/W	SKIP_BQ1_L_LBAND	(register 0x5C) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped	1'b0
			0	R/W	SKIP_BQ1_R_LBAND	(register 0x5E) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped	1'b0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xC2	1	SKIP_BQ2	7:5		Reserved		3'b000
			4	R/W	SKIP_DRC_L_HPF	L_HPF for MB and HB DRC 0 : Normal mode 1 : SKIP	1'b0
			3	R/W	SKIP_DRC_H_LPF	H_LPF for MB DRC 0 : Normal mode 1 : SKIP	1'b0
			2	R/W	SKIP_DRC_H_HPF	H_HPF for HB DRC 0 : Normal Mode 1 : SKIP	1'b0
			1	R/W	SKIP_DRC_L_LPF	L_LPF for LB DRC 0 : Normal mode 1 : SKIP	1'b0
			0	R/W	SKIP_DRC_APB	APB for LB DRC 0 : Normal mode 1 : SKIP	1'b0
0xC3	1	EQ_L_GAIN_BOOST	7:0	R/W	EQ_L_GAIN_BOOST_1_8	Control L channel bq1_bq8 gain boost	8'b00000000
0xC4	1	EQ_R_GAIN_BOOST	7:0	R/W	EQ_R_GAIN_BOOST_1_8	Control R channel bq1_bq8 gain boost	8'b00000000
0xC5	1	DF_GAIN	7:2		Reserved		5'b000000
			1	R/W	N/A	Prohibited	1'b0
			0	R/W	N/A	Prohibited	1'b0
0xD0	1	ERR_MASK	7		Reserved		1'b0
			6	R/W	MCLK_ERROR_mask	1 : Fault mask for 0x2 MCLK error, don't report to FAULTB pin 0 : No mask, report to FAULTB pin	1'b1
			5	R/W	SCLK_ERROR_mask	1 : Fault mask for 0x2 SCLK error 0 : No mask	1'b1
			4	R/W	LRCK_ERROR_mask	1 : Fault mask for 0x2 LRCK error 0 : No mask	1'b1
			3	R/W	OC_ERROR_mask	1 : Fault mask for 0x71 OC error 0 : No mask	1'b0
			2	R/W	OV_ERROR_mask	1 : Fault mask for 0x71 OV error 0 : No mask	1'b0
			1	R/W	OT_ERROR_mask	1 : Fault mask for 0x71 OT error 0 : No mask	1'b0
			0	R/W	UV_ERROR_mask	1 : Fault mask for 0x71 UV error 0 : No mask	1'b0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xD1	1	ERR_TYPE	7		Reserved		1'b0
			6	R/W	MCLK_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch	1'b0
			5	R/W	SCLK_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch	1'b0
			4	R/W	LRCK_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch	1'b0
			3	R/W	OC_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch	1'b0
			2	R/W	OV_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch	1'b0
			1	R/W	OT_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch	1'b0
			0	R/W	UV_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch	1'b0
0xF0	1	DIG_TEST1	7:0	R/W	N/A	Prohibited	8'b00000000
0xF1	1	DIG_TEST2	7:0	R	N/A	Prohibited	8'b00000000
0xF2	1	DIG_TEST3	7:0	R/W	N/A	Prohibited	8'b00000000
0xF3	1	DIG_TEST4	7	R	N/A	Prohibited	1'b0
			6:2		Reserved		5'b00000
			1	R/W	N/A	Prohibited	1'b0
			0	R/W	N/A	Prohibited	1'b0
0xF4	1	DIG_TEST5	7:4		N/A	Prohibited	4'b0000
			3	R/W	N/A	Prohibited	1'b0
			2:0	R/W	N/A	Prohibited	3'b100

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a VQFN-28L 4x5 package, the thermal resistance, θ_{JA} , is 27.4°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below :

$$P_{D(MAX)} = (150^\circ\text{C} - 25^\circ\text{C}) / (27.4^\circ\text{C/W}) = 4.56\text{W for a VQFN-28L 4x5 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curves in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

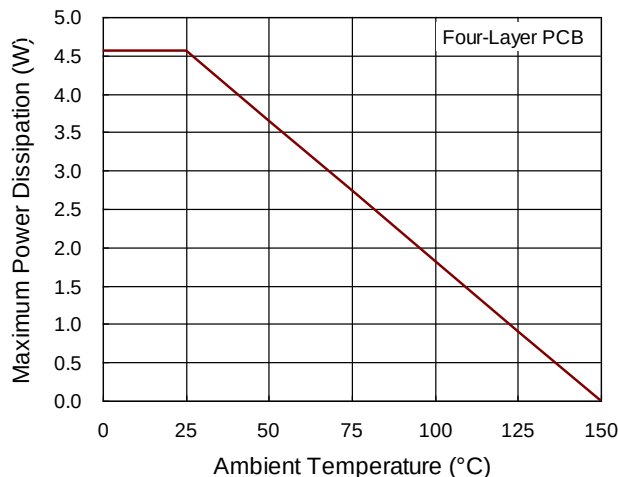
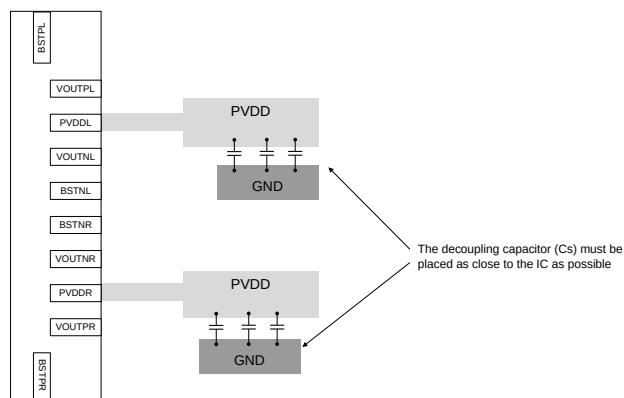


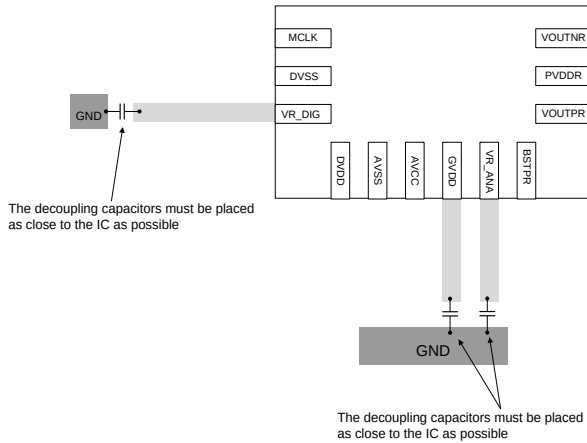
Figure 5. Derating Curve of Maximum Power Dissipation

Layout Guide

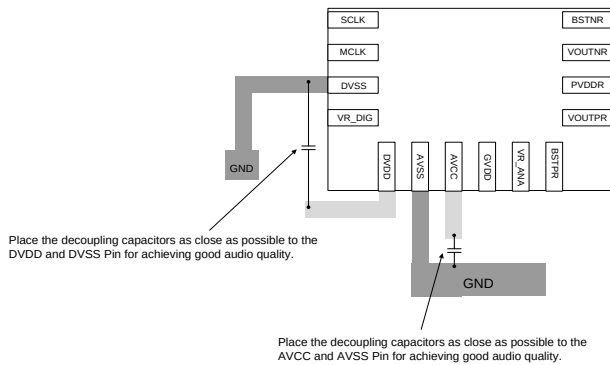
- Place the decoupling capacitors as close as possible to the PVCC and GND, then use shortest trace to link these capacitors, and use more vias for GND link to GND layer to reduce parasitic inductance and resistance. The trace width is 30 mil at least.



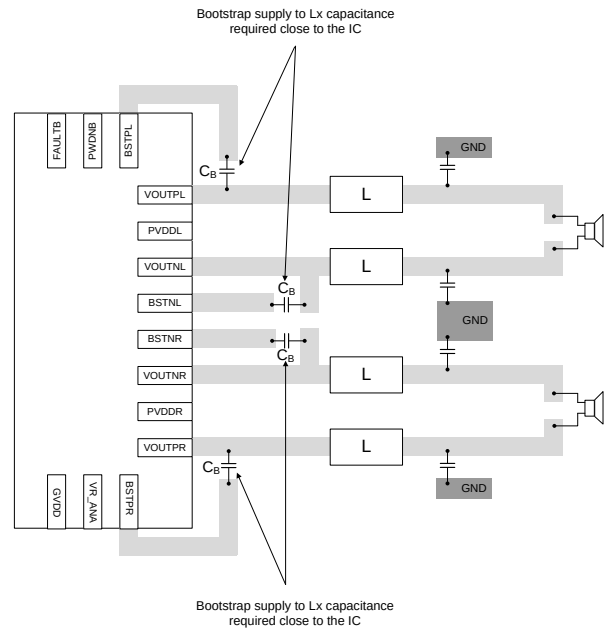
- The VR_DIG VR_ANA and GVDD decoupling capacitors must be placed as close to the IC as possible.



- Place the decoupling capacitors as close as possible to the DVDD and DVSS Pin, AVCC and AVSS Pin for achieving good audio quality, The trace width of DVDD is 6 mil at least and The trace width of AVCC is 30 mil at least.

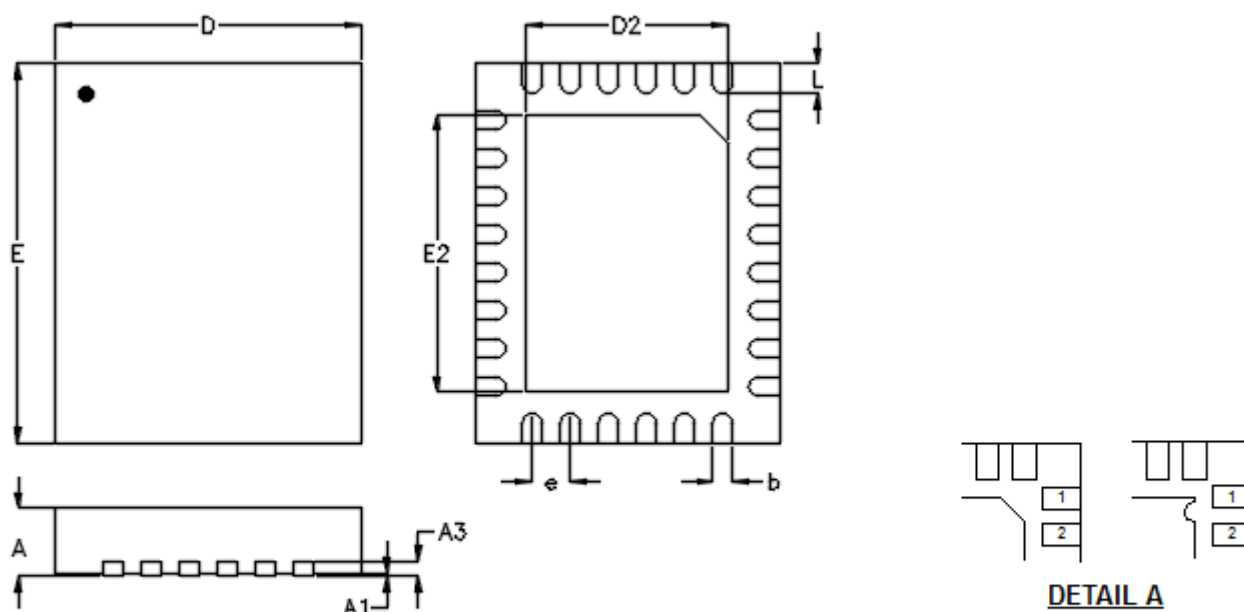


- The traces of VOUTPL VOUTNL VOUTPR and VOUTNR should be kept equal width and length respectively, and Bootstrap supply to Lx capacitance required close to the IC.



- If possible, coplanar ground fill on both sides for differential pair of speaker out shielding

Outline Dimension



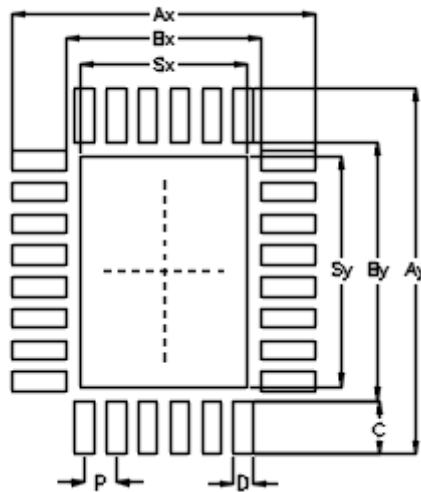
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.900	4.100	0.154	0.161
D2	2.600	2.700	0.102	0.106
E	4.900	5.100	0.193	0.201
E2	3.600	3.700	0.142	0.146
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 28L QFN 4x5 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN4*5-28	28	0.50	4.80	5.80	3.10	4.10	0.85	0.30	2.65	3.65	±0.05

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