SY2A58215

15A H-bridge Motor Driver for Automotive Applications

General Description

The SY2A58215 is a 15A H-bridge motor driver for automotive applications. The highly integrated H-bridge driver block consists of two half-bridges with internal logic control and gate drive

The following protections are included for reliable operation: cross-conduction, current limit, output short circuit and thermal shutdown. An analog current sense output can be used to monitor the current through the power stage.

The device is packaged in SOP16 package.

Features

- Output Current 15A
- Undervoltage Lockout
- Overvoltage Clamp
- Thermal Shutdown Protection
- Cross-conduction Protection
- Current Limit Protection
- Protection against Loss of Ground and Loss of VCC
- Output Short Circuit Protections
- Low Power Standby Mode
- PWM Work Mode
- Current Sense Output
- Diagnostic Function
- SOP16 Package
- AECQ100 Qualified

Applications

- Automotive
- DC Brushed Motor Drivers

Typical Application

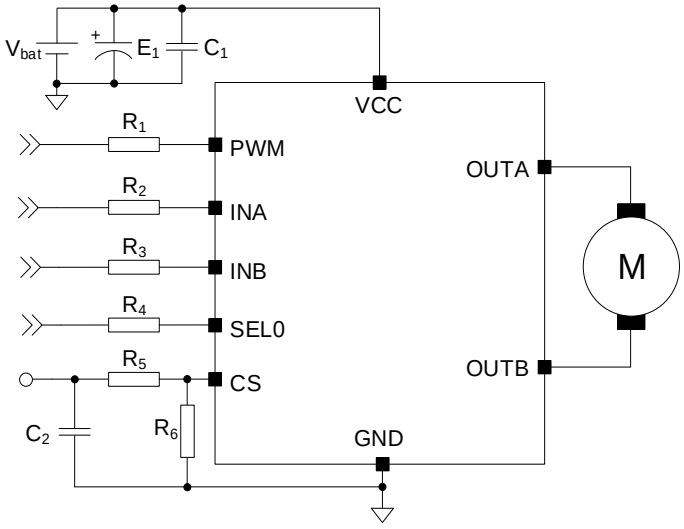


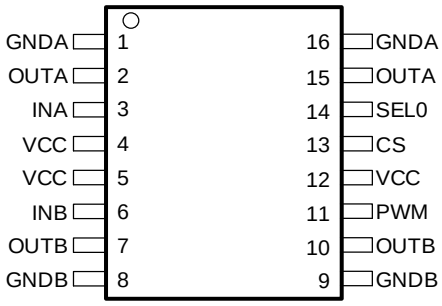
Figure 1. Schematic Diagram

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY2A58215FFP	SOP16 RoHS Compliant and Halogen Free	***ETFxyz***

x=year code, y=week code, z= lot number code

Pinout (Top View)



Pin No	Pin Name	Pin Description
1,16	GNDA	Source of low-side switch A.
2,15	OUTA	Source of high-side switch A / drain of low-side switch A.
3	INA	OUTA control input.
4,5,12	VCC	Power supply.
6	INB	OUTB control input.
7,10	OUTB	Source of high-side switch B / drain of low-side switch B.
8,9	GNDB	Source of low-side switch B.
11	PWM	PWM control of the low-side power MOS.
13	CS	Mixed analog sense output and fault diagnostic output.
14	SEL0	Combined with INA and INB to configure the CS information to the output.

Functional Block Diagram

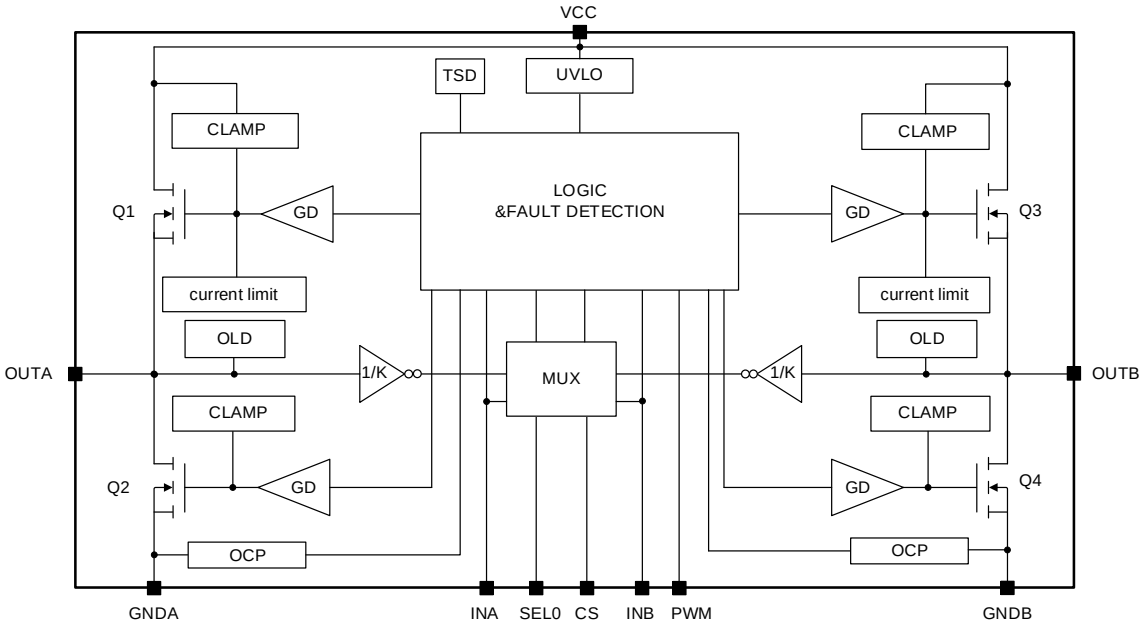


Figure 2. Block Diagram

Absolute Maximum Ratings (Note 1)

(All voltages are referenced to GND unless otherwise noted.)

Parameter		Min	Max	Unit
VCC		-0.3	38	V
OUTA, OUTB		-0.3	38	V
$I_{reverse}$			15	A
I_{CS}		-20	10	mA
$I_{INX,PWM,SEL0}$		-1	10	mA
Junction Temperature Range (T_J)		-40	150	°C
Storage Temperature Range		-55	150	°C
Electrostatic Discharge (Note 2)	HBM (Human Body Model) INX, PWM, SEL0, CS	2		kV
	HBM (Human Body Model) VCC, OUTA, OUTB	4		
	CDM (Charge Device Model)	1		

Thermal Information

Parameter(Note 3)	Typ.	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	55	°C/W
θ_{JC} Junction-to-case Thermal Resistance	17	

Recommended Operating Conditions

(All voltages are referenced to GND unless otherwise noted.)(Note 4)

Parameter	Min	Max	Unit
VCC	4	28	V
OUTA, OUTB	-0.1	28	V
INA, INB, SEL0, PWM	-0.1	5	V
Junction Temperature (T_J)	-40	150	°C

Electrical Characteristics (Note 5)

(T_A =-40°C to 125°C, VCC=7V to 28V, unless otherwise specified.)

Parameter		Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Current	Quiescent VCC Supply Current	I_{QVCC}	INA=INB=0, SEL0=PWM=0, T_A=25°C, VCC=13V			1	μA
			INA=INB=0, SEL0=PWM=0, T_A=85°C, VCC=13V(Note 6)			1	μA
			INA=INB=0, SEL0=PWM=0, T_A=125°C, VCC=13V			8	μA
	Operation VCC Supply Current	I_{OPVCC}	INA or INB=5V, PWM=0V or 5V, SEL0=x		3.5	6	mA
	Off State VCC Supply Current	I_{OFFVCC}	INA=INB=0, SEL0=5V, PWM=0		2	4	mA
Power MOSFETs	High Side Power MOSFETs Turn on Resistance	R_{ONHS}	I_{OUT}=3.5A, T_A=25°C (Note 6)		40		mΩ
			I_{OUT}=3.5A, T_A=-40°C to 125°C			85	mΩ
	Low Side Power MOSFETs Turn on Resistance	R_{ONLS}	I_{OUT}=-3.5A, T_A=25°C (Note 6)		20		mΩ
			I_{OUT}=-3.5A, T_A=-40°C to 125°C			60	mΩ
	Off-state Output Current of One Leg	I_{LKOFF}	INA=INB=0V, PWM=0V, VCC=13V, T_A=25°C	-0.2		1	μA
			INA=INB=0V, PWM=0V, VCC=13V, T_A=125°C	-0.2		3.5	μA
	Free-wheeling Diode Forward Voltage	V_f	I_{OUT}=-3.5A, T_A=125°C		0.7	0.9	V
Input Signal (INA, INB, SEL0, PWM)	Logic "1" Input Voltage	V_{IH}		2.1			V
	Logic "0" Input Voltage	V_{IL}				0.9	V
	Input Voltage Hysteresis	V_{IHYS}		0.2			V
	High Level Logic Bias Current	I_{INH}	V_{IN}=2.1V			10	μA
	Low Level Logic Bias Current	I_{INL}	V_{IN}=0.9V	1			μA
	Input Clamp Voltage	V_{ICL}	I_{IN}=1mA	6.1		8.3	V
			I_{IN}=-1mA (Note 6)		-0.7		V
Thermal Shutdown	High Side Thermal Shutdown Threshold	T_{SD_HS}		150	170	190	°C
	High Side Thermal Shutdown Hysteresis	T_{SDHYS_HS}	(Note 6)		7		°C
	High Side Thermal Shutdown Reset Threshold	T_{SD_HSRST}		135			°C
	Low Side Thermal Shutdown Threshold	T_{SD_LS}		150	170	190	°C
Under Voltage Lock Out	VCC under Voltage Rising Threshold	VCC_{UVON}			4	5	V
	VCC under Voltage Hysteresis	VCC_{UVHYS}	(Note 6)		0.5		V
Open Load Detection	Off-state Open Load Detection Threshold	V_{OL}	INA=INB=0V, PWM=0V, SEL0=5V for OUTA; SEL0=0 and within t_{DSTB} for OUTB	2	3	4	V
	Off-state Output Sink Current	$I_{L\ (off2)}$	INA=INB=0V, V_{OUT}=V_{OL}, PWM=0V, SEL0=5V for OUTA; SEL0=0V for OUTB	-135		-15	μA
Current Protection	High Side Current Limit	I_{LIM_HS}		15	22	30	A
	Low Side Shutdown Current	I_{SD_LS}		18	27	36	A
	Time to Shut down for the Low Side	t_{SD_LS}	INA=5V, INB=0V, PWM=5V(Note 6)		5		μs
Voltage Clamp	High Side Clamp Voltage (VCC to OUTA =0 or OUTB=0)	V_{CLPHS}	I_{OUT}=100mA, t_{clamp}=1ms	38	46		V
	Low Side Clamp Voltage (OUTA=VCC or OUTB=VCC)	V_{CLPLS}	I_{OUT}=100mA, t_{clamp}=1ms	38	46		V
	Total Clamp Voltage (VCC to GND)	V_{CLP}	I_{OUT}=100mA, t_{clamp}=1ms	38	46	52	V
Current Sense	Multi-sense Clamp Voltage	V_{CS_CL}	VCC=18V, I_{SENSE}=-5mA		15.3		V
			VCC=18V, I_{SENSE}= 5mA	-17.3		-13.3	V
	I_{OUT}/I_{SENSE}	K_0	I_{OUT}=0.1A, V_{SENSE}=0.5V, T_A=-40°C to 125°C	665			
	I_{OUT}/I_{SENSE}	K_1	I_{OUT}=0.2A, V_{SENSE}=0.5V, T_A=-40°C to 125°C	1083	1900	2716	
	I_{OUT}/I_{SENSE}	K_2	$I_{O\ UT}$=3.5A, V_{SENSE}=4V, T_A=-40°C to 125°C	1315	1540	1779	
	I_{OUT}/I_{SENSE}	K_3	I_{OUT}=5.5A, V_{SENSE}=4V, T_A=-40°C to 125°C (Note 6)	1357	1540	1727	
	Analog Sense Current Drift	DK_0/K_0	I_{OUT}=0.1A, V_{SENSE}=0.5V, T_A=-40°C to 125°C (Note 6)	-25		25	%
	Analog Sense Current Drift	DK_1/K_1	I_{OUT}=0.2A, V_{SENSE}=0.5V, T_A=-40°C to 125°C (Note 6)	-21		21	%
	Analog Sense Current Drift	DK_2/K_2	I_{OUT}=3.5A, V_{SENSE}=4V, T_A=-40°C to 125°C (Note 6)	-6		6	%
	Analog Sense Current Drift	DK_3/K_3	I_{OUT}=5.5A, V_{SENSE}=4V, T_A=-40°C to 125°C (Note 6)	-6		6	%
	Max Analog Sense Output Voltage	V_{SENSE}	VCC=7V, SEL0=5V, INA=5V,PWM=0V, I_{OUT}=2A, R_{SENSE}=10kΩ, T_A=125°C	5			V
	Current Sense Saturation Current	I_{SENSE_SAT}	VCC=13V, INA=5V, INB=0V, V_{SENSE} =4V, SEL0=5V, T_A=125°C	4.6			mA
	Output Saturation Current	I_{OUT_SAT}	VCC=13V, INA=5V, INB=0V, V_{SENSE} =4V, SEL0=5V, T_A=125°C (Note 6)	8			A

	VCC- Output Voltage for CS Shutdown	V_{OUT_SD}	INA=5V, INB=0V, SEL0=5V, R_{SENSE}=2.7kΩ, I_{OUT}=3.5A (Note 6)		3		V
	CS Leakage Current	I_{SENSE_LK}	I_{OUTA}=0A, V_{SENSE}=0V, INx=0V, SEL0=0; T_A=-40°C to 125°C (Standby)	-0.2		0.5	μA
			I_{OUTA}=0A, V_{SENSE}=0V, INx=0V, SEL0=5V; T_A=-40°C to 125°C (No Standby)	-0.2		0.5	μA
			I_{OUTA}=0A, INx=5V, PWM=5V; T_A=-40°C to 125°C	-0.2		15	μA
	CS Output Voltage in Fault Condition	V_{SENSEH}	VCC=13V, R_{SENSE}=1kΩ, For example: OUTA in open load, INA=0V, I_{OUTA}=0A, OUTA=4V, SEL0=5V	5		7	V
	CS Output Current in Fault Condition	I_{SENSEH}	VCC=13V, V_{SENSE}=V_{SENSEH}	7	20	30	mA

Timing

(T_A =-40°C to 125°C, VCC=13V, R_{LOAD}=3.7Ω, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PWM Frequency	f				20	kHz
HS Turn-on Delay Time	$t_{d(on)\_HS}$	Input rise time < 1μs, INx to OUTx rise edge 90% (Note 6)		25		μs
HS Turn-off Delay Time	$t_{d(off)\_HS}$	Input rise time < 1μs, INx to OUTx fall edge 10% (Note 6)		15		μs
HS Rise Time	t_{r_HS}	OUTx edge 10%-80% (Note 6)		10		μs
HS Fall Time	t_{f_HS}	OUTx edge 90%-20% (Note 6)		0.6		μs
LS Turn-on Delay Time	$t_{d(on)\_LS}$	Input rise time < 1μs, INx to OUTx fall edge 90% (Note 6)		0.4		μs
LS Turn-off Delay Time	$t_{d(off)\_LS}$	Input rise time < 1μs, INx to OUTx rise edge 10% (Note 6)		2		μs
LS Rise Time	t_{r_LS}	OUTx edge 10%-80%		0.7	1.5	μs
LS Fall Time	t_{f_LS}	OUTx edge 90%-20%		0.2	0.6	μs
Low-side Turn on Delay Time	t_{cross}	Input rise time < 1 μs	40	140	350	μs
Off-state Diagnostic Delay Time from Falling Edge of INPUT	t_{DIADLF}	INA=5V to 0V; INB=0; SEL0=5V; PWM=0V; I_{OUT}=0A; OUTA=4V	40	140	350	μs
Off-state Diagnostic Delay Time from Rising Edge of V_{OUT}	t_{DIADLR}	INA=INB=0V; PWM=0V; OUTx=0V to 4V; SEL0=5V for OUTA; SEL0=0V and within t_{DSTB} for OUTB		5	30	μs
Input Reset Time for High Side Fault Unlatch	$t_{LT\_RS\_HS}$	V_{INx}=5V to 0V; HSx fault	3	10	20	μs
Input Reset Time for Low Side Fault Unlatch	$t_{LT\_RS\_LS}$	V_{INx}=0V to 5V; LSx fault	3	10	20	μs
Standby Mode Blanking Time	t_{DSTB}	VCC=13V, INA=INB=PWM=0V, SEL0 from 5V to 0V	0.2	1	1.8	ms

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

Note 3: θ_{JA}, θ_{JC} is measured in the natural convection at T_A = 25°C on Silergy demo test board.

Note 4: The device is not guaranteed to function outside its operating conditions.

Note 5: Unless otherwise stated, limits are 100% production tested at $T_A \approx T_J$ = -40 to 125˚C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 6: This spec is guaranteed by design.

Switching Timing

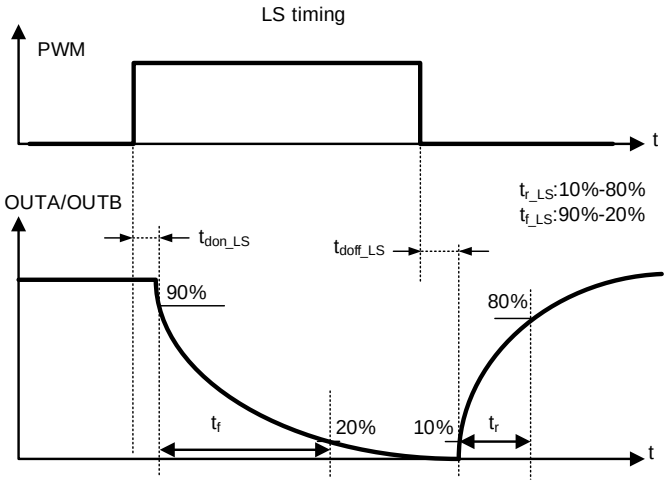


Figure 3. Definition of the LS Switching Timing (INA=INB=0)

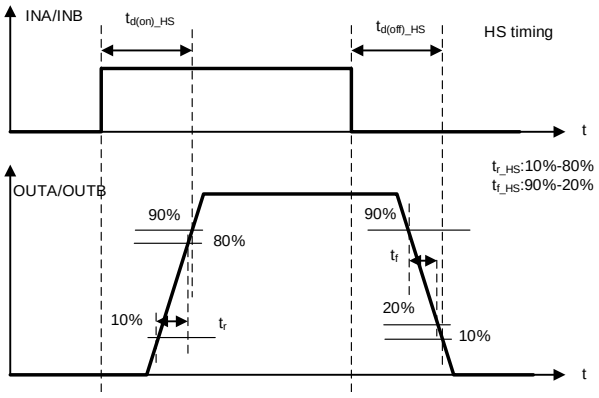


Figure 4. Definition of the HS Switching Timing

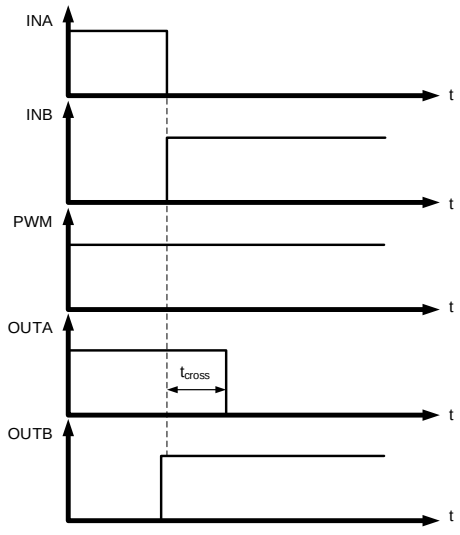


Figure 5. t_{cross} (Anti Cross-Conduction)

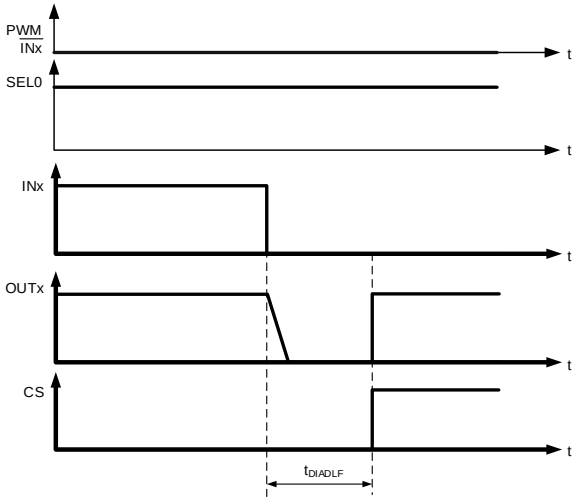


Figure 6. t_{DIADLF} (Off-State Diagnostic Delay Time from Falling Edge of INPUT)

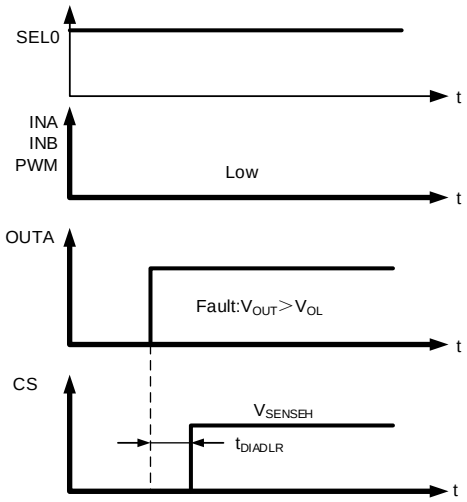


Figure 7. t_{DIADLR} (Off-State Diagnostic Delay Time from Rise Edge of OUTA/B)

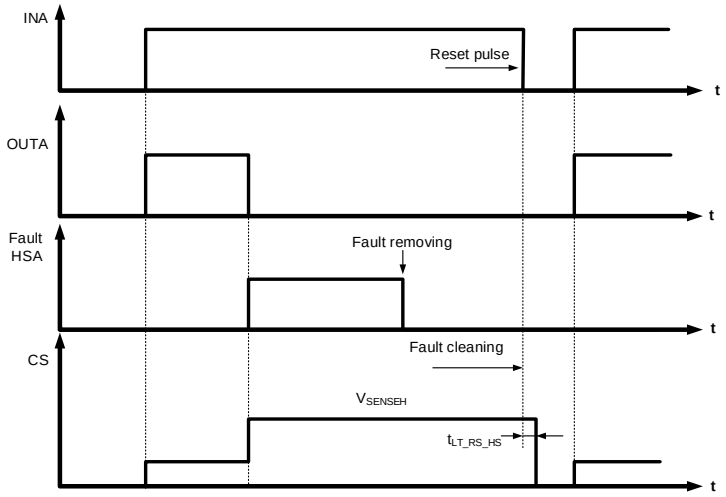


Figure 8. $t_{LT\_RS\_HS}$ (Input Reset Time for High Side Fault Unlatch)

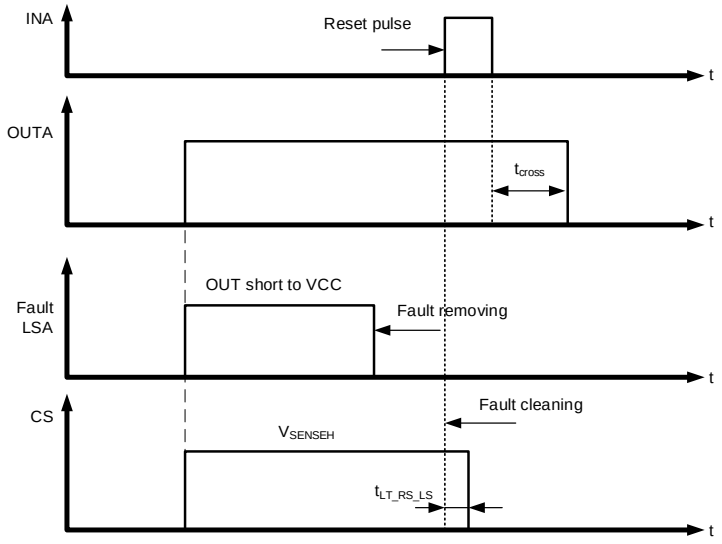
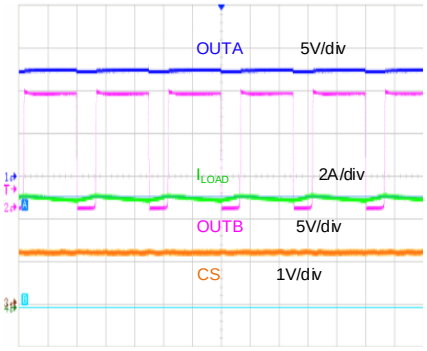


Figure 9. $t_{LT\_RS\_LS}$ (Input Reset Time for Low Side Fault Unlatch)

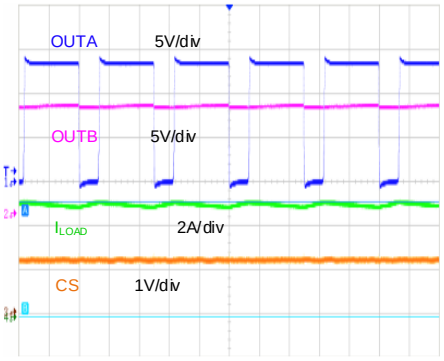
Typical Performance Characteristics

Forward OUTA→OUTB
(VCC=13V I_{LOAD}=5A
CH1:OUTA CH2:OUTB CH3:CS CH4:I_{LOAD})



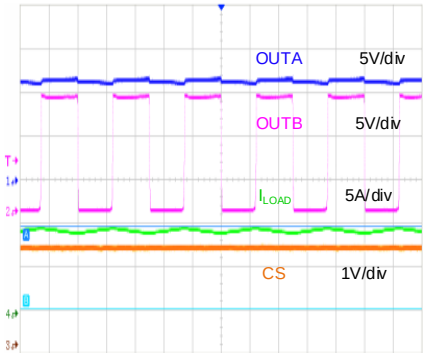
Time (20μs/div)

Reverse OUTB→OUTA
(VCC=13V I_{LOAD}=5A
CH1:OUTA CH2:OUTB CH3:CS CH4:I_{LOAD})



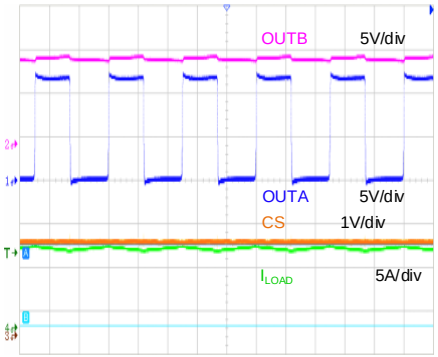
Time (20μs/div)

Forward OUTA→OUTB
(VCC=13V I_{LOAD}=10A
CH1:OUTA CH2:OUTB CH3:CS CH4:I_{LOAD})



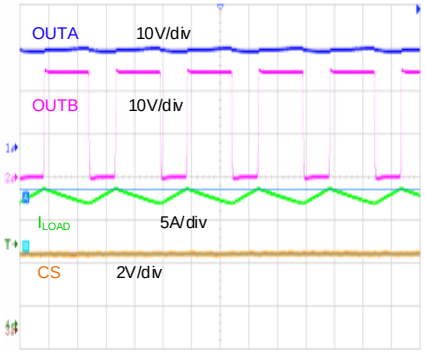
Time (20μs/div)

Reverse OUTB→OUTA
(VCC=13V I_{LOAD}=10A
CH1:OUTA CH2:OUTB CH3:CS CH4:I_{LOAD})



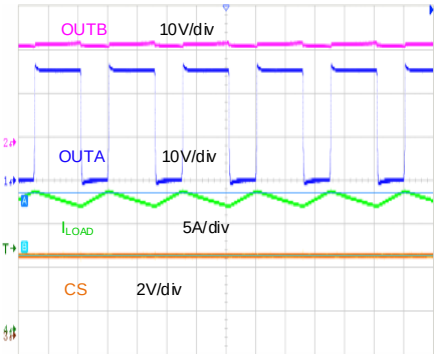
Time (20μs/div)

Forward OUTA→OUTB
(VCC=28V I_{LOAD}=15A
CH1:OUTA CH2:OUTB CH3:CS CH4:I_{LOAD})



Time (20μs/div)

Reverse OUTB→OUTA
(VCC=28V I_{LOAD}=15A
CH1:OUTA CH2:OUTB CH3:CS CH4:I_{LOAD})



Time (20μs/div)

Detailed Description

Logic Truth Table

The output state is dependent on the states of the INA, INB, SEL0, and PWM.

Table 1. Truth Table in Normal Operating Conditions

INA	INB	SEL0	PWM	CS	HSA	LSA	HSB	LSB
1	1	1	x	Current Monitoring HSA	ON	OFF	ON	OFF
		0		Current Monitoring HSB				
1	0	1	1	Current Monitoring HSA	ON	OFF	OFF	ON
			0		ON	OFF	OFF	OFF
1	0	0	1	Hi-Z	ON	OFF	OFF	ON
			0		ON	OFF	OFF	OFF
0	1	1	1	Hi-Z	OFF	ON	ON	OFF
			0		OFF	OFF	ON	OFF
0	1	0	1	Current Monitoring HSB	OFF	ON	ON	OFF
			0		OFF	OFF	ON	OFF
0	0	1	1	Hi-Z	OFF	ON	OFF	ON
		0						
0	0	1	0	Ref to Table 3	OFF	OFF	OFF	OFF
		0			OFF	OFF	OFF	OFF

Table 2. OUTA Fault Conditions Truth Table

Digital Input Pins				CS	Comment
INA	INB	PWM	SEL0		
0	0	1	0	V_{SENSEH}	LSB protection triggered; LSB latched off
0	0	1	1	V_{SENSEH}	LSA protection triggered; LSA latched off
0	1	x	0	V_{SENSEH}	HSB protection triggered; HSB latched off
0	1	1	1	V_{SENSEH}	LSA protection triggered; LSA latched off
1	0	1	0	V_{SENSEH}	LSB protection triggered; LSB latched off
1	0	x	1	V_{SENSEH}	HSA protection triggered; HSA latched off
1	1	x	1	Hi-Z	HSB protection triggered; HSB latched off
1	1	x	0	Hi-Z	HSA protection triggered; HSA latched off

Table 3. Truth Table in Off-State

INA	INB	SEL0	PWM	OUTA	OUTB	CS
0	0	1	0	$V_{OUTA}>V_{OL}$	x	V_{SENSEH}
				$V_{OUTA}<V_{OL}$	x	Hi-Z
		0		x	$V_{OUTB}>V_{OL}$	V_{SENSEH}
				x	$V_{OUTB}<V_{OL}$	Hi-Z

Operation Waveforms of Typical Application

The device operation waveforms in a typical application are shown in Figure 10 and 11.

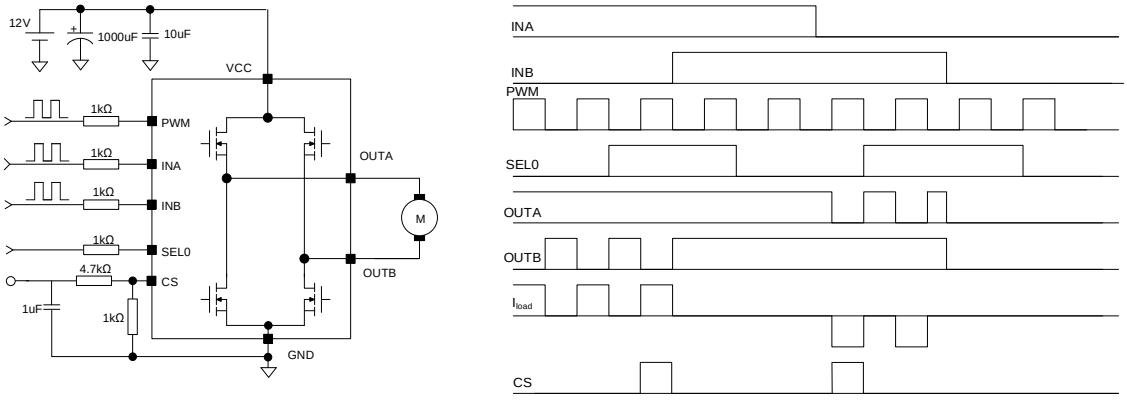


Figure 10. Normal Operation Waveforms

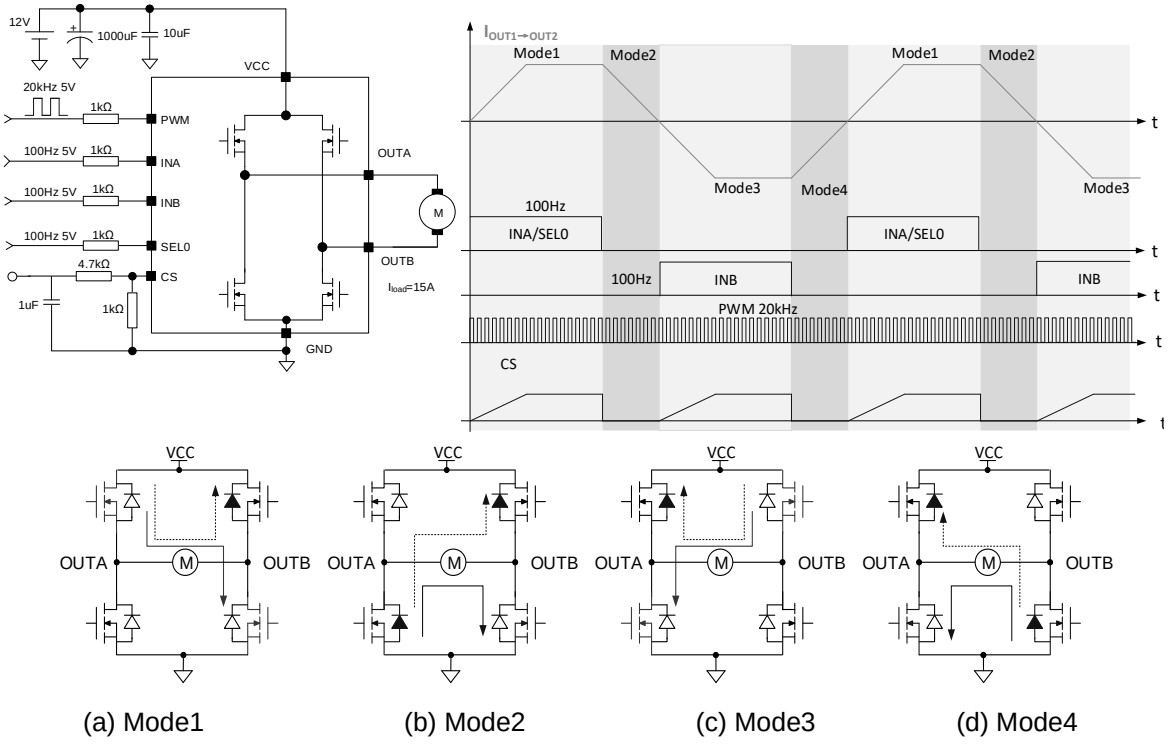


Figure 11. Typical Application: Waveforms in Normal Operation

Table 4. Normal Operation Truth Table

Mode	INA	INB	PWM	SEL0	CS	Function
1	High	Low	20kHz	High	Current Monitoring HSA	Forward
2	Low	Low		Low	Hi-Z	Coast
3	Low	High		Low	Current Monitoring HSB	Reverse
4	Low	Low		Low	Hi-Z	Coast

Power On

VCC power on with a fast slope rate (＜10V/us): when VCC is above UVLO threshold (VCC_{UVON}), OUTA and OUTB are pulled up to VCC (HSx turn on) after a delay of around 25μs.

VCC power on with a slow slope rate (1V/ms): when VCC is above UVLO threshold (VCC_{UVON}), OUTA and OUTB are pulled up to VCC (HSx turn on) with a delay of around 1μs.

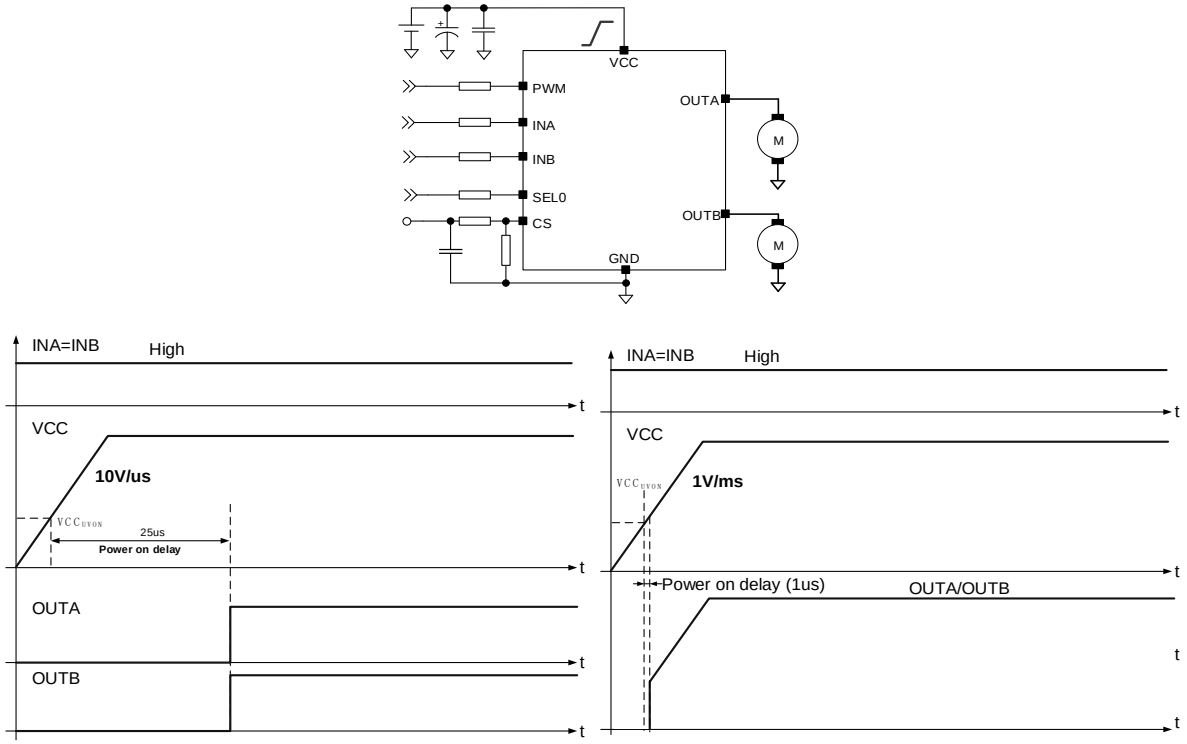


Figure 12. Power on Timing with Different VCC Slopes

Standby Mode

To enter standby mode, all logic pins must be set to low for at least t_{DSTB} (from the moment when the last input pin is set to low). In standby mode, the device is placed in low power mode (current consumption is less than 3uA). To exit standby mode, it is sufficient to set one of logic pins (INA/INB/SEL0/PWM) from low to high. Operation resumes after a delay.

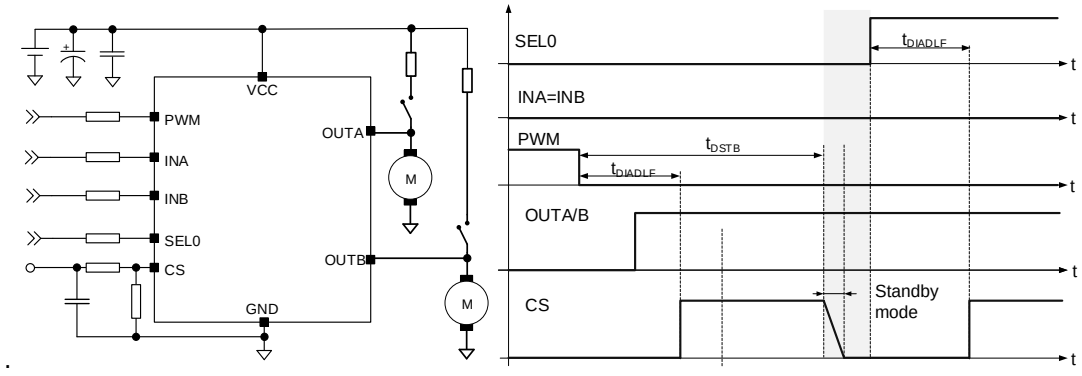


Figure 13. Standby Mode Waveform

Table 5. Truth Table in Standby Mode

INA	INB	PWM	SEL0	Enter Standby
H→L	L	L	L	t_{DSTB}
L	H→L	L	L	
L	L	H→L	L	
L	L	L	H→L	

CS Output

Current During Normal Operation

The CS output is proportional to the load current flowing through the activated high side, selected by SEL0. The sensed current is scaled based on an internally set ratio K. This current can be easily converted to a voltage by using an external resistor, allowing continuous load monitoring and abnormal condition detection.

Diagnostics Output in Fault Conditions

The CS pin serves a dual purpose, signaling fault events as shown below:

(a) Fault condition on the activated high side (in ON state) is triggered by overtemperature protection, where the CS output is selected by SEL0 to the high side in a fault state.

(b) Fault condition on the activated low side (in ON state) is triggered by overcurrent shutdown or overtemperature protection, where the CS output is selected by SEL0 to the same pin (of high side) where the low side is in a fault state.

(c) OL detection in OFF state (INA=INB=PWM=L) is selected by SEL0. For the H-bridge, special care must be taken for the OUTB (SEL0=L) because the fixed voltage is available only before the device enters its standby mode after t_{DSTB} (when all control signals are set to low). In standby mode, CS is pulled down after 47μs (CS fall time is 47μs).

Diagnostic Flag During NO Fault Conditions

The pin delivers a fixed voltage (V_{SENSEH}) in following configurations: full bridge is in OFF state (load connected between OUTA and OUTB, INA=INB=PWM=0), applying activated external pull-up resistor on the pin which is opposite to the monitored one by the CS output (pull-up on OUTB while SEL0=1; or pull-up on OUTA while SEL0=0). Special care must be taken for the configuration where an external pullup is applied on OUTA (SEL0=0) as the device enters standby mode after t_{DSTB}.

Normal operation (SEL0=1/0, corresponding to OUTA/OUTB)

Current provided by the CS output:

$$I_{SENSE} = \frac{I_{OUT}}{K} \quad (1)$$

Voltage on R_{SENSE}:

$$V_{SENSE} = R_{SENSE} I_{SENSE} = R_{SENSE} \frac{I_{OUT}}{K} \quad (2)$$

Where:

V_{SENSE} is the voltage measured on R_{SENSE} resistor. I_{SENSE} is the current provided from the CS pin in current output mode. I_{OUT} is the current flowing in the selected high side. K factor represents the current mirror ratio between the Power MOSFET and the sense MOSFET.

Current Sense in Overload Condition (Failure Flag Indication)

Faults caused by overtemperature and open load in the OFF state are indicated by the CS pin pulled to the V_{SENSEH} (internal LDO).

Conditions causing the CS pin being pulled to V_{SENSEH} include:

- Current flowing in the active high-side triggers overtemperature protection, or the junction temperature exceeds overtemperature threshold.
- Short-circuit to GND: The CS output is enabled by SEL0. The OUTx pin with active high-side is also selected by SEL0.

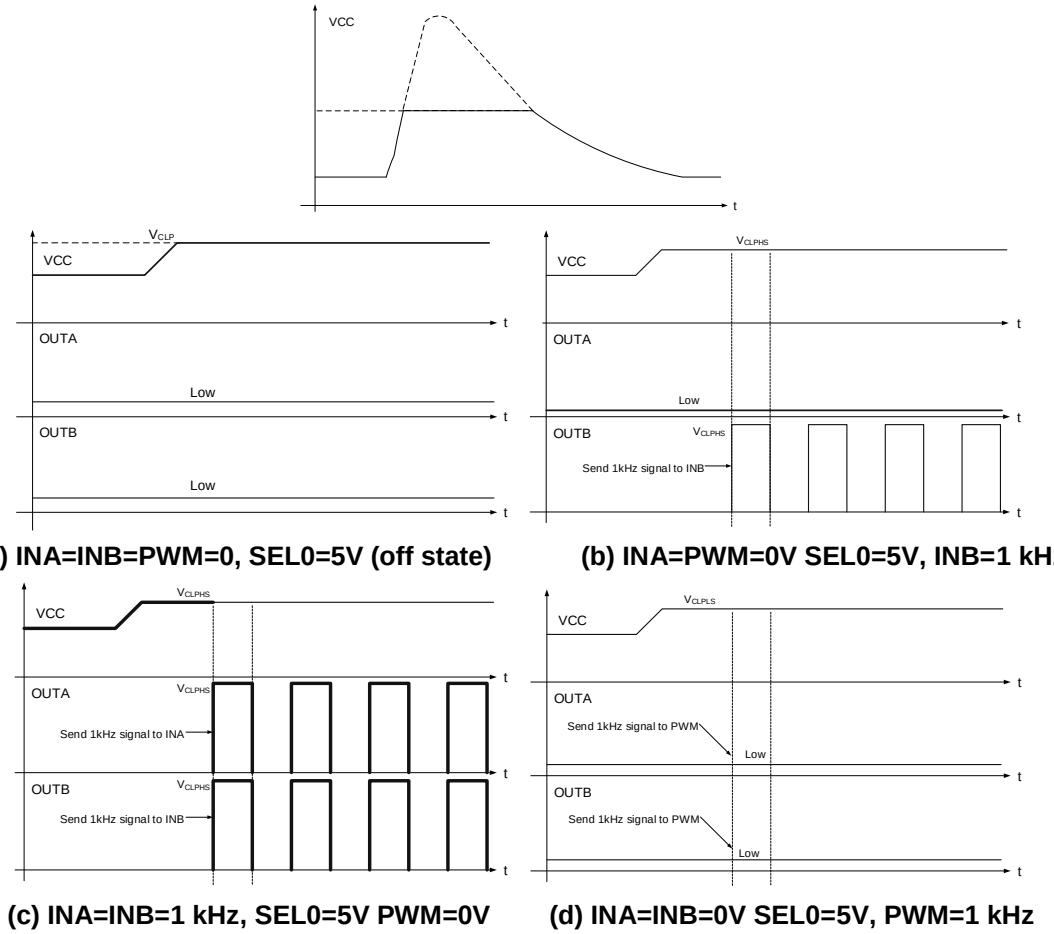
- Current flowing in active low-side output triggers cut-off current protection (I_{OUT} >I_{SD_LS}), or junction temperature exceeds overtemperature threshold (SEL0=H, CS output represents LSA fault; SEL0=L, CS output represents LSB fault).
- Voltage on OUTx pin in OFF state (INA=INB =PWM =L) exceeds V_{OL} threshold, such as short-circuit to VCC (CS output is enabled by SEL0 and SEL0 also selects the corresponding output voltage. Special care must be taken for H-bridge for the OUTB (SEL0 = L) because the fixed voltage is only available until the device enters its standby mode after t_{DSTB} with all the control signals set to low. In these events, the CS output voltage should be controlled at the lowest level which can at least drive V_{SENSEH} as shown in the EC table.

Note: When HSx is in current limit mode, the drain-sourcing voltage of HSx changes rapidly. Once the voltage exceeds the common input voltage on the current sense op-amp, it stops operation. In other words, when the output voltage drops 3V below VCC (V_{OUT_SD} is shown in the EC table, guaranteed by design), the CS pin stops sourcing current and is pulled down by the pull-down resistor until the first thermal protection is activated.

Protection Circuits

Overvoltage Clamp

As soon as a transient voltage is higher than V_{CLP} (V_{CLPHS}/V_{CLPLS}) on the VCC, the LS MOSFET is forced to operate in the linear region while the HS MOSFET operates in the saturation region. Therefore, the HS component has very high power dissipation. For negative transients applied across the device supply pins, most of the current flows through the Power MOSFET body diodes. The current is not limited by anything other than the pulse generator intrinsic resistance. External circuitry should be used to protect the device against such events.



(a) INA=INB=PWM=0, SEL0=5V (off state) **(b) INA=PWM=0V SEL0=5V, INB=1 kHz**

(c) INA=INB=1 kHz, SEL0=5V PWM=0V **(d) INA=INB=0V SEL0=5V, PWM=1 kHz**

Figure 14. Overvoltage Clamp Protection Ideal Waveform

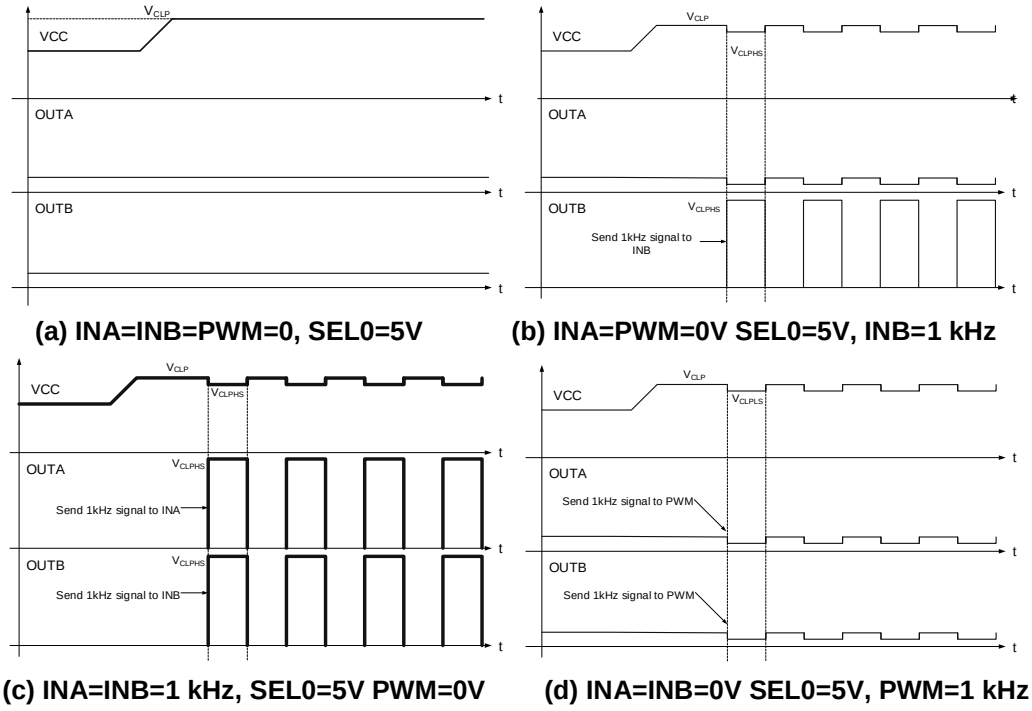


Figure 15. Overvoltage Clamp Protection Practical Waveform

Undervoltage Protection

When the supply voltage on the VCC pin falls below the undervoltage lockout threshold voltage after about 5us (t_{UVLO_filter}), all circuitry in the device is disabled and internal logic is reset. Operation resumes when VCC supply rises above the UVLO threshold after about 1us (t_{UVLO_delay}).

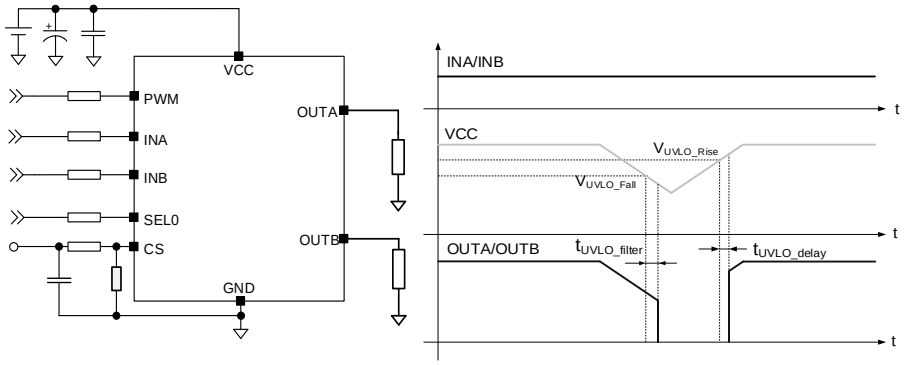


Figure 16. SY2A58215 UVLO Protection

Loss of GND Line

In the case of a GND connection loss, I_{OPVCC} flows through the ESD components present on the PWM/INA/INB/SEL0 pins, which generates I_{GND_loss} (about 10mA) using internal circuitry. The SY2A58215 compares the voltage between the logic pins (PWM/INA/INB/SEL0) and GND. When loss of GND is detected, the device enters standby mode and internal Power MOSFETs are switched off, ensuring that the motor is disabled. The device resumes normal operation after GND is reconnected.

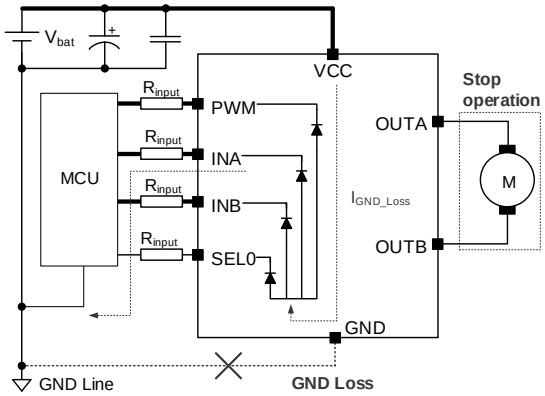


Figure 17. GND Loss Schematic

R_{input} minimum resistor value can be calculated according to the following equations:

$$V_{MCU} - {}^{1}/_{3} \times I_{GND_{loss}} \times R_{input} - V_{ESD} \leq V_{IL} \quad (3)$$

$$R_{input} \geq (V_{MCU} - V_{IL} - V_{ESD}) \times {}^{3}/_{I_{GND\_loss}} \quad (4)$$

Loss of VCC Line

When VCC is lost, the voltage starts to drop and the energy in the bulk capacitor is used to supply the motor, until the bulk capacitor is discharged and VCC falls below the UVLO threshold

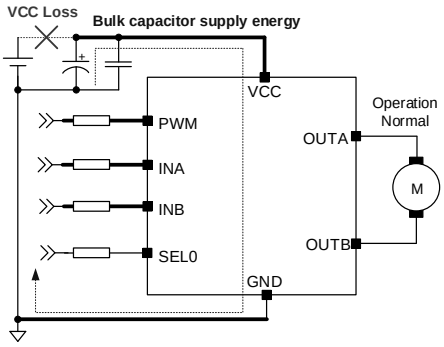


Figure 18. VCC Loss Schematic

Short-Circuit Protection

Short to VCC Protection (LS)

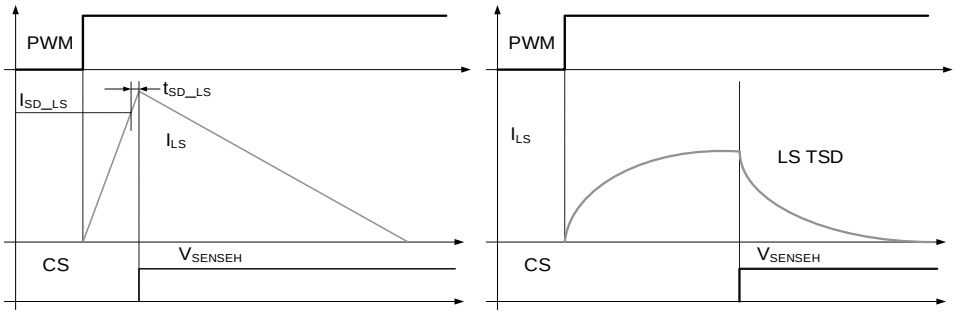
Two types of protections are available depending on the short circuits: hard short or resistive short as shown in Figure 19.

Hard Short-circuit

When OUTx pin shorts to VCC in a hard short-circuit (low parasitic resistance), once the current flowing through the LS exceeds I_{SD_LS}, the device is turned off after a filtering delay (t_{SD_LS}) and it latches as shown in Figure 19. (a). The fault condition is triggered and the CS pin will be pulled up to V_{SENSEH}. When the fault condition is removed, a short high-level pulse is driven on the INx pin corresponding to the OUTx fault and the device restarts, as shown in Figure 9.

Resistive Short-circuit

In a resistive short-circuit, the current through the LS doesn't reach I_{SD_LS}, but the temperature rises above the LS thermal shutdown threshold (T_{SD_LS}) which causes the device to switch off and latch, as shown in Figure 19. (b). The fault condition is triggered and the CS pin will be pulled up to V_{SENSEH}. When the fault condition is removed, a short high-level pulse is driven on the INx pin corresponding to the OUTx fault and the device restarts, as shown in Figure 9).



(a) Hard Short-circuit **(b) Resistive Short-circuit**

Figure 19. Short to VCC Protection

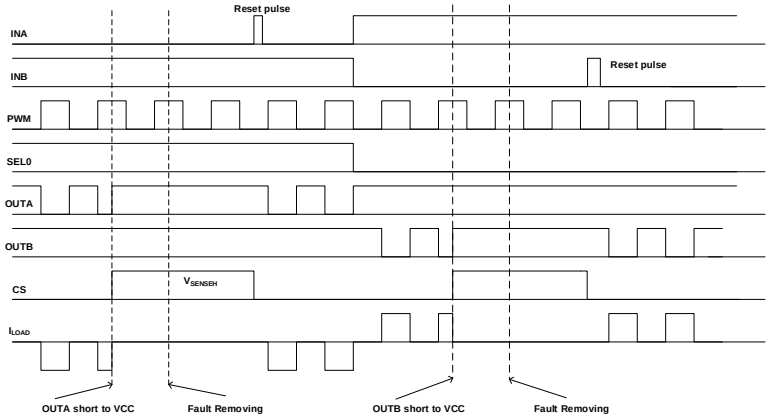


Figure 20. OUTx Short to VCC and Fault Clearing

Short to GND protection

I When the OUTx is shorted to GND, the HSx will operate in the saturation region for a filtering delay time, $t_{LIM\_HS\_filter}$ (accounting for the op-amp response time) after the current limit threshold I_{LIM_HS} is reached. After about 10us, the HS driver is disabled and the CS pin will be pulled up to V_{SENSEH}. When the fault condition is removed, a short high-level pulse is driven on the INx pin corresponding to the OUTx fault and the device restarts as shown in Figure 8.

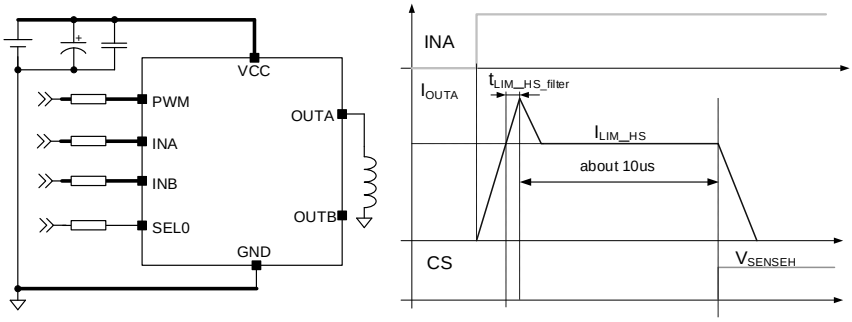


Figure 21. HSA Short Protection

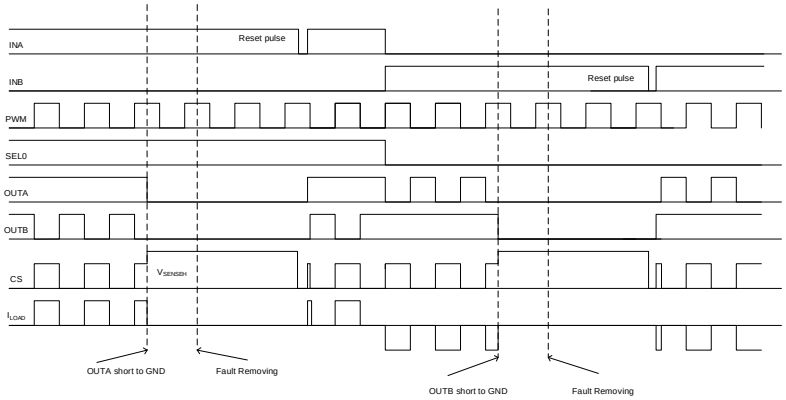


Figure 22. OUT Short to GND and Fault Clearing

Shoot-Through Protection

The SY2A58215 doesn't allow both Power MOSFETs to be active in the same half-bridge at the same time to prevent shoot-through events. Because turning off the HS is slower than turning on the LS, a delay time (t_{cross}) is added to ensure LS MOSFET is turned on only after turning off HS MOSFET. Therefore, t_{cross} is longer than the HS turn-off time (Figure 23).

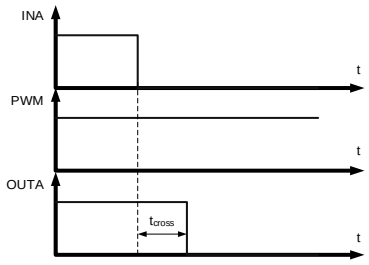
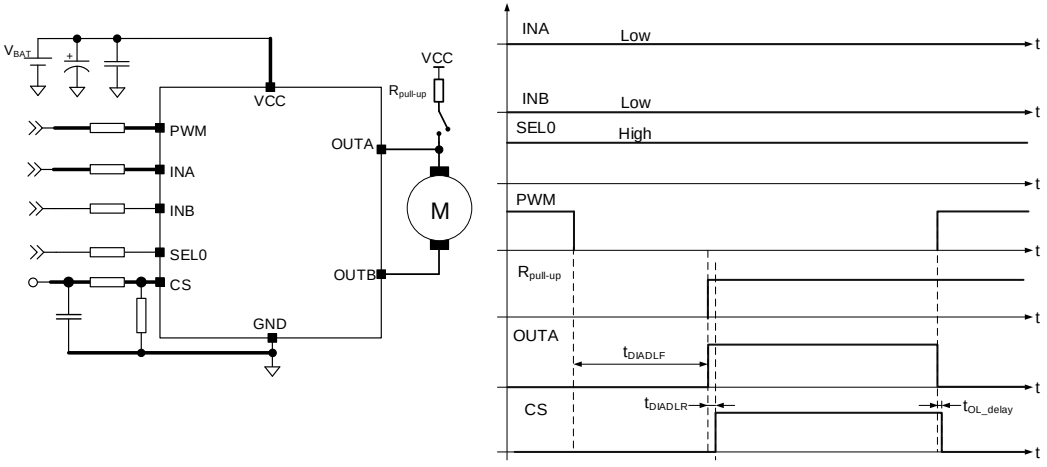


Figure 23. Anti-Shoot-Through

Open Load Detection in Off-State (OL)

In off state (INA=INB=PWM=Low, SEL0=H), open load detection is active after a filtering time (t_{DIADLF}). When the OUTA voltage is above the open load detection threshold, the CS pin will be pulled up to V_{SENSEH} after a filtering time (t_{DIADLR}). SEL0 can be set to low and the open load detection on OUTB can also be performed (within t_{staby} for OUTB). OUTx needs a pull-up resistor $R_{pull-up}$ in normal application as shown in Figure 24. When OUTx voltage falls below the threshold or the device is out of off state, operation resumes after a delay time t_{OL_delay} (about 3μs).



(a) OL Configuration **(b) OL Waveform**

Figure 24. Open Load Detection Configuration

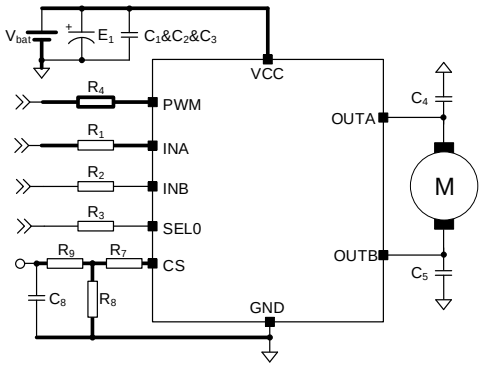
The maximum value of the pull-up resistor $R_{pull-up}$ connected to Vbat supply can be calculated according to equation 5:

$$R_{\text{pull-up}} \leq \frac{V_{BAT}-V_{OL\_MAX}}{-2*I_{L(off2)\_MIN}} \quad (5)$$

Thermal Shutdown Protection (TSD)

If the temperature of Power MOSFET exceeds approximately 170°C (T_{SD_HS}), the corresponding gate driver is disabled and the CS pin will be pulled up to V_{SENSEH}. During this state, all Power MOSFET gate drivers are disabled and the CS pin is pulled up to V_{SENSEH} until the temperature drops to a safe level (T_{SD_HSRST}). Thermal shutdown events indicate excessive power dissipation, insufficient heatsinking or high ambient temperature.

Application Schematic

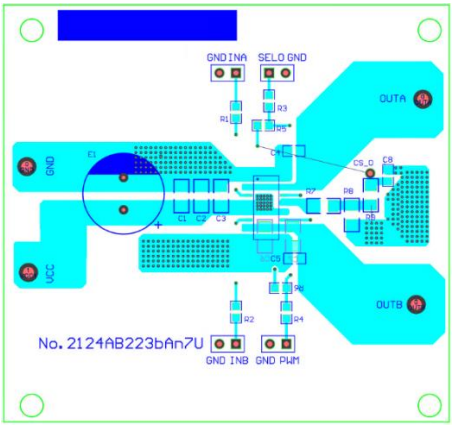


BOM List

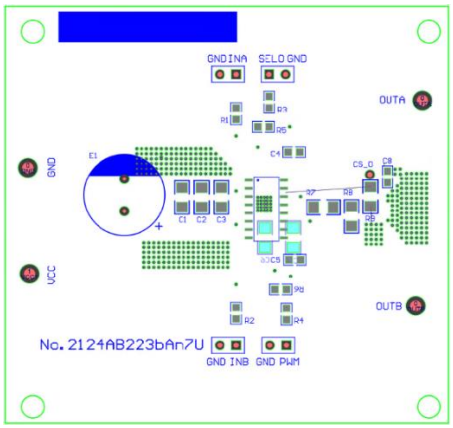
Reference Designator	Description	Package Info	Note
C1 C2 C3	10uF/50V	1206	
C4 C5	100nF/50V	0603	
E1	100uF/E_{cap}/50V		
C8	1uF/16V	0805	
R1 R2 R3 R4	1kΩ/1%	0603	
R7 R8	270Ω/1%	1206	
R9	4.7kΩ/1%	1206	

Layout Guidelines

- A PCB floor plan is important to minimize current loop areas. Arranging the power components properly and avoiding sharp corners and narrow paths allow the current to flow smoothly.
- All filtering capacitors (mainly C1&C2&C3 for VCC) must be placed as close as possible to the device pins to keep the parasitic capacitance and inductance of the PCB traces as low as possible.
- Placing two decoupling capacitors (VCC) on the same layer improves the noise immunity. If GND and VCC plate are not on same layer, connect them with multi vias.
- Placing a capacitor between OUT and GND reducing the sparking during the communication of DC motor.
- A multilayer PCB is better than a 2-layer PCB for heat dissipation. To improve thermal and electrical conduction, a 2-ounce or higher copper thickness may be used in place of the standard 1-ounce. If there are several GND planes, using vias to connect them can also help the thermal and electrical conduction.

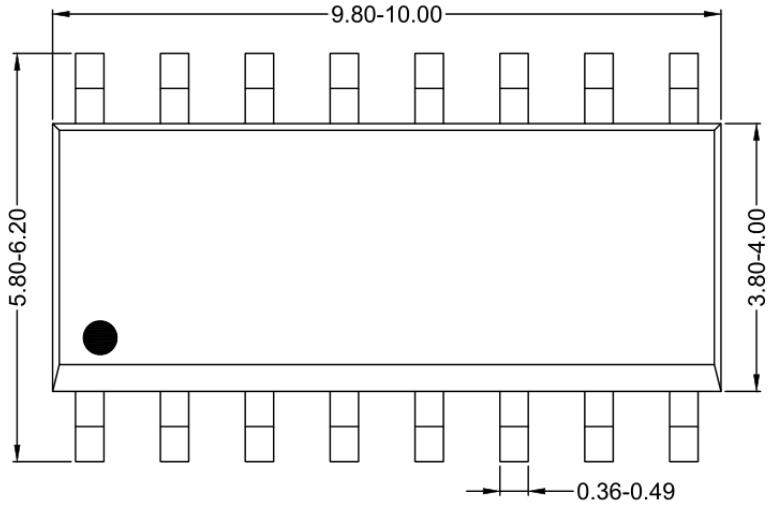


Top Layer

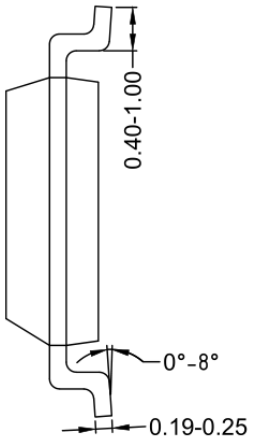


Top Silkscreen

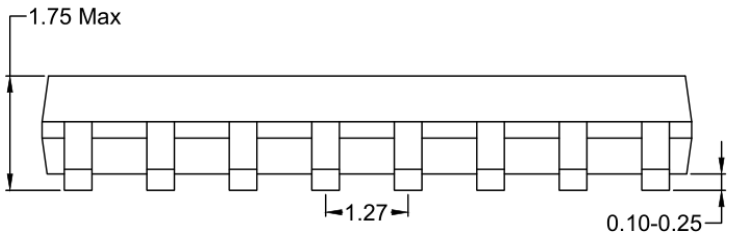
SOP16 Package Outline Drawing



Top View



Side View

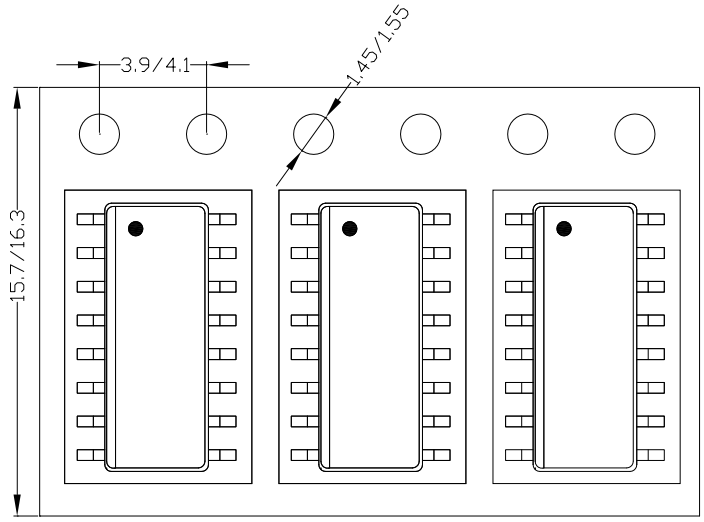


Front View

Note: All dimensions are in millimeters and exclude mold flash & metal burr.

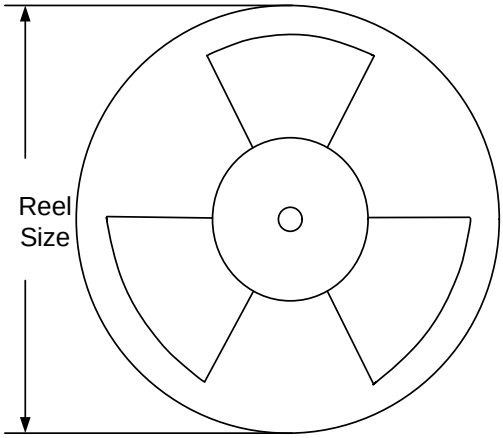
Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Feeding direction ⟶

Reel Dimensions



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer Length(mm)	Leader Length (mm)	Qty per Reel
SOP16 & SOP16E	16	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description
0.9	November 06, 2023	Initial Release
0.9A	December 08, 2023	Add Note 4 in IQVCC test condition
1.0	February 13, 2025	Production Release. Language improvements for clarity
1.0A	June 2, 2025	Revise the typo of formula (3) in page17

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