SA52902

H- Bridge Gate Drivers for Automotive Applications

General Description

The SA52902 is a compact H-bridge gate driver designed to control high-side and low-side N-channel power MOSFETs. The device integrates driver power supplies, a current shunt amplifier, and protection monitors. The protection monitors include undervoltage and overvoltage monitors, V_{DS} overcurrent and V_{GS} gate fault monitors for the external MOSFETs, off-state open load and short-circuit protection, sleep mode braking, a limp home function, and internal thermal warning and shutdown. A compact QFN5×5-32 (with wettable flanks) package is utilized to minimize peripheral circuit design.

Features

- H-Bridge / Half-Bridge Gate Drivers
  - Double Charge Pump Supports 100% PWM
  - Supports Half-Bridge, H-Bridge, and SPI Control Modes
- Smart Gate Driver Architecture
  - 0.5mA-62mA, 16-level Peak Source/Sink Current Output (SPI Configured)
  - Integrated Dead-Time Handshaking (8-level Configurable)
- Wide Common-Mode Current Shunt Amplifier
  - Supports Inline, High-Side or Low-Side Current Sensing
  - Configurable Gain Settings: 10, 20, 40, 80V/V
  - Adjustable PWM Blanking Scheme
- SPI: Comprehensive Configuration and Diagnostics
- Spread Spectrum Clocking to Reduce EMI
- Integrated Protection Features:
  - Supply and Regulator Voltage Monitors
  - MOSFET V_{DS} Overcurrent and V_{GS} Gate Fault Monitors
  - Dedicated Driver Disable Pin (DRVOFF)
  - Fault Condition Indicator Pin (nFLT)
  - Device Thermal Warning and Shutdown
  - Charge Pump for Reverse Polarity MOSFET
  - Off State Open Load and Short Circuit Diagnostics
  - Sleep-Mode Motor Brake
  - Limp Home Function
- MSL Rating: MSL1
- QFN5×5-32 Package (Wettable)
- AEC-Q100 Qualified

Applications

- Power Seat Modules
- Power Trunk and Lift Gate
- Door Module
- Automotive Brushed DC Motors
- Body Control Modules

Typical Application

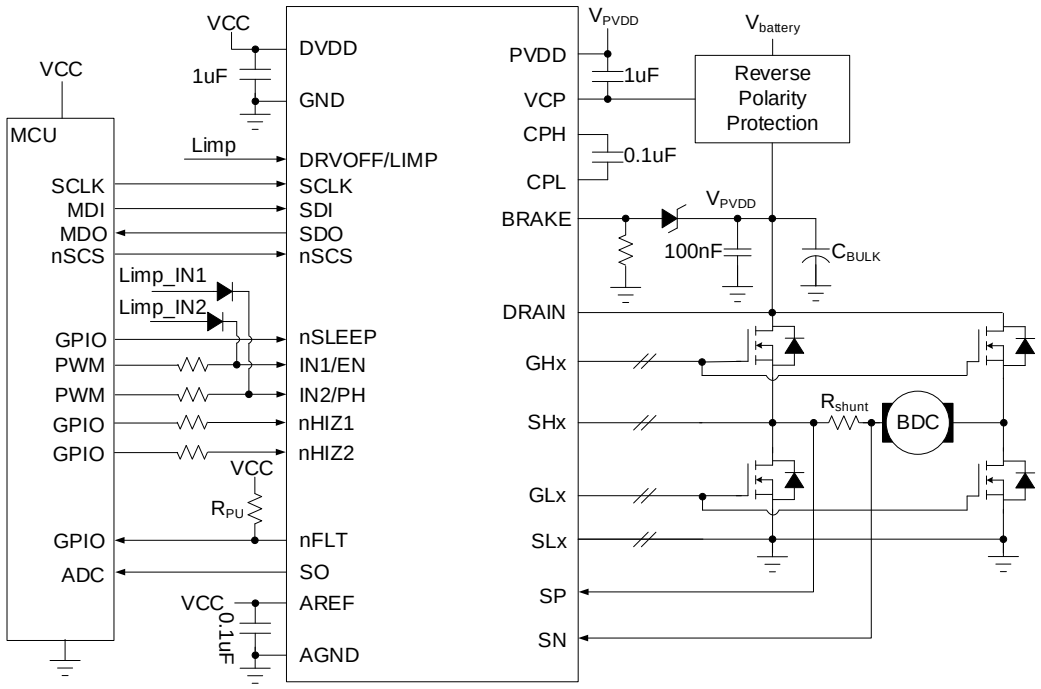


Figure 1. SA52902 Typical Application Circuit

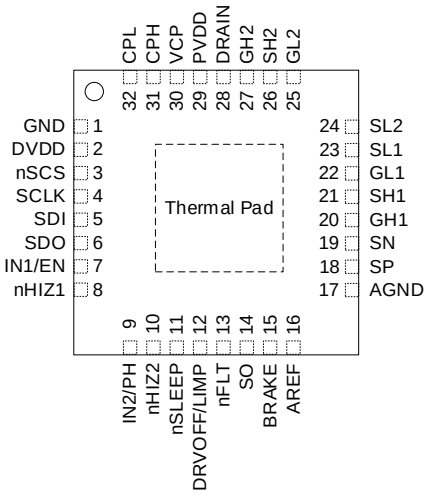
Ordering Information

Ordering Part Number	Package Type	Top Mark
SA52902QEQ	QFN5×5-32 RoHS Compliant and Halogen Free	***HNB**xyz*

Device code: HNB

x=year code, y=week code, z= lot number code

Pinout (Top View)



Pin No	Pin Name	IO	Type	Pin Description
1	GND	IO	Ground	Device ground. Connect this pin to the system ground.
2	DVDD	I	Power	Supplies power to the device's logic and digital output circuits. A 1.0μF, 6.3V ceramic capacitor should be placed between DVDD and GND pins for stable operation.
3	nSCS	I	Digital	Serial chip select. Driving this pin low activates SPI communication. Includes an internal pullup resistor.
4	SCLK	I	Digital	Serial clock input. Serial data is transmitted and received on the corresponding rising and falling edges of this pin. Includes an internal pulldown resistor.
5	SDI	I	Digital	Serial data input. Data is received on the falling edge of the SCLK pin. Includes an internal pulldown resistor.
6	SDO	O	Digital	Serial data output. Data is transmitted on the rising edge of the SCLK pin. Push-pull output.
7	IN1/EN	I	Digital	Half-bridge control input. Refer to PWM mode description for details. Internal pulldown.
8	nHIZ1	I	Digital	Half-bridge control input. Refer to PWM mode description for details. Internal pulldown.
9	IN2/PH	I	Digital	Half-bridge control input. Refer to PWM mode description for details. Internal pulldown.
10	nHIZ2	I	Digital	Half-bridge control input. Refer to PWM mode description for details. Internal pulldown.
11	nSLEEP	I	Digital	Device enable pin. Driving this pin low will shut down the device and it will enter sleep mode. Includes an internal pulldown resistor.
12	DRVOFF/ LIMP	I	Digital	Multi-function pin for either driver shutdown input or Limp home input. When used as DRVOFF, logic high to pull down both high-side and low-side gate driver output. When used as LIMP, logic high to activate the limp home function.
13	nFLT	O	Digital	Fault indicator output. This pin is driven low to signal a fault condition. Open-drain output. Requires an external pull up resistor.
14	SO	O	Analog	Shunt amplifier output.
15	BRAKE	I	Digital	Powered-off braking pin. A logic high enables low-side gate drivers while in low-power sleep mode. Includes an internal pulldown resistor.
16	AREF	I	Power	Provides external voltage reference and power supply for the current sense amplifiers. Connect a 0.1μF, 6.3V ceramic capacitor between AREF and AGND.
17	AGND	IO	Power	Device ground. Connect to system ground.
18	SP	I	Analog	Positive input of the shunt amplifier. Connect to the positive terminal of the current shunt resistor.

19	SN	I	Analog	Negative input of the shunt amplifier. Connect to the negative terminal of the current shunt resistor.
20	GH1	O	Analog	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
21	SH1	I	Analog	High-side source sense input. Connect to the high-side power MOSFET source.
22	GL1	O	Analog	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
23	SL1	I	Analog	Low-side MOSFET gate drive sense and power return. Connect to system ground with low impedance path to the low-side MOSFET ground return.
24	SL2	I	Analog	Low-side MOSFET gate drive sense and power return. Connect to system ground with low impedance path to the low-side MOSFET ground return.
25	GL2	O	Analog	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
26	SH2	I	Analog	High-side source sense input. Connect to the high-side power MOSFET source.
27	GH2	O	Analog	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
28	DRAIN	I	Analog	Voltage sense input for the bridge MOSFET drains. Connect to the common node of the high-side MOSFET drains.
29	PVDD	I	Power	Device driver power supply input. Connect to the bridge power supply. Connect a 0.1μF, PVDD-rated ceramic capacitor and local bulk capacitance greater than or equal to 10μF between PVDD and GND.
30	VCP	IO	Power	Charge pump output. Connect a 1μF, 16V ceramic capacitor between VCP and PVDD.
31	CPH	IO	Power	Charge pump switching node. Connect a 100nF, PVDD-rated ceramic capacitor between CPH and CPL.
32	CPL	IO	Power	Charge pump switching node. Connect a 100nF, PVDD-rated ceramic capacitor between CPH and CPL.

Block Diagram

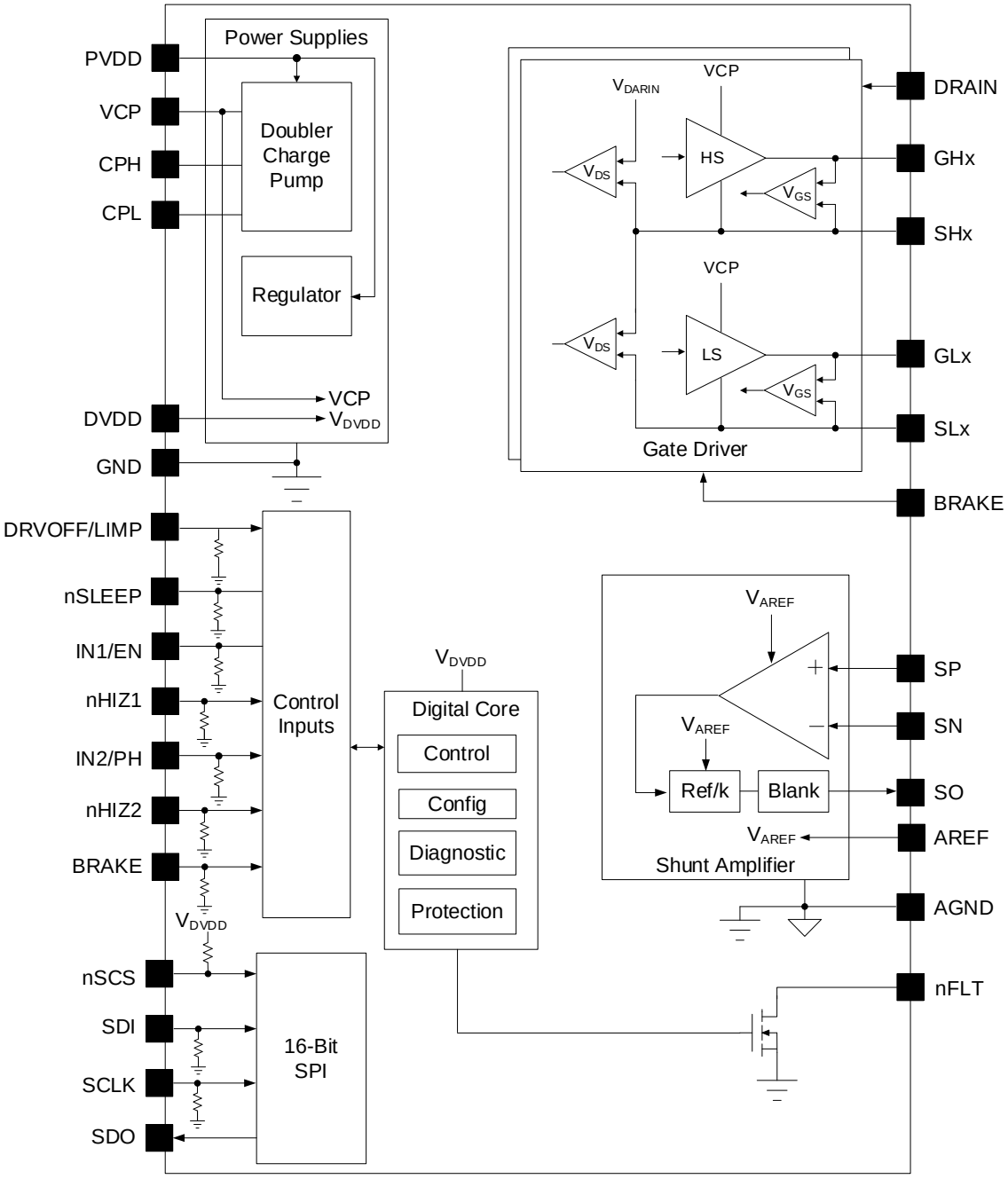


Figure 2. SA52902 Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)		**Min.**	**Max.**	**Unit**
PVDD		-0.3	40	V
DRAIN		-0.3	40	V
AGND/GND		-0.3	0.3	V
VCP		-0.3	55	V
CPH		V_{PVDD}-0.3	V_{VCP}+0.3	V
CPL		-0.3	V_{PVDD}+0.3	V
DVDD		-0.3	5.75	V
DRVOFF/LIMP, IN1/EN, IN2/PH, nHIZx, nSLEEP, nSCS, SCLK, SDI, BRAKE		-0.3	5.75	V
nFLT,SDO		-0.3	V_{DVDD}+0.3	V
GHx		-2	V_{VCP}+0.3	V
GHx (transient 1μs)		-5	V_{VCP}+0.3	V
GHx (with respect to SHx)		-0.3	13.5	V
SHx		-2	40	V
SHx(transient 1μs)		-5	40	V
GLx		-2	13.5	V
GLx (transient 1μs)		-3	13.5	V
GLx (with respect to PGNDx)		-0.3	13.5	V
SLx		-2	2	V
SLx (transient 1μs)		-3	3	V
AREF		-0.3	5.75	V
SN, SP		-2	V_{VCP}+0.3	V
SN, SP (transient 1μs)		-5	V_{VCP}+0.3	V
SN, SP (differential voltage)		-5.75	5.75	V
Electrostatic Discharge	HBM (Human Body Model)	2000		V
	CDM (Charge Device Model) corner pins	750		
	CDM (Charge Device Model) other pins	500		
Ambient Temperature Range		-40	125	°C
Junction Temperature (T_J)		-40	150	°C
Storage Temperature		-55	150	°C

Thermal Information

Parameter (Note 2)	**Value**	**Unit**
θ_{JA} Junction-to-Ambient Thermal Resistance (QFN5×5-32)	40.8	°C/W
$\theta_{JC\ TOP}$ Junction-to-Case Thermal Resistance (QFN5×5-32)	7.6	

Recommended Operating Conditions (All voltages are referenced to GND unless otherwise noted.)

Parameter (Note 3)	**Min.**	**Max.**	**Unit**
Driver Power Supply Voltage, PVDD	4.9	37	V
High Side Average Gate Drive Current, GHx	0	15	mA
Low Side Average Gate Drive Current, GLx	0	15	mA
Digital Power Supply Voltage, DVDD	3	5.5	V
Digital Input Voltage, DRVOFF/ LIMP, IN1/EN, IN2/PH, nHIZx, nSLEEP, nSCS, SCLK, SDI, BRAKE	0	5.5	V
Digital Output Current (SDO)	0	5	mA

Open Drain Pullup Voltage, nFLT	0	5.5	V
Open Drain Output Current, nFLT	0	5	mA
Amplifier Reference Supply Voltage, AREF	3	5.5	V
Amplifier Output Current, SO	0	5	mA
Operation Ambient Temperature Range	-40	125	°C
Operation Junction Temperature Range	-40	150	°C

Electrical Characteristics

T_A =-40°C to 125°C, V_{PVDD}=4.9V to 37V, Typical V_{PVDD}=13.5V and T_A=25°C, unless otherwise specified. (Note 4)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power Supply Current(DRAIN,DVDD,PVDD,VCP)						
PVDD Sleep Mode Current	I_{PVDDQ}	V_{PVDD},V_{DRAIN}=13.5V,nSLEEP=0V		3.5	5	μA
DRAIN Sleep Mode Current	I_{DRAINQ}	V_{PVDD},V_{DRAIN}=13.5V,nSLEEP=0V		0.1	1	μA
DVDD Sleep Mode Current	I_{DVDDQ}	V_{PVDD},V_{DRAIN}=13.5V,nSLEEP=0V		0.1	2	μA
PVDD Active Mode Current	I_{PVDD}	V_{PVDD}, V_{DRAIN}=13.5V,nSLEEP=5V		4	6	mA
DRAIN Active Mode Current	I_{DRAIN}	V_{PVDD}, V_{DRAIN} =13.5V, nSLEEP=5V, V_{DS_LVL}≤500mV		335	410	μA
DVDD Active Mode Current	I_{DVDD}	V_{DVDD}=5V,SDO=0V		2	3.5	mA
Digital Oscillator Switching Frequency	f_{OSC}	Primary frequency of spread spectrum		14.25		MHz
Turn on Time	t_{WAKE}	nSLEEP =5V to active mode			1	ms
Turn off Time	t_{SLEEP}	nSLEEP =0V to sleep mode			1	ms
Charge Pump Regulator Voltage with Respect to PVDD Double Mode	V_{VCP}	V_{PVDD} ≥13V, I_{VCP}≤ 15mA	9.5	10.5	11	V
		V_{PVDD} =11V, I_{VCP}≤15mA (Note 5)	8.4	10	11	
		V_{PVDD} =9V, I_{VCP}≤ 11mA	6.95	8	9	
		V_{PVDD} =7V, I_{VCP}≤ 7.5mA (Note 5)	5.4	6	7	
		V_{PVDD}=5.5V, I_{VCP}≤5mA	4.35	5	5.5	
Charge Pump Switching Frequency	f_{VCP}	Primary frequency of spread spectrum		400		kHz
Logic-Level Inputs(BRAKE,DRVOFF/LIMP,IN1/EN,IN2/PH,nHIZx,nSLEEP,nSCS,SCLK,SDI)						
Logic “1” Input Voltage	V_{IH}	DRVOFF/LIMP, IN1/EN, IN2/PH, nHIZx, nSLEEP, SCLK, SDI	V_{DVDD}*0.7		V_{DVDD}	V
		BRAKE	1.8		V_{DVDD}	
Logic “0” Input Voltage	V_{IL}	DRVOFF/LIMP, IN1/EN, IN2/PH, nHIZx, nSLEEP, SCLK, SDI	0		V_{DVDD}*0.3	
		BRAKE	0.6			
Input Voltage Hysteresis	V_{IHYS}	DRVOFF/LIMP, IN1/EN, IN2/PH, nHIZx, nSLEEP, SCLK, SDI		V_{DVDD}*0.1		
		BRAKE		0.3		
High Level Logic Bias Current	I_{INH}	V_{DIN}=5V, DRVOFF, IN1/EN, IN2/PH, nHIZx, nSLEEP, SCLK, SDI		50	100	μA
		V_{DIN}=5V, V_{DVDD}=5V, nSCS	-1		1	
		V_{DIN}=5V, nSLEEP=0V, BRAKE		5		
		V_{DIN}=5V, nSLEEP=5V, BRAKE		47.5		
Low Level Logic Bias Current	I_{INL}	V_{DIN}=0V,BRAKE,DRVOFF/nFLT, IN1/EN,IN2/PH, nSLEEP, SCLK, SDI	-1		1	
		V_{DIN}=0V, nSCS		50	80	
Input Pulldown Resistance	R_{PD}	To GND, DRVOFF, IN1/EN, IN2/PH, nHIZx, nSLEEP, SCLK, SDI	50	100	150	kΩ
		To GND, nSLEEP=0V, BRAKE		1000		
		To GND, nSLEEP=5V, BRAKE		100		
Input Pullup resistance	R_{PU}	To DVDD, nSCS	50	100	150	
Logic-Level Outputs (nFLT, SDO)						
Output Logic Low Voltage	V_{OL}	I_{DOUT} = 5mA			0.5	V
Output Logic High Voltage	V_{OH}	I_{DOUT} =-5mA, SDO	V_{DVDD}*0.8			
Open-drain Logic High Current	I_{ODZ}	V_{OD} = 5V, nFLT	-1		1	μA
Gate Drivers (GHx, GLx)						
GHx Low Level Output Voltage	V_{GHx_L}	I_{DRVN_HS} = I_{STRONG}, I_{GHx} = 1mA, GHx to SHx	0		0.25	V
GLx Low Level Output Voltage	V_{GLx_L}	I_{DRVN_LS} = I_{STRONG}, I_{GLx} = 1mA, GLx to SLx	0		0.25	V
GHx High Level Output Voltage	V_{GHx_H}	I_{DRVP_HS} = I_{HOLD}, I_{GHx} = 1mA, VCP to GHx	0		0.25	V
GLx High Level Output Voltage	V_{GLx_H}	I_{DRVP_LS} = I_{HOLD}, I_{GLx} = 1mA, 10.5V≤V_{PVDD}≤37V, GLx to SLx	8.35	10.5	12.5	V
		I_{DRVP_LS} = I_{HOLD}, I_{GLx} = 1mA, 4.9V ≤ V_{PVDD} ≤ 10.5V, GLx to SLx		8.3		V
Peak Gate Current (source) SPI Control	I_{DRVP_SPI}	I_{DRVP_x}=0000b, V_{GSx}=3V V_{PVDD}≥7V	0.2	0.5	0.8	mA
		I_{DRVP_x}=0001b, V_{GSx}=3V V_{PVDD}≥7V	0.5	1	1.5	
		I_{DRVP_x}=0010b, V_{GSx}=3V V_{PVDD}≥7V	1.3	2	2.7	
		I_{DRVP_x}=0011b, V_{GSx}=3V V_{PVDD}≥7V	2.1	3	3.9	
		I_{DRVP_x}=0100b, V_{GSx}=3V V_{PVDD}≥7V	2.9	4	5.1	
		I_{DRVP_x}=0101b, V_{GSx}=3V V_{PVDD}≥7V	4.5	6	7.5	
		I_{DRVP_x}=0110b, V_{GSx}=3V V_{PVDD}≥7V	6	8	10	

		I_{DRVP_x}=0111b, V_{GSx}=3V V_{PVDD}≥7V	9	12	15	
		I_{DRVP_x}=1000b, V_{GSx}=3V V_{PVDD}≥7V	12	16	20	
		I_{DRVP_x}=1001b, V_{GSx}=3V V_{PVDD}≥7V	15	20	25	
		I_{DRVP_x}=1010b, V_{GSx}=3V V_{PVDD}≥7V	18	24	30	
		I_{DRVP_x}=1011b, V_{GSx}=3V V_{PVDD}≥7V	21	28	35	
		I_{DRVP_x}=1100b, V_{GSx}=3V V_{PVDD}≥7V	23.25	32	38.75	
		I_{DRVP_x}=1101b, V_{GSx}=3V V_{PVDD}≥7V	26.5	40	50	
		I_{DRVP_x}=1110b, V_{GSx}=3V V_{PVDD}≥7V	28	48	60	
		I_{DRVP_x}=1111b, V_{GSx}=3V V_{PVDD}≥7V	30	62	77.5	
Peak Gate Current (sink) SPI Control	I_{DRVN_SPI}	I_{DRVN_x}=0000b, V_{GSx}=3V V_{PVDD}≥7V	0.15	0.5	0.85	mA
		I_{DRVN_x}=0001b, V_{GSx}=3V V_{PVDD}≥7V	0.35	1	1.65	
		I_{DRVN_x}=0010b, V_{GSx}=3V V_{PVDD}≥7V	0.85	2	3.15	
		I_{DRVN_x}=0011b, V_{GSx}=3V V_{PVDD}≥7V	1.4	3	4.6	
		I_{DRVN_x}=0100b, V_{GSx}=3V V_{PVDD}≥7V	2.1	4	5.9	
		I_{DRVN_x}=0101b, V_{GSx}=3V V_{PVDD}≥7V	3.5	6	8.5	
		I_{DRVN_x}=0110b, V_{GSx}=3V V_{PVDD}≥7V	5	8	11	
		I_{DRVN_x}=0111b, V_{GSx}=3V V_{PVDD}≥7V	8	12	16	
		I_{DRVN_x}=1000b, V_{GSx}=3V V_{PVDD}≥7V	11.5	16	20	
		I_{DRVN_x}=1001b, V_{GSx}=3V V_{PVDD}≥7V	14.7	20	25	
		I_{DRVN_x}=1010b, V_{GSx}=3V V_{PVDD}≥7V	18	24	30	
		I_{DRVN_x}=1011b, V_{GSx}=3V V_{PVDD}≥7V	21	28	35	
		I_{DRVN_x}=1100b, V_{GSx}=3V V_{PVDD}≥7V	23.25	32	38.75	
		I_{DRVN_x}=1101b, V_{GSx}=3V V_{PVDD}≥7V	30	40	52	
		I_{DRVN_x}=1110b, V_{GSx}=3V V_{PVDD}≥7V	36	48	62	
		I_{DRVN_x}=1111b, V_{GSx}=3V V_{PVDD}≥7V	46.5	62	80	
Gate Pullup Hold Current	I_{HOLD}	V_{PVDD}≥7V ,V_{GSx} =3V	5	16	30	mA
Gate Pulldown Strong Current	I_{STRONG}	V_{PVDD}≥7V V_{GSx} =3V, I_{DRV}= 0.5 to 12mA	30	62	100	mA
		V_{PVDD}≥7V, V_{GSx} =3V, I_{DRV}= 16 to 62mA	45	128	205	
Low-side Semi-Active Gate Pulldown	R_{PDSA_LS}	GLx to SLx, V_{GSx} = 3V		2.7		kΩ
		GLx to SLx, V_{GSx} = 1V		5		
High-Side Passive Gate Pulldown Resistor	R_{PD_HS}	GHx to SHx		150		
Low-Side Passive Gate Pulldown Resistor	R_{PD_LS}	GLx to SLx		150		
Switch-Node Sense Leakage Current	I_{SHx}	Into SHx, SHx =DRAIN≤ 37V, GHx–SHx=0V, nSLEEP=0V	-1		1	µA
		Into SHx, SHx = DRAIN ≤ 37V, GHx–SHx=0V, nSLEEP=5V	-150	-100		
Gate Driver Timings (GHx, GLx)						
Low-Side Rising Propagation Delay	t_{PDR_LS}	Input to GLx rising		300	600	ns
Low-Side Falling Propagation Delay	t_{PDF_LS}	Input to GLx falling				
High-Side Rising Propagation Delay	t_{PDR_HS}	Input to GHx rising				
High-Side Falling Propagation Delay	t_{PDF_HS}	Input to GHx falling				
Internal Handshake Dead-Time	t_{DEAD}	GLx/GHx falling 10% to GHx/GLx rising 10%		350		ns
Insertable Digital Dead-Time SPI Device	$t_{DEAD\_D\_SPI}$	VGS_TDEAD=000b, Handshake only		0		ns
		VGS_TDEAD=001b	150	250	350	
		VGS_TDEAD=010b	400	500	600	
		VGS_TDEAD=011b	600	750	900	
		VGS_TDEAD=100b	800	1000	1200	
		VGS_TDEAD=101b	1600	2000	2400	
		VGS_TDEAD=110b	3400	4000	4600	
		VGS_TDEAD=111b	7200	8000	8800	
Current Shunt Amplifiers (AREF,SNx,SOx,SPx)						
Common Mode Input Range	V_{COM}		-2		V_{PVDD}+2	V
Sense Amplifier Gain SPI Device	$G_{CSA,\ SPI}$	CSA_GAIN = 00b	9.75	10	10.25	V/V
		CSA_GAIN = 01b	19.5	20	20.5	
		CSA_GAIN = 10b	39	40	41	
		CSA_GAIN = 11b	78	80	82	
Sense Amplifier Settling Time to ±1%	t_{SET}	V_{SO_STEP}=1.5V, G_{CSA}=10V/V, C_{SO}=60pF (Note 5)		2.2		µs
		V_{SO_STEP}=1.5V, G_{CSA}=20V/V, C_{SO}=60pF (Note 5)		2.2		
		V_{SO_STEP}=1.5V, G_{CSA}=40V/V, C_{SO}=60pF (Note 5)		2.2		
		V_{SO_STEP}=1.5V, G_{CSA}=80V/V, C_{SO}=60pF (Note 5)		3		
Sense Amplifier Output Blanking Time SPI Device	$t_{BLK,\ SPI}$	CSA_BLK = 000b, % of t_{DRIVE} period		0		%
		CSA_BLK = 001b, % of t_{DRIVE} period		25		

		CSA_BLK = 010b, % of t_{DRIVE} period		37.5		
		CSA_BLK = 011b, % of t_{DRIVE} period		50		
		CSA_BLK = 100b, % of t_{DRIVE} period		62.5		
		CSA_BLK = 101b, % of t_{DRIVE} period		75		
		CSA_BLK = 110b, % of t_{DRIVE} period		87.5		
		CSA_BLK = 111b, % of t_{DRIVE} period		100		
Output Slew Rate	t_{SLEW}	C_{SO}=60pF		2.5		V/μs
Output Voltage Bias SPI Device	V_{BIAS_SPI}	V_{SPx}=V_{SNx}=0V, CSA_DIV=0b		V_{AREF}/2		V
		V_{SPx}=V_{SNx}=0V, CSA_DIV=1b		V_{AREF}/8		
Linear Output Voltage Range	V_{LINEAR}	V_{AREF}=3.3V, V_{AREF} =5V	0.25		V_{AREF}-0.25	V
Input Offset Voltage	V_{OFF}	V_{SPx}=V_{SNx}=0V, T_J=25°C	-1.5		1.5	mV
Input Offset Voltage Drift	V_{OFF_D}	V_{SPx}=V_{SNx}=0V (Note 5)		±10	±25	μV/°C
Input Bias Current	I_{BIAS}	V_{SPx} = V_{SNx} = 0V			10	μA
Input Bias Current Offset	I_{BIAS_OFF}	I_{SPx}–I_{SNx}	-1		1	μA
AREF Input Current	I_{AREF}	V_{AREF} =3.3V, V_{AREF} =5V		1	1.8	mA
Common Mode Rejection Ratio	CMRR	DC, –40≤ T_J≤ 125°C		80		dB
Power Supply Rejection Ratio	PSRR	PVDD to SOx, DC , –40≤ T_J≤ 125°C		100		dB
		PVDD to SOx, 20kHz (Note 5)		90		
		PVDD to SOx, 400kHz (Note 5)		70		
Protection						
PVDD Undervoltage Threshold	V_{PVDD_UV}	V_{PVDD} rising	4.325	4.625	4.9	V
		V_{PVDD} falling	4.25	4.525	4.8	
PVDD Undervoltage Hysteresis	$V_{PVDD\_UV\_HYS}$	Rising to falling threshold		100		mV
PVDD Undervoltage Deglitch Time	$t_{PVDD\_UV\_DG}$		8	10	12.75	μs
PVDD Overvoltage Threshold	V_{PVDD_OV}	V_{PVDD} rising, PVDD_OV_LVL=0b	21	22.5	24	V
		V_{PVDD} falling, PVDD_OV_LVL=0b	20	21.5	23	
		V_{PVDD} rising, PVDD_OV_LVL=1b	27	28.5	30	
		V_{PVDD} falling, PVDD_OV_LVL=1b	26	27.5	29	
PVDD Overvoltage Hysteresis	$V_{PVDD\_OV\_HYS}$	Rising to falling threshold		1		V
PVDD Overvoltage Deglitch Time	$t_{PVDD\_OV\_DG}$	PVDD_OV_DG = 00b	0.75	1	1.5	μs
		PVDD_OV_DG = 01b	1.5	2	2.5	
		PVDD_OV_DG = 10b	3.25	4	4.75	
		PVDD_OV_DG = 11b	7	8	9	
DVDD Supply POR Threshold	V_{DVDD_POR}	DVDD falling	2.5	2.7	2.9	V
		DVDD rising	2.6	2.8	3	
DVDD POR Hysteresis	$V_{DVDD\_POR\_HYS}$	Rising to falling threshold		100		mV
DVDD POR Deglitch Time	$t_{DVDD\_PRO\_DG}$		5	8	12.75	μs
Charge Pump Undervoltage Threshold SPI Device	$V_{CP\_UV\_SPI}$	V_{VCP}-V_{PVDD}, V_{VCP} falling V_{VCP_UV}=0b	3	3.6	4.2	V
		V_{VCP}-V_{PVDD}, V_{VCP} falling V_{VCP_UV}=1b	4	5	6	
Charge Pump Undervoltage Deglitch Time	$t_{CP\_UV\_DG}$		8	10	12.75	μs
High-Side Driver V_{GS} Protection Clamp	V_{GS_CLP}		12	13.5	15.5	V
Gate Voltage Monitor Threshold SPI Device	V_{GS_LVL}	V_{GHx}–V_{SHx}, V_{GLx}–V_{SLx} VGS_LVL=0b	1.1	1.4	1.75	V
		V_{GHx}–V_{SHx}, V_{GLx}–V_{SLx} VGS_LVL=1b	0.8	1	1.2	V
V_{GS} Fault Monitor Deglitch Time	$t_{GS\_FLT\_DG}$		1.5	2	2.75	μs
V_{GS} Handshake Monitor Deglitch Time	$t_{GS\_HS\_DG}$	(Note 5)		70		ns
V_{GS} and V_{DS} Monitor Blanking Time SPI Device	t_{DRIVE_SPI}	VGS_TDRV = 00b	80	96	100	μs
		VGS_TDRV = 01b	1.5	2	2.5	
		VGS_TDRV = 10b	3.25	4	4.75	
		VGS_TDRV = 11b	7.5	8	9	
V_{DS} Overcurrent Protection Threshold SPI Device	$V_{DS\_LVL\_SPI}$	VDS_LVL = 0000b	0.03	0.06	0.095	V
		VDS_LVL = 0001b	0.05	0.08	0.115	
		VDS_LVL = 0010b	0.07	0.1	0.135	
		VDS_LVL = 0011b	0.09	0.12	0.155	
		VDS_LVL = 0100b	0.11	0.14	0.175	
		VDS_LVL = 0101b	0.13	0.16	0.195	
		VDS_LVL = 0110b	0.15	0.18	0.22	
		VDS_LVL = 0111b	0.17	0.2	0.245	
		VDS_LVL = 1000b	0.27	0.3	0.345	
		VDS_LVL = 1001b	0.36	0.4	0.45	
		VDS_LVL = 1010b	0.45	0.5	0.55	
		VDS_LVL = 1011b	0.54	0.6	0.66	
		VDS_LVL = 1100b	0.63	0.7	0.77	

		VDS_LVL = 1101b	0.9	1	1.1	
		VDS_LVL = 1110b	1.26	1.4	1.54	
		VDS_LVL = 1111b	1.8	2	2.2	
V_{DS} Overcurrent Protection Deglitch Time SPI Device	$t_{DS\_DG\_SPI}$	VDS_DG = 00b	0.75	1	1.5	µs
		VDS_DG = 01b	1.5	2	2.5	
		VDS_DG = 10b	3.25	4	4.75	
		VDS_DG = 11b	7.5	8	9	
Offline Diagnostic Current Source	I_{OLD}	Pull up current		3		mA
		Pull down current		3		
Offline State Open Load Resistance Detection Threshold	R_{OLD}	VDS_LVL=1.4V, V_{DRAIN}=V_{PVDD}=13.5V (Note 5)		22		kΩ
		VDS_LVL=2V, V_{DRAIN}=V_{PVDD}=13.5V (Note 5)		10		
Power Off Braking Gate Source Current	I_{POB_P}			15		mA
Power Off Braking Gate Sink Current	I_{POB_N}			17		mA
Power Off Braking Gate Pull Up Voltage	V_{POB}	V_{PVDD} ≥ 8V	5.5		12.5	V
Power Off Braking Turn-On Time	t_{POB_ON}			13		µs
Power Off Braking Turn-Off Time	t_{POB_OFF}			2.5		µs
Power Off Braking V_{DS} Comparator Threshold	V_{POB_VDS}	Rising	250	350	450	mV
Power Off Braking V_{DS} Comparator Deglitch Time	t_{POB_VDS}		1.5	4	6	µs
Thermal Warning Temperature	T_{OTW}	T_J Rising	125	145	170	°C
Thermal Warning Hysteresis	T_{HYS}			25		
Thermal Shutdown Temperature	T_{OTSD}	T_J Rising	150	165	190	
Thermal Shutdown Hysteresis	T_{HYS}			25		

SPI Timing

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SCLK Minimum Period	t_{SCLK}	(Note 5)	100			ns
SCLK Minimum High Time	t_{SCLKH}	(Note 5)	50			
SCLK Minimum Low Time	t_{SCLKL}	(Note 5)	50			
SDI Input Data Setup Time	t_{SU_SDI}	(Note 5)	25			
SDI Input Data Hold Time	t_{H_SDI}	(Note 5)	25			
SDO Output Data Delay Time, C_L=20pF	t_{D_SDO}	(Note 5)			30	
nSCS Input Setup Time	t_{SU_nSCS}	(Note 5)	25			
nSCS Input Hold Time	t_{H_nSCS}	(Note 5)	25			
nSCS Minimum High Time	t_{HI_nSCS}	(Note 5)	450			
Enable Delay Time, nSCS Low to SDO active	t_{EN_nSCS}	(Note 5)			50	
Disable Delay Time, nSCS High to SDO Hi-Z	t_{DIS_nSCS}	(Note 5)			50	

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured under still air while T_A=25°C, and chip mounted on a highly effective four-layer test board with thermal vias.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \approx T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

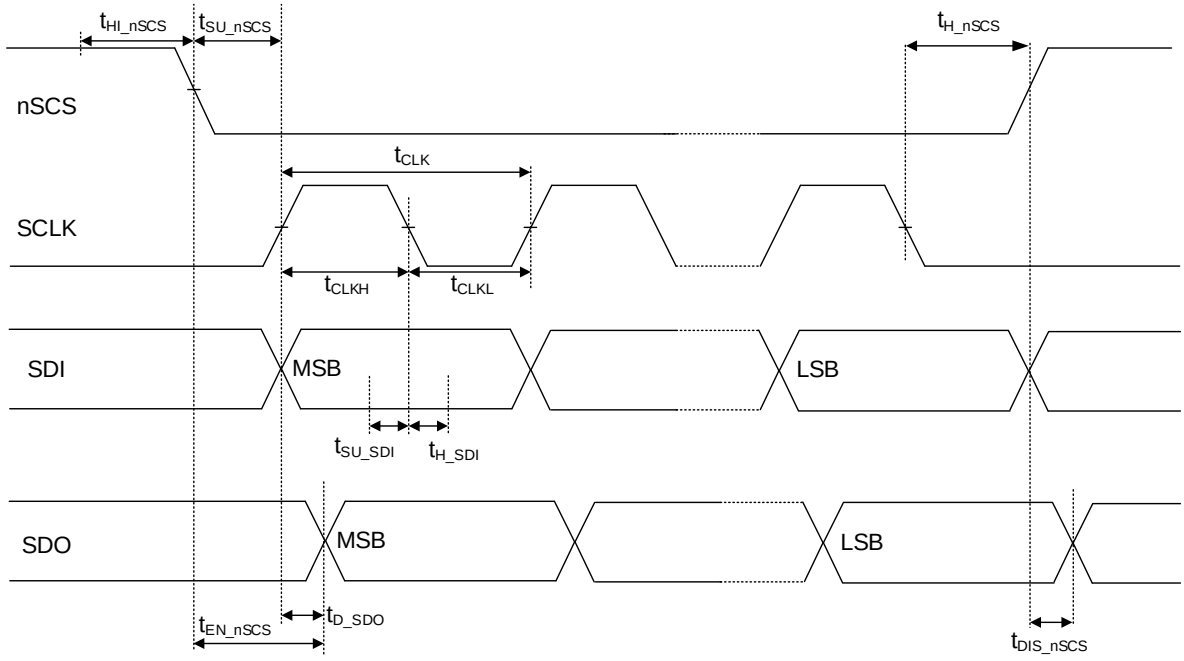
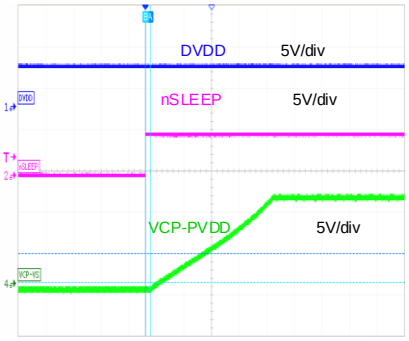


Figure 3. SPI Timing Diagram

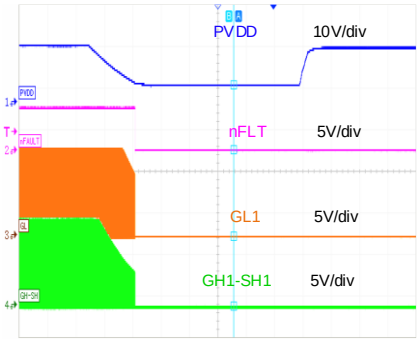
Typical Performance Characteristics

Charge Pump Setup
(CH1:DVDD CH2:nSLEEP CH4:VCP-PVDD)



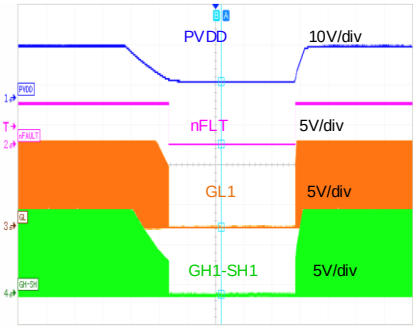
Time (100μs/div)

PWM Operation During PVDD_UV Latch
(CH1:PVDD CH2:nFLT CH3:GL1 CH4:GH1-SH1)



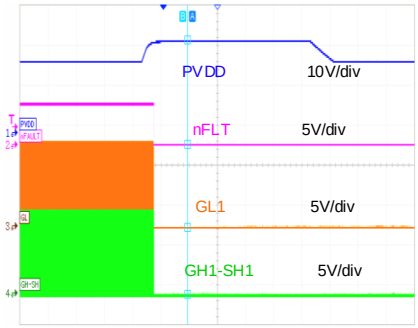
Time (200ms/div)

PWM Operation During PVDD_UV Automatic Recovery
(CH1:PVDD CH2:nFLT CH3:GL1 CH4:GH1-SH1)



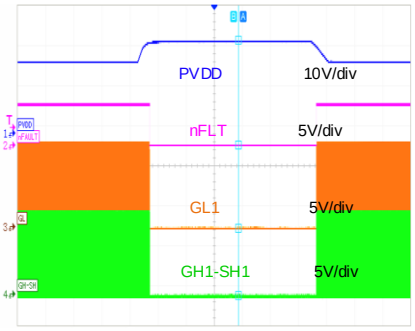
Time (200ms/div)

PWM Operation During PVDD_OV Latch
(CH1:PVDD CH2:nFLT CH3:GL CH4:GH-SH)



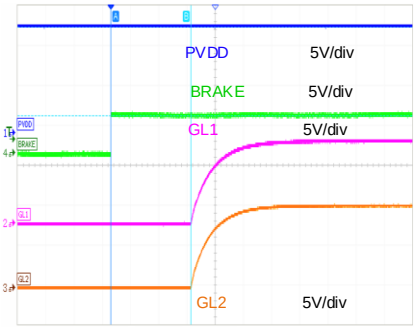
Time (200ms/div)

PWM Operation During PVDD_OV Automatic Recovery
(CH1:PVDD CH2:nFLT CH3:GL1 CH4:GH1-SH1)



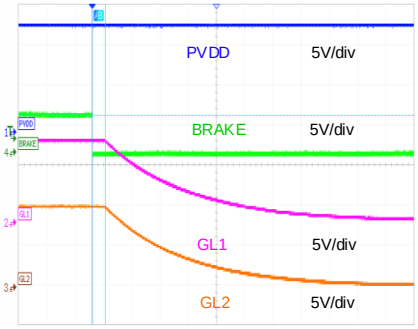
Time (200ms/div)

BRAKE On Triggers POB
(CH1:PVDD CH2:GL1 CH3:GL2 CH4:BRAKE)



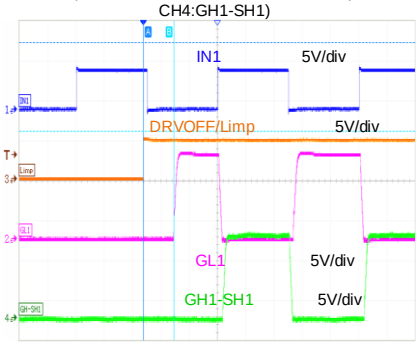
Time (5μs/div)

BRAKE Off Exits POB
(CH1:PVDD CH2:GL1 CH3:GL2 CH4:BRAKE)



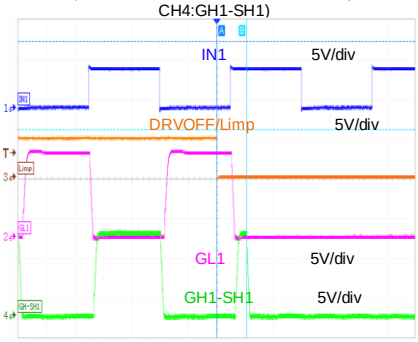
Time (5μs/div)

Pull-Up DRVOFF/Limp Enter Limp Home Mode
(CH1:IN1 CH2:GL1 CH3:DRVOFF/Limp CH4:GH1-SH1)



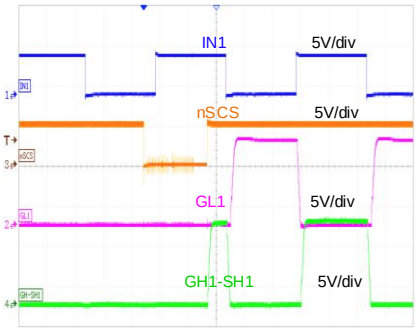
Time (10μs/div)

Pull-Down DRVOFF/Limp Exit Limp Home Mode
(CH1:IN1 CH2:GL1 CH3:DRVOFF/Limp CH4:GH1-SH1)



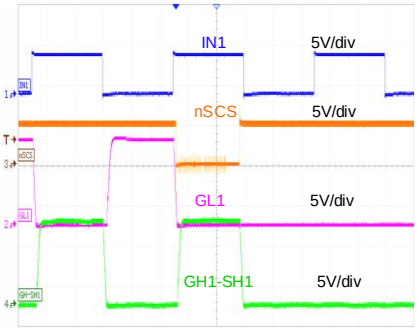
Time (10μs/div)

EN_DRV=1b Enable Gate Driver
(CH1:IN1 CH2:GL1 CH3:nSCS CH4:GH1-SH1)



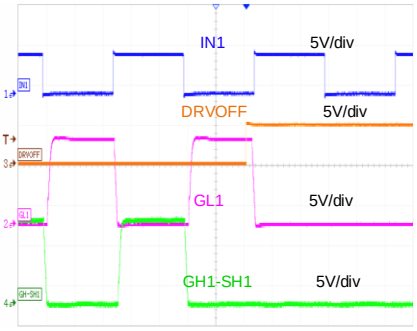
Time (10μs/div)

EN_DRV=0b Disable Gate Driver
(CH1:IN1 CH2:GL1 CH3:nSCS CH4:GH1-SH1)



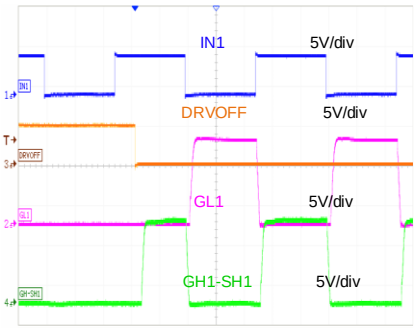
Time (10μs/div)

Pull Up DRVOFF Pin Disable Gate Driver
(CH1:IN1 CH2:GL1 CH3:DRVOFF CH4:GH1-SH1)



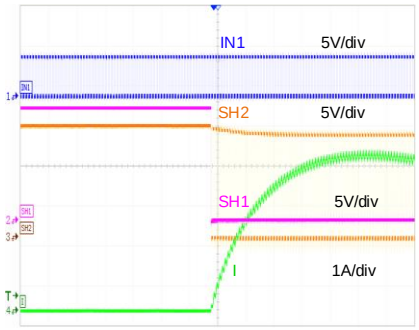
Time (10μs/div)

Pull Down DRVOFF Enable Gate Driver
(CH1:IN1 CH2:GL1 CH3:DRVOFF CH4:GH1-SH1)



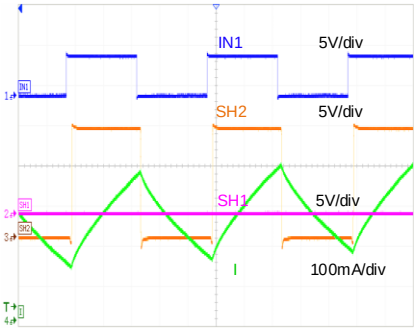
Time (10μs/div)

Motor Driver Startup
(CH1:IN1 CH2:SH1 CH3:SH2 CH4:I)



Time (500μs/div)

Smooth Operation of the Motor Driver
(CH1:IN1 CH2:SH1 CH3:SH2 CH4:I)



Time (10μs/div)

Detailed Description

Half-Bridge Control

The SA52902 features five PWM modes to accommodate various control schemes and output load configurations. The PWM mode is set through the SPI register settings BRG_MODE / EN_LIMP and the LIMP pin. The modes are detailed below, along with additional information regarding their functions. For SPI device variants, the gate driver outputs can be controlled through both the IN1/EN, IN2/PH, nHIZx input pins, the S_IN1/EN, S_IN2/PH, and S_nHIZx register settings.

Table 1. Input PWM Modes

PWM Mode	SPI Interface(BRG_MODE)	EN_LIMP	LIMP PIN
Limp Home Control	X	1	H
Half-Bridge Control	00b	0	X
H-Bridge Control	01b(PH/EN)	0	X
	10b(PWM)	0	X
Split HS and LS Solenoid Control	11b	0	X

Limp Home Control

In limp home mode (fail-safe mode), the input pins IN1/EN and nHIZ1 are routed to SH1, and the input pins IN2/PH and nHIZ2 are routed to SH2. In this mode, the DRVOFF pins and the corresponding register configuration are disabled.

Limp home mode is activated via the LIMP pin. The LIMP pin is multiplexed with the DRVOFF function. When the EN_LIMP register is set to 1 it functions as the LIMP pin; when EN_LIMP is set to 0, it serves as the DRVOFF pin (DRVOFF/LIMP pin).

Table 2. Limp Home Control

Limp	INx	SPI Configure	nHIZx	GHx	GLx	SHx
1	0	x	1	L	H	L
	0	x	0	L	L	HiZ
	1	x	1	H	L	H
	1	x	0	L	L	HiZ

Half-Bridge Control

In half-bridge control mode, each gate driver can be individually operated using the corresponding IN1/EN and IN2/PH input pins. The SA52902 internally handles dead-time generation between the high-side and low-side switches, enabling control of each half-bridge with a single PWM input.

The IN1/EN and IN2/PH signals can be controlled through the SPI registers and input pins. The register setting for S_IN1/EN corresponds to the function of IN1/EN, while the register setting for S_IN2/PH corresponds to the function of IN2/PH. SPI control for IN1/EN and IN2/PH can be enabled through the IN1/EN_MODE and IN2/PH_MODE register settings. Additionally, the nHIZ1/nHIZ2 pin and the S_HIZ1/S_HIZ2 register settings can be used to disable IN1/EN and IN2/PH independently. The HIZ1 signal is the logical OR of the nHIZ1 pin and the S_HIZ1 register setting. The HIZ2 signal is the logical OR of the nHIZ2 pin and the S_HIZ2 register setting.

Table 3. Half-Bridge Control (BRG_MODE=00b)

nHIZx	INx	GHx	GLx	SHx
0	x	L	L	HiZ
1	0	L	H	L
1	1	H	L	H

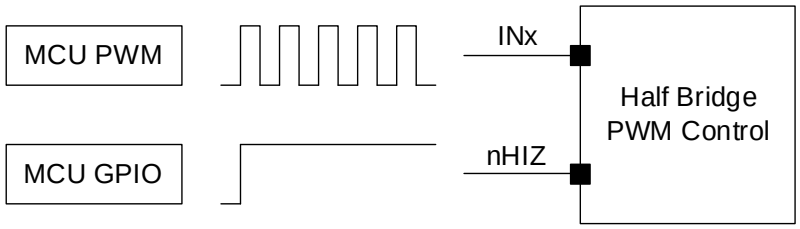


Figure 4. Half Bridge Control

H-Bridge Control

In H-bridge control, both half-bridge gate drivers can be operated as an H-bridge gate driver using the IN1/EN and IN2/PH input pins. The H-bridge mode features two input control schemes that can be configured through the SPI BRG_MODE register setting. The PH/EN mode enables the H-bridge to be controlled using a speed/direction interface commanded by one PWM signal and one GPIO signal. The PWM mode enables a more advanced control scheme that typically requires two PWM signals. This configuration enables the H-bridge driver to achieve four distinct output states, offering enhanced control flexibility when needed. In H-bridge control mode, the default active behavior is low-side active in both PH/EN and PWM modes. For SPI device variants, the freewheeling state can be configured via the BRG_FW register, allowing selection between low-side and high-side active freewheeling. Additionally, the S_HIZx register functions are disabled in the H-bridge control modes. The H-bridge can be placed in a Hi-Z state using either the DRVOFF pin or the EN_DRV register setting.

Table 4. PH/EN H-Bridge Control (BRG_MODE = 01b)

IN1/EN	IN2/PH	BRG_FW	GH1	GL1	GH2	GL2	SH1	SH2	DESCRIPTION
0	X	0b	L	H	L	H	L	L	Low side active freewheel
0	X	1b	H	L	H	L	H	H	High side active freewheel
1	0	X	L	H	H	L	L	H	Drive SH2-> SH1 (Reverse)
1	1	X	H	L	L	H	H	L	Drive SH1-> SH2 (Forward)

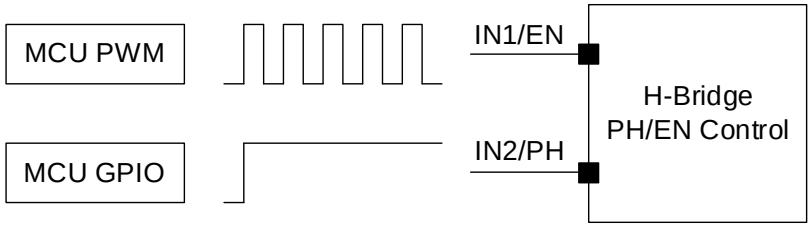


Figure 5. H-Bridge Control PH/EN Mode

Table 5. PWM H-Bridge Control (BRG_MODE = 10b)

IN1/EN	IN2/PH	BRG_FW	GH1	GL1	GH2	GL2	SH1	SH2	DESCRIPTION
0	0	X	L	L	L	L	Z	Z	Diode Freewheel (coast)
0	1	X	L	H	H	L	L	H	Drive SH2-> SH1 (Reverse)
1	0	X	H	L	L	H	H	L	Drive SH1-> SH2 (Forward)
1	1	0b	L	H	L	H	L	L	Low side active freewheel
1	1	1b	H	L	H	L	H	H	High side active freewheel

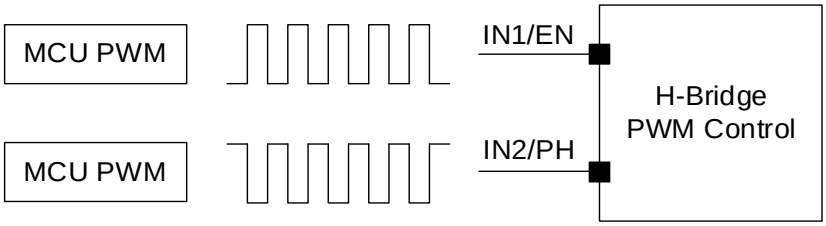


Figure 6. H-Bridge Control PWM Mode

Split HS and LS Solenoid Control

In split high-side and low-side (HS/LS) solenoid control mode, only the GH1 and GL2 gate driver outputs are active. GH1 is controlled via IN1/EN, while GL2 is controlled through IN2/PH. This mode allows the H-bridge to drive a floating solenoid load connected between the opposing high-side and low-side external MOSFETs.

In this mode, the S_HIZx register functions are disabled. The H-bridge can be placed in a Hi-Z state using the DRVOFF pin or by configuring the EN_DRV register setting on SPI devices.

Table 6. Split HS and LS Control (BRG_MODE = 11b)

IN1/EN	IN2/PH	GH1	GL1	GH2	GL2	DESCRIPTION
0	X	L	Inactive	Inactive	X	Solenoid disabled
1	X	H	Inactive	Inactive	X	Solenoid enabled
X	0	X	Inactive	Inactive	L	Solenoid PWM off
X	1	X	Inactive	Inactive	H	Solenoid PWM on

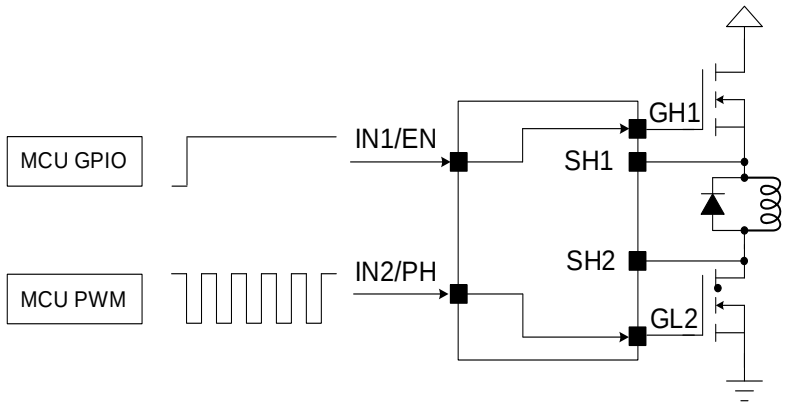


Figure 7. Split HS and LS PWM Control

Smart Gate Driver

The SA52902 incorporates an advanced and adjustable floating smart gate driver architecture, optimized for precise MOSFET control and reliable switching performance. It includes features such as configurable slew rate control, a driver state machine for dead-time handshaking, mitigation of parasitic dv/dt-induced gate coupling, and detection of gate faults in the external MOSFETs.

Table 7. Smart Gate Driver Symbol Description

Function	Symbol	Description
IDRIVE/TDRIVE	I_{DRVP}	Programmable gate driver source current for adjustable MOSFET slew rate control. Set through the IDRVP_x control register.
	I_{DRVN}	Programmable gate driver sink current for adjustable MOSFET slew rate control. Set through the IDRVN_x control register.
	I_{HOLD}	Fixed gate driver pull up hold current is applied during non-switching period.
	I_{STRONG}	Fixed gate driver strong pull down current is applied during non-switching period.
	t_{DRIVE}	$I_{DRVP/N}$ drive current duration before I_{HOLD} or I_{STRONG}. Also provides V_{GS} and V_{DS} fault monitor blanking period. Set through the VGS_TDRV_x control register.
	t_{PD}	Propagation delay between the logic control input and the corresponding gate driver output transition.
	t_{DEAD}	Body diode conduction period between high-side and low-side switch transition. Set through the VGS_TDEAD_x control register.

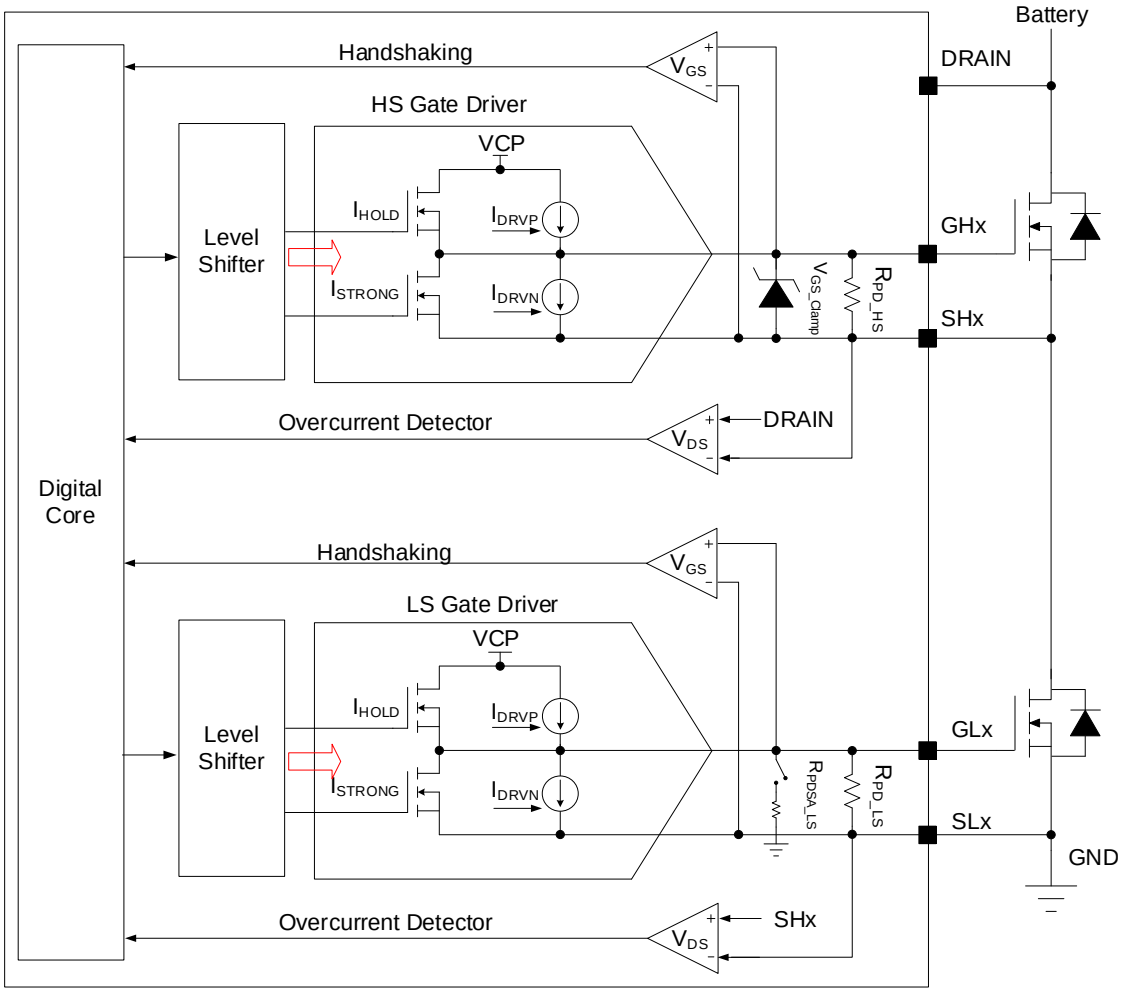


Figure 8. SA52902 Gate Driver Functional Block Diagram

Figure 8 illustrates a high-level functional block diagram of the half-bridge gate driver architecture. The gate driver blocks offer a range of functions for MOSFET driving, status feedback, and fault protection. This includes complementary push-pull high-side and low-side gate drivers with adjustable drive currents, control logic level shifters, V_{DS}, V_{GS}, and V_{SH} (switch-node) feedback comparators, a high-side Zener clamp, as well as active and passive pulldown resistors.

V_{SHx} Slew Rate Control (IDRIVE)

The IDRIVE feature within the smart gate drive architecture provides adjustable gate drive current control to modify the external MOSFET VDS slew rate. This is accomplished through programmable pull-up (IDRVP) and pull-down (IDRVN) current sources integrated within the internal gate driver circuitry.

The VDS slew rates of external MOSFETs play critical role in minimizing radiated and conducted EMI, dv/dt parasitic gate coupling, diode reverse recovery effects, and voltage transients at the half-bridge switch node. IDRIVE functions based on the principle that VDS slew rate is primarily determined by the rate of gate charge or gate current delivered during the MOSFET Q_{GD} or Miller charging region. By regulating this gate current, the gate driver can effectively control the switching slew rate of the external power MOSFETs.

IDRIVE enables the SA52902 to dynamically adjust gate driver current levels using the IDRVP_x and IDRVN_x SPI registers. The device offers 16 programmable settings ranging from 0.5mA to 62mA for both source and sink currents, as detailed in Table 8. The peak gate drive current is applied during the tDRIVE interval. Once the MOSFET switching completes and the t_{DRIVE} period ends, the gate driver transitions to a hold current (I_{HOLD}) for the pull-up path. This transition helps limit output current under short circuit conditions and enhances overall driver efficiency.

Table 8. I_{DRIVE} Source (I_{DRVP}) and Sink (I_{DRVN}) Current

Source Current IDRVP_x/ Sink Current IDRVN_x	Driver Current
0000b	0.5mA
0001b	1mA
0010b	2mA
0011b	3mA
0100b	4mA
0101b	5mA
0110b	6mA
0111b	7mA
1000b	8mA
1001b	12mA
1010b	16mA
1011b	20mA
1100b	24mA
1101b	31mA
1110b	48mA
1111b	62mA

Gate Drive State Machine (TDRIVE)

The TDRIVE function of the advanced gate driver is an integrated gate drive state machine that manages automatic dead-time insertion, prevents parasitic dv/dt gate coupling, and detects MOSFET gate faults.

The first stage of the TDRIVE state machine implements an automatic dead-time handshake. Dead time refers to the interval during which the body diode of the external MOSFET is free-wheeling between the switching events of the high-side and low-side MOSFETs, preventing shoot-through. The device utilizes V_{GS} monitoring to execute a break-and-make dead time strategy by sensing the external MOSFET V_{GS} voltage to determine the optimal moment for enabling the external MOSFETs. This adaptive approach allows the gate driver to compensate for the dead time for variations in the system, including temperature changes, component aging, voltage fluctuations, and variations in the external MOSFET parameters. Additionally, a fixed digital dead time (t_{DEAD_D}) can be configured through SPI registers, if further delay is required.

The second stage of the TDRIVE state machine mitigates parasitic dv/dt -induced gate charge coupling. It accomplishes this by applying a strong gate pulldown current (I_{STRONG}) when the MOSFET is turned off. This strong pulldown current helps to rapidly discharge any parasitic charge coupled from the switching node of the half-bridge.

The third stage of the TDRIVE state machine implements a gate fault detection mechanism that monitors the MOSFET gate voltage for abnormalities. This function detects issues such as pin-to-pin solder defects, gate failures, or conditions where the gate voltage becomes stuck high or low. It utilizes the V_{GS} monitors to verify that the gate voltage reaches the expected threshold following the t_{DRIVE} interval. If the voltage remains outside the defined range, the device flags a corresponding fault condition. To prevent false detections, the selected t_{DRIVE} duration should exceed the time required to charge or discharge the MOSFET gate. The t_{DRIVE} setting does not constrain the minimum PWM pulse width and will terminate early if a new PWM command is issued.

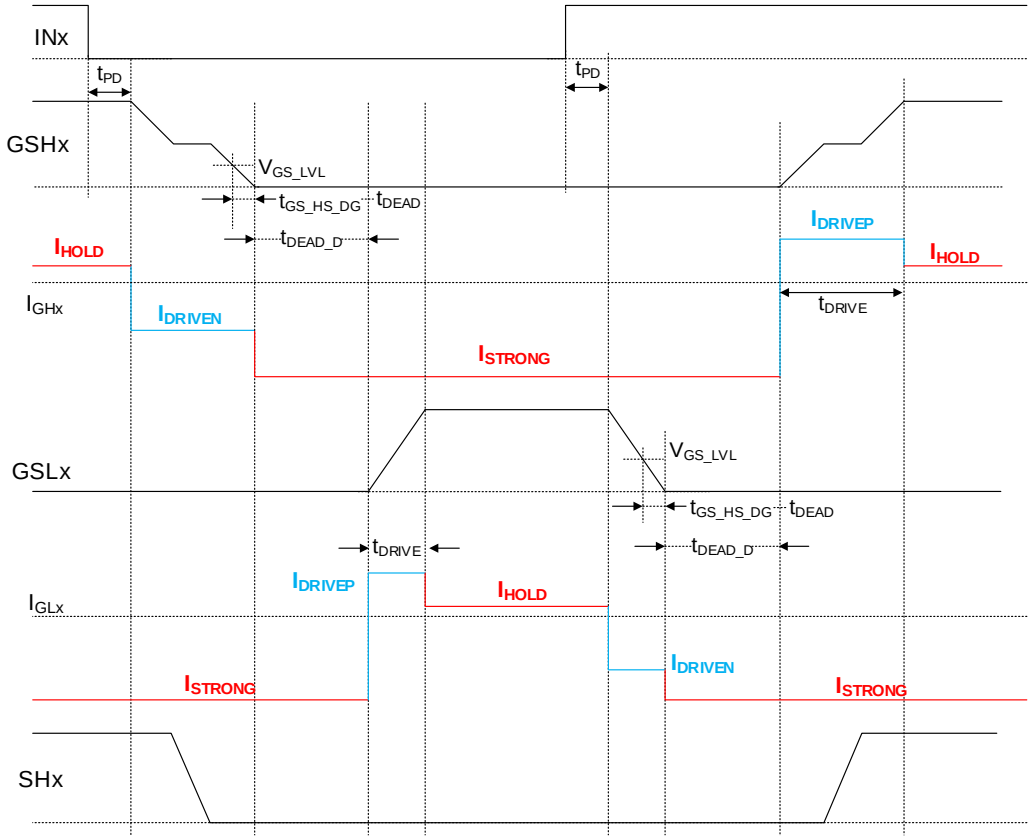


Figure 9. TDRIVE Turn On/Off

Doubler (Single-Stage) Charge Pump

The high-side gate drive voltage for the external MOSFET is supplied by a doubler charge pump powered by the PVDD input. This charge pump enables the high-side gate drivers to properly bias the external N-channel MOSFET with respect to its source voltage across a wide input supply voltage range. The charge pump output is regulated to maintain a fixed voltage with respect to V_{PVDD} and supports an average output current capability of 15 mA. The charge pump is continuously monitored for undervoltage events to prevent under-driven MOSFET conditions.

As the charge pump output is referenced to the PVDD pin voltage, the device is not intended to handle significant voltage differentials between PVDD and DRAIN; therefore, these differences should be minimized.

The charge pump requires a low ESR 1µF, 16 V ceramic capacitor (X5R or X7R recommended) between the PVDD and VCP pins to act as the storage capacitor. An additional low ESR 100 nF, PVDD-rated ceramic capacitor (also X5R or X7R recommended) should be placed between the CPH and CPL pins to serve as the flying capacitor.

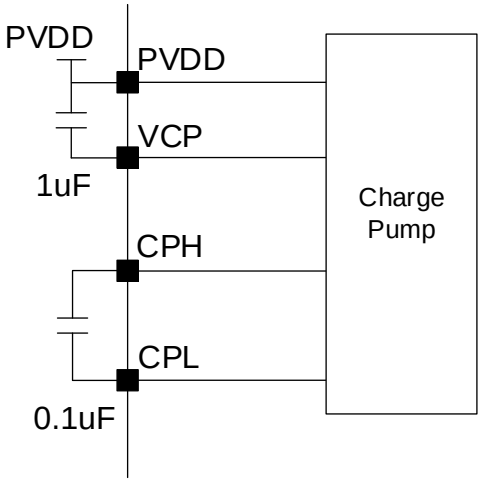


Figure 10. Charge Pump Structure

Wide Common-Mode Current Shunt Amplifier

The SA52902 integrates wide common-mode, bidirectional current-shunt amplifier for current sampling sensing using shunt resistors in external half-bridges. Current sampling is commonly used for overcurrent protection, torque control, or commutation with an external controller. It can sample low-side, high-side, or inline current by utilizing the high common-mode range of the current amplifier. The current shunt amplifier includes functions such as programmable gain configuration, output blanking time configuration, and a dedicated voltage reference pin (AREF) to set a midpoint bias voltage for the amplifier output. A simplified block diagram is shown in Figure 11. SP should be connected to the positive terminal of the shunt resistor, while SN should be connected to the negative terminal of the shunt resistor. If the amplifier is not utilized, the SN, and SP inputs can be tied to AGND, and AGND should be connected to PCB GND, with the AREF and SO output left floating.

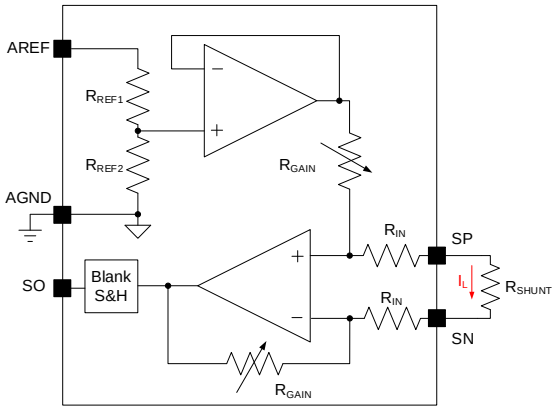


Figure 11. SA52902 Amplifier Simplified Block Diagram

A detailed block diagram is shown in Figure 12. The wide common mode amplifier is implemented using a two-stage differential structure. The first differential stage supports a wide common mode input, provides a differential output, and has a fixed gain of G = 1. The second differential stage allows for variable gain adjustment, with G values of 10, 20, 40, or 80. The total gain of the two stages will be G = 10, 20, 40, or 80.

The amplifier can also produce an output voltage bias determined by the voltage present at the AREF pin. The AREF pin connects to a divider network and a buffer, which then sets the output voltage bias for the differential amplifier. In SPI mode, the gain is configured through the CSA_GAIN register, and the reference division ratio is set through the CSA_DIV register.

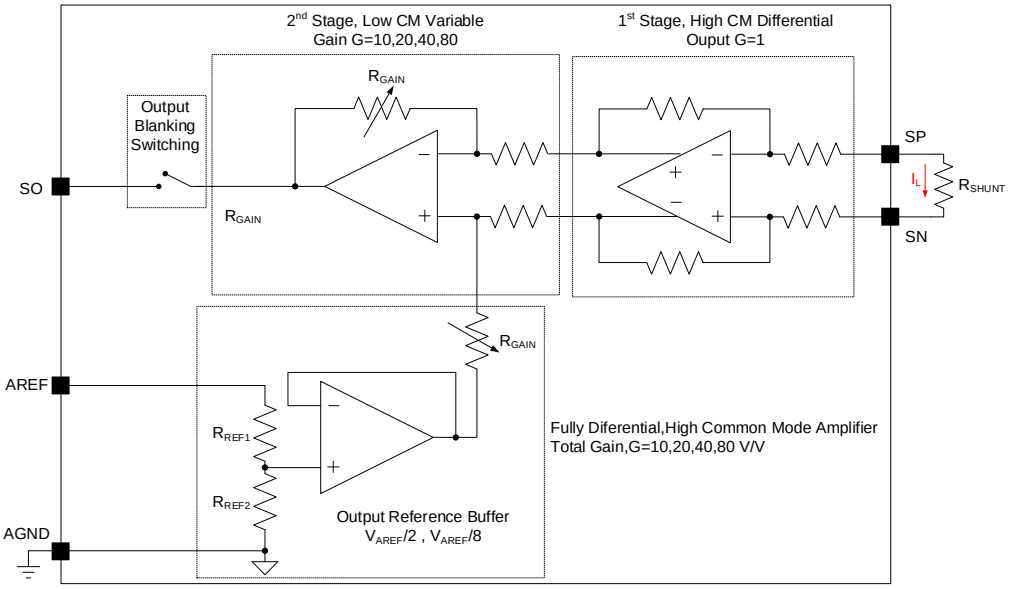


Figure 12. Amplifier Detailed Block Diagram

Lastly, the amplifier features an output blanking or sample-and-hold switch. The output switch can be used to disconnect the amplifier output during PWM switching to reduce output noise (blanking) or during motor braking to maintain the output value if the shunt is used in a high-side or low-side configuration (sample and hold). The blanking circuit can be triggered based on the active half-bridge (half-bridge 1 or half-bridge 2) through the CSA_BLK_SEL register setting. The blanking period can be programmed using the CSA_BLK register setting. The sample-and-hold circuit can be enabled with the CSA_SH_EN register setting. When active, the sample-and-hold function will trigger whenever the driver enters high-side or low-side braking. To utilize either the blanking or sample-and-hold functions, an output hold-up capacitor is required to stabilize the amplifier output when it is disconnected. It is typically recommended that this capacitor be placed after a series resistor in an RC filter configuration to limit the direct capacitance seen at the amplifier output.

Figure 13 illustrates the amplifier blanking function. This feature allows the amplifier output to enter a Hi-Z state during switching transitions, though it is not enabled by default. Blanking can be useful when noise from wide common-mode swings or ground shifts occurs during the PWM switching transition and interferes with the amplifier output. As depicted, the function disables the amplifier output for a defined interval following a transition on either GHx or GLx. The duration of this interval is set by the t_{BLK} value, which is configured via the CSA_BLK register.

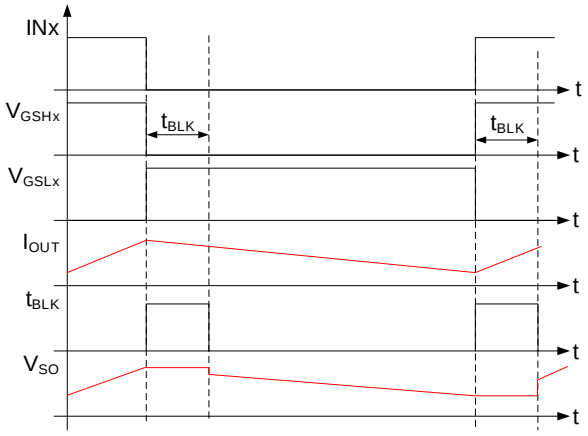


Figure 13. Amplifier Blanking Waveform

Figure 14 illustrates an example of the amplifier's sample and hold function. This feature can place the amplifier output in a Hi-Z state during current recirculation in the H-bridge, although it is not enabled by default. This function is particularly useful

when the shunt resistor is placed on either the low or the high side of the H-bridge, where current information may be lost during current recirculation. As shown, the sample and hold function preserves the last amplifier output state by maintaining the charge on the output capacitor. Normal amplifier operation resumes once the H-bridge exits the recirculation phase.

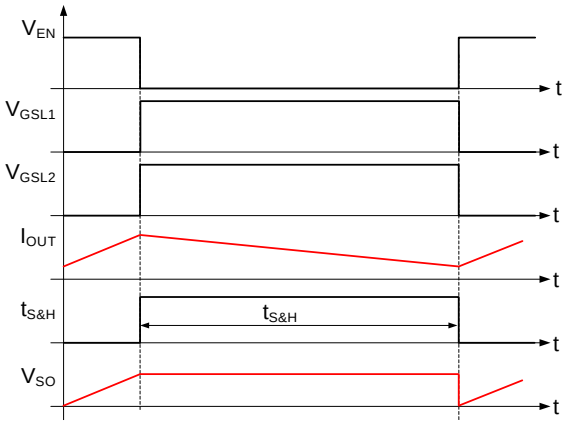


Figure 14. Amplifier Sample & Hold Waveform

Protection Functions

Gate Driver Disable (DRVOFF and EN_DRV)

The SA52902 features a dedicated driver disable function via the DRVOFF pin. When DRVOFF is asserted, it enables the gate driver pull-downs, regardless of the pin or SPI inputs. For SPI device variants, the EN_DRV function is available to facilitate a controlled power-up sequence. Following device power-up, the gate drivers remain disabled until the EN_DRV register bit is asserted. This functionality allows the system to power up and perform configuration sequences before enabling the gate drivers.

Fault Reset (CLR_FLT)

The SA52902 provides a defined procedure for clearing fault conditions from the driver and resuming operation, managed through the CLR_FLT register bit. To clear a reported fault, the CLR_FLT register bit must be asserted after the fault condition has been removed. Once asserted, the driver clears the fault condition and automatically resets the CLR_FLT register bit. This feature is only available on SPI-enabled device variants.

DVDD Logic Supply Power on Reset (DVDD_POR)

When the input logic supply voltage on the DVDD pin falls below the V_{DVDD_POR} threshold for longer than the $t_{DVDD\_POR\_DG}$ time, or when the nSLEEP pin is pulled down to low, the device enters its inactive state, disabling the gate drivers, charge pump, and protection monitors. Normal operation resumes when the DVDD undervoltage condition is removed or the nSLEEP pin is pulled high. After a DVDD power-on reset (POR), the POR register bit is asserted until CLR_FLT is cleared.

PVDD Supply Undervoltage Protection (PVDD_UV)

When the PVDD pin falls below the V_{PVDD_UV} threshold for longer than the $t_{PVDD\_UV\_DG}$ time, the SA52902 detects a PVDD undervoltage condition. After detecting this condition, the gate driver pull-downs are enabled, the charge pump is disabled, and the nFLT pin, FAULT register bit, and PVDD_UV register bit are asserted. The PVDD undervoltage monitor can recover in two different modes, which are set through the PVDD_UV_MODE register.

Latched Fault Mode: After the undervoltage fault is removed, the fault state remains latched, and the charge pump is disabled until CLR_FLT is cleared.
Automatic Recovery Mode: After the undervoltage fault is removed, the nFLT pin and FAULT register bit are automatically cleared, and the charge pump automatically restarts. The PVDD_UV register bit remains latched until CLR_FLT is cleared.

PVDD Overvoltage Protection (PVDD_OV)

When the PVDD pin exceeds the V_{PVDD_OV} threshold for longer than the $t_{PVDD\_OV\_DG}$ time, the SA52902 detects a PVDD overvoltage fault, and actions are taken according to the PVDD_OV_MODE register. The overvoltage threshold and deglitch time can be adjusted through the PVDD_OV_LVL and PVDD_OV_DG registers. The PVDD overvoltage monitor can respond and recover in four different modes, which are set through the PVDD_OV_MODE register.

Latched Fault Mode: When an overvoltage fault is detected, the gate driver pull-downs are activated, and the nFLT pin, FAULT register bit, and PVDD_OV register bit are asserted. The fault state remains latched even after the fault condition is removed and must be cleared by setting the CLR_FLT bit.

Automatic Recovery Mode: Upon detecting an overvoltage fault, the gate driver pull-downs are enabled, and the nFLT pin, FAULT register bit, and PVDD_OV register bit are asserted. Once the fault clears, the nFLT pin and FAULT register bit is automatically de-asserted, and the driver resumes operation. The PVDD_OV bit remains latched until cleared via CLR_FLT.

Disabled Mode: The PVDD overvoltage monitor is turned off. No response or fault reporting occurs.

VCP Charge Pump UVLO (VCP_UV)

When the VCP voltage falls below the V_{VCP_UV} threshold for longer than the $t_{VCP\_UV\_DG}$ time, the SA52902 detects a VCP undervoltage fault. After detecting the undervoltage condition, the gate driver pull-downs are enabled, and the nFLT pin, FAULT register bit, and VCP_UV register bit are asserted. The UV threshold can be configured through the VCP_UV_LVL

register. The VCP undervoltage monitor can recover in two different modes, which are set through the VCP_UV_MODE register.

Latched Fault Mode: The charge pump is disabled in latched fault mode. Once the undervoltage condition is removed, the fault state remains latched, and the charge pump remains disabled until cleared via CLR_FLT.

Automatic Recovery Mode: After the UVLO is removed, the nFLT pin and FAULT register bit are automatically cleared, and the driver restarts automatically. The VCP_UV register bit remains latched until CLR_FLT is cleared.

MOSFET V_{DS} Overcurrent Protection (VDS_OCP)

If the MOSFET's V_{DS} overcurrent comparator exceeds the threshold defined by V_{DS_LVL} for a duration longer than the t_{DS_DG} deglitch time, the SA52902 flags a V_{DS} overcurrent fault. Both the voltage threshold and deglitch time are configurable via the V_{DS_LVL} and V_{DS_DG} registers. Additionally, in independent half-bridge and SA52902 split HS/LS PWM control modes (BRG_MODE = 00b or 11b), the device can be configured to disable all half-bridges or only the associated half-bridge in which the fault occurred through the VDS_IND register. The VDS overcurrent monitor supports four different response modes, selectable through the VDS_MODE register.

Latched Fault Mode: When an overcurrent event is detected, the gate driver pull-downs are activated, and the nFLT pin, FAULT register bit, and associated VDS register bit are asserted. The fault state remains latched even after the fault condition is removed and must be cleared by setting the CLR_FLT bit.

Cycle-by-Cycle Mode: When an overcurrent event is detected, the gate driver pull-downs are activated, and the nFLT pin, FAULT register bit, and associated VDS register bit are asserted. The next PWM input clears the nFLT pin and FAULT register bit, allowing the driver to automatically restart. The VDS register bit remains asserted until cleared using the CLR_FLT command.

Warning Report Only Mode: The overcurrent event is indicated through the WARN and corresponding VDS register bits. The device does not take any protective action. The warning remains latched until the CLR_FLT command is issued.

Disabled Mode: The VDS overcurrent monitors are inactive and will neither respond to nor report any fault conditions.

When a V_{DS} overcurrent fault is detected, the gate pull-down current can be adjusted to control the turn-off speed of the external MOSFET. Modifying this parameter helps reduce the risk of shoot-through. This setting is configurable via the VDS_IDRVN register on SPI-enabled devices.

Gate Driver Fault (VGS_GDF)

If the V_{GS} voltage fails to exceed the threshold defined by V_{GS_LVL} within the t_{DRIVE} period, the SA52902 detects a V_{GS} gate fault. In independent half-bridge and SA52902 split HS/LS PWM control modes (BRG_MODE=00b or 11b), the device can be configured to disable all half-bridges or only the fault half-bridge by using the VGS_IND register. The V_{GS} gate fault monitor supports four distinct response and recovery modes, selectable through the VGS_MODE register.

Latched Fault Mode: When a gate fault is detected, the gate driver pull-downs are activated, and the nFLT pin, FAULT register bit, and corresponding VGS register bit are asserted. The fault condition remains latched even after the issue is resolved and must be cleared by issuing the CLR_FLT command.

Cycle-by-Cycle Mode: After a gate fault is detected, the gate driver pull-downs are activated, and the nFLT pin, FAULT register bit, and corresponding VGS register bit are asserted. After 15 PMW input cycles will clear the nFLT pin and FAULT register bit, and will automatically restart the driver. The VGS register bit remains asserted until the CLR_FLT command is issued.

Warning Report Only Mode: The gate fault is indicated through the WARN and corresponding VGS register bits. The device does not take any protective action. The warning remains latched until the CLR_FLT command is issued.

Disabled Mode: The VGS gate fault monitors are inactive and will neither respond to nor report any fault conditions.

Power Off Braking Function (POB)

The SA52902 provides the capability to enable the low-side gate drivers while the device is in sleep mode (nSLEEP = L). This allows the external low-side power MOSFETs to be activated. Enabling the external low-side MOSFETs permits the external half-bridges to short the back EMF of the motor. This action can help prevent reverse driving of the motor by an external force from overcharging the system power supply. This function is available only while the device is in its low-power sleep mode. The function is activated by setting the BRAKE pin to a logic high. The BRAKE pin will enable or disable the low-side gate drivers for both half-bridges simultaneously. The powered-off braking function requires the PVDD voltage supply to enable the low-side gate drivers without the DVDD power supply.

In the event of a short circuit, a simple overcurrent detector circuit with a deglitch filter time is provided to disable the low-side MOSFET if a high current flows through it while braking is enabled. Since the normal overcurrent protection circuits are disabled in sleep mode, the device requires an additional overcurrent protection (OCP) function. The values of the overcurrent comparator and RC deglitch filter are fixed and cannot be adjusted.

The powered-off braking function is enabled through the BRAKE pin. To reduce quiescent current draw, the pulldown resistance of the BRAKE pin is decreased to 1MΩ while the device is in low-power sleep mode. If the powered-off braking function is not utilized, the BRAKE pin should be connected directly to GND or left floating.

Several methods can be used to pull up the BRAKE pin, depending on the desired control scheme:

Option 1: Voltage-triggered Pull-up with a passive Zener diode. An external Zener diode can be added to the BRAKE pin to establish an overvoltage trigger that is lower than the internal overvoltage monitor.

Option 2: The MCU provides a fixed digital output high or a digital output in response to motor movement detected by the sensor or rising voltage. A digital output to the BRAKE pin can directly control whether the power-off braking function is enabled (LO = disabled, HI = enabled).

Option 3: The power-off braking function can be disabled by connecting the BRAKE pin directly to the PCB ground, or it can simply be left floating.

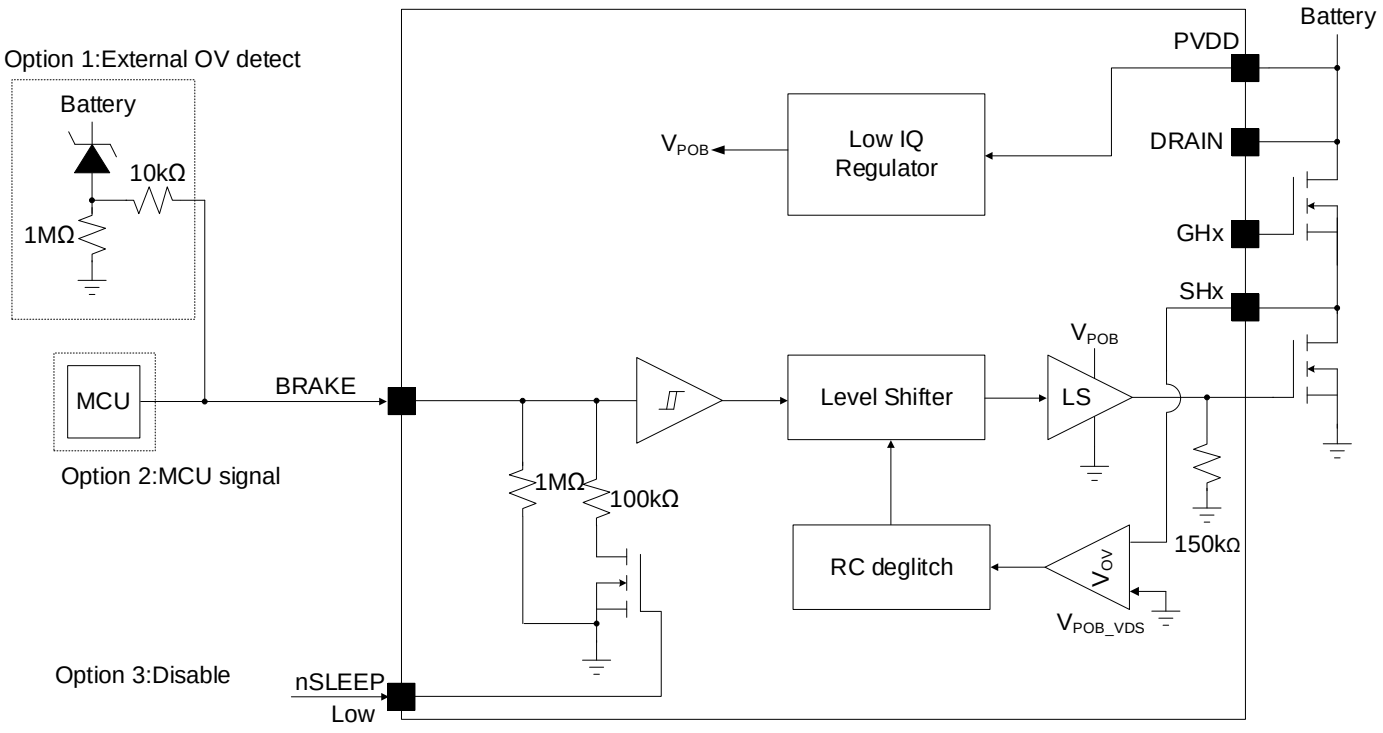


Figure 15. SA52902 Power Off Braking

Thermal Warning (OTW)

If the die temperature exceeds the T_{OTW} thermal warning threshold, the SA52902 issues an overtemperature warning by asserting the WARN and OTW register bits. After the temperature returns to a safe range, the WARN and OTW register bits remain latched until the CLR_FLT command is issued.

Thermal Shutdown (OTSD)

If the die temperature exceeds the T_{OTSD} thermal shutdown threshold, the gate driver pull-downs are activated, the charge pump is disabled, and the nFLT pin, FAULT register bit, and OTSD register bit are asserted. Once the overtemperature condition clears, the fault remains latched until the CLR_FLT is issued.

Off State Short Circuit and Open Load Detection (OOL and OSC)

The device provides the necessary hardware to conduct off-state diagnostics for short circuits and open loads across the MOSFETs and load. This functionality uses integrated pull-up and pull-down current sources on the SHx pin, which connects to the midpoint of the external half-bridge. The off-state diagnostics are controlled by the associated bits in the OLSC_CTRL register. First, the off-state diagnostic mode must be enabled through the EN_OLSC register. Then, the individual current sources can be activated through the PD_SHx and PU_SHx registers. The voltage on the SHx pin will be continuously monitored through the internal V_{DS} comparators. During the diagnostic state, the V_{DS} comparators will report real-time voltage feedback on the SHx in the SPI registers within the associated VDS register status bit.

Before enabling the off-state diagnostics, it is recommended to set the half-bridges to the disabled state using the EN_DRV register. Additionally, the V_{DS} comparator threshold (V_{DS_LVL}) should be adjusted to 1V or greater to ensure sufficient margin for the internal blocking diode forward voltage drop. The V_{DS} comparators will begin real-time voltage feedback immediately after OLSC_EN is set. Feedback should be disregarded until the proper pull-up and pull-down configuration is established.

To execute the offline diagnostic sequence correctly, follow these steps:

- Set the EN_DRV control register to 0b to disable the output drivers.
- Set the OLSC_EN control register to 1b to enable offline diagnostics.
- Enable the PD_SHx and PU_SHx control registers as required for the test.
- Read back the VDS_x status registers to assess the output state.
- Disable the PD_SHx and PU_SHx control registers.
- Set the OLSC_EN control register to 0b to disable the offline diagnostics.
- Set EN_DRV control register to 1b to re-enable the output drivers.

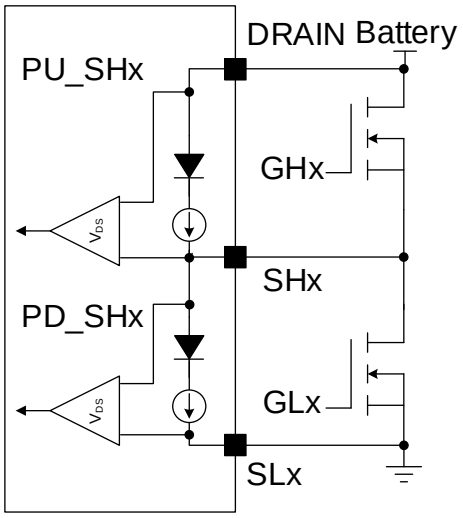


Figure 16. Off State Diagnosis

Fault Detection and Response Summary Table

Table 9. Fault Detection and Response Summary

Name	Condition	SPI Bit	Mode	Digital Core	Charge Pump	Gate Drivers	Current Sense	Response
Disable Driver	DRVOFF=High	N/A	N/A	Active	Active	Pull Down	Active	N/A
DVDD Power -on-Reset	DVDD < V_{DVDD_POR}	POR	N/A	Reset	Disable	Semi-Active Pull Down	Disable	SPI
PVDD Undervoltage	PVDD < V_{PVDD_UV}	UV, PVDD_UV	Latched	Active	Disabled	Semi-Active Pull Down	Disable	nFLT, SPI
			Automatic	Active	Disabled	Semi-Active Pull Down	Disable	nFLT, SPI
PVDD Overvoltage	PVDD > V_{PVDD_OV}	OV, PVDD_OV	Latched	Active	Active	Pull Down	Active	nFLT, SPI
		OV, PVDD_OV	Automatic	Active	Active	Pull Down	Active	nFLT, SPI
		OV, PVDD_OV	Warning	Active	Active	Active	Active	WARN, SPI
		N/A	Disabled	Active	Active	Active	Active	N/A
VCP Undervoltage	VCP < V_{VCP_UV}	UV, VCP_UV	Latched	Active	Disabled	Semi-Active Pull Down	Disabled	nFLT, SPI
			Automatic	Active	Active	Semi-Active Pull Down	Disabled	nFLT, SPI
VDS Overcurrent	VDS > V_{VDS_LVL}	DS_GS, VDS_X	Latched	Active	Active	I_{VDS_IDRVN} Pull Down	Active	nFLT, SPI
			Cycle	Active	Active	I_{VDS_IDRVN} Pull Down	Active	nFLT, SPI
			Warning	Active	Active	Active	Active	WARN, SPI
			Disabled	Active	Active	Active	Active	N/A
VGS Gate Fault	VGS > V_{VGS_LVL}	DS_GS, VGS_X	Latched	Active	Active	Pull Down	Active	nFLT, SPI
			Cycle	Active	Active	Pull Down	Active	nFLT, SPI
			Warning	Active	Active	Active	Active	WARN, SPI
			Disabled	Active	Active	Active	Active	N/A
Thermal Warning	T_J > T_{OTW}	OT, OTW	Automatic	Active	Active	Active	Active	WARN, SPI
Thermal Shutdown	T_J > T_{OTSD}	OT, OTSD	Latched	Active	Disabled	Semi-Active Pull Down	Disabled	nFLT, SPI
Offline Open Load	N/A	VDS_X	MCU	Active	Active	Pull Down	Active	SPI
Offline Short Circuit	N/A	VDS_X	MCU	Active	Active	Pull Down	Active	SPI

Programming

SPI Interface

The device supports a standard 16-bit SPI for control. The SPI interface is a synchronous serial interface used for address and data transfer at bit rates of up to 10 MHz. It is configured in 8-bit bytes, designed to interface with a standard SPI bus. Four pins are utilized for communication on the SPI: SCLK (synchronous clock), nSCS (chip select, active low), SDI (data input to the device for write operations), and SDO (data output from the device for read operations), as shown in Figure 17.

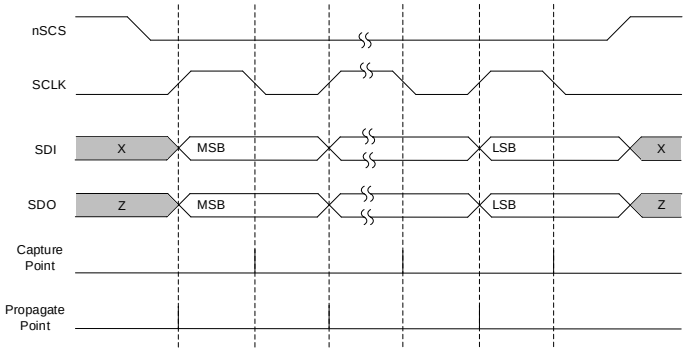


Figure 17. SPI Target Timing Diagram

A valid frame must meet the following conditions:

- The SCLK pin must remain low during both the high-to-low and low-to-high transitions of the nSCS pin.
- The nSCS pin should be pulled high between data words.
- When the nSCS pin is high, inputs on the SCLK and SDI pins are ignored, and the SDO pin enters a high-impedance

(Hi-Z) state.

- Data is latched on the falling edge of SCLK and shifted out on the rising edge.
- Data transfer begins with the most significant bit (MSB).
- Each SPI transaction must consist of exactly 16 SCLK cycles to be valid.
- If the number of bits sent to the SDI pin deviates from 16, a frame error (SCLK_FLT) is generated, and the data is discarded.
- For write operations, the current content of the target register is shifted out on the SDO pin immediately following the 8-bit command portion.

SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- W (bit 14): 1 Read/Write control bit
- Ax: 6-bit register address
- Dx: 8-bit data payload.

SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- W (bit 14): 1 Read/Write control bit
- Ax: 6-bit register address
- Dx: 8-bit data payload

The SDO output data word is 16 bits long, with the first 8 bits comprising the IC status register. The report word contains the content of the register being accessed. For a write command (W0 = 0), the response word consists of the fault status indication bits followed by the existing data in the register being written to. For a read command (W0 = 1), the response word contains the fault status indication bits followed by the data currently in the register being read.

Table 10. SDI Input Data Word Format

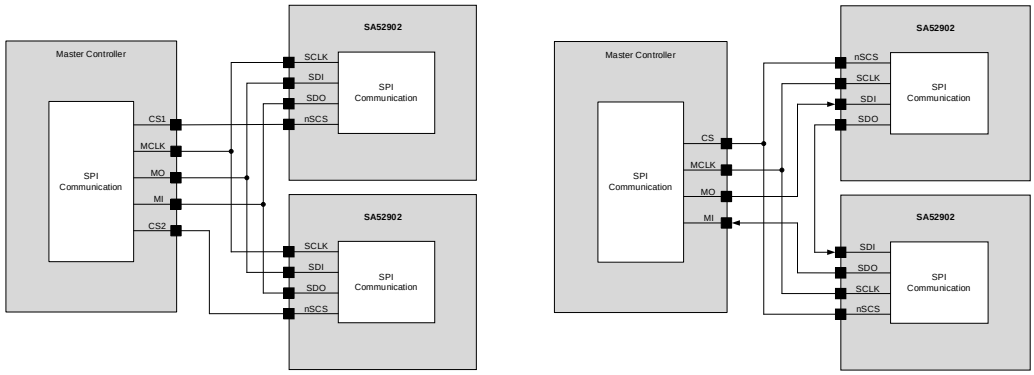
		R/W	Address						Data							
Bit	B15	B14	B13	B12	B11	B10	B9	D8	B7	B6	B5	B4	B3	B2	B1	B0
Data	0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 11. SDO Output Data Word Format

	IC Status								Data							
Bit	B15	B14	B13	B12	B11	B10	B9	D8	B7	B6	B5	B4	B3	B2	B1	B0
Data	1	1	FAULT	WARN	DS_GS	UV	OV	OT	D7	D6	D5	D4	D3	D2	D1	D0

SPI Interface for Multiple Targets

Multiple SA52902 devices can be interfaced with the controller either with or without using a daisy chain configuration. To connect ‘n’ SA52902 devices without daisy chaining, the controller must provide 'n' separate I/O lines for the individual nSCS pins, as shown in Figure 18(a). Alternatively, when using a daisy chain configuration, a single nSCS line can be shared among multiple devices, as shown in Figure 18(b).



(a) Without Daisy Chain *(b) With Daisy Chain*

Figure 18. Multiple Device SPI Operation

SPI Interface for Multiple Targets in Daisy Chain

The device supports daisy chain operation with other devices that utilize the same SPI protocol. The controller output (MO) is connected to a target input (SDI), and the first target output (SDO) is connected to the next target input (SDI) to form a chain. The SDO of the final target in the chain is connected to the controller input (MI) to complete the loop of the SPI communication frame. In a daisy chain configuration, a single chip select, and a clock are connected in parallel to each target device, allowing the microcontroller to control or access the SPI devices.

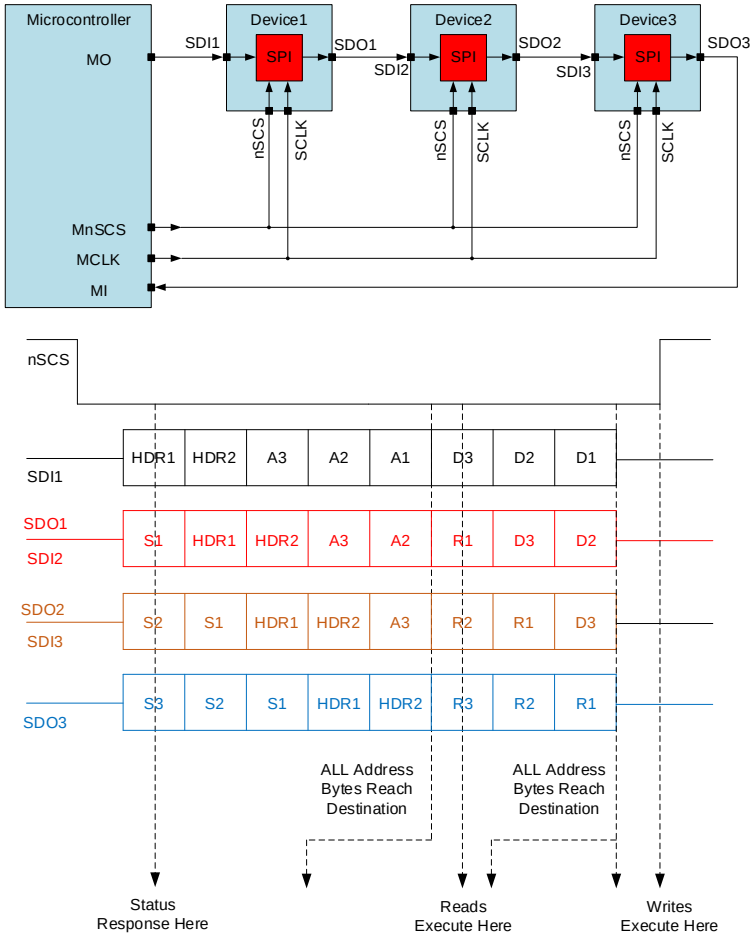


Figure 19. Daisy Chain SPI Operation

The first device in the chain, as illustrated in the figure above, receives data from the controller in the format depicted as SDI1 in Figure 19:

1). 2 bytes of Header

2). 3 bytes of Address

3). 3 bytes of Data

Once the data has been transmitted through the entire chain, the controller receives it in the format shown as SDO3 in Figure 19:

1). 3 bytes of Status

2). 2 bytes of Header (should match the information originally sent by the controller)

3). 3 bytes of Report

The header bytes include information on the total number of devices connected in the daisy chain and a global clear fault command. This command clears the fault registers of all devices on the rising edge of the chip select (nSCS) signal. Bits N5 through N0 are 6 bits that represent the number of devices in the chain, as shown in Figure 20. A maximum of 63 devices can be connected in a single daisy chain. The 5 least significant bits (LSBs) of the HDR2 register are “don’t care” bits, which the MCU can use to verify the integrity of the daisy chain connection. The header bytes must begin with 1 and 0 as the two most significant bits (MSBs).

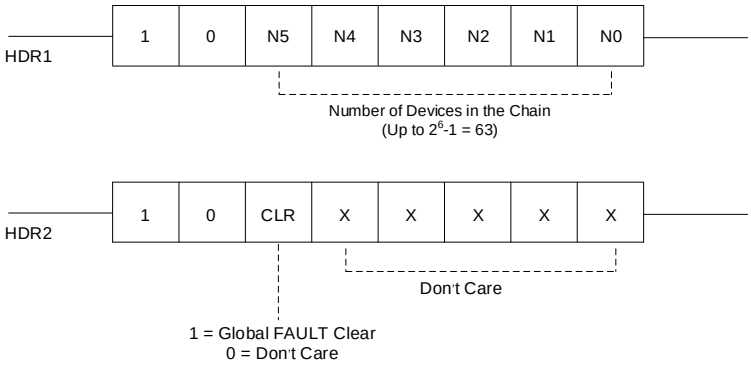


Figure 20. Header Bits

The Status byte conveys the fault status register information for each device in the daisy chain, as illustrated in Figure 21. This allows the controller to monitor fault conditions without issuing separate read commands for each device. By eliminating the need for individual queries, this approach improves system efficiency in detecting and identifying device-level faults.

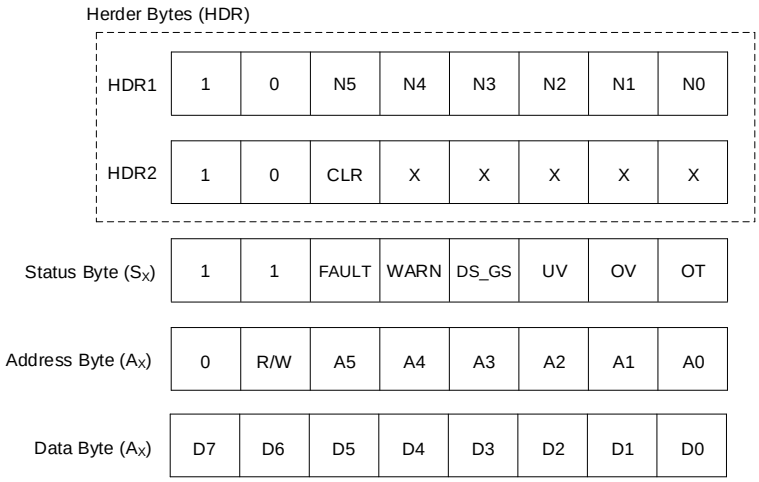


Figure 21. Daisy Chain Read Registers

As data passes through each device in the daisy chain, a device determines its position by counting the number of Status bytes received before the first Header byte. For instance, in a three-device setup, the second device in the chain will receive two Status bytes before receiving HDR1, followed by HDR2. From the count of Status bytes, the device identifies its position in the chain, and from HDR2, it determines the total number of connected devices. This enables the device to load only the address and data bytes relevant to its position while ignoring unrelated bits. This protocol ensures faster communication with minimal latency and supports up to 63 devices in a single chain.

Register Map

Name	7	6	5	4	3	2	1	0	Type	Add
IC_STAT_1	SPI_OK	POR	FAULT	WARN	DS_GS	UV	OV	OT	R	00h
VGS_VDS_STAT	VGS_H1	VGS_L1	VGS_H2	VGS_L2	VDS_H1	VDS_L1	VDS_H2	VDS_L2	R	01h
IC_STAT_2	PVDD_UV	PVDD_OV	VCP_UV	OTW	OTSD	RSVD	SCLK_FLT	ADDR_FLT	R	02h
RSVD_STAT	RSVD								R	03h
IC_CTRL1	EN_DRV	SSC_DIS	IN1/EN_MODE	IN2/PH_MODE	LOCK			CLR_FLT	R/W	04h
BRG_CTRL	VGS_HS_DIS	BRG_MODE		BRG_FW	S_IN1/EN	S_IN2/PH	S_HIZ1	S_HIZ2	R/W	05h
DRV_CTRL_1	IDRVP_HS				IDRVN_HS				R/W	06h
DRV_CTRL_2	IDRVP_LS				IDRVN_LS				R/W	07h
DRV_CTRL_3	VGS_MODE		VGS_TDRV		VGS_TDEAD			VGS_IND	R/W	08h
VDS_CTRL_1	VDS_MODE		VDS_DG		VDS_IDRVN		VGS_LVL	VDS_IND	R/W	09h
VDS_CTRL_2	VDS_HS_LVL				VDS_LS_LVL				R/W	0Ah
OLSC_CTRL	EN_LIMP	RSVD		OLSC_EN	PU_SH1	PD_SH1	PU_SH2	PD_SH2	R/W	0Bh
UVOV_CTRL	PVDD_UV_MODE	PVDD_OV_MODE		PVDD_OV_DG		PVDD_OV_LVL	VCP_UV_MODE	VCP_UV_LVL	R/W	0Ch
CSA_CTRL	CSA_SH_EN	CSA_BLK_SEL	CSA_BLK			CSA_DIV	CSA_GAIN		R/W	0Dh

SA52902 Status Registers

Address	Register Name	Description
0x00h	IC_STAT_1	IC status register 1
0x01h	VGS_VDS_STAT	V_{GS} and V_{DS} status register
0x02h	IC_STAT_2	IC status register 2
0x03h	RSVD_STAT	Reserved

IC_STAT1 register (Address= 0x00h), default value 0xC0h=11000000$_B$

Bit	Field	Type	Reset	Description
7	SPI_OK	R	1b	Indicates if an SPI communications fault has been detected. 0b = One or multiple SPI_CLK_FLT or SPI_ADR_FLT in past frames. 1b = No SPI fault has been detected
6	POR		1b	Indicates power-on-reset condition. 0b = No power-on-reset condition detected. 1b = Power-on reset condition detected.
5	FAULT		0b	Fault indicator. Reflects the state of the nFLT pin.
4	WARN		0b	Warning indicator
3	DS_GS		0b	Logic OR of the VDS and VGS fault indicators.
2	UV		0b	Undervoltage indicator.
1	OV		0b	Overvoltage indicator.
0	OT		0b	Logic OR of OTW and OTSD.

VGS_VDS_STAT register (Address= 0x01h), default value 0x00h=00000000$_B$

Bit	Field	Type	Reset	Description
7	VGS_H1	R	0b	Indicates a VGS gate fault on the high-side 1 MOSFET.
6	VGS_L1		0b	Indicates a VGS gate fault on the low-side 1 MOSFET.
5	VGS_H2		0b	Indicates a VGS gate fault on the high-side 2 MOSFET.
4	VGS_L2		0b	Indicates a VGS gate fault on the low-side 2 MOSFET.
3	VDS_H1		0b	Indicates a VDS overcurrent fault on the high-side 1 MOSFET.
2	VDS_L1		0b	Indicates a VDS overcurrent fault on the low-side 1 MOSFET.
1	VDS_H2		0b	Indicates a VDS overcurrent fault on the high-side 2 MOSFET.
0	VDS_L2		0b	Indicates a VDS overcurrent fault on the low-side 2 MOSFET.

IC_STAT_2 register (Address= 0x02h), default value 0x00=00000000$_B$

Bit	Field	Type	Reset	Description
7	PVDD_UV	R	0b	Indicates an undervoltage fault on PVDD pin.
6	PVDD_OV		0b	Indicates an overvoltage fault on PVDD pin.
5	VCP_UV		0b	Indicates an undervoltage fault on VCP pin.
4	OTW		0b	Indicates an overtemperature warning.
3	OTSD		0b	Indicates an overtemperature shutdown.
2	RSVD		0b	Reserved
1	SCLK_FLT		0b	Indicates an SPI clock (frame) fault.
0	ADDR_FLT		0b	Indicates an SPI address fault

SA52902 Control Registers

Address	Register Name	Description
0x04h	IC_CTRL1	IC control register
0x05h	BRG_CTRL	BRG control register
0x06h	DRV_CTRL_1	DRV control register 1
0x07h	DRV_CTRL_2	DRV control register 2
0x08h	DRV_CTRL_3	DRV control register 3
0x09h	VDS_CTRL_1	VDS control register 1
0x0Ah	VDS_CTRL_2	VDS control register 2
0x0Bh	OLSC_CTRL	OLSC control register
0x0Ch	UVOV_CTRL	UVOV control register
0x0Dh	CSA_CTRL	CSA control register

IC_CTRL register (Address= 0x04h), default value 0x06h=0000 0110_B

Bit	Field	Type	Reset	Description
7	EN_DRV	R/W	0b	Enables gate drivers. 0b = Gate driver output disabled and passive pulldowns enabled. 1b = Gate driver outputs enabled.
6	SSC_DIS	R/W	0b	Disables device spread spectrum clocking 0b = Enabled. 1b =Disabled.
5	IN1/EN_MODE	R/W	0b	IN1/EN control mode. 0b = IN1/EN signal is sourced from the IN1/EN pin. 1b = IN1/EN signal is sourced from the S_IN1/EN bit.
4	IN2/PH_MODE	R/W	0b	IN2/PH control mode. 0b = IN2/PH signal is sourced from the IN2/PH pin. 1b = IN2/PH signal is sourced from the S_IN2/PH bit.
3~1	LOCK	R/W	011b	Controls access to the control registers. Bit settings not specified have no effect. 011b = Unlock all control registers. 110b = Lock the control registers by ignoring further writes except for the LOCK register.
0	CLR_FLT	R/W	0b	Clears latched fault status information. 0b = Default state. 1b = Clear latched fault bits, resets to 0b after completion. Will also clear the SPI fault status.

BRG_CTRL register (Address= 0x05h), default value 0x00h=0000 0000_B

Bit	Field	Type	Reset	Description
7	VGS_HS_DIS	R/W	0b	VGS monitor-based dead-time handshake. 0b = Enabled. 1b = Disabled. Gate drive transition based on t_{DRIVE} and t_{DEAD} time duration.
6~5	BRG_MODE		00b	H-bridge input control mode. 00b = Independent half-bridge input control. 01b = PH/EN H-bridge input control. 10b = PWM H-bridge input control. 11b = Split HS/LS solenoid input control.
4	BRG_FW		0b	H-bridge control freewheeling setting. 0b = Low-side freewheeling; 1b = High-side freewheeling.
3	S_IN1/EN		0b	Control bit for IN1/EN input signal. Enabled through IN1/EN_MODE bit.
2	S_IN2/PH		0b	Control bit for IN2/PH input signal. Enabled through IN2/PH_MODE bit.
1	S_HIZ1		0b	Control bit for HIZ1 input signal. Logic OR with the nHIZ1 pin. Active only in half-bridge input control mode. 0b = Outputs follow IN1/EN signal. 1b = Gate drivers pulldowns are enabled. Half-bridge 1 Hi-Z.
0	S_HIZ2		0b	Control bit for HIZ2 input signal. Logic OR with the nHIZ2 pin. Active only in half-bridge input control mode. 0b = Outputs follow IN2/PH signal. 1b = Gate drivers pulldowns are enabled. Half-bridge 2 Hi-Z.

DRV_CTRL_1 register (Address= 0x06h), default value 0xFF=1111 1111$_B$

Bit	Field	Type	Reset	Description
7-4	IDRVP_HS	R/W	1111b	High-side peak source pull-up current. 0000b = 0.5mA 0001b = 1mA 0010b = 2mA 0011b = 3mA 0100b = 4mA 0101b = 6mA 0110b = 8mA 0111b = 12mA 1000b = 16mA 1001b = 20mA 1010b = 24mA 1011b = 28mA 1100b = 31mA 1101b = 40mA 1110b = 48mA 1111b = 62mA
3-0	IDRVN_HS		1111b	High-side peak sink pull-down current. 0000b = 0.5mA 0001b = 1mA 0010b = 2mA 0011b = 3mA 0100b = 4mA 0101b = 6mA 0110b = 8mA 0111b = 12mA 1000b = 16mA 1001b = 20mA 1010b = 24mA 1011b = 28mA 1100b = 31mA 1101b = 40mA 1110b = 48mA 1111b = 62mA

DRV_CTRL_2 register (Address= 0x07h), default value 0xFF=1111 1111$_B$

Bit	Field	Type	Reset	Description
7-4	IDRVP_LS	R/W	1111b	Low-side peak source pull-up current. 0000b = 0.5mA 0001b = 1mA 0010b = 2mA 0011b = 3mA 0100b = 4mA 0101b = 6mA 0110b = 8mA 0111b = 12mA 1000b = 16mA 1001b = 20mA 1010b = 24mA 1011b = 28mA 1100b = 31mA 1101b = 40mA 1110b = 48mA 1111b = 62mA
3-0	IDRVN_LS		1111b	Low-side peak sink pull-down current. 0000b = 0.5mA 0001b = 1mA 0010b = 2mA

				0011b = 3mA 0100b = 4mA 0101b = 6mA 0110b = 8mA 0111b = 12mA 1000b = 16mA 1001b = 20mA 1010b = 24mA 1011b = 28mA 1100b = 31mA 1101b = 40mA 1110b = 48mA 1111b = 62mA

DRV_CTRL3 register (Address= 0x08h), default value 0x20=0010 0000$_B$

Bit	Field	Type	Reset	Description
7-6	VGS_MODE	R/W	00b	VGS gate fault monitor mode. 00b = Latched fault. 01b = Cycle by cycle. 10b = Warning report only 11b = Disabled.
5-4	VGS_TDRV		10b	VGS drive time and VDS monitor blanking time. 00b = 96µs, 01b = 2µs, 10b = 4µs, 11b = 8µs
3-1	VGS_TDEAD		000b	Insertable digital dead-time. 000b = 0ns, 001b = 250ns, 010b = 500ns, 011b = 750ns, 100b = 1000ns, 101b = 2000ns, 110b = 4000ns, 111b = 8000ns
0	VGS_IND		0b	VGS independent shutdown mode enable. Active for BRG_MODE =00b, 11b. 0b = Disabled. 1b = Enabled. VGS gate fault will only shut down the associated half-bridge.

VDS_CTRL1 register (Address= 0x09h), default value 0x20=0010 0000$_B$

Bit	Field	Type	Reset	Description
7-6	VDS_MODE	R/W	00b	VDS overcurrent monitor mode. 00b = Latched fault; 01b = Cycle by cycle. 10b = Warning report only. 11b = Disabled.
5-4	VDS_DG		10b	VDS overcurrent monitor deglitch time. 00b = 1 µs, 01b = 2µs, 10b = 4 µs, 11b = 8µs
3-2	VDS_IDRAIN		00b	IDRVN gate pulldown current after VDS_OCP fault. 00b = Programmed IDRVN; 01b = 8mA; 10b = 31mA; 11b = 62mA
1	VGS_LVL		0b	VGS monitor threshold for dead-time handshake and gate fault detection. 0b = 1.4V. 1b = 1.0V
0	VGS_IND		0b	VDS independent shutdown mode enable. Active for BRG_MODE =00b, 11b. 0b = Disabled.

				1b = Enabled. VDS overcurrent fault will only shut down the associated half-bridge

VDS_CTRL_2 register (Address= 0x0Ah), default value 0xDD=1101 1101$_B$

Bit	Field	Type	Reset	Description
7-4	VDS_HS_LVL	R/W	1101b	High-side VDS overcurrent monitor threshold. 0000b = 0.06V 00001b = 0.08V 0010b = 0.10V 0011b = 0.12V 0100b = 0.14V 0101b = 0.16V 0110b = 0.18V 0111b = 0.2V 1000b = 0.3V 1001b = 0.4V 1010b = 0.5V 1011b = 0.6V 1100b = 0.7V 1101b = 1V 1110b = 1.4V 1111b = 2V
3-0	VDS_LS_LVL		1101b	Low-side VDS overcurrent monitor threshold. 0000b = 0.06V 00001b = 0.08V 0010b = 0.10V 0011b = 0.12V 0100b = 0.14V 0101b = 0.16V 0110b = 0.18V 0111b = 0.2V 1000b = 0.3V 1001b = 0.4V 1010b = 0.5V 1011b = 0.6V 1100b = 0.7V 1101b = 1V 1110b = 1.4V 1111b = 2V

OLSC_CTRL register (Address= 0x0Bh), default value 0x80=1000 0000$_B$

Bit	Field	Type	Reset	Description
7	EN_LIMP	R/W	1 b	Configures the mode of the DRVOFF/Limp multi-function pin. 0b= Pins function as DRVOFF/Limp global driver disable. 1b= Pins function as Limp home driver case input.
6	Reserve		0b	Reserve
5				
4	OLSC_EN		0b	Offline open load and short circuit diagnostic enable. 0b = Disabled. 1b = VDS monitors set into real-time voltage monitor mode and diagnostics current sources enabled.
3	PU_SH1		0b	Half-bridge 1 pull-up diagnostic current source. Must set OLSC_EN bit to use. 0b = Disabled. 1b = Enabled.
2	PD_SH1		0b	Half-bridge 1 pull-down diagnostic current source. Must set OLSC_EN bit to use. 0b = Disabled. 1b = Enabled.

1	PU_SH2		0b	Half-bridge 2 pull-up diagnostic current source. Must set OLSC_EN bit to use. 0b = Disabled. 1b = Enabled.
0	PD_SH2		0b	Half-bridge 2 pull-down diagnostic current source. Must set OLSC_EN bit to use. 0b = Disabled. 1b = Enabled.

UVOV_CTRL register (Address= 0x0Ch), default value 0x14=0001 0100_B

Bit	Field	Type	Reset	Description
7	PVDD_UV_MODE	R/W	0b	PVDD supply undervoltage monitor mode. 0b = Latched fault. 1b = Automatic recovery.
6-5	PVDD_OV_MODE		00b	PVDD supply overvoltage monitor mode. 00b = Latched fault. 01b = Automatic recovery. 10b = Warning report only. 11b = Disabled.
4-3	PVDD_OV_DG		10b	PVDD supply overvoltage monitor deglitch time. 00b = 1µs 01b = 2µs 10b = 4µs 11b = 8µs
2	PVDD_OV_LVL		1b	PVDD supply overvoltage monitor threshold. 0b = 21.5V 1b = 28.5V
1	VCP_UV_MODE		0b	VCP charge pump undervoltage monitor mode. 0b = Latched fault. 1b = Automatic recovery
0	VCP_UV_LVL		0b	VCP charge pump undervoltage monitor threshold. 0b = 2.5V 1b = 5V

CSA_CTRL register (Address= 0x0Dh), default value 0x01=0000 0001_B

Bit	Field	Type	Reset	Description
7	CSA_SH_EN	R/W	0b	Current shunt amplifier sample and hold. 0b = Disabled 1b = Enabled
6	CSA_BLK_SEL		0b	Current shunt amplifier blanking trigger source. 0b = Half-bridge 1 1b = Half-bridge 2
5-3	CSA_BLK		000b	Current shunt amplifier blanking time. % of t_{DRV}. 000b = 0%, Disabled 001b = 25% 010b = 37.5% 011b = 50% 100b = 62.5% 101b = 75% 110b = 87.5% 111b = 100%
2	CSA_DIV		0b	Current shunt amplifier reference voltage divider. 0b = AREF / 2 1b = AREF / 8
1-0	CSA_GAIN		01b	Current shunt amplifier gain setting. 00b = 10V/V 01b = 20V/V 10b = 40V/V 11b = 80V/V

Application Information

The SA52902 is a highly integrated, two-channel gate driver designed for driving single motor. The device incorporates two N-channel half-bridge gate drivers, driver power supplies, and one current shunt amplifier. The SA52902 offers several protections and off-state detection which can be configured through SPI.

Schematic

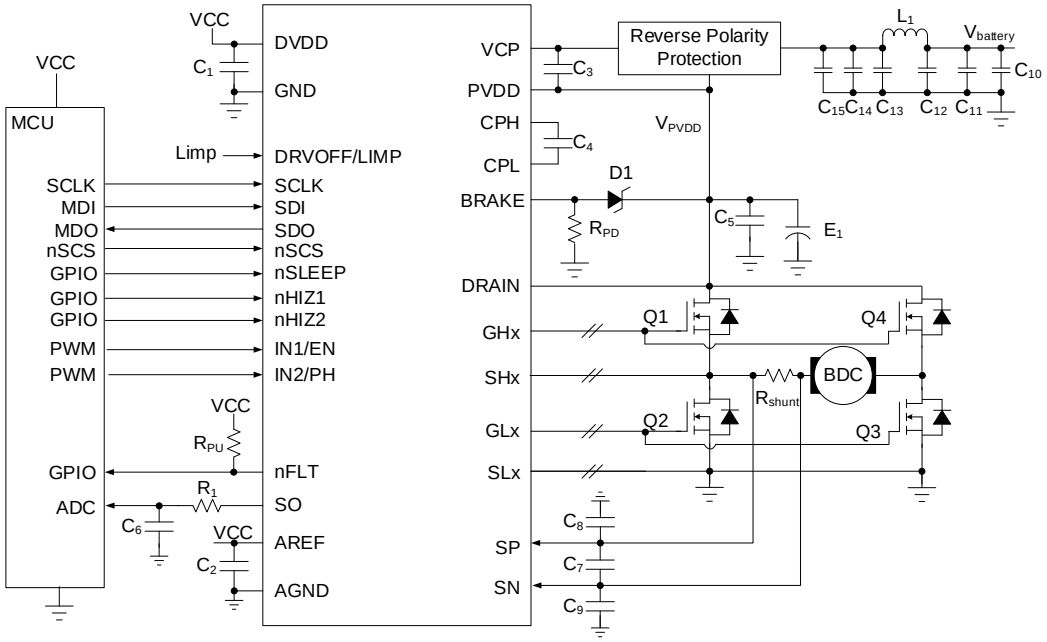


Figure 22. Typical Application Schematic

BOM List

Design Parameter	Example Value
E_1	100μF/E_{cap}/50V
C_1/C_3/C_{10}/C_{13}	1μF/50V
C_2/C_4/C_5/C_6/C_8/C_9/C_{11}/C_{14}	100nF/50V
C_7/C_{12}/C_{15}	10nF/50V
R_{shunt}	7mΩ
R1/R_{PU}	1kΩ
R_{PD}	1MΩ
D1	20V Zener (according to requirements)
L_1	2.2μH
Q1 Q_2 Q_3 Q_4	N Channel MOSFET

Note: If R_{shunt} is placed on high-side, increased attention is required for sleep current loss. In this configuration, an additional current flows through the current amplifier input resistor (approximately 500kΩ per SP/SN) between SP/SN and GND.

Layout Design

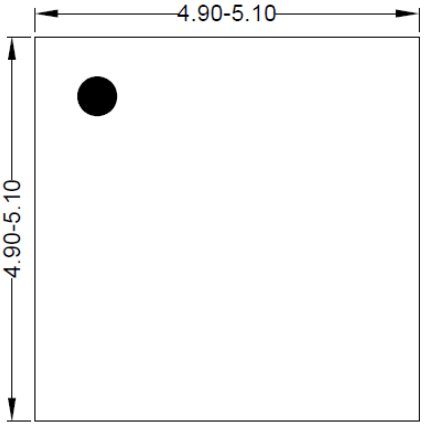
Follow these PCB layout guidelines for optimal performance and thermal dissipation:

1. Bypass the PVDD pin to GND using a low-ESR 0.1 μF ceramic bypass capacitor placed as close as possible to the PVDD pin, with a wide trace or ground plane connection to the GND pin. Additionally, use a bulk capacitor rated for the application to further bypass the PVDD pin. This can be an electrolytic capacitor with a minimum capacitance of 10μF. It

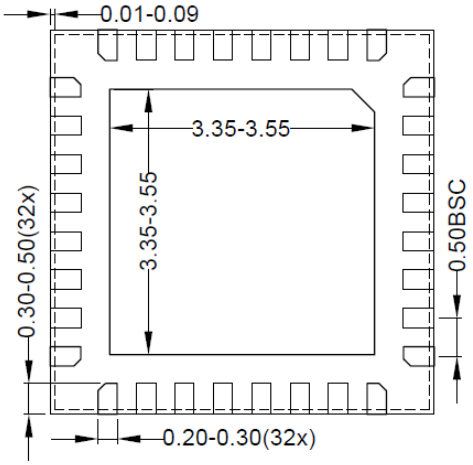
is acceptable for this bulk capacitance to be shared with that used for the external power MOSFETs.

2. Additional bulk capacitance is necessary to bypass the high current path through the external MOSFETs. This capacitance should be positioned to minimize the length of high current traces. Use wide metal traces and multiple vias to connect across PCB layers, which reduces inductance and enables the bulk capacitor to effectively supply high current during switching events.
3. Place a low-ESR 0.1μF ceramic capacitor between the CPL and CPH pins. This capacitor should be rated for PVDD and use an X5R or X7R dielectric. Additionally, place a low-ESR 1μF ceramic capacitor between the VCP and PVDD pins. This capacitor should be rated for 16V and also use an X5R or X7R dielectric.
4. Bypass the DVDD pin to GND using a 1.0μF low-ESR ceramic capacitor rated for 6.3V, with an X5R or X7R dielectric. Place this capacitor as close as possible to the DVDD pin and minimize the trace length to the GND connection. If a nearby bypass capacitor already exists for the external low-voltage power supply and power supply noise is minimal, this component may be considered optional.
5. Bypass the AREF pin to GND using a 0.1μF low-ESR ceramic capacitor rated for 6.3V with an X5R or X7R dielectric. Place the capacitor as close as possible to the AREF pin, minimizing the trace length to GND. If a nearby bypass capacitor is already present for the external low-voltage power supply and power supply noise is minimal, this component may be considered optional.
6. The DRAIN pin may be directly shorted to the PVDD pin. However, if there is a significant distance between the device and the external MOSFETs, it is recommended to use a dedicated trace to connect the DRAIN pin to the common drain node of the high-side external MOSFETs. Avoid connecting the SLx pins directly to the ground plane. Instead, use dedicated traces to connect them to the sources of the low-side external MOSFETs. These layout practices enhance the accuracy of VDS sensing for overcurrent detection.
7. Minimize the loop length for both the high-side and low-side gate driver paths. The high-side loop runs from the GHx pin to the gate of the high-side power MOSFET and returns via the MOSFET source to the SHx pin. The low-side loop extends from the GLx pin to the gate of the low-side power MOSFET and returns through the MOSFET source to the SLx pin. Reducing loop length helps improve switching performance and reduces noise.

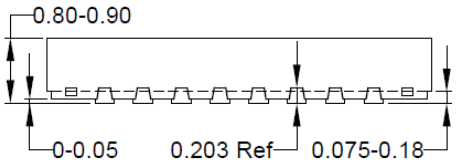
QFN5×5-32 Package Outline & PCB Layout



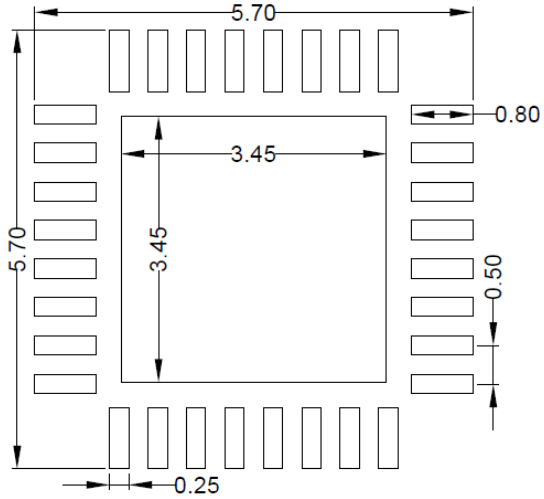
Top View



Bottom View



Front View

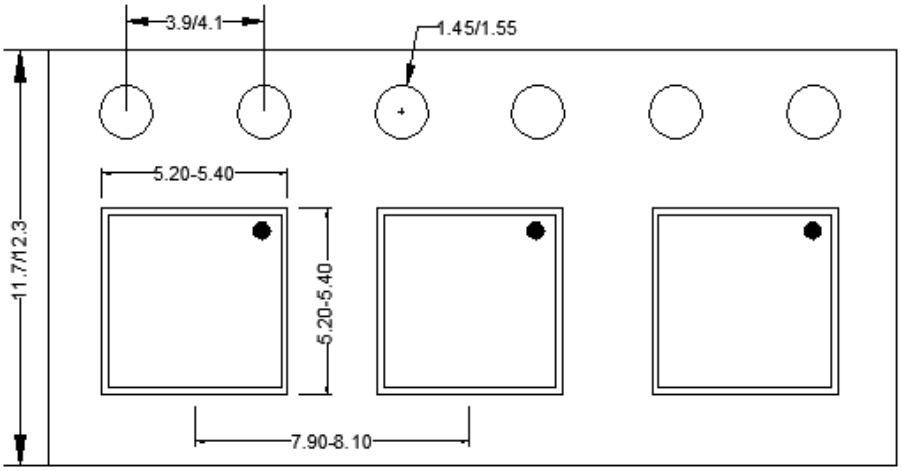


Recommended Pad Layout
(Reference Only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

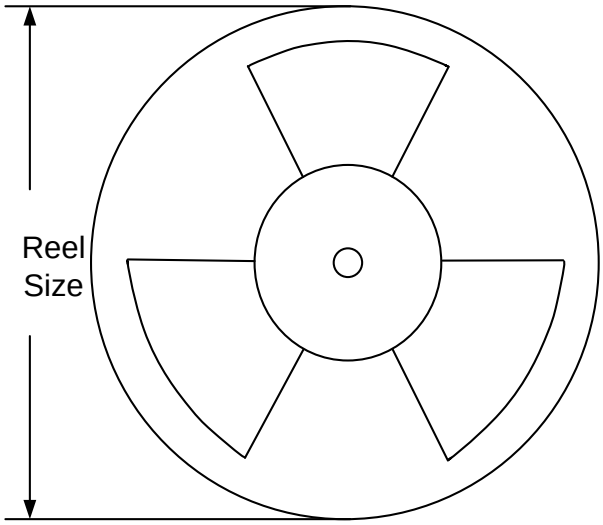
Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Feeding direction →

Reel Dimensions



Package Type	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer Length(mm)	Leader Length (mm)	Qty per Reel
QFN5×5	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
1.0	Sept. 03, 2025	Initial Release	

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