SA52122B

Twelve Half-Bridge Driver with SPI Control

General Description

The SA52122B is a twelve half-bridge motor driver solution designed for automotive, industrial, and mechatronic applications. The half-bridges are fully controllable, facilitating forward, reverse, coasting, and braking motor operations. All the functions can be programmed through a serial peripheral interface (SPI).

The device includes protection features such as overcurrent protection, open load detection, undervoltage lockout, overvoltage lockout, and thermal shutdown for reliable operation.

The open-drain nFAULT output can be configured to signal fault conditions to the host.

The device is available in a TSSOP24E package with an exposed pad for improved thermal dissipation.

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Features

- 12 Half-Bridge Outputs
- Operating Voltage: 4.5V to 32V
- Compatible with a 5V/3.3V System
- Up to 1A Output Current for Each Output
- Low-Power Sleep Mode
- SPI Up to 5MHz
- Daisy Chain Functionality
- PWM Capable Output for Frequencies of 80Hz, 100Hz, 200Hz, 400Hz, 600Hz, 800Hz, 1kHz and 2kHz with an 8-Bit Duty Cycle Resolution
- Integrated Protection Features:
  - Overcurrent Protection
  - Short-Circuit Protection
  - Open Load Detection
  - Undervoltage Lockout
  - Overvoltage Protection
  - Thermal Shutdown
- nFAULT Pin Output
- TSSOP24E Package
- MSL Rating: MSL3
- AEC-Q100 Qualified

Applications

- Automotive
- HVAC
- DC Brushed Motor Drivers
- LEDs

Typical Application

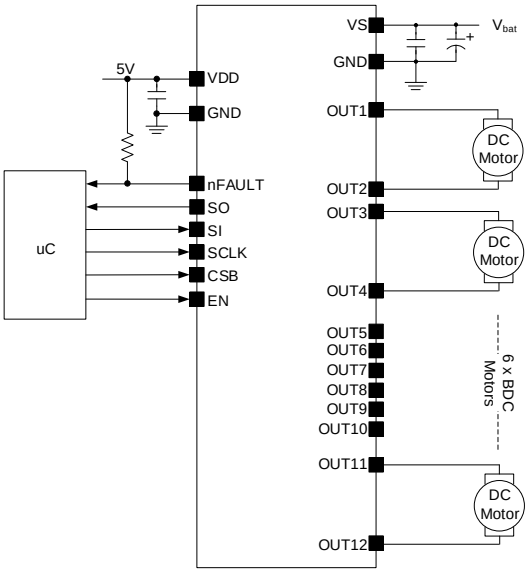


Figure 1. Typical Application Circuit

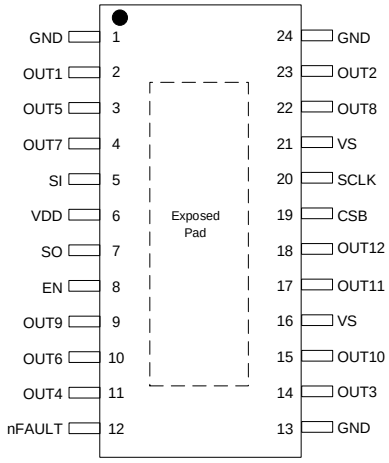
Ordering Information

Ordering Part Number	Package Type	Top Mark
SA52122BHHP	TSSOP24E RoHS Compliant and Halogen Free	***LKGxyz***

Device code: LKG

x=year code, y=week code, z= lot number code

Pinout (Top View)



Pin Name	Pin Number	Pin Description
GND	1,13,24	Ground.
OUT1	2	Half-bridge output 1.
OUT5	3	Half-bridge output 5.
OUT7	4	Half-bridge output 7.
SI	5	16-bit SPI data input.
VDD	6	Power supply for internal logic. It is recommended to choose 1nF and 100nF low-ESR ceramic bypass capacitor to filter out high-frequency noise.
SO	7	16-bit SPI data output.
EN	8	Drive enable pin. Logic high enables the device. Internal pull-down.
OUT9	9	Half-bridge output 9.
OUT6	10	Half-bridge output 6.
OUT4	11	Half-bridge output 4.
nFAULT	12	Fault indicator output. Open-drain. This pin is pulled low during a fault condition and requires an external pull-up resistor for operation.
OUT3	14	Half-bridge output 3.
OUT10	15	Half-bridge output 10.
VS	16,21	Main power supply. It is recommended to use at least 10μF capacitance to maintain a stable motor supply voltage, and choose 1nF and 100nF low-ESR ceramic bypass capacitor to filter out high-frequency noise.
OUT11	17	Half-bridge output 11.
OUT12	18	Half-bridge output 12.
CSB	19	Chip select Bar. Active low serial port operation. Internal pull-up.
SCLK	20	SPI clock input.
OUT8	22	Half-bridge output 8.
OUT2	23	Half-bridge output 2.
Exposed Pad	-	Exposed Pad. It is recommended to connect the pad to GND for heat dissipation.

Block Diagram

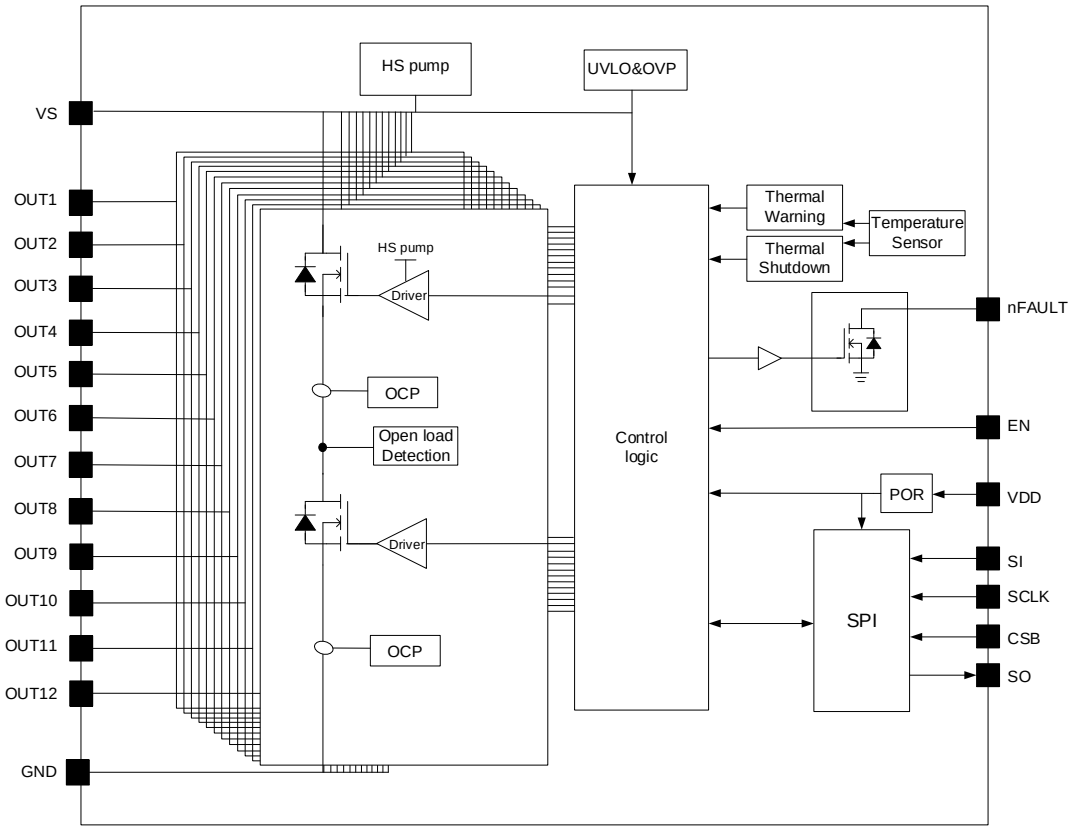


Figure 2. SA52122B Functional Block Diagram

Absolute Maximum Ratings (Note 1)

Parameter		Min	Max	Unit
VS (DC)		-0.3	40	V
OUTx (DC)		-0.3	VS+0.7	V
Digital Pins (SI, SCLK, CSB, SO, EN, and nFAULT)		-0.3	VDD+0.3	V
VDD		-0.3	5.75	V
Continuous Supply Current (VS pins) (Note 2)		0	6	A
Continuous Sink Current (GND pins) (Note 2)		0	6	A
Junction Temperature (T_J)		-40	150	°C
Storage Temperature		-65	150	°C
Electrostatic Discharge	HBM (Human Body Model) VS and OUTx pins	4k		V
	HBM (Human Body Model) all other pins	2k		
	CDM (Charge Device Model)	500		
	CDM (Charge Device Model) corner pins	750		

Thermal Information

Parameter (Note 3)	Typ.	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance (TSSOP24E)	29	°C/W
$\theta_{JC\ TOP}$ Junction-to-Case Thermal Resistance (TSSOP24E)	17.6	

Recommended Operating Conditions

Parameter (Note 4)	Min	Max	Unit
VS	4.5	32	V
VDD	3.15	5.5	V
Digital Pins	0	5.5	V
nFAULT Pullup Voltage	0	5.5	V
nFAULT Input Current	0	5	mA
Operating Temperature (T_A)	-40	125	°C
Junction Temperature (T_J)	-40	150	°C

Electrical Characteristics

(-40°C ≤ T_A ≤ 125°C, 4.5V ≤ VS ≤ 32V, 3.15V ≤ VDD ≤ 5.5V, EN=VDD, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supplies	VS Sleep Mode Current	I_{VS_sleep}	VS =40V, EN=L, T_A=25°C		0	1	μA
			VS =40V, EN=L, T_A=125°C			2	μA
	VS Standby Mode Current	$I_{VS\_standby}$	VS=13.5V, EN=H, Driver=OFF, T_A=25°C		0.8	1.6	mA
			VS=13.5V, EN=H, Driver=OFF, T_A=125°C			1.6	mA
	VS Operating Mode Current	I_{VS}	VS=13.5V, EN=H, All High-side MOSFETs=ON, T_A=25°C		3.3	5	mA
			VS=13.5V, EN=H, All High-side MOSFETs=ON, T_A=125°C			5	mA
	VS Undervoltage Lockout Voltage	V_{UVLO_FALL}	VS falling	3.7		4.3	V
		V_{UVLO_RISE}	VS rising	4		4.5	V
		V_{UVLO_HYS}			250		mV
	VS Undervoltage Lockout Deglitch Time	t_{UVLO}			10		μs
	VS Overvoltage Protection	V_{OVP}	VS rising, EXT_OVP=0b	21		25	V
			VS falling, EXT_OVP=0b	20		24	V
			VS rising, EXT_OVP=1b	32.7		35.5	V
			VS falling, EXT_OVP=1b	31.7		34.5	V
		V_{OVP_HYS}	Rising to falling hysteresis, EXT_OVP=0b		1		V
			Rising to falling hysteresis, EXT_OVP=1b		1		V
	VS Overvoltage Protection Deglitch Time	t_{OVP}			10		μs
	VDD Power On Reset Threshold	V_{POR_ON}	Supply rising	2.75		2.95	V
	VDD Power Off Reset Threshold	V_{POR_OFF}	Supply falling	2.6		2.8	V
	Logic Undervoltage Hysteresis	V_{POR_HYS}	Rising to falling hysteresis		150		mV
	VDD Operating Supply Current	I_{VDD}	VS =13.5V, VDD=3.3V, EN=H, All Low-side MOSFETs=ON, SPI=ON, T_A=25°C		2	5	mA
			VS =13.5V, VDD=3.3V, EN=H, All Low-side MOSFETs=ON, SPI=ON, T_A=125°C			5	mA
	VDD Standby Mode Current	$I_{VDD\_Standby}$	VS=13.5V, VDD=3.3V, EN=H, SPI=OFF, T_A=25°C		1	2.5	mA
			VS=13.5V, VDD=3.3V, EN=H, SPI=OFF, T_A=125°C			2.5	mA
	VDD Sleep Mode Current	I_{VDD_SLEEP}	VS=13.5V, VDD=5V, EN=L, TA=25°C		0	1.7	μA
			VS=13.5V, VDD=5V， EN=L, TA=125°C			2	μA
Logic Level Input (EN, SI, SCLK, CSB)	Input Low Voltage	V_{IL}		0		0.3* VDD	V
	Input High Voltage	V_{IH}		0.7* VDD		VDD	
	Input Logic Hysteresis	V_{HYS}		200			mV
	Input Low Current	I_{IL}	V_{IN}=0V, (SI, SCLK, EN)	-1		1	μA
			V_{IN}=0V, VDD=5V, (CSB)		45	65	
	Input High Current	I_{IH}	V_{IN}=5V, (SI, SCLK, EN)		45	65	
			V_{IN}=VDD, (CSB)	-1		1	
	Input Capacitance	C_{CAPINX}	(Note 5)			15	pF
Open-Drain Output (nFAULT)	Output Low Voltage	V_{OL}	I_{sink}=5mA	0		0.2	V
	Output High Current	I_{OH}	V_{OD}=5V	-1		1	μA
	Output Capacitance	C_{OD}	(Note 5)			15	pF
Push-Pull Output (SO)	Output Low Voltage	V_{OL}	I_{out}=-5mA	0		0.2	V
	Output High Voltage	V_{OH}	I_{out}=5mA	VDD -0.6		VDD	V
	Output Capacitance	C_{OD}	(Note 5)			30	pF
	Output Low Current	I_{OL}	V_{SO}=0V	-1		1	μA

	Output High Current	I_{OH}	V_{SO}=VDD	-1		1	μA
Power MOSFETs	High Side MOSFETs On Resistance	R_{DSON}	I_{out}=-500mA, VS=13.5V, T_A =25°C		0.75	1.1	Ω
			I_{out}=-500mA, VS=13.5V, T_A =125°C			1.5	
	Low Side MOSFETs On Resistance		I_{out}=500mA, VS=13.5V, T_A =25°C		0.75	1.1	Ω
			I_{out}=500mA, VS=13.5V, T_A =125°C			1.5	
	Output Rise and Fall Time (HS and LS)	$SR_{rise\ and\ fall}$	VS =13.5V,10%-90%, R_{LOAD}=27Ω, HBx_SR=0b		1		V/μs
			VS =13.5V,10%-90%, R_{LOAD}=27Ω, HBx_SR=1b		3.2		V/μs
	Output Dead Time (H to L / L to H)	t_{DEAD}	VS =13.5V, SR=0, HS/LS driver OFF to LS/HS driver ON	8	20	32	μs
			VS =13.5V, SR=1, HS/LS driver OFF to LS/HS driver ON	2	5	15	μs
	Propagation Delay (HS and LS ON/OFF)	t_{PD}	High-side ON or low-side ON command (SPI last transition) to OUTx transition from Hi-Z state, SR=0	5	12	25	μs
			High-side ON or low-side ON command (SPI last transition) to OUTx transition from Hi-Z state, SR=1	3	6	12	μs
	Source Leakage Current	I_{source_LC}	OUTx=0V, EN=H	-25	-10		μA
			OUTx=0V, EN=L	-2			μA
	Sink Leakage Current	I_{sink_LC}	OUTx=13.5V, EN=H, SR=0b		9	15	μA
			OUTx=13.5V, EN=H, SR=1b		9	15	μA
			OUTx=13.5V, EN=L		0	1	μA
PWM Mode	PWM Switching Frequency	f_{PWM}	PWM_CHx_FREQ[2]=0b PWM_CHx_FREQ[1:0]=00b	72	80	88	Hz
			PWM_CHx_FREQ[2]=0b PWM_CHx_FREQ[1:0]=01b	90	100	110	Hz
			PWM_CHx_FREQ[2]=0b PWM_CHx_FREQ[1:0]=10b	180	200	220	Hz
			PWM_CHx_FREQ[2]=0b PWM_CHx_FREQ[1:0]=11b	1800	2000	2200	Hz
			PWM_CHx_FREQ[2]=1b PWM_CHx_FREQ[1:0]=00b	360	400	440	Hz
			PWM_CHx_FREQ[2]=1b PWM_CHx_FREQ[1:0]=01b	540	600	660	Hz
			PWM_CHx_FREQ[2]=1b PWM_CHx_FREQ[1:0]=10b	720	800	880	Hz
			PWM_CHx_FREQ[2]=1b PWM_CHx_FREQ[1:0]=11b	900	1000	1100	Hz
Protections	Thermal Warning Temperature	T_{WARN}		120	140	170	°C
	Thermal Warning Hysteresis	T_{WARN_HYS}			20		°C
	Thermal Shutdown Temperature	T_{SD}		150	165	200	°C
	Thermal Shutdown Hysteresis	T_{HYS}			20		°C
	Over Current Shutdown (Source)	I_{OCSO}	VDD=5V, VS=13.5V	-2.2	-1.5	-1.1	A
	Over Current Shutdown (Sink)	I_{OCSI}	VDD=5V, VS=13.5V	1.1	1.5	2.2	A
	Over Current Shutdown Delay Time	t_{oc}	OCP_DEG=000b	6	10	14	μs
			OCP_DEG=001b	2.6	5	7.9	μs
			OCP_DEG=010b	0.4	2.5	5.9	μs
			OCP_DEG=011b	0.1	1	3.4	μs
			OCP_DEG=110b	18.5	30	41.5	μs
			OCP_DEG=111b	8.4	20	31.6	μs
	Open Load Detection Current	I_{OLD}	High-side	1	8	17	mA
			Low-side	4	11	20	
	Open Load Detection Current in Low Current OLD Mode	I_{OLD_LOW}	Low-side	0.5	1.2	2.1	mA
	Open Load Detection Delay Time	t_{OL}	Active OLD (Continuous Mode)	2.2	3	3.8	ms
			Active OLD (PWM Mode)	150	200	300	μs

Serial Peripheral Interface

(-40°C ≤ T_A ≤ 125°C, 4.5V ≤ VS ≤ 32V, 3.15V ≤ VDD ≤ 5.5V, EN=VDD, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}				5	MHz
SCLK High Time	t_{CLKH}	(Note 5)	100			ns
SCLK Low Time	t_{CLKL}	(Note 5)	100			ns
SI Setup Time	t_{SU_SI}	(Note 5)	40			ns
SI Hold Time	t_{HD_SI}	(Note 5)	60			ns
SO Output Data Delay Time	t_{DLY_SO}	SCLK high to SO valid(Note 5)			60	ns
CSB Setup Time	t_{SU_CSB}	(Note 5)	100			ns
CSB Hold Time	t_{HD_CSB}	(Note 5)	100			ns
CSB Disable Delay Time	t_{DIS_CSB}	CSB high to SO High-Z (Note 5)		30		ns
CSB Minimum High Time before Active Low	t_{HI_CSB}	(Note 5)	600			ns
EN Low Valid Time	t_{ENL}	VDD=5V, EN going low 50% to OUTx turning off 50% (Note 5)			30	μs
EN High to SPI Valid	t_{ENH_SPIV}	(Note 5)			200	μs

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \approx T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 3: θ_{JA} is measured with natural convection at T_A = 25°C on a four-layer Silergy evaluation board.

Note 4: The device is not guaranteed to function outside its operating conditions.

Note 5: Guaranteed by design or statistical correlation and not production tested.

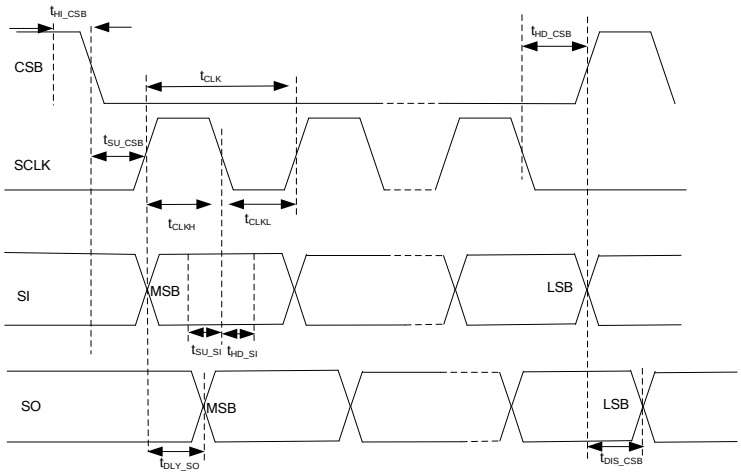
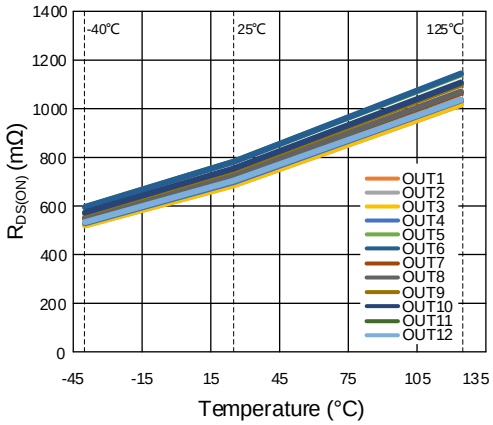


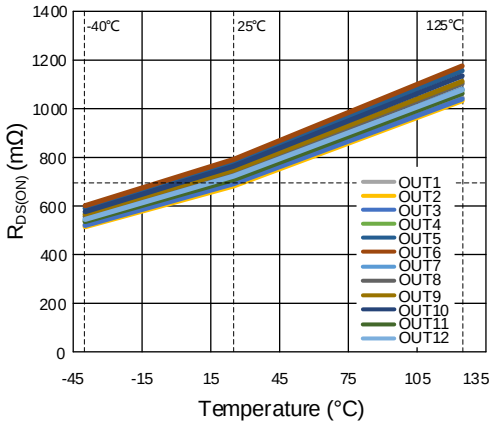
Figure 3. SPI Timing

Typical Performance Characteristics

High Side MOSFETs on Resistance

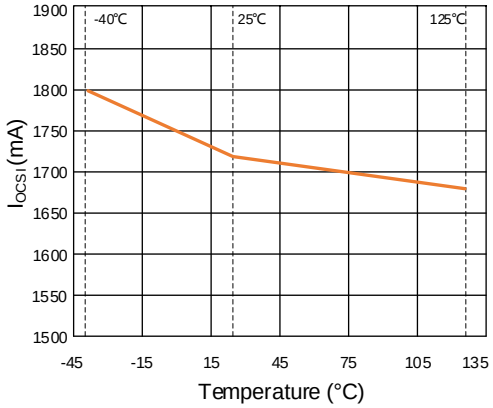


Low Side MOSFETs on Resistance



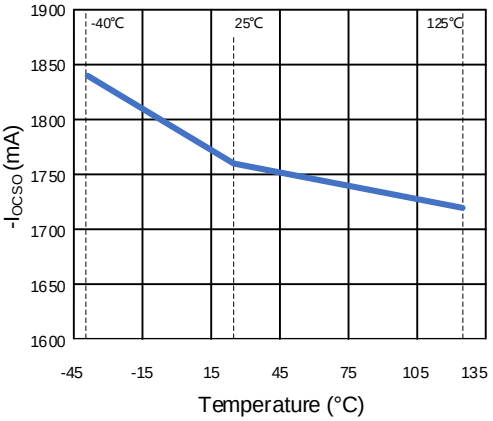
Low Side MOSFETs Over Current Limit

(VS=13.5V)



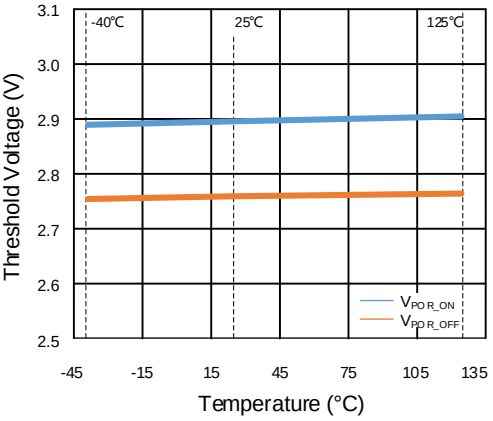
High Side MOSFETs Over Current Limit

(VS=13.5V)



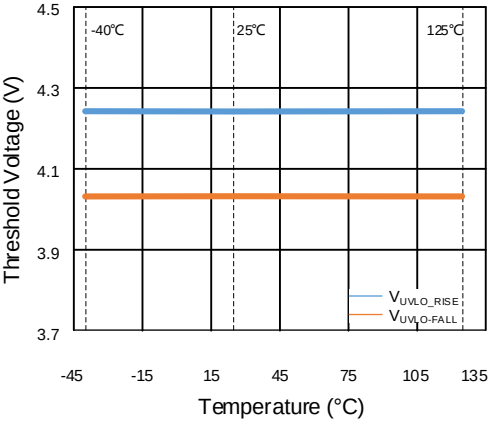
VDD Power On Reset and Power Off Reset

(VS=13.5V)

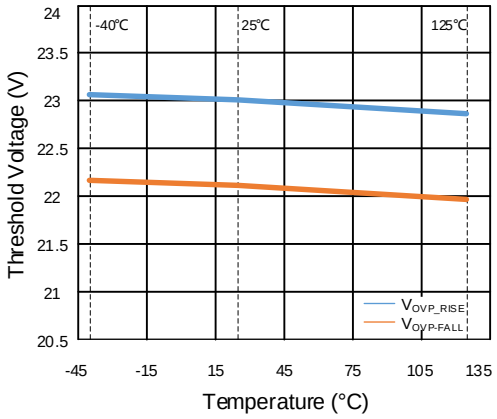


VS Undervoltage Lockout Voltage

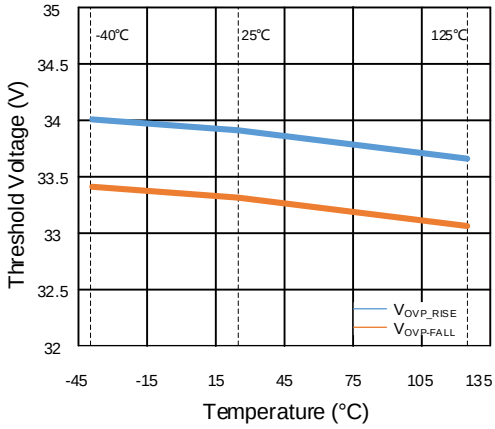
(VDD=5V)



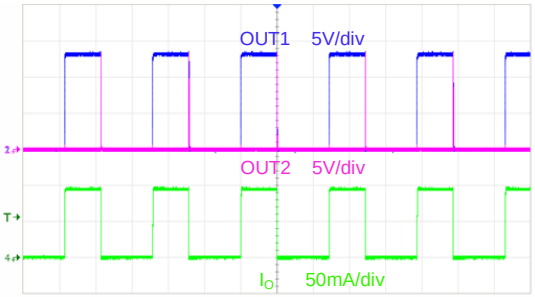
VS Overvoltage Protection Voltage
(EXT_OVP=0)



VS Overvoltage Protection Voltage
(EXT_OVP=1)

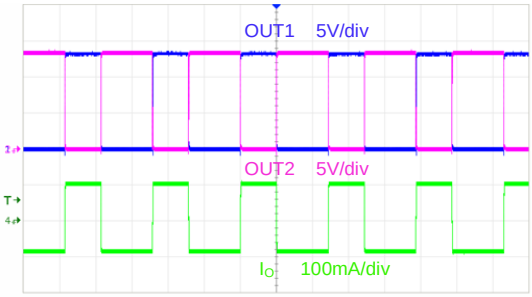


Passive Free-wheeling
(VS=13.5V Io=100mA Duty=40% Frequency=80Hz)



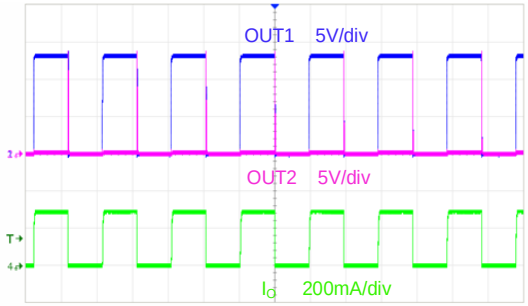
Time (5ms/div)

Active Free-wheeling
(VS=13.5V Io=100mA Duty=40% Frequency=80Hz)



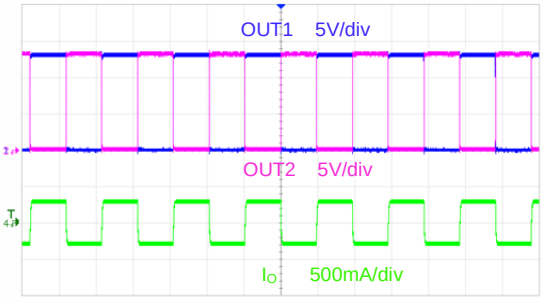
Time (5ms/div)

Passive Free-wheeling
(VS=13.5V Io=300mA Duty=50% Frequency=100Hz)



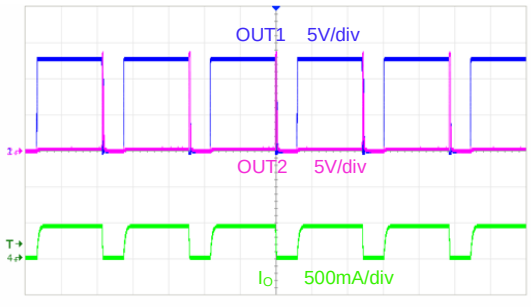
Time (5ms/div)

Active Free-wheeling
(VS=13.5V Io=300mA Duty=50% Frequency=100Hz)



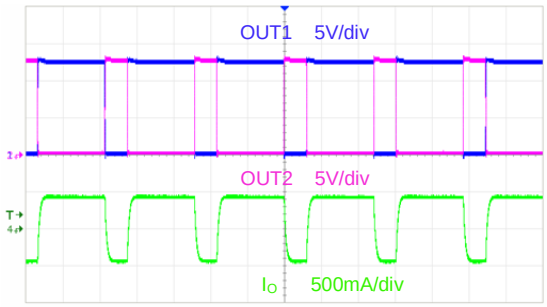
Time (5ms/div)

Passive Free-wheeling
(VS=13.5V Io=500mA Duty=75% Frequency=200Hz)



Time (2ms/div)

Active Free-wheeling
(VS=13.5V Io=500mA Duty=75% Frequency=200Hz)



Time (2ms/div)

Detailed Description

The SA52122B is a twelve half-bridge motor driver solution for automotive, industrial, and other mechatronic applications. It can be configured as six independent H-bridges. Each half-bridge is designed to support up to 1A current.

To reduce the impact of electromagnetic interference (EMI) generated by the device, a spread spectrum clocking technique for the oscillator and charge pump is designed.

The device supports a standard 16-bit, 5MHz serial peripheral interface (SPI). The device also features daisy-chain functionality, enabling the connection of multiple devices using a single CSB line.

Power Supply

VS supplies power to the MOSFETs, while VDD powers the logic circuits. Once VS is powered up, the drivers can be activated. Initially, all drivers are set to an off condition and maintain this state regardless of the VDD status. Powering up VDD resets all internal logic. All internal registers are cleared upon VDD Power-On Reset (POR).

Driving Control

The device can be configured as an H-bridge, high-side driver, or low-side driver. The half-bridge outputs of the device are designed to drive motor or LED loads. The half-bridge drivers can be programmed for continuous load driving (without PWM) or in chopping mode (with PWM). They also support parallel operation, which can be used for driving high-current loads.

Continuous Mode (Without PWM)

The half-bridge drivers can be programmed to drive loads continuously without PWM. The device can set the high-side enable bits (HBx_HS_EN) and low-side enable bits (HBx_LS_EN) in the SPI memory-mapped control registers (OP_CTRL_1, OP_CTRL_2 and OP_CTRL_3) to switch the high-side or low-side individually.

Additionally, the device will stay in Hi-Z mode a particular half-bridge's high-side and low-side switches are simultaneously set high. This configuration is illustrated in Figures 4 and 5, which show OUT1 and OUT2 driving a DC brush motor. In this setup, the motor operates in the forward direction when the high-side MOSFET of OUT1 and the low-side MOSFET of OUT2 are activated, allowing the motor current to flow from OUT1 to OUT2. Conversely, activating the high-side MOSFET of OUT2 and the low-side MOSFET of OUT1 will reverse the motor's direction, resulting in the motor current flowing from OUT2 to OUT1.

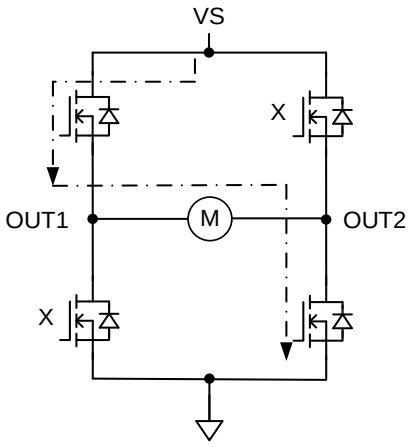


Figure 4. Continuous Mode (Forward)

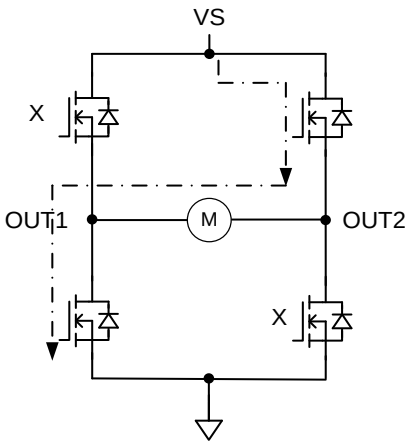


Figure 5. Continuous Mode (Reverse)

If the motor initially operates in either the forward or reverse direction, and then both the high-side and low-side are switched off, the H-bridge will enter coast mode. Due to the inductive energy, current will continue to flow in the motor, taking a path through the body diodes of the MOSFETs, as illustrated in Figures 6 and 7.

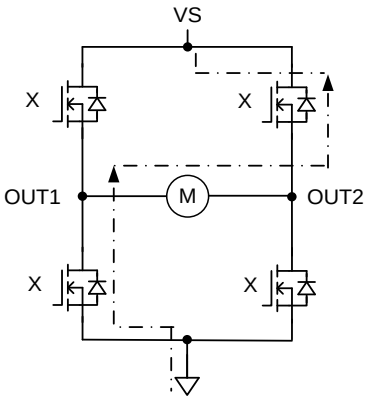


Figure 6. Coast-From Forward

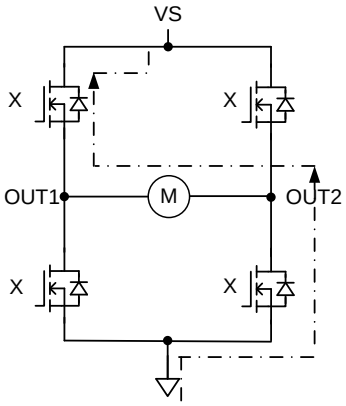


Figure 7. Coast-From Reverse

If the motor initially operates in either the forward or reverse direction and then either the high-side or low-side MOSFETs are switched on, the H-bridge will enter brake mode. In the case of low-side braking, both low-side MOSFETs of the driver are turned on. Similarly, for high-side braking, both high-side MOSFETs are turned on. These configurations are illustrated in Figures 8 and 9.

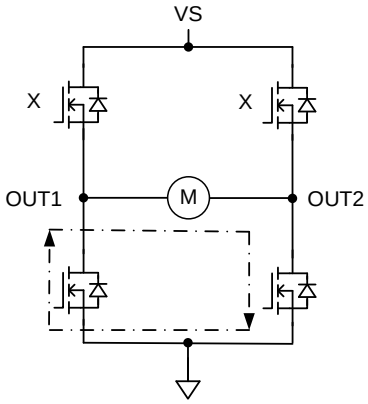


Figure 8. Brake-Low-Side

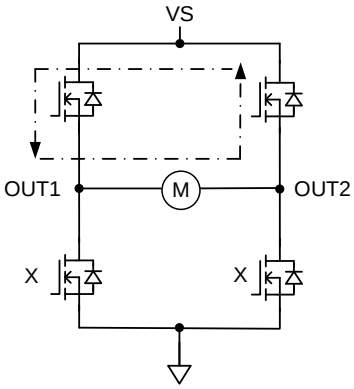


Figure 9. Brake-High-Side

Chopping Mode (With PWM)

Each half-bridge of the device can be configured for PWM mode, making it suitable for driving inductive loads such as DC brush motors. The device features twelve distinct PWM channels, each with its own duty cycle settings using an 8-bit resolution. It offers eight selectable PWM frequencies — 80Hz, 100Hz, 200Hz, 400Hz, 600Hz, 800Hz, 1kHz and 2kHz — to meet various application requirements.

The PWM chopping mode operation is performed through the following steps:

PWM Configuration

The half-bridge can be configured for continuous or chopping mode (PWM mode) through the PWM control register (PWM_CTRL_1 and PWM_CTRL_2). The HBx_PWM bit must be set to 1 to enable PWM switching mode. If not set, the half-bridge will operate in continuous mode. Additionally, setting the PWM_CHx_DIS bit in the PWM control register (PWM_CTRL_2 and PWM_CTRL_3) activates the PWM generator.

Free-Wheeling Mode (Synchronous Rectification) Disable/Enable

The device allows the selection of the synchronous rectification mode by setting the HBx_FW bit in the free-wheeling control registers (FW_CTRL_1 and FW_CTRL_2). As illustrated in Figure 10, when the HBx_FW is disabled, current flows through the high-side diode during the PWM off time. Conversely, enabling the HBx_FW bit opens the MOSFET to create an alternative current path. Figure 11 provides an example of synchronous rectification, demonstrating how the high-side

MOSFET of the OUT2 half-bridge is turned on while the low-side MOSFET of the same half-bridge is turned off during a PWM cycle.

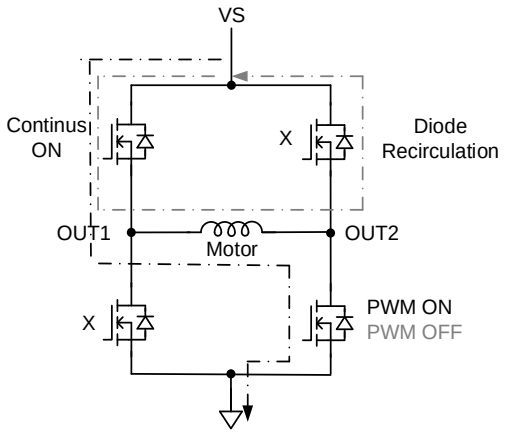


Figure 10. PWM Mode (Synchronous Rectification = OFF)

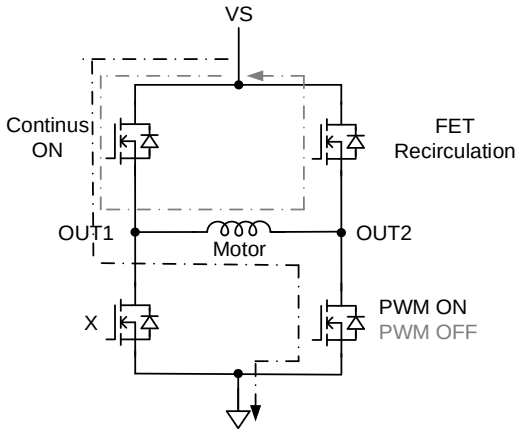


Figure 11. PWM Mode (Synchronous Rectification = ON)

PWM Channels Mapping

By configuring the PWM map control registers (PWM_MAP_CTRL_x), any OUTx half-bridge output can be mapped to any of the twelve available PWM generators. The HBx_PWM_MAP bits are used to assign any of these twelve channels, as detailed in Table 1.

Table 1. PWM Mapping

HBx_PWM MAP BITS	PWM CHANNEL
HBx_PWM_MAP[3:2]=00b; HBx_PWM_MAP[1:0]=00b	Channel 1 selected for OUTx
HBx_PWM_MAP[3:2]= 00b; HBx_PWM_MAP[1:0]=01b	Channel 2 selected for OUTx
HBx_PWM_MAP[3:2]= 00b; HBx_PWM_MAP[1:0]=10b	Channel 3 selected for OUTx
HBx_PWM_MAP[3:2]= 00b; HBx_PWM_MAP[1:0]=11b	Channel 4 selected for OUTx
HBx_PWM_MAP[3:2]=01b; HBx_PWM_MAP[1:0]=00b	Channel 5 selected for OUTx
HBx_PWM_MAP[3:2]=01b; HBx_PWM_MAP[1:0]=01b	Channel 6 selected for OUTx
HBx_PWM_MAP[3:2]=01b; HBx_PWM_MAP[1:0]=10b	Channel 7 selected for OUTx
HBx_PWM_MAP[3:2]=01b; HBx_PWM_MAP[1:0]=11b	Channel 8 selected for OUTx
HBx_PWM_MAP[3:2]=10b; HBx_PWM_MAP[1:0]=00b	Channel 9 selected for OUTx

HBx_PWM_MAP[3:2]=10b; HBx_PWM_MAP[1:0]=01b	Channel 10 selected for OUTx
HBx_PWM_MAP[3:2]=10b; HBx_PWM_MAP[1:0]=10b	Channel 11 selected for OUTx
HBx_PWM_MAP[3:2]=10b; HBx_PWM_MAP[1:0]=11b	Channel 12 selected for OUTx

PWM Channels Configuration (PWM Frequency and PWM Duty)

Each PWM generator can be independently configured with a different frequency and duty-cycle. The PWM frequency for each channel is determined by the PWM frequency control register (PWM_FREQ_CTRL_x), as shown in Table 2. The PWM duty cycle is managed using the PWM_DUTY_CHx bit in the PWM control register (PWM_DUTY_CTRL_x), as shown in Table 3.

Table 2. PWM Frequency

PWM_CHx_FREQ BITS	PWM FREQUENCY
PWM_CHx_FREQ[2]=0b; PWM_CHx_FREQ[1:0]=00b	80Hz
PWM_CHx_FREQ[2]=0b; PWM_CHx_FREQ[1:0]=01b	100Hz
PWM_CHx_FREQ[2]=0b; PWM_CHx_FREQ[1:0]=10b	200Hz
PWM_CHx_FREQ[2]=0b; PWM_CHx_FREQ[1:0]=11b	2000Hz
PWM_CHx_FREQ[2]=1b; PWM_CHx_FREQ[1:0]=00b	400Hz
PWM_CHx_FREQ[2]=1b; PWM_CHx_FREQ[1:0]=01b	600Hz
PWM_CHx_FREQ[2]=1b; PWM_CHx_FREQ[1:0]=10b	800Hz
PWM_CHx_FREQ[2]=1b; PWM_CHx_FREQ[1:0]=11b	1000Hz

Table 3. PWM Duty Control Channelx Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CHx	R/W	00000000b	00000000b = 0% PWM Duty 11111111b = 100% PWM Duty Calculate duty as a decimal (xxxxxxxxb) × 1/255

Half-Bridge Enable

Following the initial four configuration steps, the final step involves enabling the twelve high-side or low-side MOSFETs. Once the half-bridge is configured for PWM generation, activation is achieved by enabling one of these switches. Specifically, the HBx_HS_EN bit in the operation control registers (OP_CTRL_1, OP_CTRL_2, OP_CTRL_3) enables the high-side, while the HBx_LS_EN bit enables the low-side.

Protection Circuits

This device has embedded protection functions such as undervoltage, overvoltage, overcurrent, power-on reset, open load, thermal warning and thermal shutdown.

Undervoltage Lockout (UVLO)

When the voltage VS drops below the switch-off voltage threshold, V_{UVLO_FALL}, all output stages are turned off. The configuration information remains intact and uncorrupted. The VS undervoltage error bit is also latched high in the device status register (IC_STAT), and the nFAULT pin is driven low. If VS rises again and reaches the switch on the voltage V_{UVLO_RISE} threshold, the power stages will be reactivated, and the nFAULT pin is set to high-impedance. The UVLO error bit remains set until manually cleared through the CLR_FLT bit.

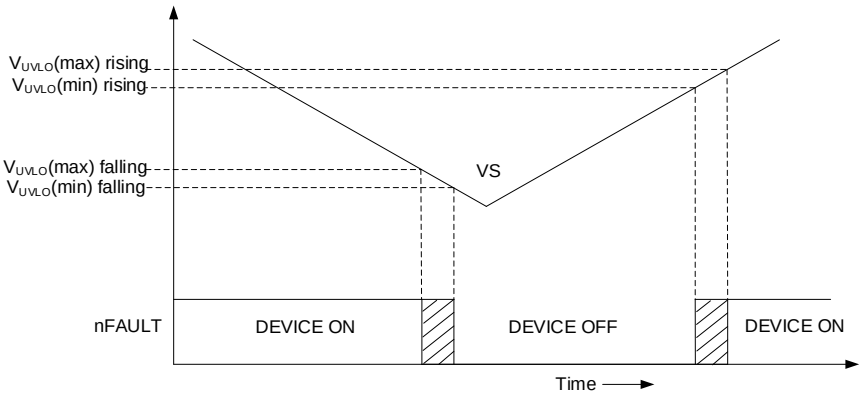


Figure 12. VS UVLO Operation

Overvoltage Protection (OVP)

If the supply voltage VS exceeds the overvoltage threshold, V_{OVP}, all output stages are automatically deactivated. Simultaneously, the VS overvoltage error bit is latched high in the device status register (IC_STAT), and the nFAULT pin is driven low. If VS falls below the threshold (V_{OVP} -V_{OVP_HYS}), the power stages are enabled, and the nFAULT pin is set to high-impedance. The OVP error bit, remains set until cleared using an SPI command through the CLR_FLT bit. Additionally, the device supports an extended overvoltage operation, allowing a higher overvoltage range of up to 32.7V, by enabling the EXT_OVP bit in the configuration register (CONFIG_CTRL).

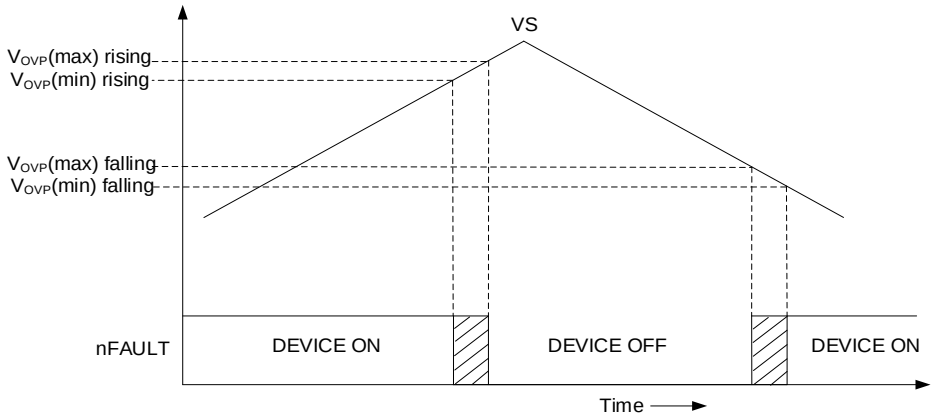


Figure 13. VS OVP Operation

VDD Power-On Reset (POR)

If the VDD logic supply falls below the undervoltage threshold, V_{POR_OFF}, the SPI interfaces will become non-functional, and the device will enter the reset mode. The digital block will be initialized, and the output stages will be switched off to a high-impedance state. The undervoltage reset mode is released once the VDD voltage level exceed the V_{POR_ON} voltage threshold. This reset event is indicated in the CONFIG_CTRL register by resetting the NPOR bit. The NPOR error bit remains latched low until it is cleared through the CLR_FLT bit.

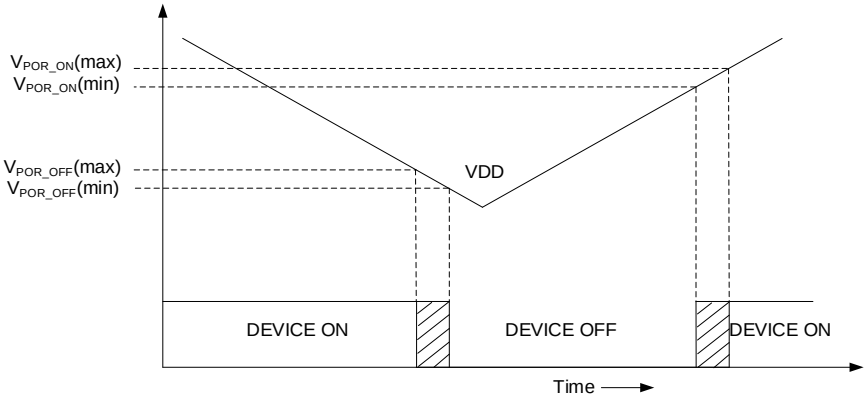


Figure 14. VDD POR Operation

Overcurrent Protection (OCP)

The device features overcurrent protection, actively monitoring the current in both the high-side and low-side drivers. If the current exceeds the overcurrent shutdown detection threshold, the affected high-side (HS) or low-side (LS) driver is immediately latched off. Simultaneously, the corresponding error bit—either HBx_HS_OCP or HBx_LS_OCP—is set and latched after the specified shutdown time, t_{OC}. To restore the normal functionality of the power switch after the overcurrent condition has been resolved, or to check if the fault persists, the user can disable the OCP fault indication on the nFAULT pin by activating the OCP_REP bit in the CONFIG_CTRL register.

Notes:

- For 20V < VS < 25V, the OCP deglitch filter time must be limited to 10µs (Default Deglitch Value, OCP_DEG = 000b).
- For VS > 25V, the OCP deglitch filter time must be limited to 1µs (Lowest Deglitch Value, OCP_DEG = 011b).

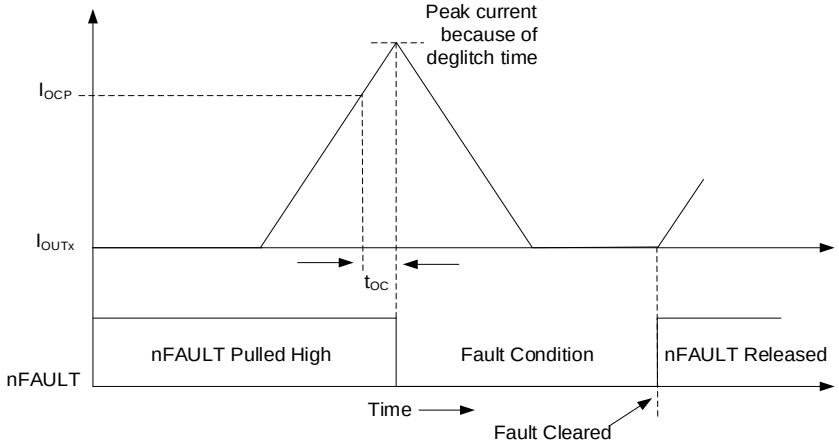


Figure 15. Over Current Protection

Open Load Detection (OLD)

The open-load detection (OLD) function is used to detect a proper load connection. The device supports active OLD and low-current OLD:

Active OLD

Active OLD can identify an open-load condition on the OUTx pins during load operation. As shown in Figure 16, if the motor current (I_{OUTx}) falls below the open-load current threshold (I_{OLD}) and the fault condition persists for longer than the open-load deglitch time (t_{OL}), the device will recognize this as an active open-load fault. In this case, the nFAULT pin will be driven low. Once the open-load condition is resolved and the CLR_FLT bit is set to 1, the nFAULT pin is released.

The controller can detect the presence of an open-load condition by reading the device registers. The OLD bit in the device status register (IC_STAT) and either the HBx_HS_OLD or HBx_LS_OLD bit in the open-load status register (OLD_STAT_x) will be set to 1 to indicate an open-load fault.

Two control registers (OLD_CTRL_1 and OLD_CTRL_2) are used to configure the OLD function. The HBx_OLD_DIS bit in the OLD_CTRL_1 register allows the user to disable OLD on the OUTx pins, although OLD is enabled by default on the device. The OLD_REP bit in the OLD_CTRL_2 register determines whether a fault is reported on the nFAULT pin. The OLD_OP bit sets the device's response to an active OLD fault: if OLD_OP = 0, the OUTx pins switch to the Hi-Z state, stopping the output drive. Otherwise, the OUTx pins maintain their previous state and do not respond to the OLD fault.

Low-Current OLD

The device also incorporates a low-current OLD mode, which operates similarly to active open-load detection. The primary distinction between the low-current open-load and the active open-load is the current detection threshold, which is approximately ten times lower in the low-current open-load mode. This mode is functional only with the low-side MOSFET. Activating the low-current OLD mode simultaneously deactivates the high-side OLD for the respective half-bridge.

As illustrated in Figure 17, if the motor current (I_{OUTx}) drops below the low-current open-load threshold (I_{OLD_LOW}) and the fault condition persists longer than the open-load deglitch filter time (t_{OL}), the device detects a low-current open-load fault. In this case, the nFAULT pin will be driven low. The fault condition can be cleared, and the nFAULT pin released, by resolving the open-load condition and setting the CLR_FLT bit to 1.

The host controller can also read the register to determine whether an open-load condition exists. The OLD bit in the device status register (IC_STAT) and the HBx_LS_OLD bit in the open-load status register (OLD_STAT_x) will be set to 1 to indicate a low-current open-load fault.

Notes: The following limitations apply when low-current OLD detection is enabled.

- The corresponding overcurrent threshold for the low-side MOSFET is reduced by a factor of 10(~150mA typ.).
- The R_{DSON} of the low-side MOSFET will increase by a factor of 10(~7.5Ω typical), requiring thermal performance monitoring.

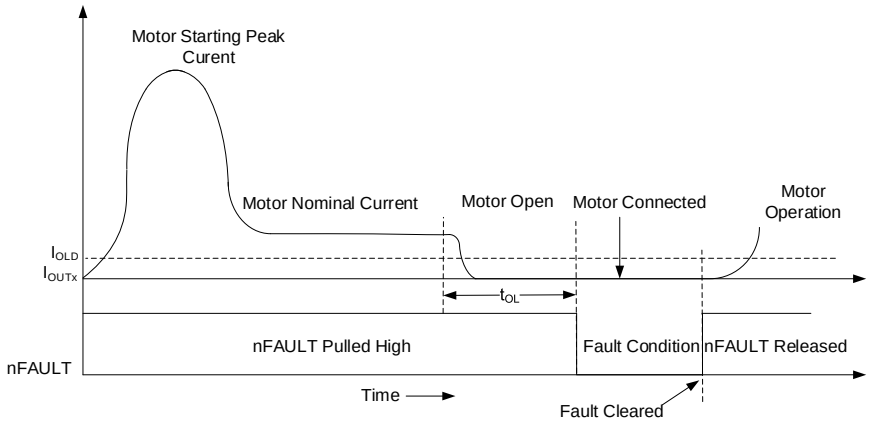


Figure 16. Active Open-Load Detection

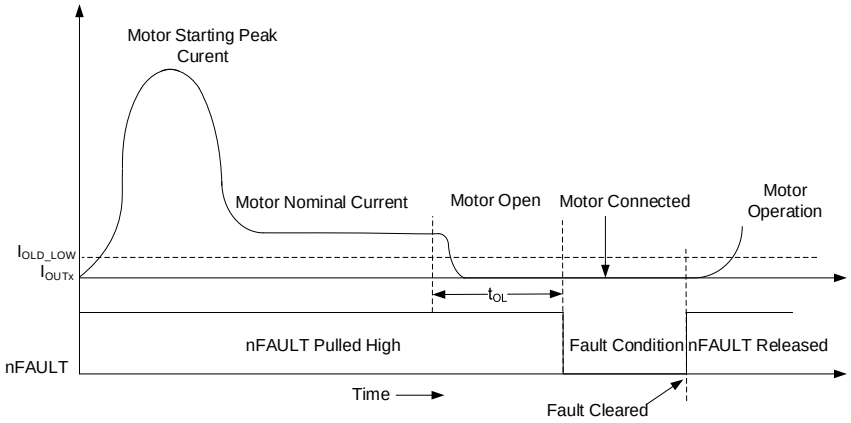


Figure 17. Low-Current OLD

Thermal Warning (OTW)

The device offers overtemperature warning and shutdown protection. If one or more temperature sensors reach the warning threshold, the temperature pre-warning bit, OTW, is set in the device status (IC_STAT) register. This bit is latched and can only be cleared through the SPI, while the output stages remain activated. The reporting of OTW on the nFAULT pin can be enabled by setting the overtemperature warning reporting (OTW_REP) bit in the configuration control (CONFIG_CTRL) register. The nFAULT pin is released when the die temperature decreases below the thermal warning (T_{WARN} -T_{WARN_HYS}).

Thermal Shutdown (TSD)

If one or more temperature sensors reach the shutdown temperature threshold, all outputs are disabled and latched off, and the nFAULT pin is driven low. The OTSD bit is set in the device status (IC_STAT) register. All outputs will be activated, and the nFAULT pin is released when the die temperature decreases below the thermal shutdown threshold (T_{SD}-T_{HYS}).. The OTSD bit remains latched high, indicating a thermal event has occurred until a clear fault command is issued through the CLR_FLT bit. This protection feature cannot be disabled.

Programming Configuration

The device can be controlled using a standard 16-bit SPI interface, with data communication initiated by clocking in the Most Significant Bit (MSB) first. The SPI interface operates as a synchronous serial interface, allowing for address and data transfer at bit rates of up to 5MHz. It is configured for 8-bit byte transfers, making it compatible with a standard SPI bus. Communication over the SPI utilizes four pins: SCLK (synchronous clock), CSB (chip select, active low), SI (data input to the device for write operations), and SO (data output from the device for read operations), as depicted in Figure 18.

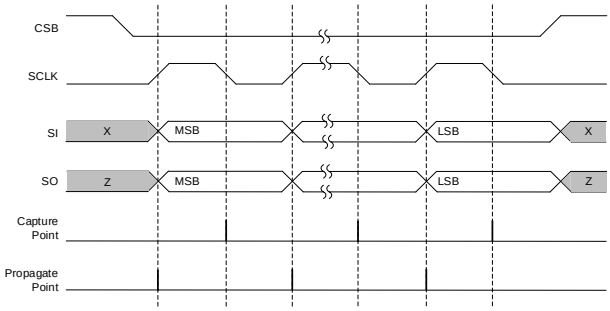


Figure 18. SPI Data Frame

A valid frame on the SPI interface must adhere to the following conditions:

1. When the CSB pin is set to high, the device disregards any signal on the SCLK and SI pins, and the SO pin enters a high impedance (Hi-Z) state.
2. Data is captured on the falling edge of SCLK, and data is propagated on the rising edge of SCLK.

3. The most significant bit (MSB) is always shifted in and out first.
4. A complete transaction requires a full sequence of 16 SCLK cycles.
5. The data word transmitted to the SI pin must consist of exactly 16 bits.
6. For write commands, the current data in the register written to is shifted out on the SO pin, following the 8-bit command data.

SPI Format

Each SPI communication sequence with the device begins with an address byte, followed by a data byte. The device's SPI functionality includes one Read/Write (R/W) bit located at bit position 14; six address bits, and eight data bits. The control registers are READ/WRITE registers. To set the control register to READ, bit 14 in the address byte must be set to '1'; otherwise, set it to '0' for WRITE. As the microcontroller transmits the address byte via the SI pin, the device's Status Register data is simultaneously shifted out through the SO pin. The subsequent data byte, comprising bits 7 to 0, is used to configure the half-bridges or retrieve the device's status information. The mapping of the SPI Registers is shown in Table 6.

Table 4. SI Input Data Word Format

		R/W	Address						Data							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 5. SO Output Data Word Format

			Address						Data							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	1	1	OTSD	OLD	OCP	UVLO	OVP	NPOR	D7	D6	D5	D4	D3	D2	D1	D0

Daisy Chain

The device is designed to support daisy chain operation with other devices that utilize the same SPI protocol, as demonstrated in Figure 19. In this setup, the controller's output (MO) is connected to the serial input (SI) of the first target device. The serial output (SO) of this device is then connected to the SI of the next target, forming a chain. The SO of the last target in the chain is linked to the controller's input (MI), thereby completing the SPI communication loop.

In a daisy chain configuration, a single chip select (CSB) and a clock signal (SCLK) are distributed in parallel across all target devices. These connections enable the microcontroller to control and access the SPI devices efficiently. Figure 20 illustrates the topology and corresponding waveforms when three devices are interconnected in a series configuration.

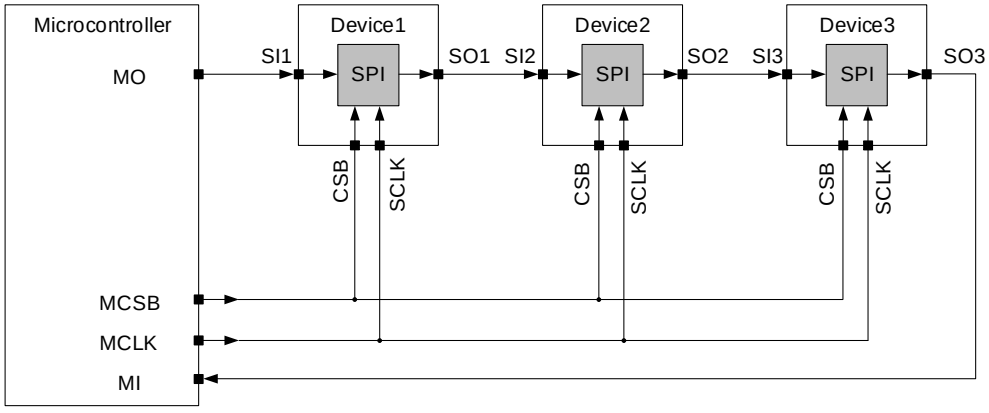


Figure 19. SPI Daisy Chain

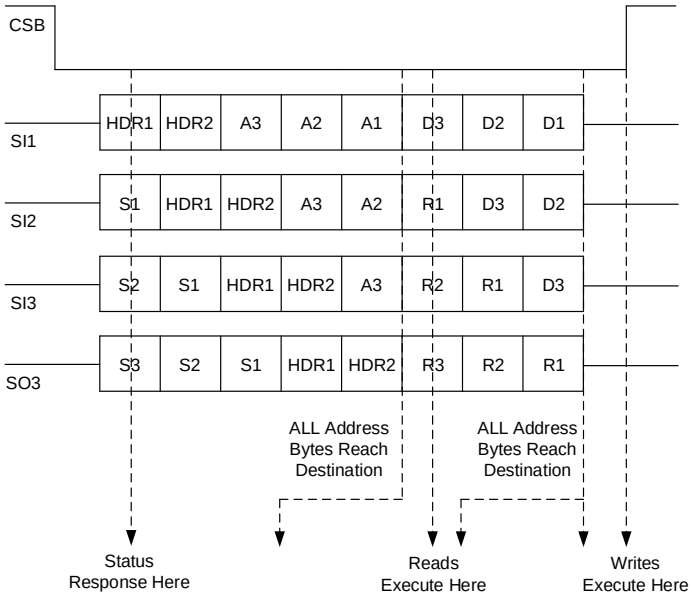


Figure 20. Daisy Chain SPI Operation

In the daisy chain configuration depicted above, the first device in the chain receives data from the controller in the following format, as shown in SI1 of Figure 20:

1. 2 bytes of Header
2. 3 bytes of Address
3. 3 bytes of Data

Once the data has been transmitted through the chain, the controller receives it back in the format illustrated in SO3 of Figure 20:

1. 3 bytes of Status
2. 2 bytes of Header (which should be identical to the information sent by the controller)
3. 3 bytes of Report

The two header bytes carry critical information, including the number of devices in the chain and a global clear fault command. The N5 to N0 bits in Header 1 indicate that up to 63 (2^6-1) devices can be connected in series per daisy chain connection. The CLR bit in Header 2 serves as a global clear fault command that resets the fault registers of all devices in the chain. Both header bytes must start with 1 and 0.

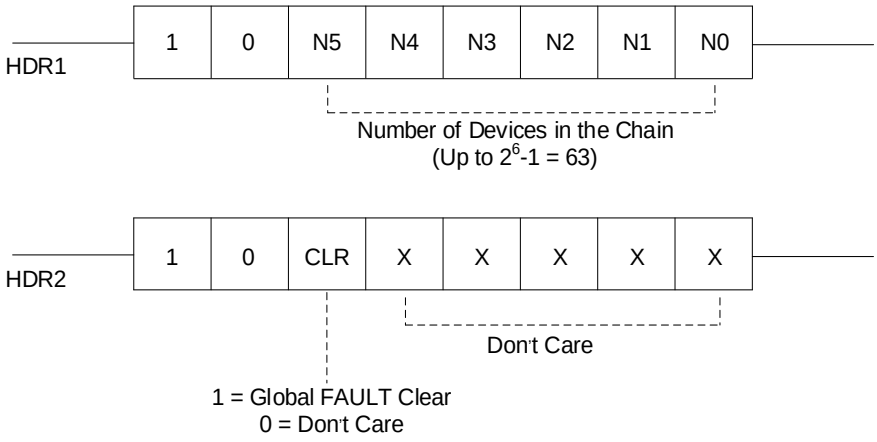


Figure 21. Header Bits

All devices in the configuration will relay their fault status through the status byte, as shown in Figure 22. This feature enables convenient and efficient monitoring of controller fault status, enhancing the overall functionality of the device.

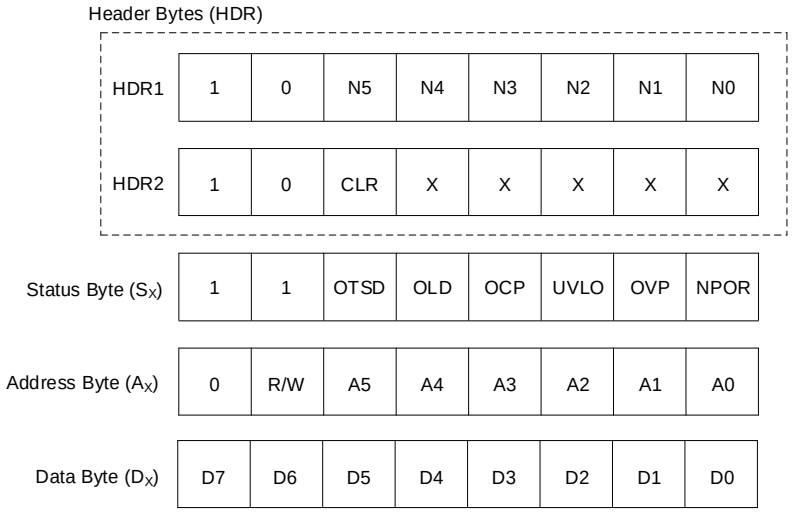


Figure 22. Daisy Chain Read Registers

The device determines its position in the chain by counting the number of status bytes that follow the header byte. As illustrated in Figure 20, device 2 identifies its position by recognizing one status byte (S1) following the header, while device 3 identifies two status bytes (S1, S2) after the header. Once the device determines the position and the total number of devices connected in the chain, each device can load the relevant address and data bytes into its buffer, effectively bypassing irrelevant bits. This method ensures efficient operation, even in a chain comprising of up to 63 devices.

Table 6. SA52122B Register Map

Name	7	6	5	4	3	2	1	0	Type	Address
IC_STAT	Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR	R	00h
OCP_STAT_1	HB4_HS_OCP	HB4_LS_OCP	HB3_HS_OCP	HB3_LS_OCP	HB2_HS_OCP	HB2_LS_OCP	HB1_HS_OCP	HB1_LS_OCP	R	01h
OCP_STAT_2	HB8_HS_OCP	HB8_LS_OCP	HB7_HS_OCP	HB7_LS_OCP	HB6_HS_OCP	HB6_LS_OCP	HB5_HS_OCP	HB5_LS_OCP	R	02h
OCP_STAT_3	HB12_HS_OCP	HB12_LS_OCP	HB11_HS_OCP	HB11_LS_OCP	HB10_HS_OCP	HB10_LS_OCP	HB9_HS_OCP	HB9_LS_OCP	R	03h
OLD_STAT_1	HB4_HS_OLD	HB4_LS_OLD	HB3_HS_OLD	HB3_LS_OLD	HB2_HS_OLD	HB2_LS_OLD	HB1_HS_OLD	HB1_LS_OLD	R	04h
OLD_STAT_2	HB8_HS_OLD	HB8_LS_OLD	HB7_HS_OLD	HB7_LS_OLD	HB6_HS_OLD	HB6_LS_OLD	HB5_HS_OLD	HB5_LS_OLD	R	05h
OLD_STAT_3	HB12_HS_OLD	HB12_LS_OLD	HB11_HS_OLD	HB11_LS_OLD	HB10_HS_OLD	HB10_LS_OLD	HB9_HS_OLD	HB9_LS_OLD	R	06h
CONFIG_CTRL	Reserved	IC_ID			OCP_REP		EXT_OVP	CLR_FLT	R/W	07h
OP_CTRL_1	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN	R/W	08h
OP_CTRL_2	HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN	R/W	09h
OP_CTRL_3	HB12_HS_EN	HB12_LS_EN	HB11_HS_EN	HB11_LS_EN	HB10_HS_EN	HB10_LS_EN	HB9_HS_EN	HB9_LS_EN	R/W	0Ah
PWM_CTRL_1	HB8_PWM	HB7_PWM	HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM	R/W	0Bh
PWM_CTRL_2	PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS	HB12_PWM	HB11_PWM	HB10_PWM	HB9_PWM	R/W	0Ch
FW_CTRL_1	HB8_FW	HB7_FW	HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW	R/W	0Dh
FW_CTRL_2	Reserved				HB12_FW	HB11_FW	HB10_FW	HB9_FW	R/W	0Eh
PWM_MAP_CTRL_1	HB4_PWM_MAP [1:0]		HB3_PWM_MAP [1:0]		HB2_PWM_MAP [1:0]		HB1_PWM_MAP[1:0]		R/W	0Fh
PWM_MAP_CTRL_2	HB8_PWM_MAP [1:0]		HB7_PWM_MAP [1:0]		HB6_PWM_MAP [1:0]		HB5_PWM_MAP [1:0]		R/W	10h
PWM_MAP_CTRL_3	HB12_PWM_MAP [1:0]		HB11_PWM_MAP [1:0]		HB10_PWM_MAP [1:0]		HB9_PWM_MAP [1:0]		R/W	11h
PWM_FREQ_CTRL_1	PWM_CH4_FREQ [1:0]		PWM_CH3_FREQ [1:0]		PWM_CH2_FREQ [1:0]		PWM_CH1_FREQ [1:0]		R/W	12h
PWM_DUTY_CTRL_1	PWM_DUTY_CH1								R/W	13h
PWM_DUTY_CTRL_2	PWM_DUTY_CH2								R/W	14h
PWM_DUTY_CTRL_3	PWM_DUTY_CH3								R/W	15h
PWM_DUTY_CTRL_4	PWM_DUTY_CH4								R/W	16h
SR_CTRL_1	HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR	R/W	17h
SR_CTRL_2	Reserved				HB12_SR	HB11_SR	HB10_SR	HB9_SR	R/W	18h
OLD_CTRL_1	HB8_OLD_DIS	HB7_OLD_DIS	HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS	R/W	19h
OLD_CTRL_2	OLD_REP	OLD_OP	Reserved		HB12_OLD_DIS	HB11_OLD_DIS	HB10_OLD_DIS	HB9_OLD_DIS	R/W	1Ah
OLD_CTRL_3	OCP_DEG			Reserved	HB12_LOLD_EN	HB11_LOLD_EN	HB10_LOLD_EN	HB9_LOLD_EN	R/W	1Bh
OLD_CTRL_4	HB8_LOLD_EN	HB7_LOLD_EN	HB6_LOLD_EN	HB5_LOLD_EN	HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN	R/W	24h
PWM_CTRL_3	PWM_CH12_DIS	PWM_CH11_DIS	PWM_CH10_DIS	PWM_CH9_DIS	PWM_CH8_DIS	PWM_CH7_DIS	PWM_CH6_DIS	PWM_CH5_DIS	R/W	26h
PWM_MAP_CTRL_4	HB4_PWM_MAP [3:2]		HB3_PWM_MAP [3:2]		HB2_PWM_MAP [3:2]		HB1_PWM_MAP [3:2]		R/W	27h
PWM_MAP_CTRL_5	HB8_PWM_MAP [3:2]		HB7_PWM_MAP [3:2]		HB6_PWM_MAP [3:2]		HB5_PWM_MAP [3:2]		R/W	28h
PWM_MAP_CTRL_6	HB12_PWM_MAP [3:2]		HB11_PWM_MAP [3:2]		HB10_PWM_MAP [3:2]		HB9_PWM_MAP [3:2]		R/W	29h
PWM_FREQ_CTRL_2	PWM_CH8_FREQ [1:0]		PWM_CH7_FREQ [1:0]		PWM_CH6_FREQ [1:0]		PWM_CH5_FREQ [1:0]		R/W	2Ah
PWM_FREQ_CTRL_3	PWM_CH12_FREQ [1:0]		PWM_CH11_FREQ [1:0]		PWM_CH10_FREQ [1:0]		PWM_CH9_FREQ [1:0]		R/W	2Bh
PWM_FREQ_CTRL_4	PWM_CH8_FREQ [2]	PWM_CH7_FREQ [2]	PWM_CH6_FREQ [2]	PWM_CH5_FREQ [2]	PWM_CH4_FREQ [2]	PWM_CH3_FREQ [2]	PWM_CH2_FREQ [2]	PWM_CH1_FREQ [2]	R/W	2Ch
PWM_FREQ_CTRL_5	Reserved	Reserved	Reserved	Reserved	PWM_CH12_FREQ [2]	PWM_CH11_FREQ [2]	PWM_CH10_FREQ [2]	PWM_CH9_FREQ [2]	R/W	2Dh
PWM_DUTY_CTRL_5	PWM_DUTY_CH5								R/W	2Eh
PWM_DUTY_CTRL_6	PWM_DUTY_CH6								R/W	2Fh
PWM_DUTY_CTRL_7	PWM_DUTY_CH7								R/W	30h
PWM_DUTY_CTRL_8	PWM_DUTY_CH8								R/W	31h
PWM_DUTY_CTRL_9	PWM_DUTY_CH9								R/W	32h
PWM_DUTY_CTRL_10	PWM_DUTY_CH10								R/W	33h
PWM_DUTY_CTRL_11	PWM_DUTY_CH11								R/W	34h
PWM_DUTY_CTRL_12	PWM_DUTY_CH12								R/W	35h

SPI Status Registers

The read-only status registers are used to report warning and fault conditions.

IC_STAT

IC_ Status Register (Address =0x00) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR
R	R	R	R	R	R	R	R

Field	Bits	Type	Description
Reserved	D7	R	Reserved. Always reads as '0'
OTSD	D6	R	Temperature shutdown error detection 0_B Junction temperature below temperature shutdown threshold 1_B Junction temperature has reached the temperature shutdown threshold
OTW	D5	R	Temperature pre-warning error detection 0_B Junction temperature below temperature pre-warning threshold 1_B Junction temperature has reached the temperature pre-warning threshold
OLD	D4	R	Open-load error detection 0_B No Open-load 1_B Open-load
OCP	D3	R	Overcurrent error detection 0_B No overcurrent 1_B Overcurrent
UVLO	D2	R	VS Undervoltage error detection 0_B No undervoltage on VS detected 1_B Undervoltage on VS detected
OVP	D1	R	VS Overvoltage error detection 0_B No overvoltage on VS detected 1_B Overvoltage on VS detected
NPOR	D0	R	No Power on Reset (NPOR) detection 0_B POR on EN or VDD supply rail 1_B No POR

OCP_STAT_1

Overcurrent Error Status of Half-bridge Outputs 1-4 (Address =0x01) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_OC	HB4_LS_OC	HB3_HS_OC	HB3_LS_OC	HB2_HS_OC	HB2_LS_OC	HB1_HS_OC	HB1_LS_OC
R	R	R	R	R	R	R	R

Field	Bits	Type	Description
HB4_HS_OC	D7	R	High-side (HS) switch of half-bridge 4 overcurrent detection 0_B No error on HS4 switch 1_B Overcurrent detected on HS4 switch
HB4_LS_OC	D6	R	Low-side (LS) switch of half-bridge 4 overcurrent detection 0_B No error on LS4 switch 1_B Overcurrent detected on LS4 switch
HB3_HS_OC	D5	R	High-side (HS) switch of half-bridge 3 overcurrent detection 0_B No error on HS3 switch 1_B Overcurrent detected on HS3 switch
HB3_LS_OC	D4	R	Low-side (LS) switch of half-bridge 3 overcurrent detection 0_B No error on LS3 switch 1_B Overcurrent detected on LS3 switch
HB2_HS_OC	D3	R	High-side (HS) switch of half-bridge 2 overcurrent detection 0_B No error on HS2 switch 1_B Overcurrent detected on HS2 switch
HB2_LS_OC	D2	R	Low-side (LS) switch of half-bridge 2 overcurrent detection 0_B No error on LS2 switch 1_B Overcurrent detected on LS2 switch
HB1_HS_OC	D1	R	High-side (HS) switch of half-bridge 1 overcurrent detection 0_B No error on HS1 switch 1_B Overcurrent detected on HS1 switch
HB1_LS_OC	D0	R	Low-side (LS) switch of half-bridge 1 overcurrent detection 0_B No error on LS1 switch 1_B Overcurrent detected on LS1 switch

OCP_STAT_2

Overcurrent Error Status of Half-bridge Outputs 5-8 (Address =0x02) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_HS_OC	HB8_LS_OC	HB7_HS_OC	HB7_LS_OC	HB6_HS_OC	HB6_LS_OC	HB5_HS_OC	HB5_LS_OC
R	R	R	R	R	R	R	R

Field	Bits	Type	Description
HB8_HS_OC	D7	R	High-side (HS) switch of half-bridge 8 overcurrent detection 0_B No error on HS8 switch 1_B Overcurrent detected on HS8 switch
HB8_LS_OC	D6	R	Low-side (LS) switch of half-bridge 8 overcurrent detection 0_B No error on LS8 switch 1_B Overcurrent detected on LS8 switch
HB7_HS_OC	D5	R	High-side (HS) switch of half-bridge 7 overcurrent detection 0_B No error on HS7 switch 1_B Overcurrent detected on HS7 switch
HB7_LS_OC	D4	R	Low-side (LS) switch of half-bridge 7 overcurrent detection 0_B No error on LS7 switch 1_B Overcurrent detected on LS7 switch
HB6_HS_OC	D3	R	High-side (HS) switch of half-bridge 6 overcurrent detection 0_B No error on HS6 switch 1_B Overcurrent detected on HS6 switch
HB6_LS_OC	D2	R	Low-side (LS) switch of half-bridge 6 overcurrent detection 0_B No error on LS6 switch 1_B Overcurrent detected on LS6 switch
HB5_HS_OC	D1	R	High-side (HS) switch of half-bridge 5 overcurrent detection 0_B No error on HS5 switch 1_B Overcurrent detected on HS5 switch
HB5_LS_OC	D0	R	Low-side (LS) switch of half-bridge 5 overcurrent detection 0_B No error on LS5 switch 1_B Overcurrent detected on LS5 switch

OCP_STAT_3

Overcurrent Error Status of Half-bridge Outputs 9-12 (Address =0x03) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB12_HS_OC	HB12_LS_OC	HB11_HS_OC	HB11_LS_OC	HB10_HS_OC	HB10_LS_OC	HB9_HS_OC	HB9_LS_OC
R	R	R	R	R	R	R	R

Field	Bits	Type	Description
HB12_HS_OC	D7	R	High-side (HS) switch of half-bridge 12 overcurrent detection 0_B No error on HS12 switch 1_B Overcurrent detected on HS12 switch
HB12_LS_OC	D6	R	Low-side (LS) switch of half-bridge 12 overcurrent detection 0_B No error on LS12 switch 1_B Overcurrent detected on LS12 switch
HB11_HS_OC	D5	R	High-side (HS) switch of half-bridge 11 overcurrent detection 0_B No error on HS11 switch 1_B Overcurrent detected on HS11 switch
HB11_LS_OC	D4	R	Low-side (LS) switch of half-bridge 11 overcurrent detection 0_B No error on LS11 switch 1_B Overcurrent detected on LS11 switch
HB10_HS_OC	D3	R	High-side (HS) switch of half-bridge 10 overcurrent detection 0_B No error on HS10 switch 1_B Overcurrent detected on HS10 switch
HB10_LS_OC	D2	R	Low-side (LS) switch of half-bridge 10 overcurrent detection 0_B No error on LS10 switch 1_B Overcurrent detected on LS10 switch
HB9_HS_OC	D1	R	High-side (HS) switch of half-bridge 9 overcurrent detection 0_B No error on HS9 switch 1_B Overcurrent detected on HS9 switch
HB9_LS_OC	D0	R	Low-side (LS) switch of half-bridge 9 overcurrent detection 0_B No error on LS9 switch 1_B Overcurrent detected on LS9 switch

OLD_STAT_1

Open Load Error Status of Half-bridge Outputs 1-4 (Address =0x04) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_OL	HB4_LS_OL	HB3_HS_OL	HB3_LS_OL	HB2_HS_OL	HB2_LS_OL	HB1_HS_OL	HB1_LS_OL
R	R	R	R	R	R	R	R

Field	Bits	Type	Description
HB4_HS_OL	D7	R	High-side (HS) switch of half-bridge 4 open load detection 0_B No error on HS4 switch (default value) 1_B Open load detected on HS4 switch
HB4_LS_OL	D6	R	Low-side (LS) switch of half-bridge 4 open load detection 0_B No error on LS4 switch (default value) 1_B Open load detected on LS4 switch
HB3_HS_OL	D5	R	High-side (HS) switch of half-bridge 3 open load detection 0_B No error on HS3 switch (default value) 1_B Open load detected on HS3 switch
HB3_LS_OL	D4	R	Low-side (LS) switch of half-bridge 3 open load detection 0_B No error on LS3 switch (default value) 1_B Open load detected on LS3 switch
HB2_HS_OL	D3	R	High-side (HS) switch of half-bridge 2 open load detection 0_B No error on HS2 switch (default value) 1_B Open load detected on HS2 switch
HB2_LS_OL	D2	R	Low-side (LS) switch of half-bridge 2 open loadt detection 0_B No error on LS2 switch (default value) 1_B Open load detected on LS2 switch
HB1_HS_OL	D1	R	High-side (HS) switch of half-bridge 1 open load detection 0_B No error on HS1 switch (default value) 1_B Open load detected on HS1 switch
HB1_LS_OL	D0	R	Low-side (LS) switch of half-bridge 1 open load detection 0_B No error on LS1 switch (default value) 1_B Open load detected on LS1 switch

OLD_STAT_2

Open Load Error Status of Half-bridge Outputs 5-8 (Address =0x05) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_HS_OL	HB8_LS_OL	HB7_HS_OL	HB7_LS_OL	HB6_HS_OL	HB6_LS_OL	HB5_HS_OL	HB5_LS_OL
R	R	R	R	R	R	R	R

Field	Bits	Type	Description
HB8_HS_OL	D7	R	High-side (HS) switch of half-bridge 8 open load detection 0_B No error on HS8 switch 1_B Open load detected on HS8 switch
HB8_LS_OL	D6	R	Low-side (LS) switch of half-bridge 8 open load detection 0_B No error on LS8 switch 1_B Open load detected on LS8 switch
HB7_HS_OL	D5	R	High-side (HS) switch of half-bridge 7 open load detection 0_B No error on HS7 switch 1_B Open load detected on HS7 switch
HB7_LS_OL	D4	R	Low-side (LS) switch of half-bridge 7 open load detection 0_B No error on LS7 switch 1_B Open load detected on LS7 switch
HB6_HS_OL	D3	R	High-side (HS) switch of half-bridge 6 open load detection 0_B No error on HS6 switch 1_B Open load detected on HS6 switch
HB6_LS_OL	D2	R	Low-side (LS) switch of half-bridge 6 open load detection 0_B No error on LS6 switch 1_B Open load detected on LS6 switch
HB5_HS_OL	D1	R	High-side (HS) switch of half-bridge 5 open load detection 0_B No error on HS5 switch 1_B Open load detected on HS5 switch
HB5_LS_OL	D0	R	Low-side (LS) switch of half-bridge 5 open load detection 0_B No error on LS5 switch 1_B Open load detected on LS5 switch

OLD_STAT_3

Open Load Error Status of Half-bridge Outputs 9-12 (Address =0x06) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB12_HS_OL	HB12_LS_OL	HB11_HS_OL	HB11_LS_OL	HB10_HS_OL	HB10_LS_OL	HB9_HS_OL	HB9_LS_OL
R	R	R	R	R	R	R	R

Field	Bits	Type	Description
HB12_HS_OL	D7	R	High-side (HS) switch of half-bridge 12 open load detection 0_B No error on HS12 switch 1_B Open load detected on HS12 switch
HB12_LS_OL	D6	R	Low-side (LS) switch of half-bridge 12 open load detection 0_B No error on LS12 switch 1_B Open load detected on LS12 switch
HB11_HS_OL	D5	R	High-side (HS) switch of half-bridge 11 open load detection 0_B No error on HS11 switch 1_B Open load detected on HS11 switch
HB11_LS_OL	D4	R	Low-side (LS) switch of half-bridge 11 open load detection 0_B No error on LS11 switch 1_B Open load detected on LS11 switch
HB10_HS_OL	D3	R	High-side (HS) switch of half-bridge 10 open load detection 0_B No error on HS10 switch 1_B Open load detected on HS10 switch
HB10_LS_OL	D2	R	Low-side (LS) switch of half-bridge 10 open load detection 0_B No error on LS10 switch 1_B Open load detected on LS10 switch
HB9_HS_OL	D1	R	High-side (HS) switch of half-bridge 9 open load detection 0_B No error on HS9 switch 1_B Open load detected on HS9 switch
HB9_LS_OL	D0	R	Low-side (LS) switch of half-bridge 9 open load detection 0_B No error on LS9 switch 1_B Open load detected on LS9 switch

SPI Control Registers

The Control Register are used to configure the device. The control registers are read and write capable.

CONFIG_CTRL

Configuration Register (Address =0x07) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	IC_ID			OCP_REG	OTW_REG	EXT_OVP	CLR_FLT
R	R	R	R	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
Reserved	D7	R	Reserved. Always reads as '0'
IC_ID	D6	R	Reserved. Always reads as '0'
	D5	R	Reserved. Always reads as '0'
	D4	R	Reserved. Always reads as '0'
OCP_REG	D3	R/W	0_B Overcurrent condition is reported in nFAULT pin 1_B Overcurrent condition warning is not reported in nFAULT pin
OTW_REG	D2	R/W	0_B Overtemperature warning is not reported in nFAULT pin 1_B Overtemperature warning is reported in nFAULT pin
EXT_OVP	D1	R/W	0_B Overvoltage protection threshold is at 21V min. 1_B Overvoltage protection threshold is at 32.7V min.
CLR_FLT	D0	R/W	0_B Faults not cleared 1_B Clear all faults

OP_CTRL_1

Half-Bridge Output Control 1 (Address =0x08) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB4_HS_EN	D7	R/W	Half-bridge output 4 High side switch enable 0_B HS4 OFF 1_B HS4 ON
HB4_LS_EN	D6	R/W	Half-bridge output 4 Low side switch enable 0_B LS4 OFF 1_B LS4 ON
HB3_HS_EN	D5	R/W	Half-bridge output 3 High side switch enable 0_B HS3 OFF 1_B HS3 ON
HB3_LS_EN	D4	R/W	Half-bridge output 3 Low side switch enable 0_B LS3 OFF 1_B LS3 ON
HB2_HS_EN	D3	R/W	Half-bridge output 2 High side switch enable 0_B HS2 OFF 1_B HS2 ON
HB2_LS_EN	D2	R/W	Half-bridge output 2 Low side switch enable 0_B LS2 OFF 1_B LS2 ON
HB1_HS_EN	D1	R/W	Half-bridge output 1 High side switch enable 0_B HS1 OFF 1_B HS1 ON
HB1_LS_EN	D0	R/W	Half-bridge output 1 Low side switch enable 0_B LS1 OFF 1_B LS1 ON

OP_CTRL_2

Half-Bridge Output Control 2 (Address =0x09) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB8_HS_EN	D7	R/W	Half-bridge output 8 High side switch enable 0_B HS8 OFF 1_B HS8 ON
HB8_LS_EN	D6	R/W	Half-bridge output 8 Low side switch enable 0_B LS8 OFF 1_B LS8 ON
HB7_HS_EN	D5	R/W	Half-bridge output 7 High side switch enable 0_B HS7 OFF 1_B HS7 ON
HB7_LS_EN	D4	R/W	Half-bridge output 7 Low side switch enable 0_B LS7 OFF 1_B LS7 ON
HB6_HS_EN	D3	R/W	Half-bridge output 6 High side switch enable 0_B HS6 OFF 1_B HS6 ON
HB6_LS_EN	D2	R/W	Half-bridge output 6 Low side switch enable 0_B LS6 OFF 1_B LS6 ON
HB5_HS_EN	D1	R/W	Half-bridge output 5 High side switch enable 0_B HS5 OFF 1_B HS5 ON
HB5_LS_EN	D0	R/W	Half-bridge output 5 Low side switch enable 0_B LS5 OFF 1_B LS5 ON

OP_CTRL_3

Half-Bridge Output Control 3 (Address =0x0A) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB12_HS_EN	HB12_LS_EN	HB11_HS_EN	HB11_LS_EN	HB10_HS_EN	HB10_LS_EN	HB9_HS_EN	HB9_LS_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB12_HS_EN	D7	R/W	Half-bridge output 12 High side switch enable 0_B HS12 OFF 1_B HS12 ON
HB12_LS_EN	D6	R/W	Half-bridge output 12 Low side switch enable 0_B LS12 OFF 1_B LS12 ON
HB11_HS_EN	D5	R/W	Half-bridge output 11 High side switch enable 0_B HS11 OFF 1_B HS11 ON
HB11_LS_EN	D4	R/W	Half-bridge output 11 Low side switch enable 0_B LS11 OFF 1_B LS11 ON
HB10_HS_EN	D3	R/W	Half-bridge output 10 High side switch enable 0_B HS10 OFF 1_B HS10 ON
HB10_LS_EN	D2	R/W	Half-bridge output 10 Low side switch enable 0_B LS10 OFF 1_B LS10 ON
HB9_HS_EN	D1	R/W	Half-bridge output 9 High side switch enable 0_B HS9 OFF 1_B HS9 ON
HB9_LS_EN	D0	R/W	Half-bridge output 9 Low side switch enable 0_B LS9 OFF 1_B LS9 ON

PWM_CTRL_1

Half-Bridge PWM Control 1 (Address =0x0B) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_PWM	HB7_PWM	HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB8_PWM	D7	R/W	0_B Half-bridge 8 is operating in continuous mode 1_B Half-bridge 8 is operating in PWM mode
HB7_PWM	D6	R/W	0_B Half-bridge 7 is operating in continuous mode 1_B Half-bridge 7 is operating in PWM mode
HB6_PWM	D5	R/W	0_B Half-bridge 6 is operating in continuous mode 1_B Half-bridge 6 is operating in PWM mode
HB5_PWM	D4	R/W	0_B Half-bridge 5 is operating in continuous mode 1_B Half-bridge 5 is operating in PWM mode
HB4_PWM	D3	R/W	0_B Half-bridge 4 is operating in continuous mode 1_B Half-bridge 4 is operating in PWM mode
HB3_PWM	D2	R/W	0_B Half-bridge 3 is operating in continuous mode 1_B Half-bridge 3 is operating in PWM mode
HB2_PWM	D1	R/W	0_B Half-bridge 2 is operating in continuous mode 1_B Half-bridge 2 is operating in PWM mode
HB1_PWM	D0	R/W	0_B Half-bridge 1 is operating in continuous mode 1_B Half-bridge 1 is operating in PWM mode

PWM_CTRL_2

Half-Bridge PWM Control 2 (Address =0x0C) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS	HB12_PWM	HB11_PWM	HB10_PWM	HB9_PWM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_CH4_DIS	D7	R/W	0_B PWM Generator-4 is enabled 1_B PWM Generator-4 is disabled
PWM_CH3_DIS	D6	R/W	0_B PWM Generator-3 is enabled 1_B PWM Generator-3 is disabled
PWM_CH2_DIS	D5	R/W	0_B PWM Generator-2 is enabled 1_B PWM Generator-2 is disabled
PWM_CH1_DIS	D4	R/W	0_B PWM Generator-1 is enabled 1_B PWM Generator-1 is disabled
HB12_PWM	D3	R/W	0_B Half-bridge 12 is operating in continuous mode 1_B Half-bridge 12 is operating in PWM mode
HB11_PWM	D2	R/W	0_B Half-bridge 11 is operating in continuous mode 1_B Half-bridge 11 is operating in PWM mode
HB10_PWM	D1	R/W	0_B Half-bridge 10 is operating in continuous mode 1_B Half-bridge 10 is operating in PWM mode
HB9_PWM	D0	R/W	0_B Half-bridge 9 is operating in continuous mode 1_B Half-bridge 9 is operating in PWM mode

FW _CTRL_1

Free-Wheeling Configuration 1 (Address =0x0D) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
FW_HB8	FW_HB7	FW_HB6	FW_HB5	FW_HB4	FW_HB3	FW_HB2	FW_HB1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
FW_HB8	D7	R/W	HB8 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB7	D6	R/W	HB7 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB6	D5	R/W	HB6 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB5	D4	R/W	HB5 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB4	D3	R/W	HB4 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB3	D2	R/W	HB3 free-wheeling configuration

			0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB2	D1	R/W	HB2 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB1	D0	R/W	HB1 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling

FW _CTRL_2

Free-Wheeling Configuration 2 (Address =0x0E) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	FW_HB12	FW_HB11	FW_HB10	FW_HB9
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
Reserved	D7	R/W	Reserved. Always reads as '0'
Reserved	D6	R/W	Reserved. Always reads as '0'
Reserved	D5	R/W	Reserved. Always reads as '0'
Reserved	D4	R/W	Reserved. Always reads as '0'
FW_HB12	D3	R/W	HB12 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB11	D2	R/W	HB11 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB10	D1	R/W	HB10 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB9	D0	R/W	HB9 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling

PWM_MAP_CTRL_1 & PWM_MAP_CTRL_4

PWM_MAP_CTRL_1 and PWM_MAP_CTRL_4 jointly determine the PWM channel selection of half-bridge output 4~1. The PWM mapping information of half-bridge output 4~1 is shown below.

Half-Bridge Output PWM Map Control 1 (Address =0x0F) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_PWM_MAP[1:0]		HB3_PWM_MAP[1:0]		HB2_PWM_MAP[1:0]		HB1_PWM_MAP[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Half-Bridge Output PWM Map Control 4 (Address =0x27) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_PWM_MAP[3:2]		HB3_PWM_MAP[3:2]		HB2_PWM_MAP[3:2]		HB1_PWM_MAP[3:2]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB4_PWM_MAP[3:0]	NA	R/W	Half-bridge output 4 mode select

HB4_PWM_MAP[3:2]	HB4_PWM_MAP [1:0]	HB4_PWM_MAP[3:0]
00_B	00_B	0000_B PWM control with PWM Channel 1
00_B	01_B	0001_B PWM control with PWM Channel 2
00_B	10_B	0010_B PWM control with PWM Channel 3
00_B	11_B	0011_B PWM control with PWM Channel 4
01_B	00_B	0100_B PWM control with PWM Channel 5
01_B	01_B	0101_B PWM control with PWM Channel 6
01_B	10_B	0110_B PWM control with PWM Channel 7
01_B	11_B	0111_B PWM control with PWM Channel 8
10_B	00_B	1000_B PWM control with PWM Channel 9
10_B	01_B	1001_B PWM control with PWM Channel 10
10_B	10_B	1010_B PWM control with PWM Channel 11
10_B	11_B	1011_B PWM control with PWM Channel 12
11_B	x	Reserved

HB3_PWM_MAP[3:0]	NA	R/W	Half-bridge output 3 mode select

HB3_PWM_MAP[3:2]	HB3_PWM_MAP [1:0]	HB3_PWM_MAP[3:0]
00_B	00_B	0000_B PWM control with PWM Channel 1
00_B	01_B	0001_B PWM control with PWM Channel 2
00_B	10_B	0010_B PWM control with PWM Channel 3
00_B	11_B	0011_B PWM control with PWM Channel 4
01_B	00_B	0100_B PWM control with PWM Channel 5
01_B	01_B	0101_B PWM control with PWM Channel 6
01_B	10_B	0110_B PWM control with PWM Channel 7
01_B	11_B	0111_B PWM control with PWM Channel 8
10_B	00_B	1000_B PWM control with PWM Channel 9
10_B	01_B	1001_B PWM control with PWM Channel 10
10_B	10_B	1010_B PWM control with PWM Channel 11
10_B	11_B	1011_B PWM control with PWM Channel 12
11_B	x	Reserved

HB2_PWM_MAP[3:0]	NA	R/W	Half-bridge output 2 mode select

HB2_PWM_MAP[3:2]	HB2_PWM_MAP [1:0]	HB2_PWM_MAP[3:0]
00_B	00_B	0000_B PWM control with PWM Channel 1
00_B	01_B	0001_B PWM control with PWM Channel 2
00_B	10_B	0010_B PWM control with PWM Channel 3
00_B	11_B	0011_B PWM control with PWM Channel 4
01_B	00_B	0100_B PWM control with PWM Channel 5
01_B	01_B	0101_B PWM control with PWM Channel 6
01_B	10_B	0110_B PWM control with PWM Channel 7
01_B	11_B	0111_B PWM control with PWM Channel 8
10_B	00_B	1000_B PWM control with PWM Channel 9
10_B	01_B	1001_B PWM control with PWM Channel 10
10_B	10_B	1010_B PWM control with PWM Channel 11
10_B	11_B	1011_B PWM control with PWM Channel 12
11_B	x	Reserved

HB1_PWM_MAP[3:0]	NA	R/W	Half-bridge output 1 mode select

HB1_PWM_MAP[3:2]	HB1_PWM_MAP [1:0]	HB1_PWM_MAP[3:0]
00_B	00_B	0000_B PWM control with PWM Channel 1
00_B	01_B	0001_B PWM control with PWM Channel 2
00_B	10_B	0010_B PWM control with PWM Channel 3
00_B	11_B	0011_B PWM control with PWM Channel 4
01_B	00_B	0100_B PWM control with PWM Channel 5
01_B	01_B	0101_B PWM control with PWM Channel 6
01_B	10_B	0110_B PWM control with PWM Channel 7
01_B	11_B	0111_B PWM control with PWM Channel 8
10_B	00_B	1000_B PWM control with PWM Channel 9
10_B	01_B	1001_B PWM control with PWM Channel 10
10_B	10_B	1010_B PWM control with PWM Channel 11
10_B	11_B	1011_B PWM control with PWM Channel 12
11_B	x	Reserved

PWM_MAP_CTRL_2 & PWM_MAP_CTRL_5

PWM_MAP_CTRL_2 and PWM_MAP_CTRL_5 jointly determine the PWM channel selection of half-bridge output 8~5. The PWM mapping information of half-bridge output 8~5 is shown below.

Half-Bridge Output PWM Map Control 2 (Address =0x10) [reset =0x00].

D7	D6	D5	D4	D3	D2	D1	D0
HB8_PWM_MAP[1:0]		HB7_PWM_MAP[1:0]		HB6_PWM_MAP[1:0]		HB5_PWM_MAP[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Half-Bridge Output PWM Map Control 5 (Address =0x28) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_PWM_MAP[3:2]		HB7_PWM_MAP[3:2]		HB6_PWM_MAP[3:2]		HB5_PWM_MAP[3:2]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB8_PWM_MAP[3:0]	NA	R/W	Half-bridge output 8 mode select

HB8_PWM_MAP[3:2]	HB8_PWM_MAP [1:0]	HB8_PWM_MAP[3:0]
00_B	00_B	0000_B PWM control with PWM Channel 1
00_B	01_B	0001_B PWM control with PWM Channel 2
00_B	10_B	0010_B PWM control with PWM Channel 3

			00_B	11_B	0011_B PWM control with PWM Channel 4
			01_B	00_B	0100_B PWM control with PWM Channel 5
			01_B	01_B	0101_B PWM control with PWM Channel 6
			01_B	10_B	0110_B PWM control with PWM Channel 7
			01_B	11_B	0111_B PWM control with PWM Channel 8
			10_B	00_B	1000_B PWM control with PWM Channel 9
			10_B	01_B	1001_B PWM control with PWM Channel 10
			10_B	10_B	1010_B PWM control with PWM Channel 11
			10_B	11_B	1011_B PWM control with PWM Channel 12
			11_B	x	Reserved
HB7_PWM_MAP[3:0]	NA	R/W	Half-bridge output 7 mode select		
			HB7_PWM_MAP[3:2]	HB7_PWM_MAP [1:0]	HB7_PWM_MAP[3:0]
			00_B	00_B	0000_B PWM control with PWM Channel 1
			00_B	01_B	0001_B PWM control with PWM Channel 2
			00_B	10_B	0010_B PWM control with PWM Channel 3
			00_B	11_B	0011_B PWM control with PWM Channel 4
			01_B	00_B	0100_B PWM control with PWM Channel 5
			01_B	01_B	0101_B PWM control with PWM Channel 6
			01_B	10_B	0110_B PWM control with PWM Channel 7
			01_B	11_B	0111_B PWM control with PWM Channel 8
			10_B	00_B	1000_B PWM control with PWM Channel 9
			10_B	01_B	1001_B PWM control with PWM Channel 10
			10_B	10_B	1010_B PWM control with PWM Channel 11
			10_B	11_B	1011_B PWM control with PWM Channel 12
			11_B	x	Reserved
HB6_PWM_MAP[3:0]	NA	R/W	Half-bridge output 6 mode select		
			HB6_PWM_MAP[3:2]	HB6_PWM_MAP [1:0]	HB6_PWM_MAP[3:0]
			00_B	00_B	0000_B PWM control with PWM Channel 1
			00_B	01_B	0001_B PWM control with PWM Channel 2
			00_B	10_B	0010_B PWM control with PWM Channel 3
			00_B	11_B	0011_B PWM control with PWM Channel 4
			01_B	00_B	0100_B PWM control with PWM Channel 5
			01_B	01_B	0101_B PWM control with PWM Channel 6
			01_B	10_B	0110_B PWM control with PWM Channel 7
			01_B	11_B	0111_B PWM control with PWM Channel 8
			10_B	00_B	1000_B PWM control with PWM Channel 9
			10_B	01_B	1001_B PWM control with PWM Channel 10
			10_B	10_B	1010_B PWM control with PWM Channel 11
			10_B	11_B	1011_B PWM control with PWM Channel 12
			11_B	x	Reserved
HB5_PWM_MAP[3:0]	NA	R/W	Half-bridge output 5 mode select		
			HB5_PWM_MAP[3:2]	HB5_PWM_MAP [1:0]	HB5_PWM_MAP[3:0]
			00_B	00_B	0000_B PWM control with PWM Channel 1
			00_B	01_B	0001_B PWM control with PWM Channel 2
			00_B	10_B	0010_B PWM control with PWM Channel 3
			00_B	11_B	0011_B PWM control with PWM Channel 4
			01_B	00_B	0100_B PWM control with PWM Channel 5
			01_B	01_B	0101_B PWM control with PWM Channel 6
			01_B	10_B	0110_B PWM control with PWM Channel 7
			01_B	11_B	0111_B PWM control with PWM Channel 8
			10_B	00_B	1000_B PWM control with PWM Channel 9
			10_B	01_B	1001_B PWM control with PWM Channel 10
			10_B	10_B	1010_B PWM control with PWM Channel 11
			10_B	11_B	1011_B PWM control with PWM Channel 12
			11_B	x	Reserved

PWM_MAP_CTRL_3 & PWM_MAP_CTRL_6

PWM_MAP_CTRL_3 and PWM_MAP_CTRL_6 jointly determine the PWM channel selection of half-bridge output 12~9. The PWM mapping information of half-bridge output 12~9 is shown below.

Half-Bridge Output PWM Map Control 3 (Address =0x11) [reset =0x00].

D7	D6	D5	D4	D3	D2	D1	D0
HB12_PWM_MAP[1:0]		HB11_PWM_MAP[1:0]		HB10_PWM_MAP[1:0]		HB9_PWM_MAP[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Half-Bridge Output PWM Map Control 6 (Address =0x29) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB12_PWM_MAP[3:2]		HB11_PWM_MAP[3:2]		HB10_PWM_MAP[3:2]		HB9_PWM_MAP[3:2]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB12_PWM_MAP[3:0]	NA	R/W	Half-bridge output 12 mode select
HB11_PWM_MAP[3:0]	NA	R/W	Half-bridge output 11 mode select
HB10_PWM_MAP[3:0]	NA	R/W	Half-bridge output 10 mode select
HB9_PWM_MAP[3:0]	NA	R/W	Half-bridge output 9 mode select

HB12_PWM_MAP[3:0] description:

HB12_PWM_MAP[3:2]	HB12_PWM_MAP [1:0]	HB12_PWM_MAP[3:0]
00_B	00_B	0000_B PWM control with PWM Channel 1
00_B	01_B	0001_B PWM control with PWM Channel 2
00_B	10_B	0010_B PWM control with PWM Channel 3
00_B	11_B	0011_B PWM control with PWM Channel 4
01_B	00_B	0100_B PWM control with PWM Channel 5
01_B	01_B	0101_B PWM control with PWM Channel 6
01_B	10_B	0110_B PWM control with PWM Channel 7
01_B	11_B	0111_B PWM control with PWM Channel 8
10_B	00_B	1000_B PWM control with PWM Channel 9
10_B	01_B	1001_B PWM control with PWM Channel 10
10_B	10_B	1010_B PWM control with PWM Channel 11
10_B	11_B	1011_B PWM control with PWM Channel 12
11_B	x	Reserved

HB11_PWM_MAP[3:0] description:

HB11_PWM_MAP[3:2]	HB11_PWM_MAP [1:0]	HB11_PWM_MAP[3:0]
00_B	00_B	0000_B PWM control with PWM Channel 1
00_B	01_B	0001_B PWM control with PWM Channel 2
00_B	10_B	0010_B PWM control with PWM Channel 3
00_B	11_B	0011_B PWM control with PWM Channel 4
01_B	00_B	0100_B PWM control with PWM Channel 5
01_B	01_B	0101_B PWM control with PWM Channel 6
01_B	10_B	0110_B PWM control with PWM Channel 7
01_B	11_B	0111_B PWM control with PWM Channel 8
10_B	00_B	1000_B PWM control with PWM Channel 9
10_B	01_B	1001_B PWM control with PWM Channel 10
10_B	10_B	1010_B PWM control with PWM Channel 11
10_B	11_B	1011_B PWM control with PWM Channel 12
11_B	x	Reserved

HB10_PWM_MAP[3:0] description:

HB10_PWM_MAP[3:2]	HB10_PWM_MAP [1:0]	HB10_PWM_MAP[3:0]
00_B	00_B	0000_B PWM control with PWM Channel 1
00_B	01_B	0001_B PWM control with PWM Channel 2
00_B	10_B	0010_B PWM control with PWM Channel 3
00_B	11_B	0011_B PWM control with PWM Channel 4
01_B	00_B	0100_B PWM control with PWM Channel 5
01_B	01_B	0101_B PWM control with PWM Channel 6
01_B	10_B	0110_B PWM control with PWM Channel 7
01_B	11_B	0111_B PWM control with PWM Channel 8
10_B	00_B	1000_B PWM control with PWM Channel 9
10_B	01_B	1001_B PWM control with PWM Channel 10
10_B	10_B	1010_B PWM control with PWM Channel 11
10_B	11_B	1011_B PWM control with PWM Channel 12
11_B	x	Reserved

HB9_PWM_MAP[3:0] description:

HB9_PWM_MAP[3:2]	HB9_PWM_MAP [1:0]	HB9_PWM_MAP[3:0]
00_B	00_B	0000_B PWM control with PWM Channel 1
00_B	01_B	0001_B PWM control with PWM Channel 2
00_B	10_B	0010_B PWM control with PWM Channel 3
00_B	11_B	0011_B PWM control with PWM Channel 4
01_B	00_B	0100_B PWM control with PWM Channel 5
01_B	01_B	0101_B PWM control with PWM Channel 6
01_B	10_B	0110_B PWM control with PWM Channel 7
01_B	11_B	0111_B PWM control with PWM Channel 8
10_B	00_B	1000_B PWM control with PWM Channel 9
10_B	01_B	1001_B PWM control with PWM Channel 10
10_B	10_B	1010_B PWM control with PWM Channel 11
10_B	11_B	1011_B PWM control with PWM Channel 12
11_B	x	Reserved

PWM_ FREQ_CTRL_1 & PWM_ FREQ_CTRL_2 & PWM_ FREQ_CTRL_4

PWM_ FREQ_CTRL_1, PWM_ FREQ_CTRL_2, and PWM_ FREQ_CTRL_4 jointly determine the frequency selection of PWM Channel 8~1. The frequency selection information of channel 8~1 is shown below.

PWM Channel Frequency Select 1 (Address =0x12) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_CH4_FREQ[1:0]		PWM_CH3_FREQ[1:0]		PWM_CH2_FREQ[1:0]		PWM_CH1_FREQ[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PWM Channel Frequency Select 2 (Address =0x2A) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_CH8_FREQ[1:0]		PWM_CH7_FREQ[1:0]		PWM_CH6_FREQ[1:0]		PWM_CH5_FREQ[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PWM Channel Frequency Select 4 (Address =0x2C) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_CH8_FREQ[2]	PWM_CH7_FREQ[2]	PWM_CH6_FREQ[2]	PWM_CH5_FREQ[2]	PWM_CH4_FREQ[2]	PWM_CH3_FREQ[2]	PWM_CH2_FREQ[2]	PWM_CH1_FREQ[2]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_CH8_FREQ [2:0]	NA	R/W	PWM Channel 8 frequency select PWM_CH8_FREQ [2] / PWM_CH8_FREQ [1:0] / PWM_CH8_FREQ [2:0] 1_B / 00_B / 100_B PWM frequency: 400Hz 1_B / 01_B / 101_B PWM frequency: 600Hz 1_B / 10_B / 110_B PWM frequency: 800Hz 1_B / 11_B / 111_B PWM frequency: 1000Hz 0_B / 00_B / 000_B PWM frequency: 80Hz 0_B / 01_B / 001_B PWM frequency: 100Hz 0_B / 10_B / 010_B PWM frequency: 200Hz 0_B / 11_B / 011_B PWM frequency: 2000Hz
PWM_CH7_FREQ [2:0]	NA	R/W	PWM Channel 7 frequency select PWM_CH7_FREQ [2] / PWM_CH7_FREQ [1:0] / PWM_CH7_FREQ [2:0] 1_B / 00_B / 100_B PWM frequency: 400Hz 1_B / 01_B / 101_B PWM frequency: 600Hz 1_B / 10_B / 110_B PWM frequency: 800Hz 1_B / 11_B / 111_B PWM frequency: 1000Hz 0_B / 00_B / 000_B PWM frequency: 80Hz 0_B / 01_B / 001_B PWM frequency: 100Hz 0_B / 10_B / 010_B PWM frequency: 200Hz 0_B / 11_B / 011_B PWM frequency: 2000Hz
PWM_CH6_FREQ [2:0]	NA	R/W	PWM Channel 6 frequency select PWM_CH6_FREQ [2] / PWM_CH6_FREQ [1:0] / PWM_CH6_FREQ [2:0] 1_B / 00_B / 100_B PWM frequency: 400Hz 1_B / 01_B / 101_B PWM frequency: 600Hz 1_B / 10_B / 110_B PWM frequency: 800Hz 1_B / 11_B / 111_B PWM frequency: 1000Hz 0_B / 00_B / 000_B PWM frequency: 80Hz 0_B / 01_B / 001_B PWM frequency: 100Hz 0_B / 10_B / 010_B PWM frequency: 200Hz 0_B / 11_B / 011_B PWM frequency: 2000Hz
PWM_CH5_FREQ [2:0]	NA	R/W	PWM Channel 5 frequency select PWM_CH5_FREQ [2] / PWM_CH5_FREQ [1:0] / PWM_CH5_FREQ [2:0] 1_B / 00_B / 100_B PWM frequency: 400Hz 1_B / 01_B / 101_B PWM frequency: 600Hz 1_B / 10_B / 110_B PWM frequency: 800Hz 1_B / 11_B / 111_B PWM frequency: 1000Hz 0_B / 00_B / 000_B PWM frequency: 80Hz 0_B / 01_B / 001_B PWM frequency: 100Hz 0_B / 10_B / 010_B PWM frequency: 200Hz 0_B / 11_B / 011_B PWM frequency: 2000Hz
PWM_CH4_FREQ [2:0]	NA	R/W	PWM Channel 4 frequency select PWM_CH4_FREQ [2] / PWM_CH4_FREQ [1:0] / PWM_CH4_FREQ [2:0] 1_B / 00_B / 100_B PWM frequency: 400Hz 1_B / 01_B / 101_B PWM frequency: 600Hz 1_B / 10_B / 110_B PWM frequency: 800Hz 1_B / 11_B / 111_B PWM frequency: 1000Hz 0_B / 00_B / 000_B PWM frequency: 80Hz

			0_B 01_B 001_B PWM frequency: 100Hz 0_B 10_B 010_B PWM frequency: 200Hz 0_B 11_B 011_B PWM frequency: 2000Hz
PWM_CH3_FREQ [2:0]	NA	R/W	PWM Channel 3 frequency select PWM_CH3_FREQ [2] / PWM_CH3_FREQ [1:0] / PWM_CH3_FREQ [2:0] 1_B 00_B 100_B PWM frequency: 400Hz 1_B 01_B 101_B PWM frequency: 600Hz 1_B 10_B 110_B PWM frequency: 800Hz 1_B 11_B 111_B PWM frequency: 1000Hz 0_B 00_B 000_B PWM frequency: 80Hz 0_B 01_B 001_B PWM frequency: 100Hz 0_B 10_B 010_B PWM frequency: 200Hz 0_B 11_B 011_B PWM frequency: 2000Hz
PWM_CH2_FREQ [2:0]	NA	R/W	PWM Channel 2 frequency select PWM_CH2_FREQ [2] / PWM_CH2_FREQ [1:0] / PWM_CH2_FREQ [2:0] 1_B 00_B 100_B PWM frequency: 400Hz 1_B 01_B 101_B PWM frequency: 600Hz 1_B 10_B 110_B PWM frequency: 800Hz 1_B 11_B 111_B PWM frequency: 1000Hz 0_B 00_B 000_B PWM frequency: 80Hz 0_B 01_B 001_B PWM frequency: 100Hz 0_B 10_B 010_B PWM frequency: 200Hz 0_B 11_B 011_B PWM frequency: 2000Hz
PWM_CH1_FREQ [2:0]	NA	R/W	PWM Channel 1 frequency select PWM_CH1_FREQ [2] / PWM_CH1_FREQ [1:0] / PWM_CH1_FREQ [2:0] 1_B 00_B 100_B PWM frequency: 400Hz 1_B 01_B 101_B PWM frequency: 600Hz 1_B 10_B 110_B PWM frequency: 800Hz 1_B 11_B 111_B PWM frequency: 1000Hz 0_B 00_B 000_B PWM frequency: 80Hz 0_B 01_B 001_B PWM frequency: 100Hz 0_B 10_B 010_B PWM frequency: 200Hz 0_B 11_B 011_B PWM frequency: 2000Hz

PWM_ FREQ_CTRL_3 & PWM_ FREQ_CTRL_5

PWM_ FREQ_CTRL_3 and PWM_ FREQ_CTRL_5 jointly determine the frequency selection of PWM Channel 12~9. The frequency selection information of channel 12~9 is shown below.

PWM Channel Frequency Select 3 (Address =0x2B) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_CH12_FREQ[1:0]		PWM_CH11_FREQ[1:0]		PWM_CH10_FREQ[1:0]		PWM_CH9_FREQ[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PWM Channel Frequency Select 5 (Address =0x2D) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	PWM_CH12_FREQ[2]	PWM_CH11_FREQ[2]	PWM_CH10_FREQ[2]	PWM_CH9_FREQ[2]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_CH12_FREQ [2:0]	NA	R/W	PWM Channel 12 frequency select PWM_CH12_FREQ [2] / PWM_CH12_FREQ [1:0] / PWM_CH12_FREQ [2:0] 1_B 00_B 100_B PWM frequency: 400Hz 1_B 01_B 101_B PWM frequency: 600Hz 1_B 10_B 110_B PWM frequency: 800Hz 1_B 11_B 111_B PWM frequency: 1000Hz 0_B 00_B 000_B PWM frequency: 80Hz 0_B 01_B 001_B PWM frequency: 100Hz 0_B 10_B 010_B PWM frequency: 200Hz 0_B 11_B 011_B PWM frequency: 2000Hz
PWM_CH11_FREQ [2:0]	NA	R/W	PWM Channel 11 frequency select PWM_CH11_FREQ [2] / PWM_CH11_FREQ [1:0] / PWM_CH11_FREQ [2:0] 1_B 00_B 100_B PWM frequency: 400Hz 1_B 01_B 101_B PWM frequency: 600Hz 1_B 10_B 110_B PWM frequency: 800Hz 1_B 11_B 111_B PWM frequency: 1000Hz

			0_B	00_B	000_B PWM frequency: 80Hz
			0_B	01_B	001_B PWM frequency: 100Hz
			0_B	10_B	010_B PWM frequency: 200Hz
			0_B	11_B	011_B PWM frequency: 2000Hz
PWM_CH10_FREQ [2:0]	NA	R/W	PWM Channel 10 frequency select		
			PWM_CH10_FREQ [2]	PWM_CH10_FREQ [1:0]	PWM_CH10_FREQ [2:0]
			1_B	00_B	100_B PWM frequency: 400Hz
			1_B	01_B	101_B PWM frequency: 600Hz
			1_B	10_B	110_B PWM frequency: 800Hz
			1_B	11_B	111_B PWM frequency: 1000Hz
			0_B	00_B	000_B PWM frequency: 80Hz
			0_B	01_B	001_B PWM frequency: 100Hz
			0_B	10_B	010_B PWM frequency: 200Hz
			0_B	11_B	011_B PWM frequency: 2000Hz
PWM_CH9_FREQ [2:0]	NA	R/W	PWM Channel 9 frequency select		
			PWM_CH9_FREQ [2]	PWM_CH9_FREQ [1:0]	PWM_CH9_FREQ [2:0]
			1_B	00_B	100_B PWM frequency: 400Hz
			1_B	01_B	101_B PWM frequency: 600Hz
			1_B	10_B	110_B PWM frequency: 800Hz
			1_B	11_B	111_B PWM frequency: 1000Hz
			0_B	00_B	000_B PWM frequency: 80Hz
			0_B	01_B	001_B PWM frequency: 100Hz
			0_B	10_B	010_B PWM frequency: 200Hz
			0_B	11_B	011_B PWM frequency: 2000Hz

PWM_DUTY_CTRL_1

PWM Channel 1 Duty Cycle Configuration (Address =0x13) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH1	D7:D0	R/W	PWM Channel 1 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM_DUTY_CTRL_2

PWM Channel 2 Duty Cycle Configuration (Address =0x14) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH2							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH2	D7:D0	R/W	PWM Channel 2 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM_DUTY_CTRL_3

PWM Channel 3 Duty Cycle Configuration (Address =0x15) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH3							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH3	D7:D0	R/W	PWM Channel 3 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM_DUTY_CTRL_4

PWM Channel 4 Duty Cycle Configuration (Address =0x16) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH4							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH4	D7:D0	R/W	PWM Channel 4 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

SR _CTRL_1

The Slew Rate Configuration 1 (Address =0x17) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB8_SR	D7	R/W	HB8 slew rate configuration 0_B 1 V/μs 1_B 3.2V/μs
HB7_SR	D6	R/W	HB7 slew rate configuration 0_B 1 V/μs 1_B 3.2V/μs
HB6_SR	D5	R/W	HB6 slew rate configuration 0_B 1V/μs 1_B 3.2V/μs
HB5_SR	D4	R/W	HB5 slew rate configuration 0_B 1V/μs 1_B 3.2V/μs
HB4_SR	D3	R/W	HB4 slew rate configuration 0_B 1V/μs 1_B 3.2V/μs
HB3_SR	D2	R/W	HB3 slew rate configuration 0_B 1V/μs 1_B 3.2V/μs
HB2_SR	D1	R/W	HB2 slew rate configuration 0_B 1V/μs 1_B 3.2V/μs
HB1_SR	D0	R/W	HB1 slew rate configuration 0_B 1V/μs 1_B 3.2V/μs

SR _CTRL_2

The Slew Rate Configuration 2 (Address =0x18) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	HB12_SR	HB11_SR	HB10_SR	HB9_SR
R	R	R	R	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
Reserved	D7	R	Reserved. Always reads as '0'
Reserved	D6	R	Reserved. Always reads as '0'
Reserved	D5	R	Reserved. Always reads as '0'
Reserved	D4	R	Reserved. Always reads as '0'
HB12_SR	D3	R	HB12 slew rate configuration 0_B 1V/μs 1_B 3.2V/μs
HB11_SR	D2	R/W	HB11 slew rate configuration 0_B 1V/μs 1_B 3.2V/μs
HB10_SR	D1	R/W	HB10 slew rate configuration 0_B 1V/μs

			1_B 3.2V/μs
HB9_SR	D0	R/W	HB9 slew rate configuration 0_B 1V/μs 1_B 3.2V/μs

OLD _CTRL_1

The Open Load Detection Control 1 (Address =0x19) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_OLD_DIS	HB7_OLD_DIS	HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB8_OLD_DIS	D7	R/W	HB8 open load detection configuration 0_B Open-load detection on half-bridge 8 is enabled 1_B Open-load detection on half-bridge 8 is disabled
HB7_OLD_DIS	D6	R/W	HB7 open load detection configuration 0_B Open-load detection on half-bridge 7 is enabled 1_B Open-load detection on half-bridge 7 is disabled
HB6_OLD_DIS	D5	R/W	HB6 open load detection configuration 0_B Open-load detection on half-bridge 6 is enabled 1_B Open-load detection on half-bridge 6 is disabled
HB5_OLD_DIS	D4	R/W	HB5 open load detection configuration 0_B Open-load detection on half-bridge 5 is enabled 1_B Open-load detection on half-bridge 5 is disabled
HB4_OLD_DIS	D3	R/W	HB4 open load detection configuration 0_B Open-load detection on half-bridge 4 is enabled 1_B Open-load detection on half-bridge 4 is disabled
HB3_OLD_DIS	D2	R/W	HB3 open load detection configuration 0_B Open-load detection on half-bridge 3 is enabled 1_B Open-load detection on half-bridge 3 is disabled
HB2_OLD_DIS	D1	R/W	HB2 open load detection configuration 0_B Open-load detection on half-bridge 2 is enabled 1_B Open-load detection on half-bridge 2 is disabled
HB1_OLD_DIS	D0	R/W	HB1 open load detection configuration 0_B Open-load detection on half-bridge 1 is enable 1_B Open-load detection on half-bridge 1 is disable

OLD _CTRL_2

The Open Load Detection Control 2 (Address =0x1A) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
OLD_REP	OLD_OP	Reserved		HB12_OLD_DIS	HB11_OLD_DIS	HB10_OLD_DIS	HB9_OLD_DIS
R/W	R/W	R	R	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
OLD_REP	D7	R/W	0_B Report on nFAULT pin during OLD condition 1_B No report on nFAULT pin during OLD condition
OLD_OP	D6	R/W	0_B Half-bridges are not active after OLD condition detect 1_B Half-bridges are active after OLD condition detect
Reserved	D5	R	Reserved. Always reads as ‘0’
Reserved	D4	R	Reserved. Always reads as ‘0’
HB12_OLD_DIS	D3	R/W	HB12 open load detection configuration 0_B Open-load detection on half-bridge 12 is enabled 1_B Open-load detection on half-bridge 12 is disabled
HB11_OLD_DIS	D2	R/W	HB11 open load detection configuration 0_B Open-load detection on half-bridge 11 is enabled 1_B Open-load detection on half-bridge 11 is disabled
HB10_OLD_DIS	D1	R/W	HB10 open load detection configuration 0_B Open-load detection on half-bridge 10 is enabled 1_B Open-load detection on half-bridge 10 is disabled
HB9_OLD_DIS	D0	R/W	HB9 open load detection configuration 0_B Open-load detection on half-bridge 9 is enabled 1_B Open-load detection on half-bridge 9 is disabled

OLD _CTRL_3

The Open Load Detection Control 3 (Address =0x1B) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
OCP_DEG			Reserved	HB12_LOLD_EN	HB11_LOLD_EN	HB10_LOLD_EN	HB9_LOLD_EN
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
OCP_DEG	D7:D5	R/W	000_B OCP deglitch filter time is 10μs 001_B OCP deglitch filter time is 5μs 010_B OCP deglitch filter time is 2.5μs 011_B OCP deglitch filter time is 1μs 110_B OCP deglitch filter time is 30μs 111_B OCP deglitch filter time is 20μs
Reserved	D4	R/W	Reserved. Always reads as '0'
HB12_LOLD_EN	D3	R/W	HB12 low-current OLD detection configuration 0_B Low-current OLD detection on half-bridge 12 is disabled 1_B Low-current OLD detection on half-bridge 12 is enabled
HB11_LOLD_ EN	D2	R/W	HB11 low-current OLD detection configuration 0_B Low-current OLD detection on half-bridge 11 is disabled 1_B Low-current OLD detection on half-bridge 11 is enabled
HB10_LOLD_ EN	D1	R/W	HB10 low-current OLD detection configuration 0_B Low-current OLD detection on half-bridge 10 is disabled 1_B Low-current OLD detection on half-bridge 10 is enabled
HB9_LOLD_ EN	D0	R/W	HB9 low-current OLD detection configuration 0_B Low-current OLD detection on half-bridge 9 is disabled 1_B Low-current OLD detection on half-bridge 9 is enabled

OLD _CTRL_4

The Open Load Detection Control 4 (Address =0x24) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_LOLD_EN	HB7_LOLD_EN	HB6_LOLD_EN	HB5_LOLD_EN	HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB8_LOLD_ EN	D7	R/W	HB8 low-current OLD detection configuration 0_B Low-current OLD detection on half-bridge 8 is disabled 1_B Low-current OLD detection on half-bridge 8 is enabled
HB7_LOLD_ EN	D6	R/W	HB7 low-current OLD detection configuration 0_B Low-current OLD detection on half-bridge 7 is disabled 1_B Low-current OLD detection on half-bridge 7 is enabled
HB6_LOLD_EN	D5	R/W	HB6 low-current OLD detection configuration 0_B Low-current OLD detection on half-bridge 6 is disabled 1_B Low-current OLD detection on half-bridge 6 is enabled
HB5_LOLD_ EN	D4	R/W	HB5 low-current OLD detection configuration 0_B Low-current OLD detection on half-bridge 5 is disabled 1_B Low-current OLD detection on half-bridge 5 is enabled
HB4_LOLD_ EN	D3	R/W	HB4 low-current OLD detection configuration 0_B Low-current OLD detection on half-bridge 4 is disabled 1_B Low-current OLD detection on half-bridge 4 is enabled
HB3_LOLD_ EN	D2	R/W	HB3 low-current OLD detection configuration 0_B Low-current OLD detection on half-bridge 3 is disabled 1_B Low-current OLD detection on half-bridge 3 is enabled
HB2_LOLD_ EN	D1	R/W	HB2 low-current OLD detection configuration 0_B Low-current OLD detection on half-bridge 2 is disabled 1_B Low-current OLD detection on half-bridge 2 is enabled
HB1_LOLD_ EN	D0	R/W	HB1 low-current OLD detection configuration 0_B Low-current OLD detection on half-bridge 1 is disabled 1_B Low-current OLD detection on half-bridge 1 is enabled

PWM_CTRL_3

Half-Bridge PWM Control 3 (Address =0x26) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_CH12_DIS	PWM_CH11_DIS	PWM_CH10_DIS	PWM_CH9_DIS	PWM_CH8_DIS	PWM_CH7_DIS	PWM_CH6_DIS	PWM_CH5_DIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_CH12_DIS	D7	R/W	0_B PWM Generator-12 is enabled 1_B PWM Generator-12 is disabled
PWM_CH11_DIS	D6	R/W	0_B PWM Generator-11 is enabled 1_B PWM Generator-11 is disabled
PWM_CH10_DIS	D5	R/W	0_B PWM Generator-10 is enabled 1_B PWM Generator-10 is disabled
PWM_CH9_DIS	D4	R/W	0_B PWM Generator-9 is enabled 1_B PWM Generator-9 is disabled
PWM_CH8_DIS	D3	R/W	0_B PWM Generator-8 is enabled 1_B PWM Generator-8 is disabled
PWM_CH7_DIS	D2	R/W	0_B PWM Generator-7 is enabled 1_B PWM Generator-7 is disabled
PWM_CH6_DIS	D1	R/W	0_B PWM Generator-6 is enabled 1_B PWM Generator-6 is disabled
PWM_CH5_DIS	D0	R/W	0_B PWM Generator-5 is enabled 1_B PWM Generator-5 is disabled

PWM_DUTY_CTRL_5

PWM Channel 5 Duty Cycle Configuration (Address =0x2E) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH5							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH5	D7:D0	R/W	PWM Channel 5 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM_DUTY_CTRL_6

PWM Channel 6 Duty Cycle Configuration (Address =0x2F) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH6							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH6	D7:D0	R/W	PWM Channel 6 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM_DUTY_CTRL_7

PWM Channel 7 Duty Cycle Configuration (Address =0x30) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH7							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH7	D7:D0	R/W	PWM Channel 7 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM_DUTY_CTRL_8

PWM Channel 8 Duty Cycle Configuration (Address =0x31) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH8							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH8	D7:D0	R/W	PWM Channel 8 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM_DUTY_CTRL_9

PWM Channel 9 Duty Cycle Configuration (Address =0x32) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH9							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH9	D7:D0	R/W	PWM Channel 9 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM_DUTY_CTRL_10

PWM Channel 10 Duty Cycle Configuration (Address =0x33) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH10							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH10	D7:D0	R/W	PWM Channel 10 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM_DUTY_CTRL_11

PWM Channel 11 Duty Cycle Configuration (Address =0x34) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH11							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH11	D7:D0	R/W	PWM Channel 11 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM_DUTY_CTRL_12

PWM Channel 12 Duty Cycle Configuration (Address =0x35) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH12							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH12	D7:D0	R/W	PWM Channel 12 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

Application Information

The SA52122B is a twelve half-bridge motor driver solution for automotive, industrial, and other mechatronic applications. The half-bridges are fully controllable to achieve forward, reverse, coasting, and braking motor operations. All functions can be programmed through the serial peripheral interface (SPI).

Design Specification

Input Voltage	Logic Voltage (VDD/EN)	DC Output Maximum Current	PWM Output	Duty Cycle
4.5-32V	3.3-5V	1A per channel	80/100/200/400/600/800/1000/2000Hz	0%~100%

Schematic

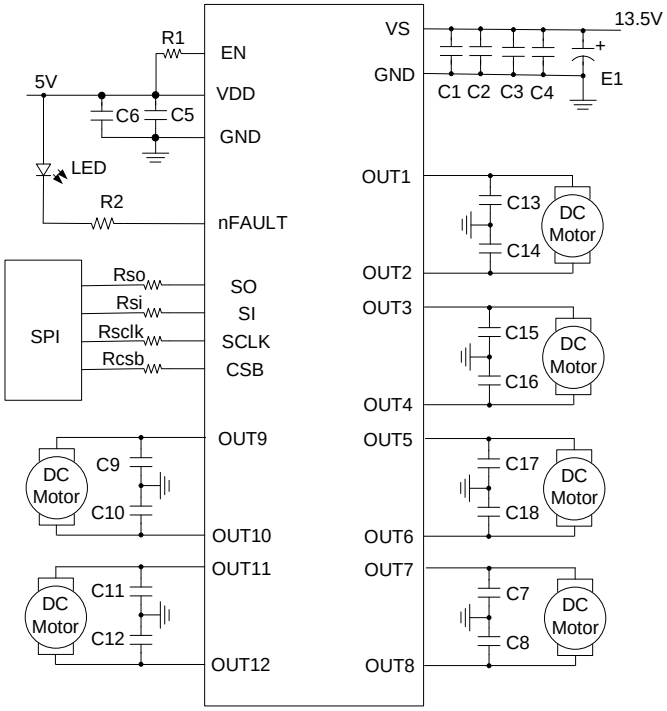


Figure 23. Typical Application Schematic

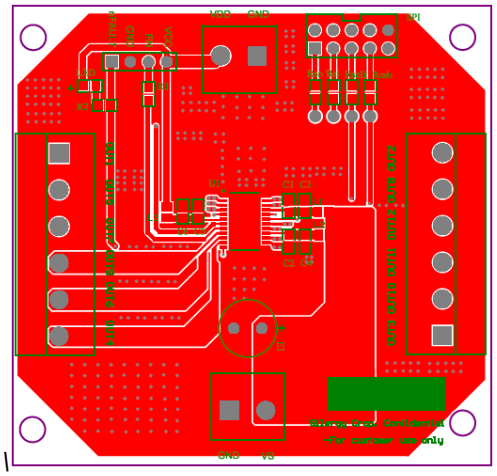
BOM List

Reference Designator	Description	Part Number	Manufacturer
U1	TSSOP24E	SA52122BHHP	Silergy
Rso, Rsclk, Rsi, Rcsb, R1	100Ω, 5%, 0603	RC0603JR-07100RL	YAGEO
R2	10kΩ, 5%, 0603	RC0603JR-0710KRL	YAGEO
E1	100uF/ 50V/E-CAP	ERS1HM101F12OT	AISHI
C1, C2,	1nF/50V	C1608NP01H102J	TDK
C3, C4	100nF/50V	C1608X7R1H104K	TDK
C5	1nF/25V	C1608X7R1E102J	TDK
C6	100nF/25V	C1608X7R1E104K	TDK
C7-C18	10nF/50V	C1608NP01H103J	TDK
LED	Green, 0603	XL-1608UGC-04	XINGLIGHT

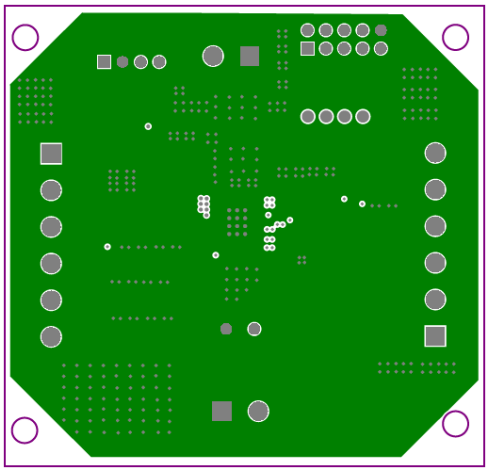
Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

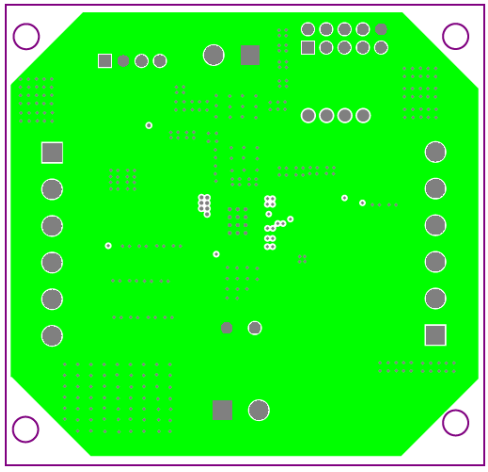
1. Place large electrolytic capacitors (E1) between VS and GND. It is recommended to use at least 10μF capacitance to maintain a stable motor supply voltage.
2. Place the input capacitors (C1, C2, C3, C4, C5, C6) as close as possible to the VS/VDD and GND pins, minimizing the loop formed by these connections. Avoid using direct vias in the power trace between the input capacitors and VS/VDD, GND to reduce parasitic inductance. It is recommended to choose 100pF~1nF for C1/C2, and 100nF~1μF for C3/ C4.
3. It is recommended to choose 100pF~1nF for C5, and 100nF~1μF for C6.
4. Keep the high current traces (VS, GND, and OUTx traces) as short and wide as possible.
5. Connect the exposed GND pad to a large copper area and place several GND vias to an internal GND plane or the bottom of the board for heat sinking and noise reduction. Maximize the GND copper area around the device to improve power dissipation.



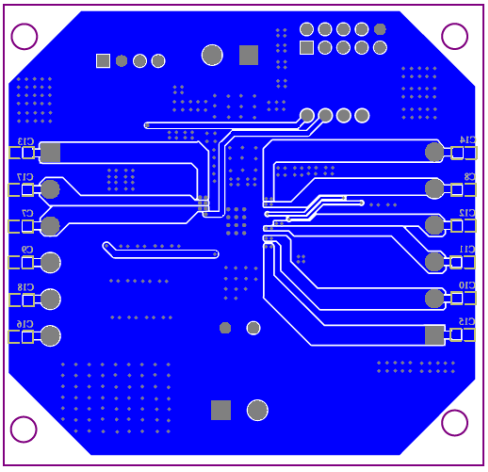
(a) Top Layer



(b) Sig1 Layer



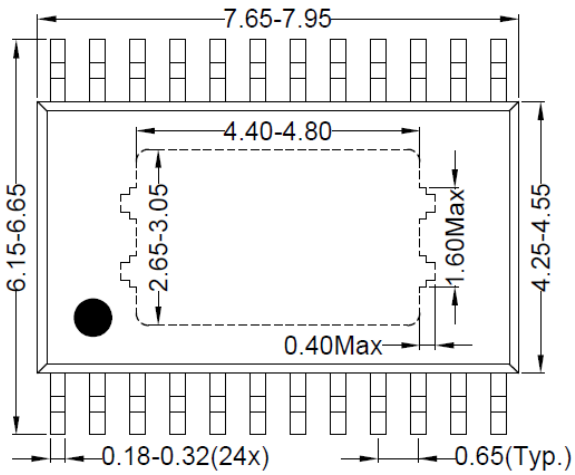
(c) Sig2 Layer



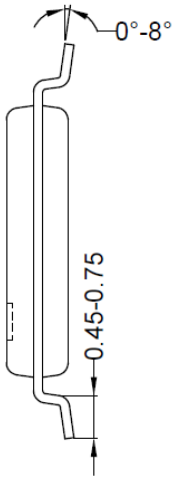
(d) Bottom Layer

Figure 24. PCB Layout Example

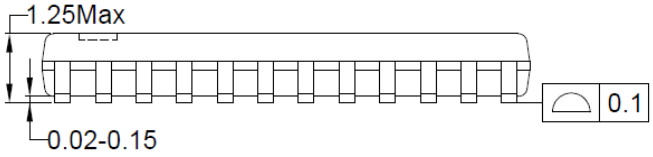
TSSOP24E Package Outline Drawing



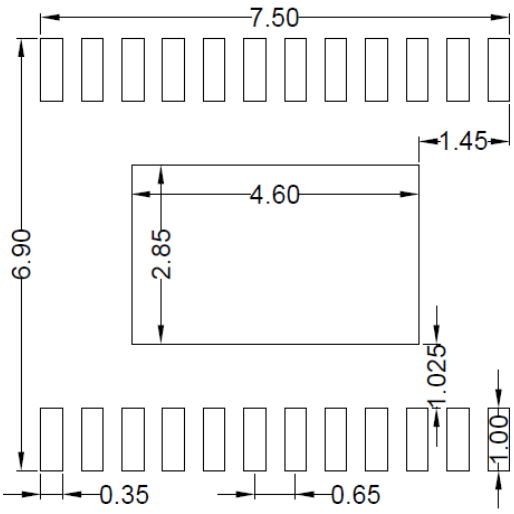
Top View



Side View



Front View

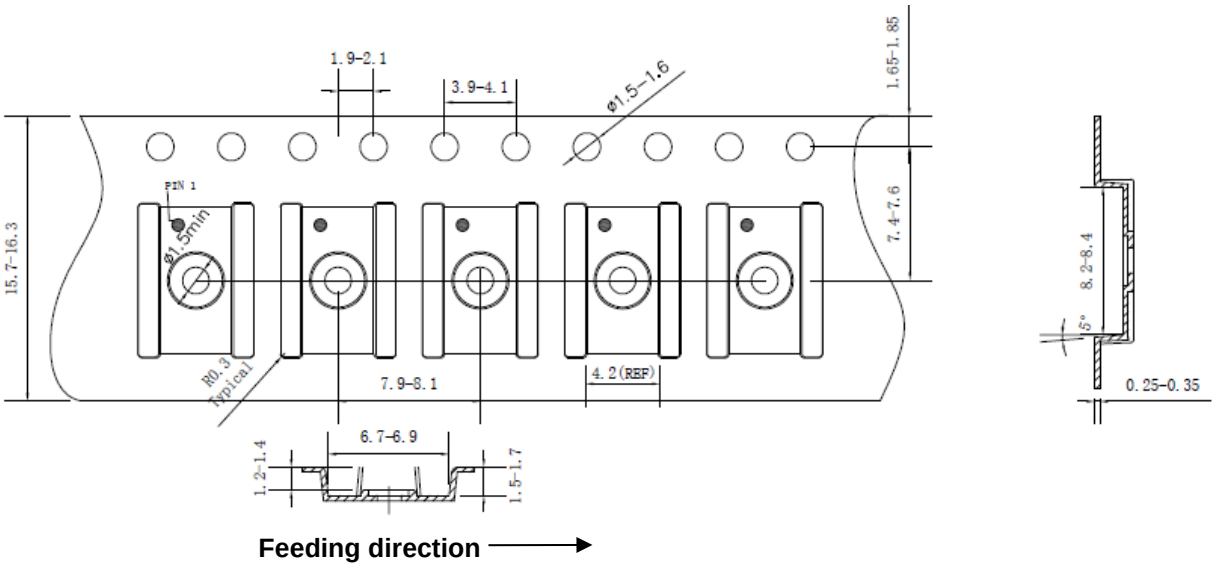


Recommended PCB Layout
(Reference Only)

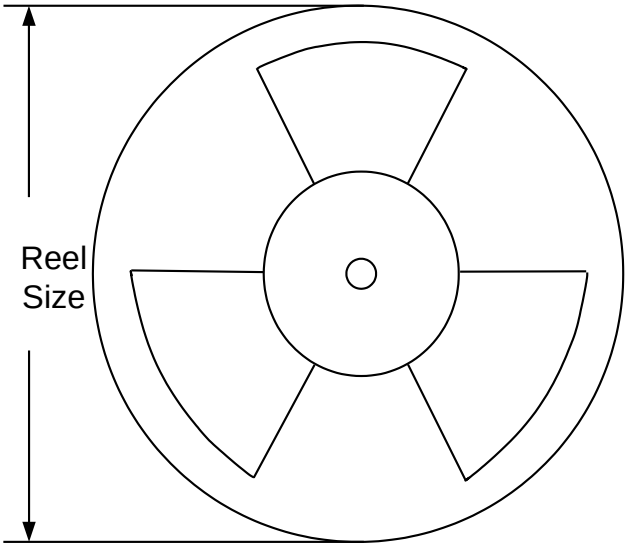
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Reel Dimensions



Package Type	Tape Width (mm)	Pocket Pitch (mm)	Reel Size (Inch)	Trailer Length (mm)	Leader Length (mm)	Qty per Reel
TSSOP24E	16	8	13"	400	400	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
1.0	Sept. 03, 2025	Initial Release	

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