# High Efficiency Fast Response, 8A, 28V Input Synchronous Buck Converter with 100mA 3.3V LDO

## General Description

The SY21288B is a high efficiency synchronous buck converter operating over a wide input voltage range of 4V to 24V and capable of delivering up to 8A current. It integrates low $R_{DS(ON)}$ top and bottom MOSFETs to minimize the conduction loss. It operates at a pseudo-constant frequency of 600kHz, to enable the use of small size inductor and capacitors. The SY21288B also provides a fixed 3.3V LDO with 100mA current capability, which can be used to power the external peripheries, such as the keyboard controller in notebook. The 3.3V LDO can switch to buck converter output to reduce power loss.

Silergy's constant on-time and ripple-based control strategy supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation, including when using low ESR output ceramic capacitors.

The SY21288B provides cycle-by-cycle current limit, input under voltage lockout, internal soft-start, output under voltage protection, over voltage protection and over temperature protection, to guarantee safe operation in all operating conditions.

## Features

- Low $R_{DS(ON)}$ for Internal MOSFETs: 20mΩ Top, 10mΩ Bottom
- Wide Input Voltage Range: 4V ~ 24V
- Fixed 3.338V Output Voltage
- 8A Continuous Output Current Capability
- 600kHz Pseudo-Constant Frequency
- ±1% Internal Reference Voltage
- Internal 1.2ms Soft-Start Limits the Inrush Current
- Constant On-Time and Ripple-Based Control to Achieve Fast Transient Responses
- Integrated 3.3V LDO with 100mA Current Capability
- Integrated 1.5Ω Bypass Switch
- PFM/USM Selectable Light Load Operation Mode
- Power Good Indicator
- Output Auto-Discharge Function
- Cycle-by-Cycle Valley and Peak Current Limit Protection for buck
- Latch-off Mode Output Under Voltage Protection for buck
- Latch-off Mode Output Over Voltage Protection for buck
- Latch-off Mode Over Temperature Protection for buck
- Auto-Recovery Mode Output Under Voltage Protection for LDO
- Auto-Recovery Mode Over Temperature Protection for LDO
- Input Under Voltage Lockout (UVLO)
- RoHS Compliant and Halogen Free
- Compact package: QFN2.5×2.5-16

## Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

## Typical Application

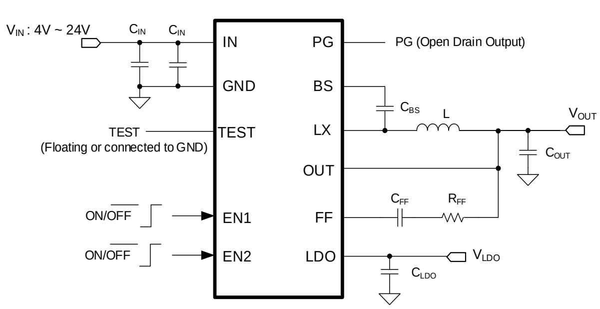



*Figure1. Schematic Diagram*

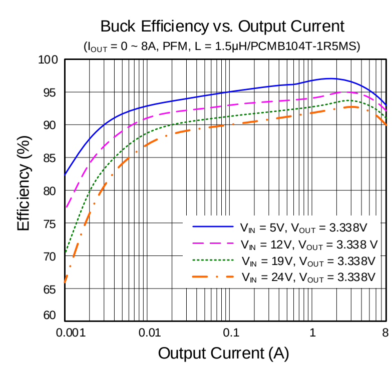


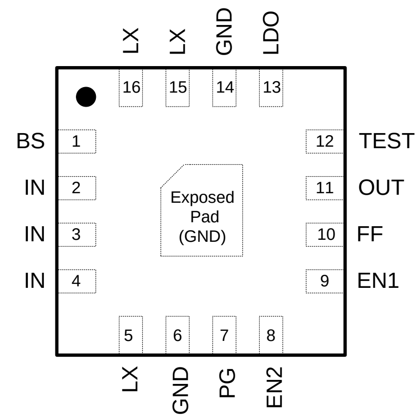

*Figure2. Buck Efficiency vs. Output Current*

## Ordering Information

| Ordering Number | Package type | Top Mark |
|---|---|---|
| SY21288BRHC | QFN2.5×2.5-16<br>RoHS Compliant and Halogen Free | **GBDxyz** |

***x = year code, y = week code, z = lot number code***

## Pinout (top view)




## Pin Description

| Pin No | Pin Name | Pin Description |
|---|---|---|
| 1 | BS | Bootstrap pin. Supply top MOSFET gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin. |
| 2, 3, 4 | IN | Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor. A 0.1μF ceramic capacitor placed in parallel is recommended to reduce high frequency noise. |
| 5, 15, 16 | LX | Inductor pin. Connect this pin to the switching node of the inductor. |
| 6, 14, EP | GND | Ground pin. |
| 7 | PG | Power good indicator pin. PG pin should be connected to $V_{IN}$ or another voltage source through a resistor (e.g., 10kΩ ~ 100kΩ). This pin becomes high when the output voltage is within 90% to 120% of regulated value under normal operation. |
| 8 | EN2 | Enable control pin for the buck converter and internal LDO. Pull high to turn on. Pull low to turn off. Do not leave this pin floating. |
| 9 | EN1 | Enable control pin of the buck converter. Pull high to turn on. Pull low to turn off. Do not leave this pin floating.<br>The pin is also used for controlling the operation mode of the buck converter under light load condition after its output is within the regulated range. When its voltage is lower than 1.6V and higher than 1V, the buck converter operates in ultra-sonic mode. When its voltage is higher than 2.2V, the buck converter operates in pulse-frequency modulation mode. |
| 10 | FF | Output feedforward pin. Connect the RC network to this pin from the node of output capacitors closest to the inductor. |
| 11 | OUT | Output pin. Connect this pin with output capacitors where you want to regulate the voltage. The pin also provides the bypass input for the 3.3V LDO. |
| 12 | TEST | For factory use only. Leave this pin floating or connect it to GND in application. |
| 13 | LDO | 3.3V LDO output pin. Decouple this pin to ground with at least a 4.7μF ceramic capacitor. |

## Block Diagram

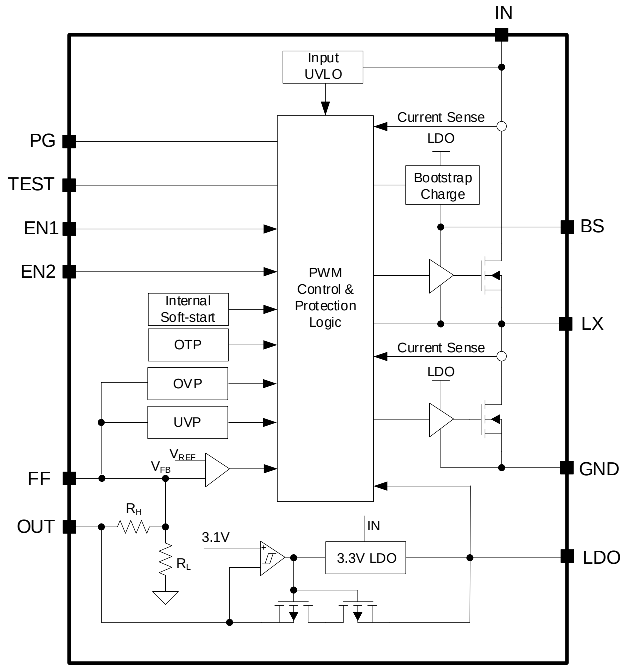



*Figure3. Block Diagram*

## Absolute Maximum Ratings

| Parameter (Note1) | Min | Max | Unit |
|---|---|---|---|
| IN | -0.3 | 28 | V |
| IN-LX, LX, PG, EN2, EN1 | -0.3 | 26 | |
| BS-LX, FF, TEST | -0.3 | 4 | |
| OUT, LDO | -0.3 | 4.5 | |
| LX, 10ns Duration | -5 | 29 | |
| LX, 20ns Duration | -1 | 28 | |
| Junction Temperature, Operating | -40 | 150 | °C |
| Lead Temperature (Soldering, 10s.) | | 260 | |
| Storage Temperature | -65 | 150 | |

## Thermal Information

| Parameter (Note2) | Typ | Unit |
|---|---|---|
| $\theta_{JA}$ Junction-to-Ambient Thermal Resistance | 33 | °C/W |
| $\theta_{JC}$ Junction-to-Case Thermal Resistance | 5.5 | |
| $P_D$ Power Dissipation $T_A$ = 25°C | 3 | W |

## Recommended Operating Conditions

| Parameter (Note3) | Min | Max | Unit |
|---|---|---|---|
| Input Voltage | 4 | 24 | V |
| Buck Output Current | | 8 | A |
| LDO Output Current | | 100 | mA |
| Ambient Temperature | -40 | 85 | °C |
| Junction Temperature | -40 | 125 | |

## Electrical Characteristics

($V_{IN}$ = 12V, $C_{OUT}$ = 66μF, $C_{FF}$ = 470pF, $R_{FF}$ = 1kΩ, $T_J$ = 25°C, $I_{OUT}$ = 1A unless otherwise specified (Note4))

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input | Voltage Range | $V_{IN}$ | | 4 | | 24 | V |
| | UVLO Rising Threshold | $V_{IN,UVLO}$ | $V_{IN}$ rising | | | 3.9 | |
| | UVLO Hysteresis | $V_{IN,HYS}$ | | | 0.5 | | |
| | Quiescent Current | $I_Q$ | $I_{OUT}$ = 0A, EN2 = EN1 = High, $V_{OUT}$ = $V_{SET}$×105% | | 80 | 100 | μA |
| | Shutdown Current 1 | $I_{SHDN1}$ | EN1 = Low, EN2 = High | | 50 | 70 | |
| | Shutdown Current 2 | $I_{SHDN2}$ | EN1 = Low, EN2 = Low | | 5 | 9 | |
| Output | Voltage Set-Point | $V_{SET}$ | CCM | 3.305 | 3.338 | 3.371 | V |
| | Discharge Current | $I_{DIS}$ | $V_{OUT}$ = 3.338V | | 90 | | mA |
| | Soft-Start Time | $t_{SS}$ | $V_{OUT}$ from 0% to 100% $V_{SET}$ (Note5) | | 1.2 | | ms |
| | OVP Threshold | $V_{OVP}$ | $V_{FB}$ rising | 117 | 120 | 123 | %$V_{REF}$ |
| | OVP Hysteresis | $V_{OVP,HYS}$ | | | 5 | | |
| | OVP Delay Time | $t_{OVP,DLY}$ | (Note5) | | 30 | | μs |
| | UVP Threshold | $V_{UVP}$ | $V_{FB}$ falling | 55 | 60 | 65 | %$V_{REF}$ |
| | UVP Delay Time | $t_{UVP,DLY}$ | (Note5) | | 200 | | μs |
| MOSFETs | Top MOSFET $R_{DS(ON)}$ | $R_{DS(ON),TOP}$ | | | 20 | | mΩ |
| | Bottom MOSFET $R_{DS(ON)}$ | $R_{DS(ON),BOT}$ | | | 10 | | |
| | Top MOSFET Current Limit Threshold | $I_{LMT,TOP}$ | | | 16 | | A |
| | Bottom MOSFET Current Limit Threshold | $I_{LMT,BOT}$ | | 10 | | | |
| | Bottom MOSFET Reverse Current Limit Threshold | $I_{LMT,RVS}$ | USM | 3 | 4.8 | | |
| Enable (EN) | Input Voltage High | $V_{EN,H}$ | | 1 | | | V |
| | Input Voltage Low | $V_{EN,L}$ | | | | 0.4 | |
| | EN1 Voltage for Ultra-sonic Mode | $V_{EN1,USM}$ | | 1 | | 1.6 | |
| | EN1 Voltage for PFM Mode | $V_{EN1,PFM}$ | | 2.2 | | $V_{IN}$ | |
| | De-Glitch Time | $t_{EN,DG}$ | (Note5) | | 40 | | μs |
| Frequency | Switching Frequency | $f_{SW}$ | CCM | 510 | 600 | 690 | kHz |
| | Ultra-Sonic Mode Frequency | $f_{USM}$ | USM, $I_{OUT}$ = 0A | 20 | | | |
| | Minimum On-Time | $t_{ON,MIN}$ | | | 50 | | ns |
| | Minimum Off-Time | $t_{OFF,MIN}$ | | | 150 | | |
| Power Good (PG) | Rising Threshold | $V_{PG,R}$ | $V_{FB}$ rising (good) | 87 | 90 | 93 | %$V_{REF}$ |
| | Falling Threshold | $V_{PG,F}$ | $V_{FB}$ falling (not good) | 80 | 83 | 86 | |
| | Delay Time | $t_{PG,R}$ | Low to high (Note5) | | 200 | | μs |
| | | $t_{PG,F}$ | High to low (Note5) | | 30 | | |
| | | $t_{PG,OFF}$ | IC shuts down (Note5) | | | 0.5 | |

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | Low Voltage | $V_{PG,LOW}$ | $V_{FB}$ = 0V, $I_{PG}$ = 5mA | | | 0.45 | V |
| LDO | Output Voltage | $V_{LDO}$ | Bypass switch turns off, $I_{LDO}$ = 30mA | 3.15 | 3.3 | 3.45 | V |
| | Dropout Voltage | $V_{DROPOUT}$ | $I_{LDO}$ = 100mA | | 300 | | mV |
| | Output Current Limit Threshold | $I_{LMT,LDO}$ | | 150 | | 300 | mA |
| BYP | $R_{DS(ON)}$ | $R_{DS(ON),BYP}$ | | | 1.5 | | Ω |
| | Turn on Voltage | $V_{BYP}$ | | 2.97 | 3.1 | | V |
| | Turn on Hysteresis | $V_{BYP, HYS}$ | | | 0.2 | | V |
| | OVP Voltage | $V_{BYP, OVP}$ | | 114 | 120 | 126 | %$V_{LDO}$ |
| OTP | Buck Temperature | $T_{OTP,BUCK}$ | $T_J$ rising (Note5) | | 150 | | °C |
| | Buck Temperature Hysteresis | $T_{BUCK,HYS}$ | $T_J$ falling (Note5) | | 15 | | °C |
| | LDO Temperature | $T_{OTP,LDO}$ | $T_J$ rising (Note5) | | 160 | | °C |
| | LDO Temperature Hysteresis | $T_{LDO,HYS}$ | $T_J$ falling (Note5) | | 25 | | °C |

**Note 1**: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2**: Package thermal resistance is measured in the natural convection at $T_A$ = 25°C on a 8.5cm×8.5cm size, four-layer Silergy Evaluation Board with 2-oz copper.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

**Note 4:** Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

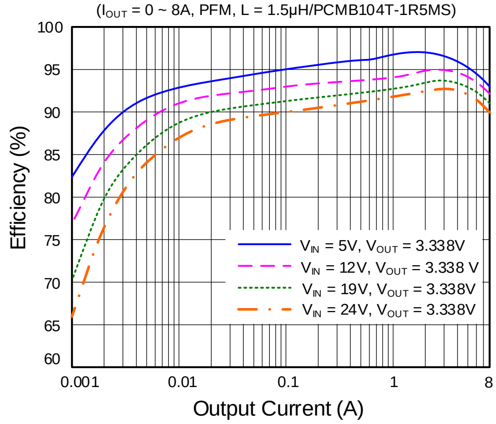
**Note 5:** Guaranteed by design.

## Typical Performance Characteristics

($T_A$ = 25°C, $V_{IN}$ = 12V, $V_{OUT}$ = 3.338V, L = 1.5μH, $C_{OUT}$ = 66μF, $C_{FF}$ = 470pF, unless otherwise noted)

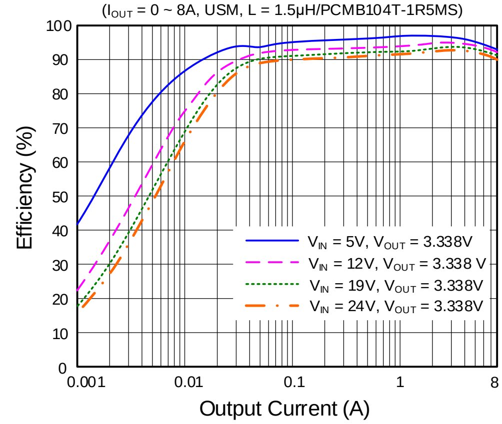
Buck Efficiency vs. Output Current

($I_{OUT}$ = 0 ~ 8A, PFM, L = 1.5μH/PCMB104T-1R5MS)



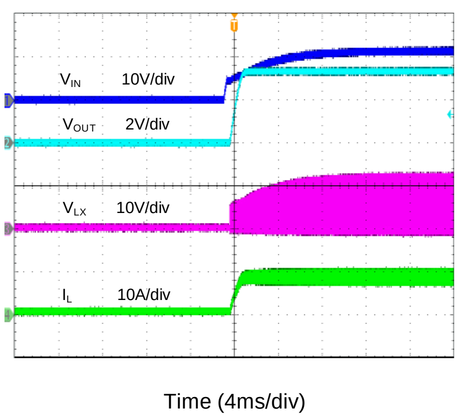

Buck Efficiency vs. Output Current

($I_{OUT}$ = 0 ~ 8A, USM, L = 1.5μH/PCMB104T-1R5MS)



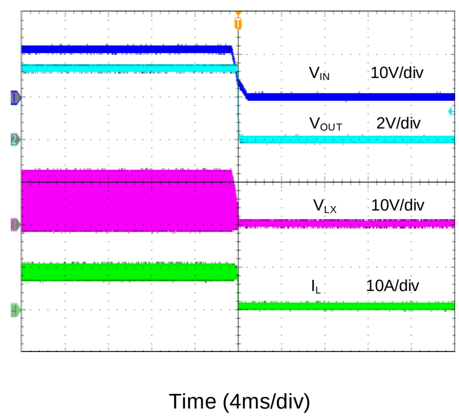

Startup from $V_{IN}$

($V_{IN}$ = 12V, $V_{OUT}$ = 3.338V, $I_{OUT}$ = 8A)



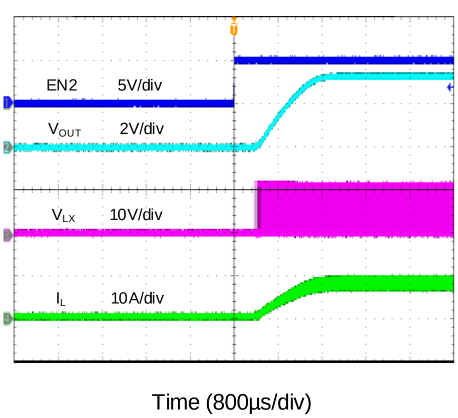

Shutdown from $V_{IN}$

($V_{IN}$ = 12V, $V_{OUT}$ = 3.338V, $I_{OUT}$ = 8A)



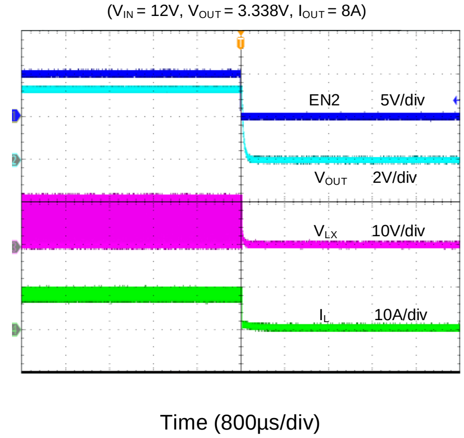

Startup from EN2

($V_{IN}$ = 12V, $V_{OUT}$ = 3.338V, $I_{OUT}$ = 8A)



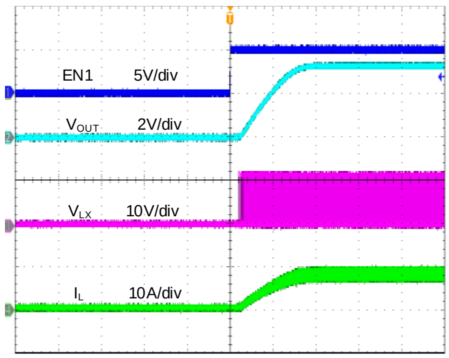

Shutdown from EN2

($V_{IN}$ = 12V, $V_{OUT}$ = 3.338V, $I_{OUT}$ = 8A)



Startup from EN1

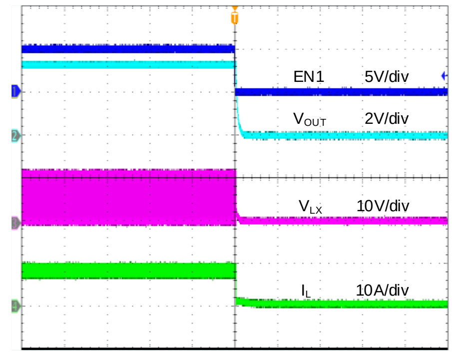
($V_{IN}$ = 12V, $V_{OUT}$ = 3.338V, $I_{OUT}$ = 8A)




Time (800µs/div)

Shutdown from EN1

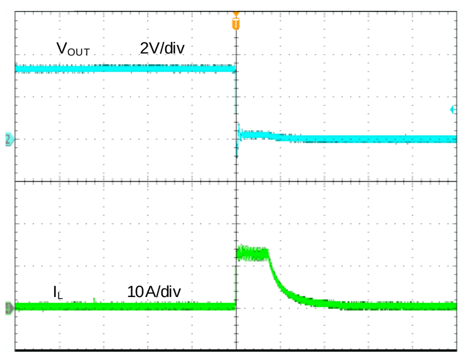
($V_{IN}$ = 12V, $V_{OUT}$ = 3.338V, $I_{OUT}$ = 8A)




Time (800µs/div)

Output Short Circuit Protection

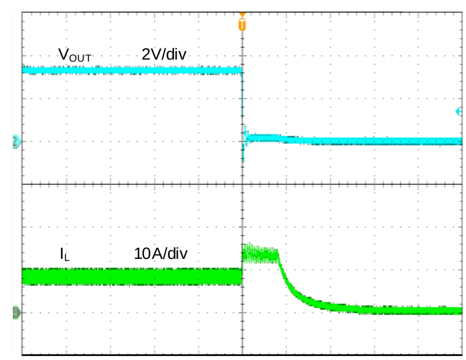
($V_{IN}$ = 12V, $V_{OUT}$ = 3.338V, $I_{OUT}$ = 0A ~ short)




Time (200µs/div)

Output Short Circuit Protection

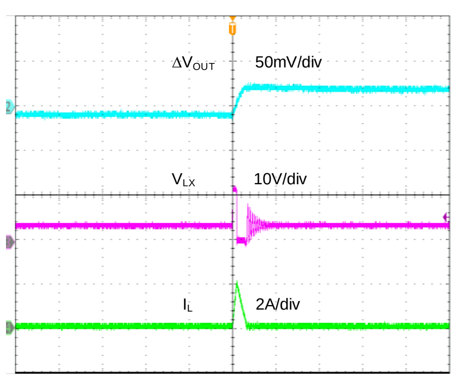
($V_{IN}$ = 12V, $V_{OUT}$ = 3.338V, $I_{OUT}$ = 8A ~ short)




Time (200µs/div)

Output Ripple

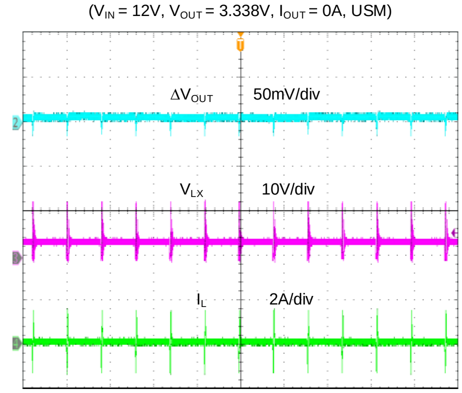
($V_{IN}$ = 12V, $V_{OUT}$ = 3.338V, $I_{OUT}$ = 0A, PFM)




Time (4µs/div)

Output Ripple

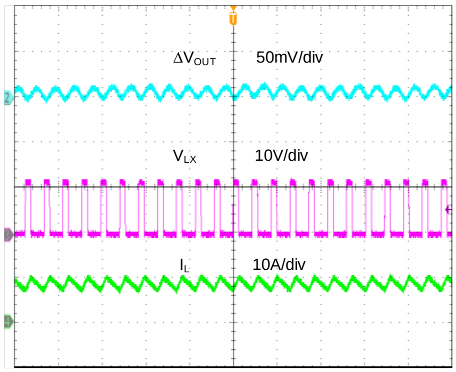
($V_{IN}$ = 12V, $V_{OUT}$ = 3.338V, $I_{OUT}$ = 0A, USM)




Time (40µs/div)

Output Ripple

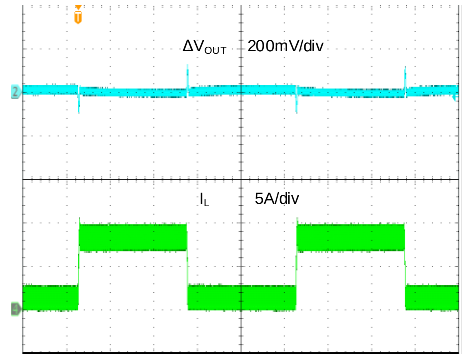
($V_{IN}$ = 12V, $V_{OUT}$ = 3.338V, $I_{OUT}$ = 8A)




Time (4μs/div)

Load Transient

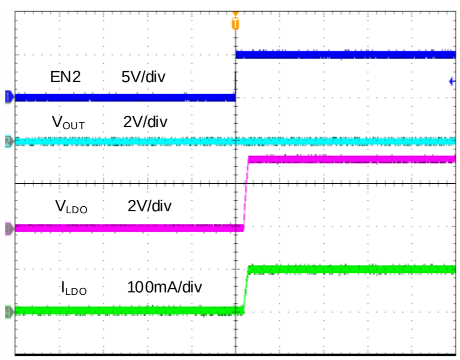
($V_{IN}$ = 12V, $V_{OUT}$ = 3.338V, $I_{OUT}$ = 0.8 ~ 8A, PFM)




Time (200μs/div)

LDO Startup from EN2

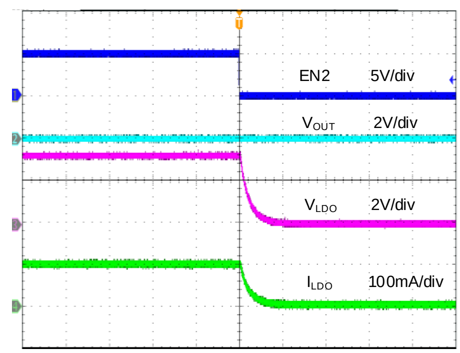
($V_{IN}$ = 12V, $I_{LDO}$ = 100mA, EN1 = Low)




Time (800μs/div)

LDO Shutdown from EN2

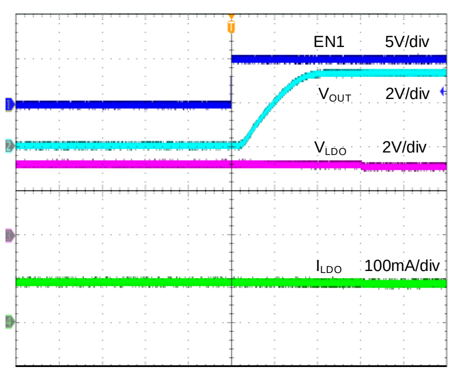
($V_{IN}$ = 12V, $I_{LDO}$ = 100mA, EN1 = Low)




Time (800μs/div)

LDO Switchover When EN1 On

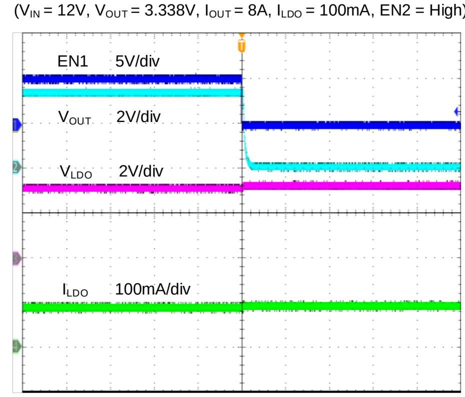
($V_{IN}$ = 12V, $V_{OUT}$ = 3.338V, $I_{OUT}$ = 8A, $I_{LDO}$ = 100mA, EN2 = High)



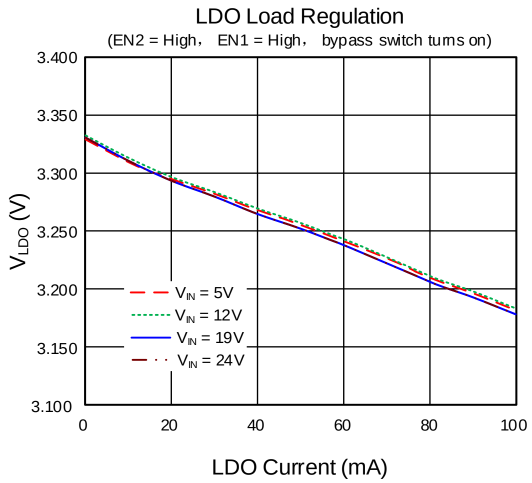

Time (800μs/div)

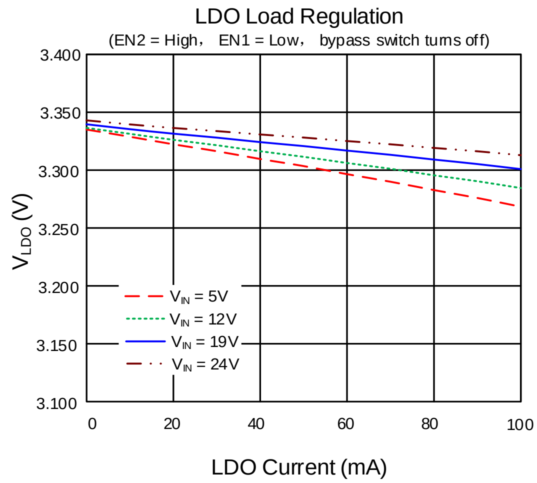
LDO Switchover When EN1 Off

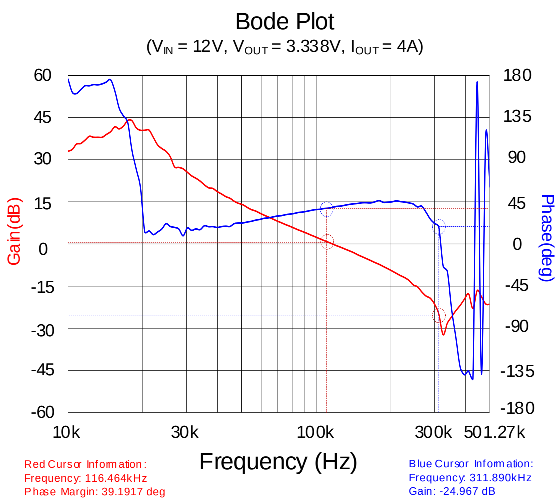
($V_{IN}$ = 12V, $V_{OUT}$ = 3.338V, $I_{OUT}$ = 8A, $I_{LDO}$ = 100mA, EN2 = High)




Time (800μs/div)


LDO Load Regulation
(EN2 = High， EN1 = High， bypass switch turns on)
3.400
3.350
3.300
3.250
3.200
3.150
3.100
0
20
40
60
80
100
VLDO (V)
VIN = 5V
VIN = 12V
VIN = 19V
VIN = 24V
LDO Current (mA)


LDO Load Regulation
(EN2 = High， EN1 = Low， bypass switch turns off)
3.400
3.350
3.300
3.250
3.200
3.150
3.100
0
20
40
60
80
100
VLDO (V)
VIN = 5V
VIN = 12V
VIN = 19V
VIN = 24V
LDO Current (mA)


Bode Plot
(VIN = 12V, VOUT = 3.338V, IOUT = 4A)
Gain(dB)
Phase(deg)
60
45
30
15
0
-15
-30
-45
-60
180
135
90
45
0
-45
-90
-135
-180
10k
30k
100k
300k
501.27k
Frequency (Hz)
Red Cursor Information:
Frequency: 116.464kHz
Phase Margin: 39.1917 deg
Blue Cursor Information:
Frequency: 311.890kHz
Gain: -24.967 dB

# Detailed Description

## General Features

### Constant On-time Architecture

Fundamental to any constant on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the top MOSFET. Each on-time ($t_{ON}$) is a "fixed" voltage ratio,

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

For example, considering that a hypothetical converter targets 3.338V output from a 12V input at 600kHz, the target on-time is

$$\frac{3.338V}{12V} \times \frac{1}{600kHz} = 464ns$$

Each $t_{ON}$ pulse is triggered by the feedback comparator when the output voltage as measured at FB node drops below the regulated value. After one $t_{ON}$ period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is lower than the regulated value. This approach avoids making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

In a COT architecture, there is no fixed clock, so the top MOSFET can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays.

### Minimum and Maximum Duty Cycle

In the COT architecture, there is no limitation for operating the part at low duty cycle, since in this case, when the on-time is close to the minimum on-time, the switching frequency is reduced as needed to always ensure a proper operation.

The device can support 3.338V fixed output even when the input voltage is as low as 4V, across the entire junction temperature range of -40°C ~ 125°C.

### Instant-PWM Operation

Silergy's COT ripple-based control strategy adds several proprietary improvements to the traditional COT architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the $t_{ON}$ duration, instant-PWM control method derives this signal internally. Another improvement optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT converters may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor may become too small to maintain stable operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the $t_{ON}$ pulse is triggered as long as the minimum off-time has been satisfied and the inductor current as measured in the bottom MOSFET is lower than its current limit threshold. As the $t_{ON}$ pulse is triggered, the bottom MOSFET turns off and the top MOSFET turns on. The inductor current ramps up linearly during the $t_{ON}$ period. At the end of the $t_{ON}$ period, the top MOSFET turns off, the bottom MOSFET turns on, and the inductor current ramps down linearly. This action also initiates the minimum off-time timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum off-time is relatively short so that during fast speed load transients, $t_{ON}$ can be retriggered with minimal delay, allowing the inductor current to ramp quickly and provide sufficient energy to the load side.

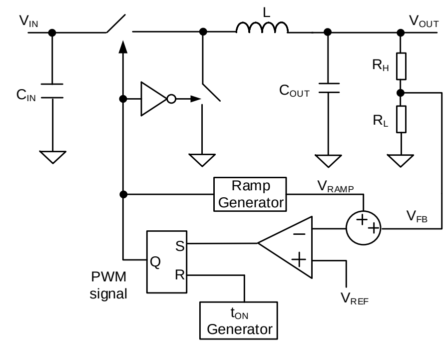



*Figure4. Silergy's COT Ripple-based Control Strategy*

In order to avoid shoot-through, a dead time ($t_{DEAD}$) is generated internally between turning the top MOSFET off and the bottom MOSFET on, as wells as between turning the bottom MOSFET off and the top MOSFET on.

### Light Load Operation Mode Selection

PFM or USM light load operation is selected using the EN1 pin. EN1 is a dual purpose input serving as the buck converter enable pin but also as mode selection pin to control operation mode of the buck converter under light load conditions, after its output is within the regulated range. If the voltage on this pin is lower than 1.6V and higher than 1V, the buck converter operates in ultra-sonic mode (USM). If the voltage on this pin is higher than 2.2V, the buck converter operates using pulse-frequency modulation (PFM) mode.

If PFM light load operation is selected, under light load conditions, typically when the load satisfies the following equation,

$$I_{OUT\_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1-D)}{2 \times f_{SW} \times L} \quad (1)$$

The current through the bottom MOSFET will ramp to near zero before the next $t_{ON}$ time. When this occurs, the bottom MOSFET turns off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, the combined feedback and ramp signals remain much higher than the reference voltage, the instant-PWM control loop will not trigger another $t_{ON}$ until needed, and the apparent operating switching frequency will correspondingly drop, improving efficiency. The switching frequency can be lower than audible frequency area under deep light load or null load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next $t_{ON}$ cycle. The buck converter enters CCM once the load current exceeds the threshold shown in (1). Above the threshold, the switching frequency stays fairly constant over the output current range.

If USM light load operation is selected, the control loop keeps the switching frequency above the audible frequency range, even under deep light load or null load conditions.

**Input Under Voltage Lockout (UVLO)**

To prevent operation before the internal circuitry is ready and to ensure that the top and bottom MOSFETs can be properly driven, the device incorporates an input undervoltage lockout protection.

The device remains in a low current state and LX node switching actions and LDO are inhibited until $V_{IN}$ exceeds the UVLO rising threshold. At that time, if EN2 is high, the LDO starts operating, and if EN1 is also high, the buck converter is enabled and soft-start ramp is initiated. If $V_{IN}$ falls below $V_{IN,UVLO}$ less than the input UVLO hysteresis, LX node switching actions and LDO will again be suppressed.

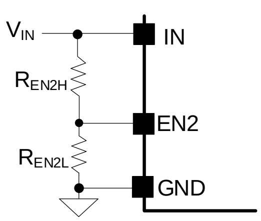



*Figure5. Enable Control*

Increasing the default input UVLO threshold can be implemented using an external resistor divider connected to EN2.

**EN2/EN1 Control**

The device has two enable pins to control the buck converter and LDO which enables system power management during low power states.

The buck converter and LDO are all turned off under S4/S5 states (EN2 = Low, EN1 = High or Low). Under S3 state (EN2 = High, EN1 = Low), only the LDO is turned on while the buck converter is turned off. Under S0 state (EN2 = High, EN1 = High), the buck converter and LDO are turned on. Only if EN2 is high could LDO be turned on, and only if EN1 and EN2 are both high could the buck converter be turned on. A summary of the low power modes based on EN2/EN1 state is shown below:

| EN2 | EN1 | STATE | LDO | Buck |
|---|---|---|---|---|
| High | High | S0 | On | On |
| High | Low | S3 | On | Off |
| Low | Low/High | S4/S5 | Off | Off |

The EN2/EN1 inputs are high-voltage capable inputs with logic-compatible threshold. EN2/EN1 logic high is defined as a voltage higher than 1V, and a logic low as a voltage lower than 0.4V.

It is not recommended to connect EN2 or EN1 pin to $V_{IN}$ or another voltage source directly. A resistor in a range of 1kΩ to 1MΩ should be used for EN2/EN1 pin in this case.

**Startup and Shutdown**

The device incorporates an internal soft-start circuit to smoothly ramp the buck converter output to the desired voltage whenever it is enabled. Internally, the soft-start circuit clamps the output at zero and then allows the output to rise to the desired voltage over approximately 1.2ms, which avoids high current flow and transients during startup. The startup and shutdown sequence are shown below:

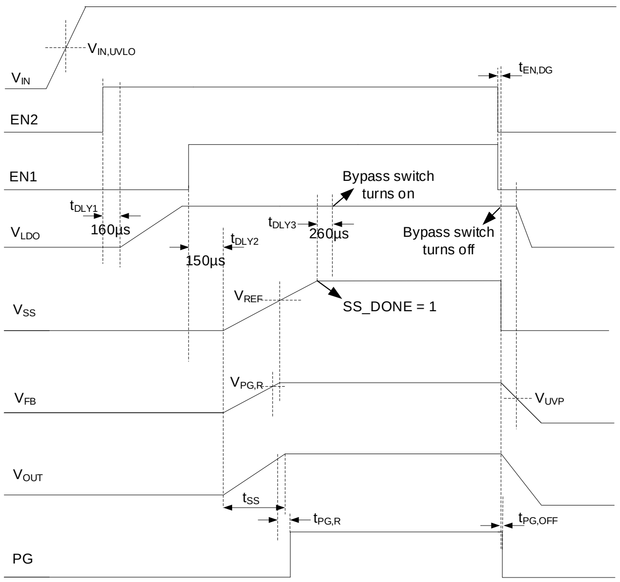



*Figure6. Startup and Shutdown Sequence*

After $V_{IN}$ exceeds the UVLO rising threshold, the internal LDO regulator is turned on after the delay time $t_{DLY1}$ if EN2 is high, the buck converter is turned on after the delay time $t_{DLY2}$ if EN1 is also high. When the output voltage is 90% of the regulated value, PG is set to the high-impedance state after the delay time $t_{PG,R}$. After the delay time $t_{DLY3}$ from SS_DONE becomes high, the LDO output switches to the buck output if the output voltage is higher than bypass switch turn on voltage. The LDO output will switch to the internal LDO regulator when either EN2 or EN1 are driven low.

The device supports startup with pre-biased output. If the output is pre-biased to a certain voltage before startup, the buck converter disables the switching of both the top MOSFET and the bottom MOSFET until the internal soft-start voltage $V_{SS}$ exceeds the sensed output voltage at the FB node. The first pulse on-time is internally calculated based the input voltage and pre-biased output voltage.

**PG Power Good Indicator**

PG is an open drain output controlled by a window comparator connected to the feedback signal. If the voltage is higher than $V_{PG,R}$ and less than $V_{OVP}$ for at least the power good delay time (low to high), PG will be set to high-impedance state.

PG should be connected to $V_{IN}$ or another voltage source through a resistor (e.g., 100kΩ). After $V_{IN}$ rises until the internal initial power is ready, the PG internal MOSFET is turned on so that PG is actively driven low before output voltage is ready. After the feedback voltage $V_{FB}$ reaches $V_{PG,R}$, PG is set to high-impedance state after a delay time of 200µs (typ.). When $V_{FB}$ drops to $V_{PG,F}$, or rises above $V_{OVP}$ for the OVP delay time, PG is driven low after a delay time of 30µs (typ.).

**Buck Output Auto-Discharge Function**

The device discharges the output voltage when the buck converter shuts down due to low $V_{IN}$ or EN2/EN1, or caused by a protection function being triggered, so that the output voltage can be discharged in a minimal time, even if the buck output load current is zero. The discharge MOSFET in parallel with the bottom MOSFET turns on after the bottom MOSFET turns off when the shutdown logic is enabled. The output discharge current is typically 90mA for $V_{OUT}$ = 3.338V. The discharge MOSFET is not active outside of these shutdown conditions.

**External Bootstrap Capacitor**

This device integrates a floating power supply for the gate driver of the top MOSFET. Proper operation requires a 0.1µF low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the N-channel top MOSFET.

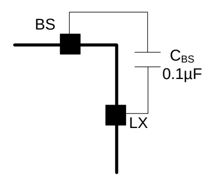



*Figure7. Bootstrap Capacitor Connection*

**LDO Output**

The device integrates a high performance, low drop-out linear regulator (LDO) and its output voltage set-point is fixed to 3.3V, which can not only power the internal gate drivers, PWM logic, analog circuitry and other blocks, but also power the external peripheries with 100mA capability. This LDO is intended mainly as an auxiliary 3.3V supply for notebook systems, when in standby mode. When the input voltage exceeds the UVLO rising threshold, and EN2 is high, LDO is turned on and supplied power by $V_{IN}$. After EN1 is also high, until the output voltage exceeds the bypass switch turn on voltage, PG is in the high-impedance state and SS_DONE continues high for the delay time $t_{DLY3}$, the internal LDO regulator will be turned off and the bypass switch will be turned on so that LDO output switches to the output voltage to reduce power consumption. Connect a 4.7µF low ESR ceramic capacitor from LDO to GND.

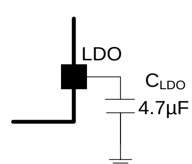



*Figure8. LDO Capacitor Connection*

## Fault Protection Modes

### Buck Output Current Limit

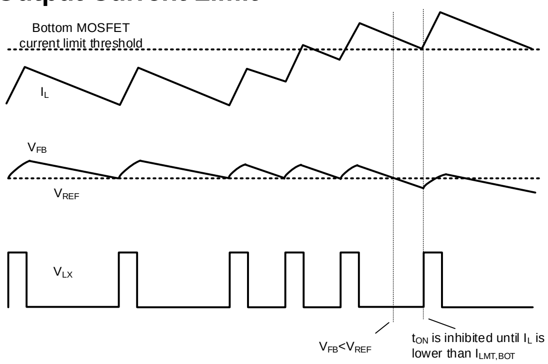



*Figure9. Bottom Current Limit Protection*

The buck converter features cycle-by-cycle “valley” current limit (bottom MOSFET current limit). The Inductor current is monitored in the bottom MOSFET when it turns on and as the inductor current ramps down. If the monitored current is higher than current limit threshold, $t_{ON}$ is inhibited until the current returns back to below the threshold.

When the valley current limit occurs, the output current limit value is

$$I_{LMT,OUT} = I_{LMT,BOT} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

The valley current limit protection limits the inductor current, but the OCP itself is a non-latched protection. When the load current is higher than the bottom MOSFET current limit threshold by one half of the peak-to-peak inductor ripple current, the output voltage starts to drop. When the feedback voltage falls below the under voltage protection (UVP) threshold, and continues for the UVP delay time, the buck converter will be disabled and enter latch-off state. Independent from this mechanism, the over temperature protection may also be triggered under the over current condition and the buck converter will be disabled and enter latch-off state.

The buck converter also features cycle-by-cycle peak current limit (top MOSFET current limit). During the $t_{ON}$ time, the top MOSFET current is monitored. If it exceeds the current limit threshold, the MOSFET will be turned off, and the bottom MOSFET will be turned on. $t_{ON}$ can be not inhibited when the bottom MOSFET current is lower than the bottom MOSFET current limit threshold.

### Buck Output Under Voltage Protection (UVP)

If $V_{OUT}$ < ~60% of the regulated value for approximately 200µs occurring when the output short circuit or the load current is much higher than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the buck converter will be disabled and set to a latch-off state. Cycle EN2 or EN1 input to re-enable the buck converter.

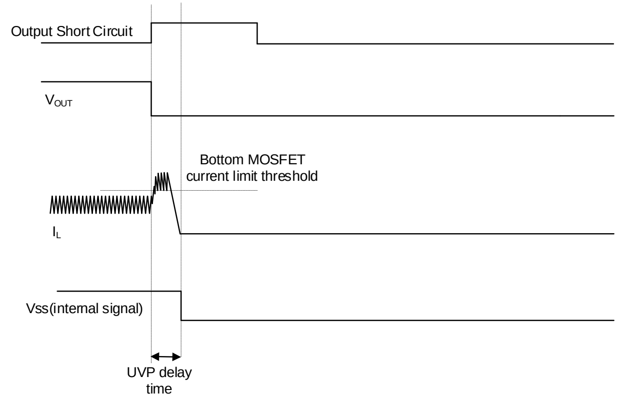



*Figure10. Output Under Voltage Protection*

### Buck Output Over Voltage Protection (OVP)

The buck converter includes output over voltage protection (OVP). If the feedback voltage rises above the reference voltage level, the top MOSFET naturally remains off and different actions are taken depending on the operation mode.

When operating in PFM light load mode, if the feedback voltage remains high, the bottom MOSFET remains on until the inductor current reaches zero and the LX node switching actions are suppressed. If the feedback voltage doesn’t exceed the OVP threshold, the LX node switching actions will be resumed when the combined feedback and ramp signals become lower than the reference voltage. If the feedback voltage exceeds the over voltage protection threshold and the output voltage exceeds the bypass switch OVP voltage for the OVP delay time, the output over voltage protection (OVP) will be triggered, and the buck converter will be disabled and enter latch off state. Cycle EN2 or EN1 input to re-enable the buck converter.

When operating in USM light load mode, if the feedback voltage remains high, the bottom MOSFET turn on time will be longer and inductor current average value becomes more and more negative until the reverse current limit is triggered, trying to make output voltage lower. If the feedback voltage exceeds the OVP threshold and the output voltage exceeds the bypass switch OVP voltage for the OVP delay time, the protection will be triggered, and the buck converter will be disabled and enter latch off state. Cycle EN2 or EN1 input to re-enable the buck converter. False OVP triggers may happen under USM light load conditions, if the inductance value is chosen too low.

**Buck Over Temperature Protection (OTP)**

The buck converter includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. When the thermal sensor detects a junction temperature exceeding 150°C, the over temperature protection (OTP) will be triggered, and the buck converter will be disabled and enter a latch off state. In this case the LDO is not disabled. Cycle EN2 or EN1 to re-enable the buck converter after the junction temperature cools down about 15°C. For continuous operation, provide adequate thermal dissipation so that the junction temperature does not exceed the OTP threshold.

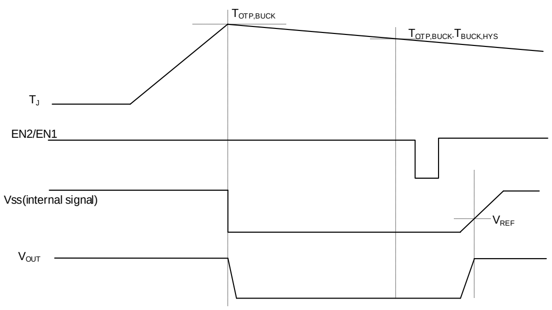



*Figure11. Over Temperature Protection*

**LDO Output Current Limit**

The device features LDO current limit to guarantee LDO safe operation in all operating conditions. When the LDO output voltage is less than the target value after LDO is turned on, the internal LDO regulator or bypass switch will operate in current limit mode until the LDO output voltage is reaches the target. For example, when a LDO output short circuit occurs, the LDO will operate in a current limit mode. The LDO will switch to normal operation after the short circuit condition is removed.

**LDO Over Temperature Protection**

The device also features auto-recovery mode LDO over temperature protection to guarantee LDO safe operation when under increased power dissipation. When the LDO thermal sensor detects that the junction temperature exceeds 160°C, the LDO will be turned off. When the junction temperature cools down by approximately 25°C, the LDO will be turned on and the buck converter will also be recovered as experiencing once EN2 or EN1 input re-enabling.

## Design Procedure

**Buck Input Capacitor Selection**

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce EMI. When selecting the input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems which are powered by a wall adapter or a long inductive cable may be susceptible to significant inductive ringing at the input of the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce input overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current,

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification. Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications a single 10μF X5R capacitor is sufficient. Place the ceramic input capacitor as close to the device's IN and GND pin as possible.

**Buck Inductor Selection**

The inductor is necessary to supply constant current to the output load while being driven by the LX node.

The buck converter operates well over a wide range of inductance values. This flexibility allows for optimization to find the best trade-off between efficiency, cost and size for a particular application. Selecting a low inductance value will help reduce size and cost and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low inductance value inductors may help reduce DC losses and increase efficiency. Choosing higher inductance value inductors tend to have higher DCR and will slow down transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current ($\Delta I_L$) about 20% ~ 50% of the desired full output load current. Start calculating the approximate inductance value by selecting the input and output voltages, the operating frequency ($f_{SW}$), the maximum output current ($I_{OUT,MAX}$) and estimating a $\Delta I_L$ as some percentage of that current.

$$\mathrm{L} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current ($\Delta I_L$) and required peak current inductor current $I_{L,PEAK}$.

$$\Delta \mathrm{I_L} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$\mathrm{I}_{L,PEAK} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

If USM light load operation is selected, make sure the inductance value is high enough to avoid reverse current limit is been triggered just under steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Selecting low loss ferrite materials is recommended.

**Buck Inductor Design Example**

Consider a typical design for a buck converter providing $3.338V_{OUT}$ at 8A from $12V_{IN}$, operating at 600kHz and using target inductor ripple current ($\Delta I_L$) of 40% or 3.2A.

First, determine the approximate inductance value:

$$\mathrm{L} = \frac{3.338V \times (12V - 3.338V)}{12V \times 600kHz \times 3.2A} = 1.25\mu H$$

Next, select the nearest standard inductance value, in this case 1.5µH, and calculate the resulting inductor ripple current ($\Delta I_L$):

$$\Delta \mathrm{I}_L = \frac{3.338V \times (12V - 3.338V)}{12V \times 600kHz \times 1.5\mu H} = 2.68A$$

$$\mathrm{I}_{L,PEAK} = 8A + \frac{2.68A}{2} = 9.34A$$

The resulting 2.68A ripple current is 2.68A/8A is ~33.5%, which is within the 20% ~ 50% target.

$$\mathrm{I}_{L,PEAK,RVS} = \frac{2.68A}{2} = 1.34A < I_{LMT,RVS}$$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 9.34A.

**Buck Output Capacitor Selection**

The buck converter provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

**Buck Steady State Output Ripple**

Steady state output voltage ripple at the switching frequency is caused by the inductor current ripple ($\Delta I_L$) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,\ ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,\ CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with $\Delta I_L$ = 2.68A using three 22µF ceramic capacitors, each with an ESR of ~6mΩ for parallel total of 66µF and 2mΩ ESR.

$$V_{RIPPLE,\ ESR} = 2.68A \times 2m\Omega = 5.36mV$$

$$V_{RIPPLE,\ CAP} = \frac{2.68A}{8 \times 66\mu F \times 600kHz} = 8.46mV$$

Total ripple = 13.82mV. The actual capacitive ripple may be higher than calculated value because the capacitance decreases with the voltage on the capacitor.

Using a 150µF 40mΩ POS cap, the above result is

$$V_{RIPPLE,\ ESR} = 2.68A \times 40m\Omega = 107.20mV$$

$$V_{RIPPLE,\ CAP} = \frac{2.68A}{8 \times 150\mu F \times 600kHz} = 3.72mV$$

Total ripple = 110.92mV.

**Buck Output Transient Undershoot/Overshoot**

If very fast load transient must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions, however, for good performance specific considerations must be addressed, especially when using small ceramic capacitors which have low capacitance at low output voltages, which results in insufficient stored energy for load transients. Output transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as

$$V_{ESR} = \Delta I_{OUT} \times ESR$$

Using the ceramic capacitor example above and a fast load transient of ± 4A, $V_{ESR}$ = ± 4A × 2mΩ = ± 8mV. The POS capacitor result with the same load transient, $V_{ESR}$ = ± 4A × 40mΩ = ± 160mV.

Capacitive undershoot (load increasing) is a function of the output capacitance, the load step, the inductor value and the input-output voltage difference and the maximum duty cycle factor. During a fast load transient, the maximum duty cycle of the buck converter is a function of $t_{ON}$ and the $t_{OFF,MIN}$, as the control scheme is designed to rapidly ramp the inductor current by grouping together many $t_{ON}$ pulses in this case. The maximum duty factor $D_{MAX}$ may be calculated by

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated by

$$V_{UNDERSHOOT,CAP} = -\frac{L \times \Delta I^2{}_{OUT}}{2 \times C_{OUT} \times \left(V_{IN,MIN} \times D_{MAX} - V_{OUT}\right)}$$

Consider a 4A load increase using the ceramic capacitor case when $V_{IN}$ = 12V. At $V_{OUT}$ = 3.338V, the result is $t_{ON}$ = 464ns, $t_{OFF,MIN}$ = 150ns, $D_{MAX}$ = 464 / (464 + 150) = 0.755 and

$$V_{UNDERSHOOT,CAP} = -\frac{1.5\mu H \times (4A)^2}{2 \times 66\mu F \times (12V \times 0.755 - 3.338V)} = -31.78mV$$

Using the POS capacitor in the above example, the result is:

$$V_{UNDERSHOOT,CAP} = -\frac{1.5\mu H \times (4A)^2}{2 \times 150\mu F \times (12V \times 0.755 - 3.338V)} = -13.98mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L \times \Delta I^2{}_{OUT}}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 4A load decrease using the ceramic capacitor case above. At $V_{OUT}$ = 3.338V the result is

$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (4A)^2}{2 \times 66\mu F \times 3.338V} = 54.47mV$$

Using the POS capacitor case, the above result is

$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (4A)^2}{2 \times 150\mu F \times 3.338V} = 23.97mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application. If the system requirements are not met, recalculate with a different configuration.

**Load Transient Considerations**

The device uses the COT ripple-based control strategy to achieve good stability and fast transient response. In applications with high step load current, adding an RC network $R_{FF}$ and $C_{FF}$ between the OUT pin and the FF pin may further speed up the load transient response. $R_{FF}$ = 1kΩ and $C_{FF}$ = 470pF have been shown to perform well in most applications. Increasing $C_{FF}$ will speed up the load transient response if there is no stability issue.

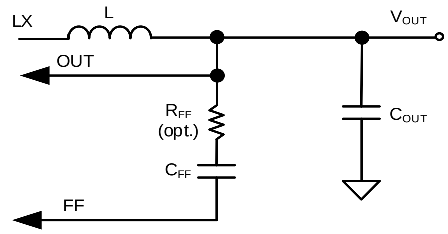



*Figure12. Feedforward Network*

Note: For $C_{OUT}$ > 500µF and when the minimum load current is low, use feedforward values of $R_{FF}$ = 1kΩ and $C_{FF}$ = 2.2nF to provide sufficient ripple to FB node for low output ripple and good transient behavior.

**Thermal Design Considerations**

Maximum power dissipation depends on the thermal resistance of the device package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}}$$

Where, $T_{J,MAX}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction to ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125℃. The junction to ambient thermal resistance $\theta_{JA}$ is layout dependent. For the QFN2.5×2.5-16 package the thermal resistance $\theta_{JA}$ is 33ºC/W when measured on a standard Silergy 8.5cm×8.5cm size four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz copper traces connected to each device pin and very large, unbroken 1-oz internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the device backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at $T_A$=25℃ may be calculated by the following formula:

$$P_{D,MAX} = \frac{125℃ - 25℃}{33℃/W} = 3W$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance $θ_{JA}$. Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.

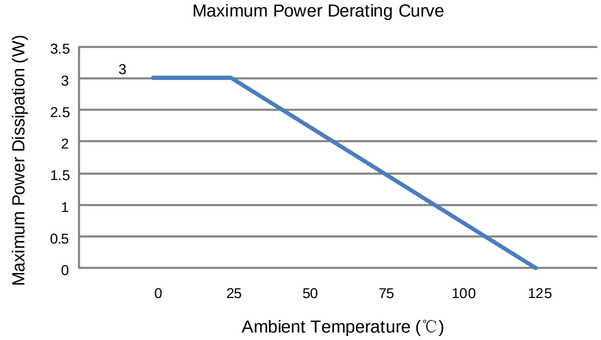
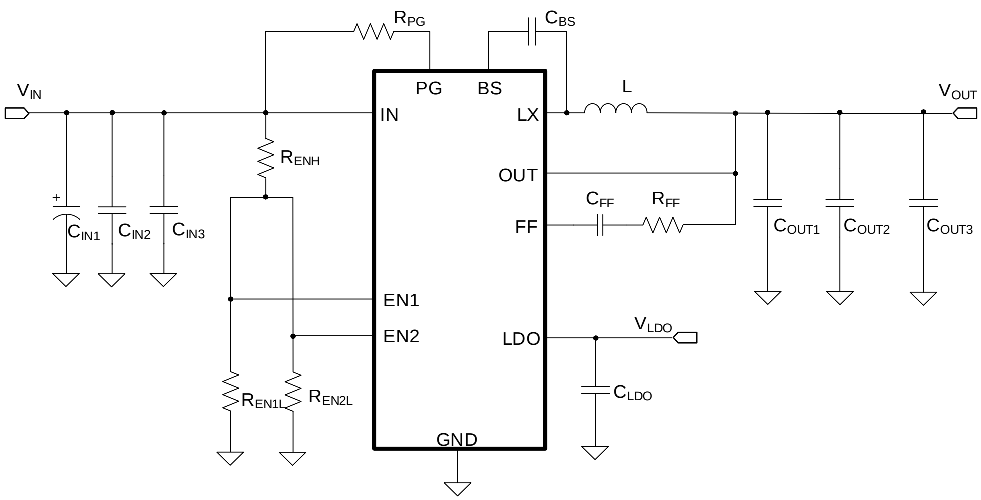



*Figure13. Maximum Power Derating Curve*

## Application Schematic ($V_{OUT}$ = 3.338V)




## BOM List

| Designator | Description | Part Number | Manufacturer |
|---|---|---|---|
| $C_{IN1}$ | 47µF/50V, Electrolytic Cap | | |
| $C_{IN2}$ | 10µF/50V/X5R, 1206 | GRM31CR61H106KA12L | mµRata |
| $C_{IN3}$, $C_{BS}$ | 0.1µF/50V/X5R, 0603 | GRM188R61H104KA93D | mµRata |
| $C_{OUT1}$, $C_{OUT2}$, $C_{OUT3}$ | 22µF/16V/X5R, 1206 | GRM31CR61C226ME15L | mµRata |
| $C_{LDO}$ | 4.7µF/16V/X5R, 0603 | GRM185R61C475KE11D | mµRata |
| $C_{FF}$ | 470pF/50V/C0G,0603 | GRM1885C1H471JA01D | mµRata |
| L | 1.5µH/16A, inductor | PCMB104T-1R5MS | CYNTEC |
| $R_{ENH}$ | 10kΩ, 1%, 0603 | | |
| $R_{EN1L}$, $R_{EN2L}$ | 1MΩ, 1%, 0603 | | |
| $R_{PG}$ | 100kΩ, 1%, 0603 | | |
| $R_{FF}$ | 1kΩ, 1%, 0603 | | |

## Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

**Input Capacitors:** Place the input capacitor close to IN and GND pins, minimizing the loop formed by these connections. The capacitor should be connected to the IN and GND using a wide copper pour. A 0.1μF input ceramic capacitor is recommended to reduce the high-frequency noise.

**Output Capacitors:** Ensure that the $C_{OUT}$ negative sides are connected to GND using wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.

**LDO Capacitor:** Place the LDO capacitor close to LDO pin using a short, direct copper trace to the nearest GND pin (pin 14).

**Feedback Network and Output Line:** Place the feedback components ($R_{FF}$ and $C_{FF}$) as close to FF pin as possible. Avoid routing the feedback line near LX, BS or other high frequency signal as it is noise sensitive. Use a Kelvin connection for the feedback sampling point at $C_{OUT}$ rather than the inductor output terminal. The output trace width should be at least 20mil wide as it is also the 100mA LDO's bypass input.

**LX Connection:** Keep LX area small to prevent excessive EMI, while using a wide copper trace to minimize parasitic resistance and inductance. Wide LX copper trace between pin 5 and pin 15, 16 should be used to improve efficiency.

**BS Capacitor:** Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX and $C_{BS}$) as short as possible.

**Control Signals:** It is not recommended to connect control signals to $V_{IN}$ or another voltage source directly. A resistor in a range of 1kΩ to 1MΩ should be used if they are pulled high.

**GND Vias:** Place adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected by a larger copper area than its size, place four GND vias on it for heat dissipation.

**PCB Board:** A four-layer layout with 2-oz copper is strongly recommended to achieve better thermal performance. The top layer and bottom layer should place power IN and GND copper area as wide as possible. Middle1 layer should be used as a GND layer for conducting heat and shielding the middle2 layer signal lines from top layer crosstalk. Place signal lines on middle2 layer instead of the other layers, so that the other layers' GND plane is not cut by signal lines.

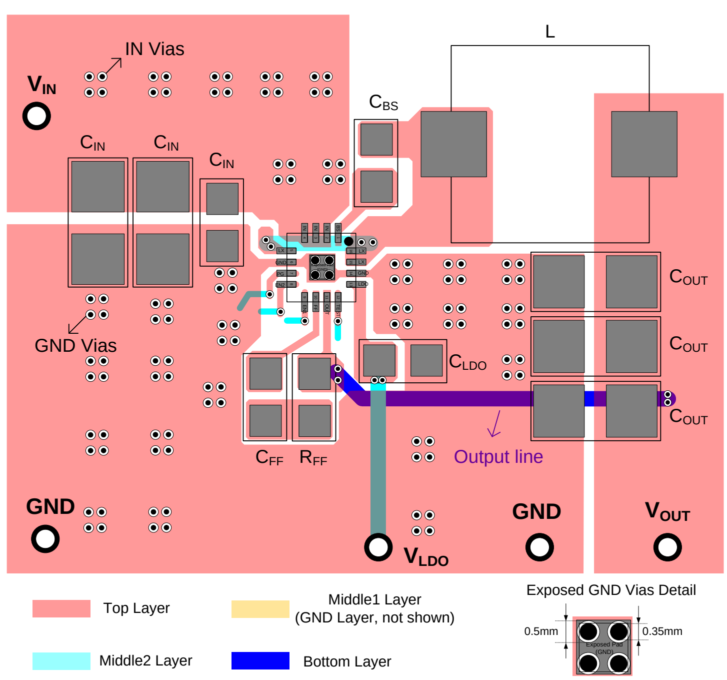
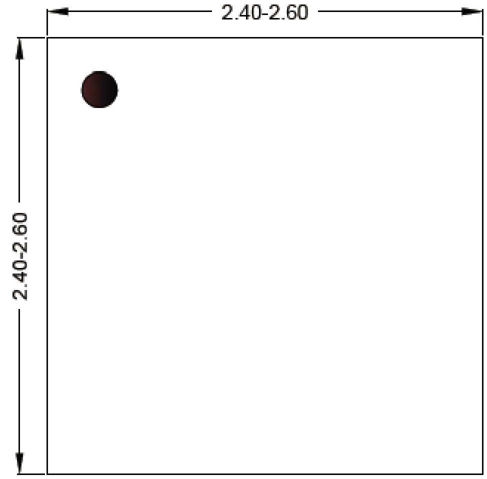
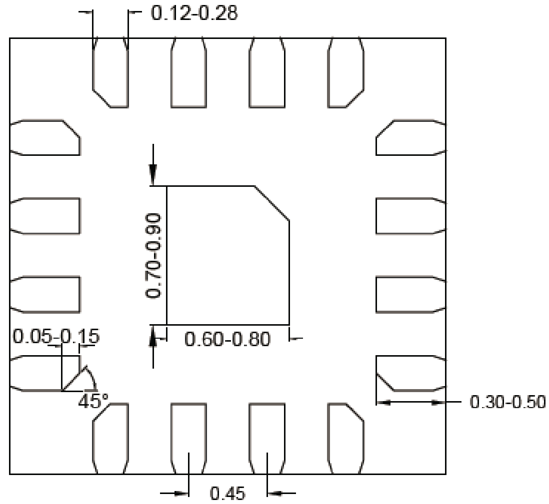



*Figure14. PCB Layout Suggestion*

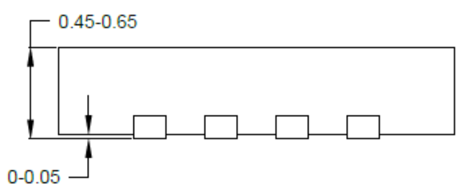
## QFN2.5×2.5-16 Package Outline Drawing



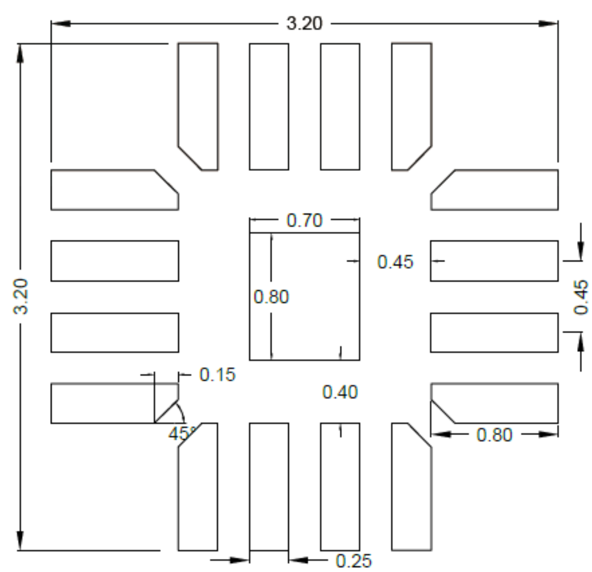

Top view




Bottom view




Side view

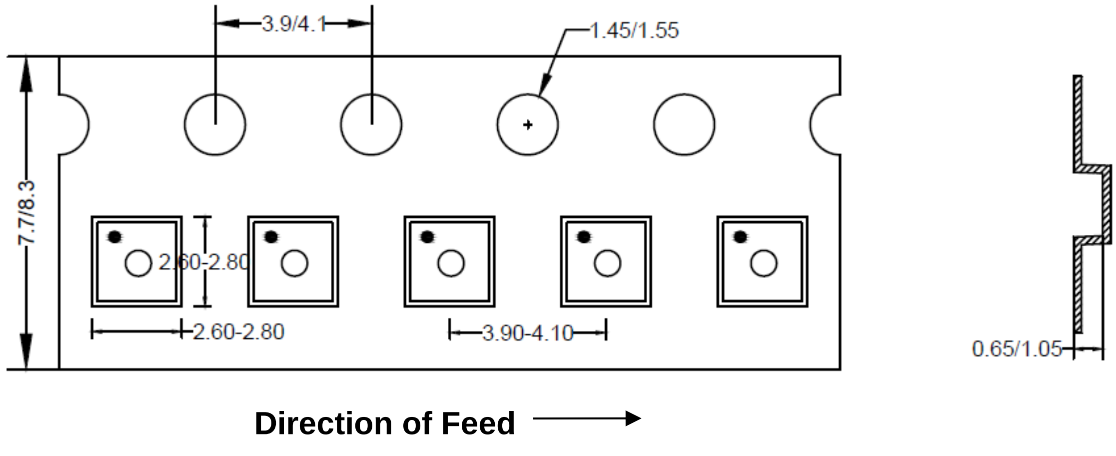



Recommended PCB layout (Reference only)

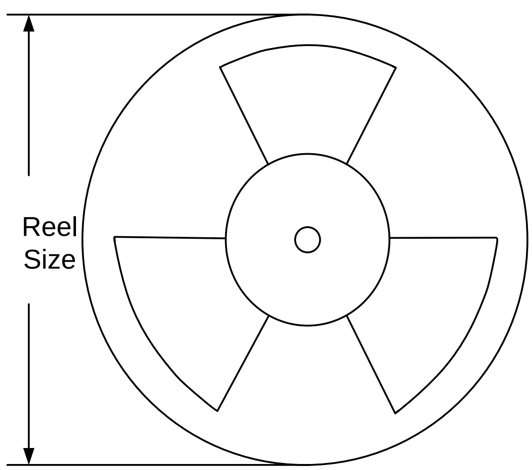
*Notes: All dimension in millimeter and exclude mold flash & metal burr.*

## Tape and Reel Information

### 1. Tape Dimensions and Pin1 Orientation




### 2. Reel Dimensions




| Package types | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|---|---|---|---|---|---|---|
| QFN2.5×2.5 | 8 | 4 | 7” | 400 | 160 | 3000 |

# Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

| Date | Revision | Change |
|---|---|---|
| Aug. 23, 2024 | Revision 1.0 | Initial Release |

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