SY21288A

High Efficiency Fast Response, 8A, 24V Input Synchronous Buck Converter

General Description

The SY21288A is a high efficiency synchronous buck converter operating over a wide input voltage range of 4V to 24V and capable of delivering up to 8A current. It integrates low $R_{DS(ON)}$ top and bottom MOSFETs to minimize the conduction loss. It operates at a pseudo-constant frequency of 600kHz, to enable the use of small size inductor and capacitors. The SY21288A also integrates a bypass switch which allows the VCC to be powered by external 3.3V power supply, further reduce the power consumption of the entire system.

Silergy's constant on-time and ripple-based control strategy supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation, including when using low ESR output ceramic capacitors.

The SY21288A provides cycle-by-cycle current limit, input under voltage lockout, internal soft-start, output under voltage protection, over voltage protection and over temperature protection, to guarantee safe operation in all operating conditions.

Features

- Low $R_{DS(ON)}$ for Internal MOSFETs: 20mΩ Top, 10mΩ Bottom
- Wide Input Voltage Range: 4V ~ 24V
- Adjustable Output Voltage: 0.6V ~ 12.5V
- Large Duty Cycle On-Time Stretch
- 8A Continuous Output Current Capability
- 600kHz Pseudo-Constant Frequency
- ±1% Internal Reference Voltage
- Internal 1ms Soft-Start Limits the Inrush Current
- Constant On-Time and Ripple-Based Control to Achieve Fast Transient Responses
- Integrated 1.5Ω Bypass Switch
- PFM/FCCM Selectable Light Load Operation Mode
- Power Good Indicator
- Output Auto-Discharge Function
- Programmable Valley Current Limit Threshold by ILMT Pin
- Cycle-by-Cycle Valley and Peak Current Limit Protection
- Hic-Cup Mode Output Under Voltage Protection
- Auto-Recovery Mode Output Over Voltage Protection
- Auto-Recovery Mode Over Temperature Protection
- Input Under Voltage Lockout (UVLO)
- RoHS Compliant and Halogen Free
- Compact Package: QFN2.5×2.5-16

Applications

- LCD-TV/Net-TV/3D-TV
- Set Top Box
- Notebook
- High Power AP

Typical Application

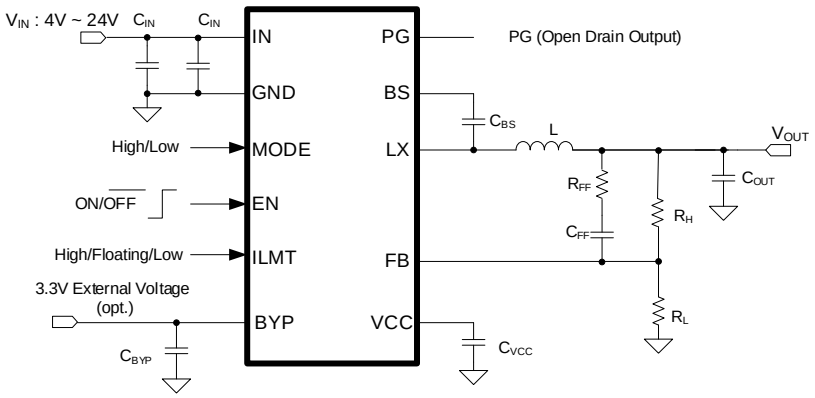


Figure1. Schematic Diagram

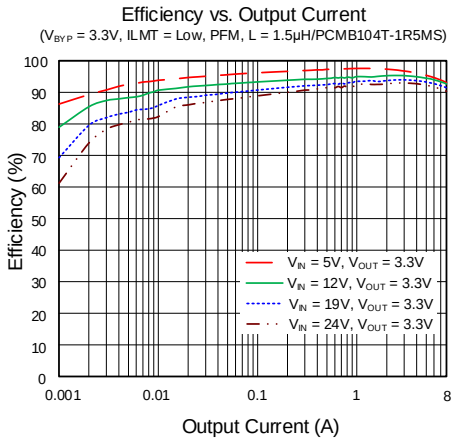


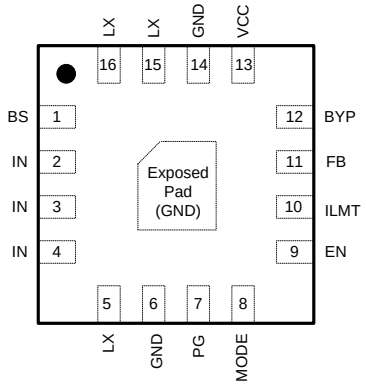
Figure2. Efficiency vs. Output Current

Ordering Information

Ordering Number	Package type	Top Mark
SY21288ARHC	QFN2.5×2.5-16 RoHS Compliant and Halogen Free	**GBBxyz**

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	BS	Bootstrap pin. Supply top MOSFET gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
2, 3, 4	IN	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor. A 0.1μF ceramic capacitor placed in parallel is recommended to reduce high frequency noise.
5, 15, 16	LX	Inductor pin. Connect this pin to the switching node of the inductor.
6, 14, EP	GND	Ground pin.
7	PG	Power good indicator pin. PG pin should be connected to V_{IN} or another voltage source through a resistor (e.g., 10kΩ ~ 100kΩ). This pin becomes high when the output voltage is within 90% to 120% of regulated value under normal operation.
8	MODE	Light load operation mode selection pin. Pull this pin low for PFM operation and pull this pin high for FCCM operation. Do not leave this pin floating.
9	EN	Enable control pin of the device. Pull high to turn on. Pull low to turn off. Do not leave this pin floating.
10	ILMT	Valley current limit threshold selection pin. See Table1 to find more details.
11	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider as shown in Figure 1. $V_{OUT} = 0.6 \times (1 + R_H/R_L)$.
12	BYP	External 3.3V bypass power supply input pin. Decouple this pin to ground with a 1μF ceramic capacitor. Make one good RC filter for BYP input if the 3.3V external power ripple is large. Leave this pin floating or connect this pin to the ground if it is not used.
13	VCC	Internal 3.3V LDO output pin. Power supply for internal analog circuits. Decouple this pin to GND with at least a 2.2μF ceramic capacitor.

Block Diagram

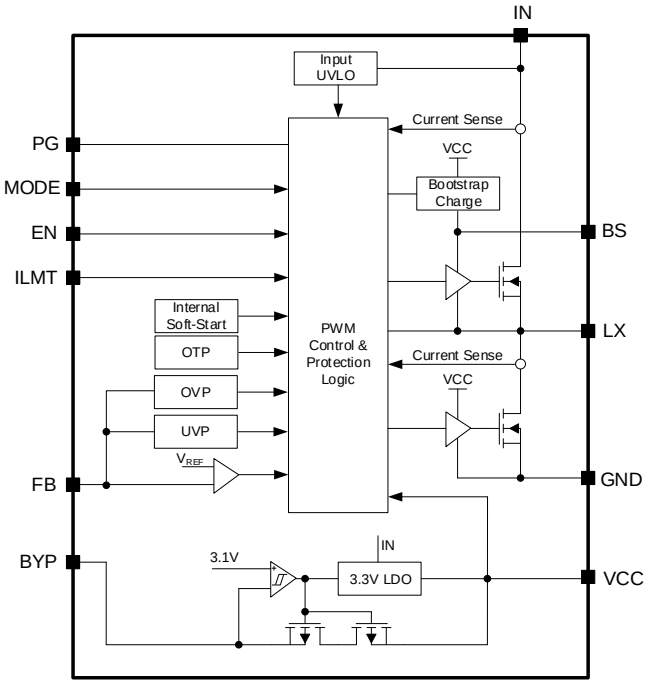


Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
IN	-0.3	26	V
IN-LX, LX, PG, EN, MODE	-0.3	IN + 0.3	
BS-LX, ILMT, VCC	-0.3	4	
FB, BYP	-0.3	6	
LX, 10ns Duration	GND - 5	IN + 3	
LX, 20ns Duration	GND - 1	IN + 2	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	33	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	5.5	
P_D Power Dissipation T_A = 25°C	3	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
Input Voltage	4	24	V
Output Voltage	0.6	12.5	
Continuous Output Current		8	A
Ambient Temperature	-40	85	°C
Junction Temperature	-40	125	

Electrical Characteristics

(V_{IN} = 12V, C_{OUT} = 66µF, C_{FF} = 220pF, R_{FF} = 1kΩ, T_J = 25°C, I_{OUT} = 1A unless otherwise specified (note4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	V_{IN}		4		24	V
	UVLO Rising Threshold	$V_{IN,UVLO}$	V_{IN} rising			3.9	
	UVLO Hysteresis	$V_{IN,HYS}$			0.3		
	Quiescent Current	I_Q	PFM, EN = High, V_{OUT} = V_{SET} × 105%		160		µA
	Shutdown Current	I_{SHDN}	EN = Low		4	9	
Output	Voltage Range	V_{OUT}		0.6		12.5	V
	Feedback Reference Voltage	V_{REF}		0.594	0.600	0.606	
	FB Input Current	I_{FB}	V_{FB} = 1V	-50		50	nA
	Discharge Current	I_{DIS}	V_{OUT} = 5V		100		mA
	Soft-Start Time	t_{SS}	V_{FB} from 0% to 100% V_{REF} (Note5)		1		ms
	OVP Threshold	V_{OVP}	V_{FB} rising	115	120	125	%V_{REF}
	OVP Hysteresis	$V_{OVP,HYS}$			5		
	OVP Delay Time	$t_{OVP,DLY}$	(Note5)		30		µs
	UVP Threshold	V_{UVP}	V_{FB} falling	55	60	65	%V_{REF}
	UVP Delay Time	$t_{UVP,DLY}$	(Note5)		200		µs
MOSFETs	Top MOSFET $R_{DS(ON)}$	$R_{DS(ON),TOP}$			20		mΩ
	Bottom MOSFET $R_{DS(ON)}$	$R_{DS(ON),BOT}$			10		
	Top MOSFET Current Limit Threshold	$I_{LMT,TOP}$			22		A
	Bottom MOSFET Current Limit Threshold	$I_{LMT,BOT}$	ILMT = Low	8			
			ILMT = Floating	12			
			ILMT = High	16			
	Bottom MOSFET Reverse Current Limit Threshold	$I_{LMT,RVS}$	FCCM mode	3	4.8		
Enable (EN)	Input Voltage High	$V_{EN,H}$		1			V
	Input Voltage Low	$V_{EN,L}$				0.4	
	Input Current	I_{EN}	V_{EN} = 3.3V			1	µA
	De-Glitch Time	$t_{EN,DG}$	(Note5)		40		µs
MODE	Voltage for PFM Mode	$V_{MODE,PFM}$		0		0.4	V
	Voltage for FCCM Mode	$V_{MODE,FCCM}$		1		V_{IN}	
	Input Current	I_{MODE}	V_{MODE} = 3.3V			1	µA
ILMT	Input Voltage High	$V_{ILMT,H}$	(Note5)	2.5			V
	Input Voltage Low	$V_{ILMT,L}$	(Note5)			0.4	
Frequency	Switching Frequency	f_{SW}	V_{OUT} = 5V, CCM	510	600	690	kHz
	Minimum On-Time	$t_{ON,MIN}$			50		ns
	Minimum Off-Time	$t_{OFF,MIN}$			150		

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Power Good (PG)	Rising Threshold	$V_{PG,R}$	V_{FB} rising (good)	87	90	93	%V_{REF}
	Falling Threshold	$V_{PG,F}$	V_{FB} falling (not good)	80	83	86	
	Delay Time	$t_{PG,R}$	Low to high (Note5)		200		μs
		$t_{PG,F}$	High to low (Note5)		30		
		$t_{PG,OFF}$	IC shuts down (Note5)			0.5	
	Low Voltage	$V_{PG,LOW}$	V_{FB} = 0V, I_{PG} = 5mA			0.45	V
VCC	Output Voltage	V_{CC}	VCC adds 1mA load	3.15	3.3	3.45	
BYP	$R_{DS(ON)}$	$R_{DS(ON),BYP}$			1.5		Ω
	Turn On Voltage	V_{BYP}		2.97	3.1		V
	Turn On Hysteresis	$V_{BYP, HYS}$			0.2		
	OVP Voltage	$V_{BYP, OVP}$			120		%V_{CC}
OTP	Temperature	T_{OTP}	T_J rising (Note5)		150		°C
	Temperature Hysteresis	T_{HYS}	T_J falling (Note5)		15		

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a 8.5cm×8.5cm size, four-layer Silergy Evaluation Board with 2-oz copper.

Note 3: The device is not guaranteed to function outside its operating conditions.

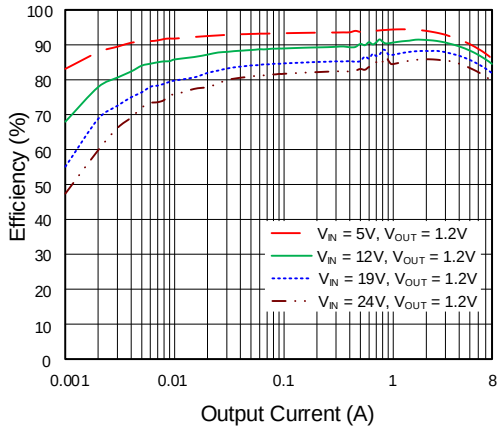
Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design.

Typical Performance Characteristics

(SY21288A, T_A = 25°C, V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5μH, C_{OUT} = 66μF, C_{FF} = 220pF, R_{FF} = 1kΩ, unless otherwise noted)

Efficiency vs. Output Current
(V_{BYP} = 3.3V, ILMT = Low, PFM, L = 1.0μH/PCMB104T-1R0MT)



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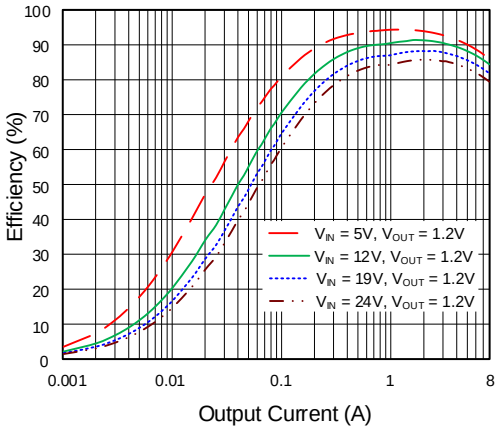

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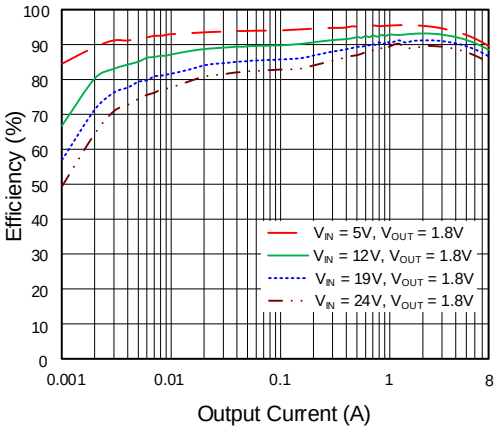

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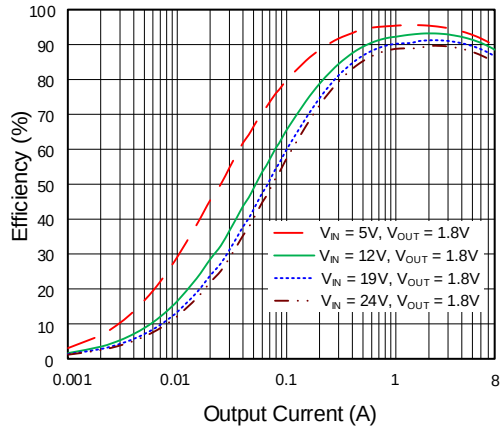
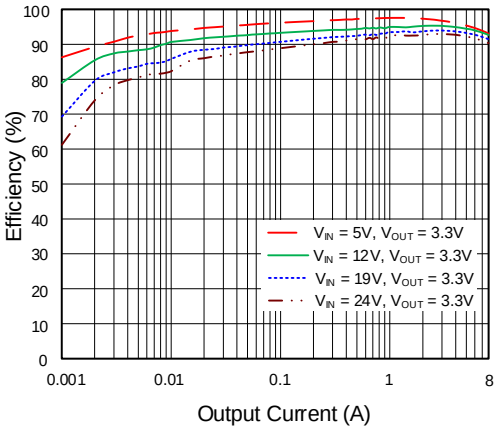
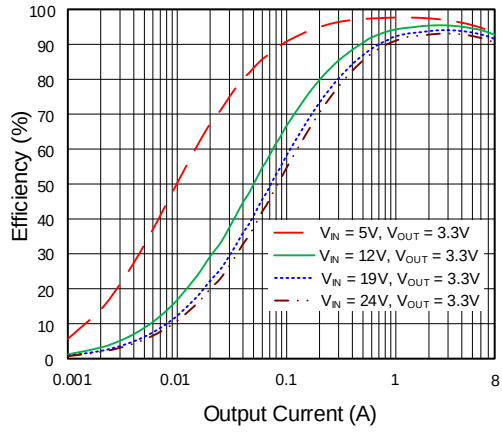


Efficiency vs. Output Current
(V_{BYP} = 3.3V, ILMT = Low, PFM, L = 1.5μH/PCMB104T-1R5MS)

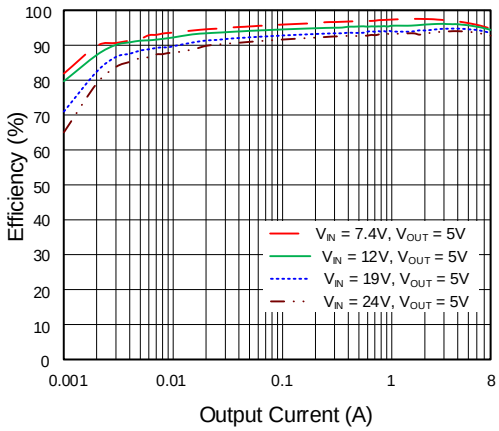


Efficiency vs. Output Current
(V_{BYP} = 3.3V, ILMT = Low, FCCM, L = 1.5μH/PCMB104T-1R5MS)



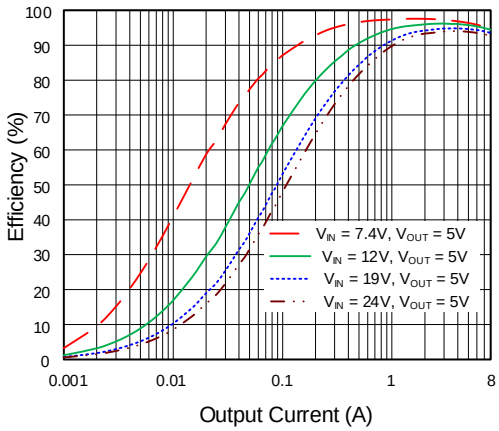
Efficiency vs. Output Current

(V_{BYP} = 3.3V, ILMT = Low, PFM, L = 1.5μH/PCMB104T-1R5MS)



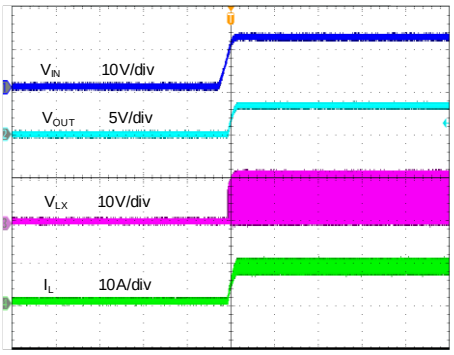
Efficiency vs. Output Current

(V_{BYP} = 3.3V, ILMT = Low, FCCM, L = 1.5μH/PCMB104T-1R5MS)



Startup from V_{IN}

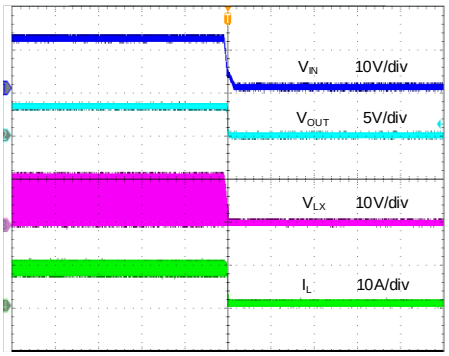
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 8A)



Time (4ms/div)

Shutdown from V_{IN}

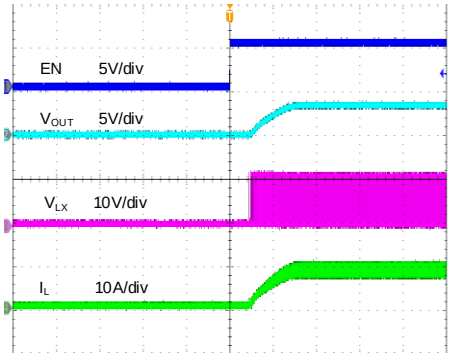
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 8A)



Time (4ms/div)

Startup from EN

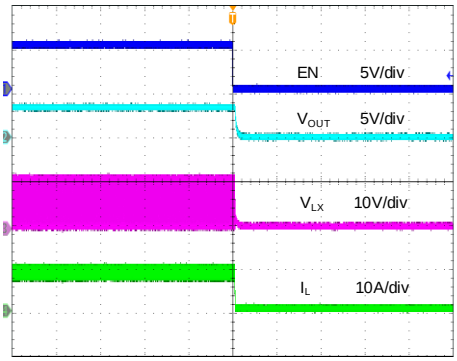
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 8A)



Time (800μs/div)

Shutdown from EN

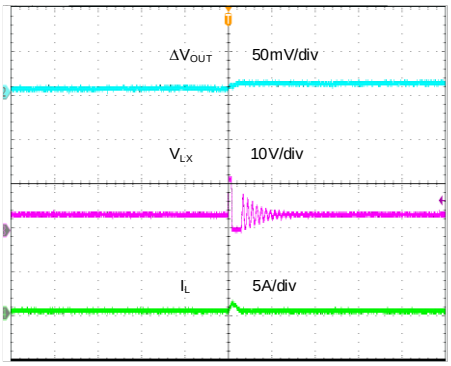
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 8A)



Time (800μs/div)

Output Ripple

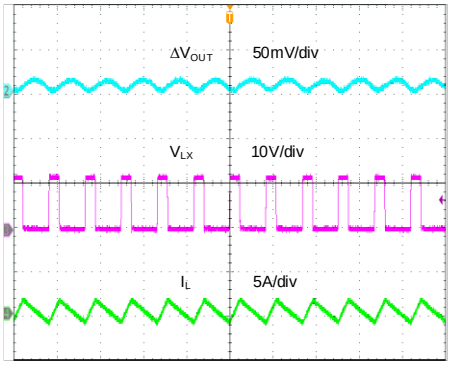
(V_{IN} =12V, V_{OUT} = 3.3V, I_{OUT} = 0A, PFM)



Time (2μs/div)

Output Ripple

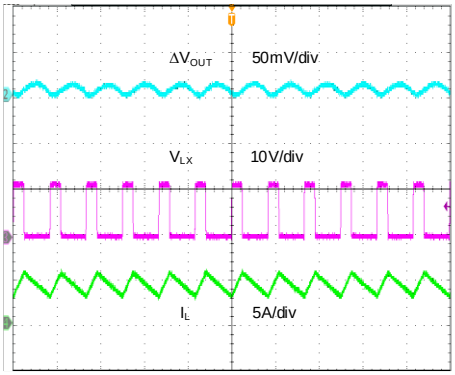
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A, FCCM)



Time (2μs/div)

Output Ripple

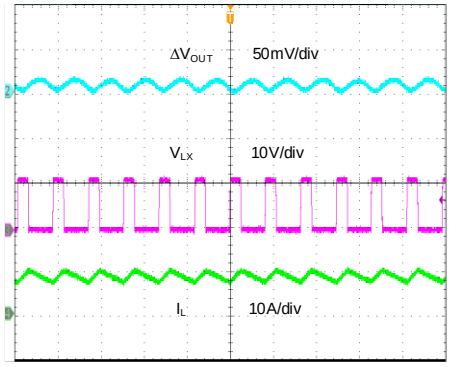
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 4A)



Time (2μs/div)

Output Ripple

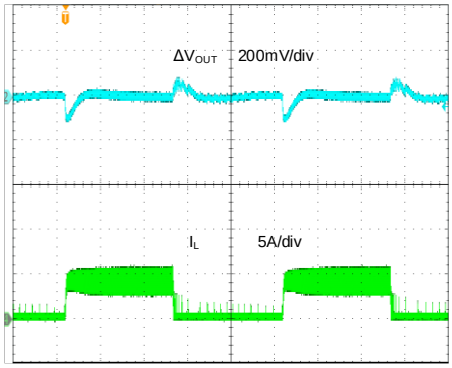
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 8A)



Time (2μs/div)

Load Transient

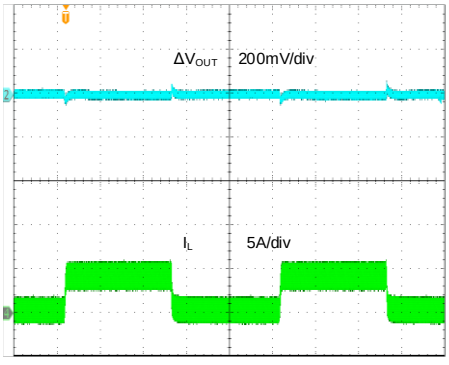
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0 ~ 4A, PFM)



Time (200μs/div)

Load Transient

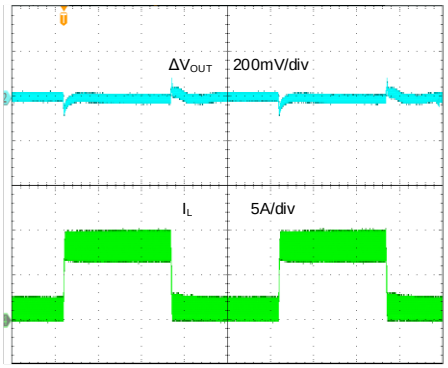
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0 ~ 4A, FCCM)



Time (200μs/div)

Load Transient

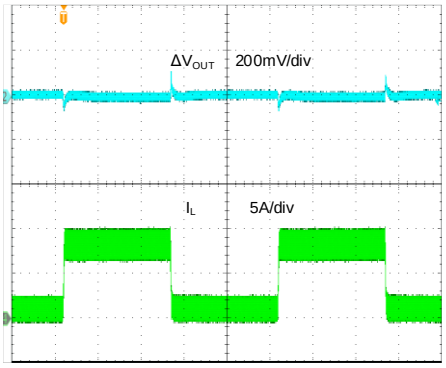
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0.8 ~ 8A, PFM)



Time (200μs/div)

Load Transient

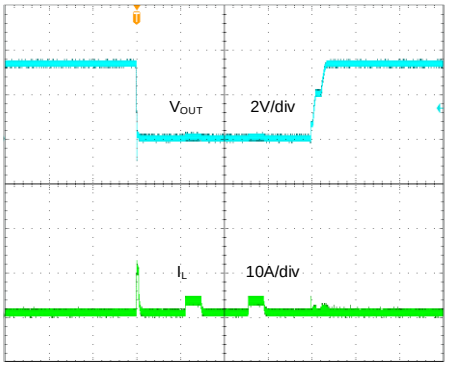
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0.8 ~ 8A, FCCM)



Time (200μs/div)

Short Circuit Protection

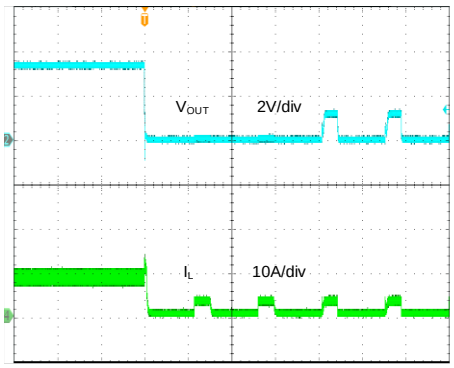
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A~Short, ILMT=Low, PFM)



Time (4ms/div)

Short Circuit Protection

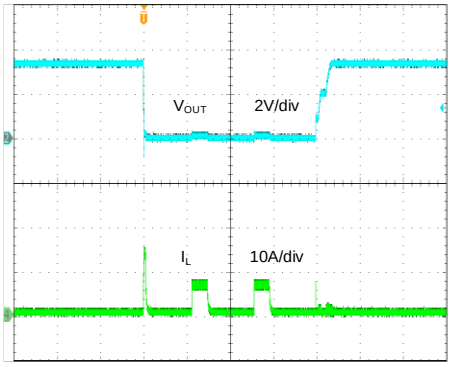
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=8A~Short, ILMT=Low)



Time (4ms/div)

Short Circuit Protection

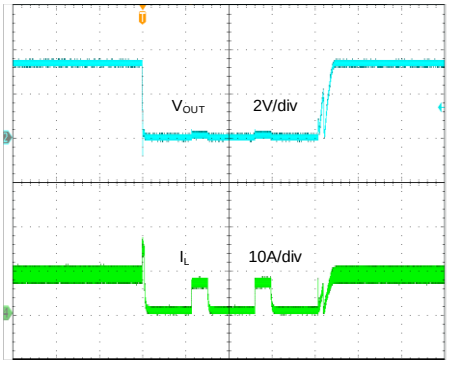
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A~Short, ILMT=Floating, PFM)



Time (4ms/div)

Short Circuit Protection

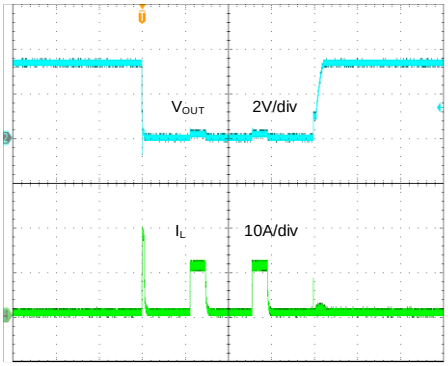
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=8A~Short, ILMT=Floating)



Time (4ms/div)

Short Circuit Protection

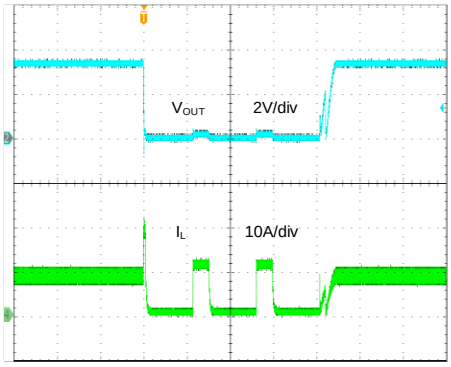
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A~Short, ILMT=High, PFM)



Time (4ms/div)

Short Circuit Protection

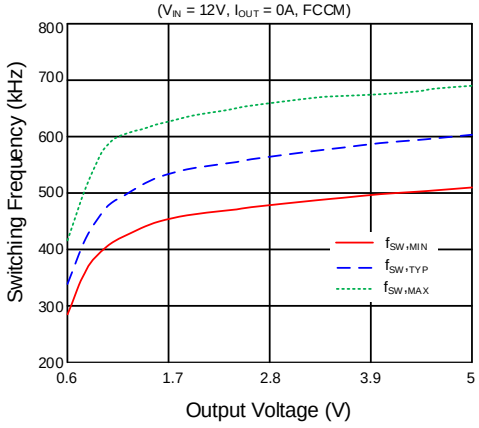
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=8A~Short, ILMT=High)



Time (4ms/div)

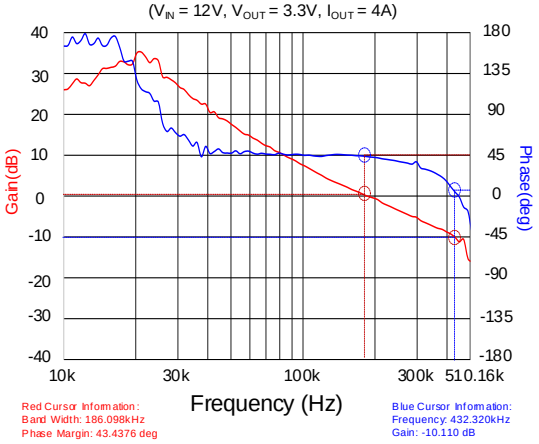
Switching Frequency vs. Output Voltage

(V_{IN} = 12V, I_{OUT} = 0A, FCCM)



Bode Plot

(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 4A)



Detailed Description

General Features

Constant On-Time Architecture

Fundamental to any constant on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the top MOSFET. Each on-time (t_{ON}) is a "fixed" voltage ratio,

$$t_{ON} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f_{SW}}\right)$$

For example, considering that a hypothetical converter targets 3.3V output from a 12V input at 600kHz, the target on-time is

$$\frac{3.3\text{V}}{12\text{V}} \times \frac{1}{600\text{kHz}} = 458\text{ns}$$

Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FB node drops below the regulated value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is lower than the regulated value. This approach avoids making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

In a COT architecture, there is no fixed clock, so the top MOSFET can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays.

Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for small duty cycle, since at very low duty cycle operation, once the on-time is close to the minimum on time, the switching frequency can be reduced as needed to always ensure a proper operation.

Under T_J = -40℃ ~ 125℃ condition, the device can support adjustable output and up to 98% duty cycle operation.

In order to convert output voltage under large duty cycle operation, the t_{ON} can be stretched to extend the duty cycle as much as it needs. When the device detects feedback voltage is lower than the reference voltage under normal on-time operation and the on-time is greater than 50% normal switching period, the t_{ON} will be stretched. The maximum limitation of t_{ON} is 4 ~ 6 normal switching cycles. The on-time stretch function is disabled when the feedback voltage is less than the under voltage protection (UVP) threshold (after the delay time typical 20μs).

Instant-PWM Operation

Silergy's COT ripple-based control strategy adds several proprietary improvements to the traditional COT architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, instant-PWM control method derives this signal internally. Another improvement optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT converters may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor may become too small to maintain stable operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum off-time has been satisfied and the inductor current as measured in the bottom MOSFET is lower than its current limit threshold. As the t_{ON} pulse is triggered, the bottom MOSFET turns off and the top MOSFET turns on. The inductor current ramps up linearly during the t_{ON} period. At the end of the t_{ON} period, the top MOSFET turns off, the bottom MOSFET turns on, and the inductor current ramps down linearly. This action also initiates the minimum off-time timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum off-time is relatively short so that during fast speed load transients, t_{ON} can be retriggered with minimal delay, allowing the inductor current to ramp quickly and provide sufficient energy to the load side.

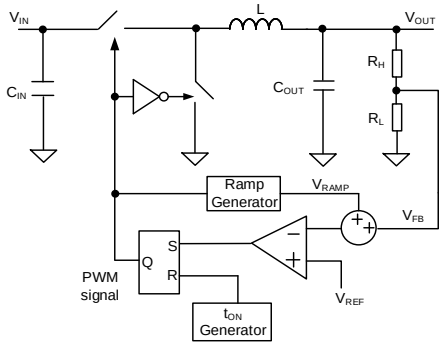


Figure4. Silergy's COT Ripple-based Control Strategy

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between turning the top MOSFET off and the bottom MOSFET on, as wells as between turning the bottom MOSFET off and the top MOSFET on.

Light Load Operation Mode Selection

PFM or FCCM light load operation is selected by MODE pin. Pull MODE pin low for pulse-frequency modulation (PFM) mode operation, and pull this pin high for forced continuous conduction mode (FCCM) operation.

If PFM light load operation is selected, under light load conditions, typically when the load satisfies the following equation,

$$I_{OUT\_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L} \quad (1)$$

the current through the bottom MOSFET will ramp to near zero before the next t_{ON} time. When this occurs, the bottom MOSFET turns off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, the combined feedback and ramp signals remain much higher than the reference voltage, the instant-PWM control loop will not trigger another t_{ON} until needed, and the apparent operating switching frequency will correspondingly drop, improving efficiency. The switching frequency can be lower than audible frequency area under deep light load or null load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the *inductor* current to remain above zero at the time of the next t_{ON} cycle. The buck converter enters CCM once the load current exceeds the threshold shown in (1). Above the threshold, the switching frequency stays fairly constant over the output current range.

If FCCM light load operation is selected, under light load conditions, the bottom MOSFET still turns on even when the inductor current crosses zero. Current flow will continue until the next t_{ON} cycle appears. The buck converter always operates under continuous conditions mode and keeps fairly constant switching frequency over all the output current range.

Input Under Voltage Lockout (UVLO)

To prevent operation before the internal circuitry is ready and to ensure that the top and bottom MOSFETs can be properly driven, the device incorporates an input under voltage lockout protection.

The device remains in a low current state and LX node switching actions are inhibited until V_{IN} exceeds the UVLO rising threshold. At that time, if EN is high, the device is enabled and soft-start ramp is initiated. If V_{IN} falls below $V_{IN,UVLO}$ less than the input UVLO hysteresis, LX node switching actions will again be suppressed.

Increasing the default input UVLO threshold can be implemented using an external resistor divider connected to EN.

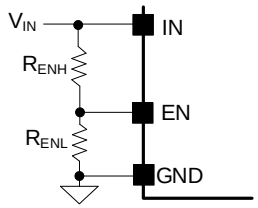


Figure5. Enable Control

Enable Control

The EN input is high-voltage capable inputs with logic-compatible threshold. EN logic high is defined as a voltage higher than 1V, and a logic low as a voltage lower than 0.4V. When the device is turned off, the shutdown current I_{SHDN} is below 9μA.

It is not recommended to connect EN pin to V_{IN} or another voltage source directly. A resistor in a range of 1kΩ to 1MΩ should be used for EN pin in this case.

Startup and Shutdown

The device incorporates an internal soft-start circuit to smoothly ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 1ms, which avoids high current flow and transients during startup. The startup and shutdown sequence is shown below.

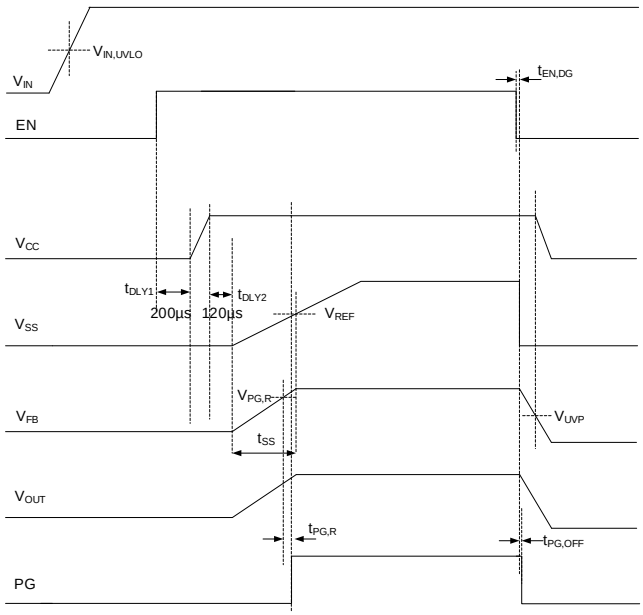


Figure6. Startup And Shutdown Sequence

After V_{IN} exceeds the UVLO rising threshold, the VCC is turned on after the delay time t_{DLY1} if EN is high, the buck converter is turned on after another delay time t_{DLY2} after VCC voltage is ready. When the output voltage is 90% of the regulated value, PG is set to the high-impedance state after the delay time $t_{PG,R}$.

The device supports startup with pre-biased output. If the output is pre-biased to a certain voltage before startup, the buck converter disables the switching of both the top MOSFET and the bottom MOSFET until the internal soft-start voltage V_{SS} exceeds the sensed output voltage at the FB node. The first pulse on-time is internally calculated based the input voltage and pre-biased output voltage.

PG Power Good Indicator

PG is an open drain output controlled by a window comparator connected to the feedback signal. If the voltage is higher than $V_{PG,R}$ and less than V_{OVP} for at least the power good delay time (low to high), PG will be set to high-impedance state.

PG should be connected to V_{IN} or another voltage source through a resistor (e.g., 100kΩ). After V_{IN} rises until the internal initial power is ready, the PG internal MOSFET is turned on so that PG is actively driven low before output voltage is ready. After the feedback voltage V_{FB} reaches $V_{PG,R}$, PG is set to high-impedance state after a delay time of 200μs (typ.). When V_{FB} drops to $V_{PG,F}$, or rises above V_{OVP} for the OVP delay time, PG is driven low after a delay time of 30μs (typ.).

Output Auto-Discharge Function

The device discharges the output voltage when the buck converter shuts down due to low V_{IN} or EN, or caused by a protection function being triggered, so that the output voltage can be discharged in a minimal time, even if the buck output load current is zero. The discharge MOFET in parallel with the bottom MOSFET turns on after the bottom MOSFET turns off when the shutdown logic is enabled. The output discharge current is typically 100mA for V_{OUT} = 5V. The discharge MOSFET is not active outside of these shutdown conditions.

External Bootstrap Capacitor Connection

This device integrates a floating power supply for the gate driver of the top MOSFET. Proper operation requires a 0.1μF low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the N-channel top MOSFET.

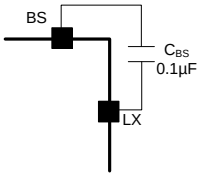


Figure7. Bootstrap Capacitor Connection

VCC Output

The device integrates a high performance, low drop-out linear regulator 3.3V VCC, which can power the internal gate drivers, PWM logic, analog circuitry and other blocks.

Once the input voltage exceeds its own UVLO (rising) threshold, and EN is high, VCC is turned on and supplied power by V_{IN}. After the BYP voltage exceeds BYP turn on voltage, the internal LDO regulator will be turned off and the bypass switch will be turned on so that VCC output can switch to BYP voltage to reduce power consumption. Connect a 2.2μF low ESR ceramic capacitor from VCC to GND. Make sure the loop formed by the VCC capacitor is shorter than the loop for the BYP capacitor, if there is placement conflict between them.

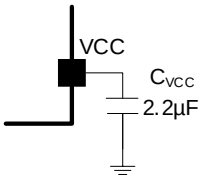


Figure8. VCC Capacitor Connection

BYP Input

When a 3.3V external power supply is connected to the BYP, the internal LDO is automatically turned off. The overall efficiency may be improved by using an external power supply. Connect a 1μF low ESR ceramic capacitor from BYP pin to GND. Using an external low pass filter consisting of a small value resistor R_{BYP} and a ceramic capacitor C_{BYP} is recommended for applications where the external power rail has significant ripple. Connect the pin to GND or leave floating if not used.

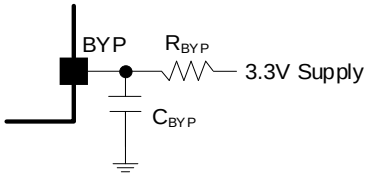


Figure9. BYP Low Pass Filter Connection

Fault Protection Modes

Output Current Limit

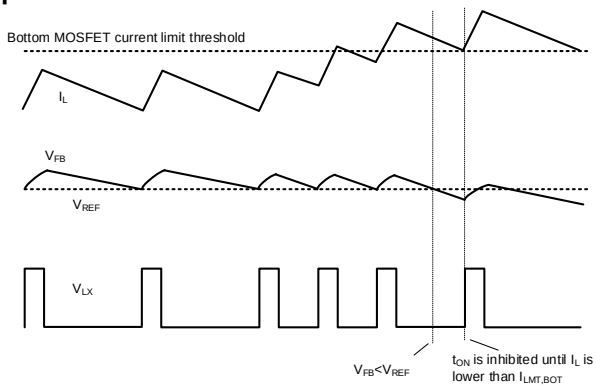


Figure10. Bottom Current Limit Protection

The buck converter features cycle-by-cycle “valley” current limit (bottom MOSFET current limit). The Inductor

current is monitored in the bottom MOSFET when it turns on and as the inductor current ramps down. If the monitored current is higher than current limit threshold, t_{ON} is inhibited until the current returns back to below the threshold.

The device supports programmable valley current limit threshold. Pull ILMT pin low, floating or high for 3 gears successively increasing valley current limit threshold. The detailed pin configuration is shown in table1. When the valley current limit occurs, the output current limit value is

$$I_{LMT,OUT} = I_{LMT,BOT} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

ILMT Gears	$I_{LMT,BOT}$	Recommended Table
ILMT = Low	≥8A	Pull ILMT to GND by ≤10kΩ Resistor
ILMT = Floating	≥12A	ILMT pin floating
ILMT = High	≥16A	Pull ILMT to VCC by ≤10kΩ Resistor

Table1: Programmable Valley Current Limit

The buck converter also features cycle-by-cycle peak current limit (top MOSFET current limit). During the t_{ON} time, the top MOSFET current is monitored. If it exceeds the current limit threshold, the MOSFET will be turned off, and the bottom MOSFET will be turned on. t_{ON} can be not inhibited when the bottom MOSFET current is lower than the bottom MOSFET current limit threshold.

Output Under Voltage Protection (UVP)

If V_{OUT} < ~60% of the regulated value for approximately 200µs occurring when the output short circuit or the load current is much heavier than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the buck converter will enter into hic-cup protection mode. The hic-cup on time is 1.5ms, and the hic-cup off time is 4.5ms. If the output fault conditions are removed, the buck converter will go back to normal operation in the nearest hic-cup on time.

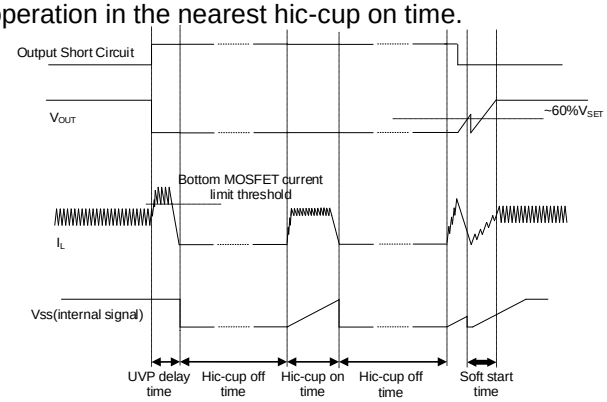


Figure11. Output Under Voltage Protection

To avoid output overshoot, the internal soft-start voltage V_{SS} should be pulled low for a while when V_{FB} exceeds UVP threshold if the output fault conditions are removed during hic-cup on time, then the V_{SS} will rise smoothly to ramp the output to the desired voltage during a new soft-start cycle.

Output Over Voltage Protection (OVP)

The buck converter includes output over voltage protection (OVP). If the feedback voltage rises above the reference voltage level, the top MOSFET naturally remains off and different actions are taken depending on the operation mode.

When operating in PFM light load mode, if the feedback voltage remains high, the bottom MOSFET remains on until the inductor current reaches zero and the LX node switching actions are suppressed. LX node switching actions will be recovered once the combined feedback and ramp signals become lower than the reference voltage.

When operating in FCCM light load mode, if the feedback voltage remains high, the bottom MOSFET turn on time will be longer and inductor current average value becomes more and more negative until the reverse current limit is triggered, trying to make output voltage lower. If the feedback voltage exceeds the OVP threshold for the OVP delay time, the protection will be triggered, and LX node switching actions will be suppressed. LX node switching actions will be recovered once the combined feedback and ramp signals become lower than the reference voltage. False OVP triggers may happen under FCCM light load conditions, if the inductance value is chosen too low.

Over Temperature Protection (OTP)

The buck converter includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. When the thermal sensor detects the junction temperature exceeds 150°C, the over temperature protection (OTP) will be triggered, and the buck converter will be disabled, once the junction temperature cools down by approximately 15°C, the buck converter will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature will not exceed the OTP threshold.

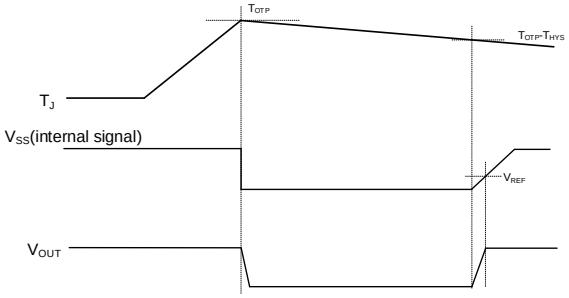


Figure12. Over Temperature Protection

Design Procedure

Feedback Resistor Divider Selection

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value of between 10kΩ and 1MΩ is strongly recommended for both resistors. If V_{SET} is 3.3V, R_H = 100kΩ is chosen, then using following equation, R_L can be calculated to be 22.1kΩ.

$$R_L = \frac{0.6V}{V_{SET} - 0.6V} \times R_H$$

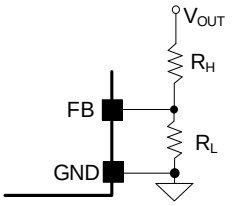


Figure13. Feedback Resistor Divider

Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce EMI. When selecting the input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems which are powered by a wall adapter or a long inductive cable may be susceptible to significant inductive ringing at the input of the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce input overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current,

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification. Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications a single 10μF X5R capacitor is sufficient. Place the ceramic input capacitor as close to the device's IN and GND pin as possible.

Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the LX node.

The buck converter operates well over a wide range of inductance values. This flexibility allows for optimization to find the best trade-off between efficiency, cost and size for a particular application. Selecting a low inductance value will help reduce size and cost and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low inductance value inductors may help reduce DC losses and increase efficiency. Choosing higher inductance value inductors tend to have higher DCR and will slow down transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) about 20% ~ 50% of the desired full output load current. Start calculating the approximate inductance value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$) and estimating a ΔI_L as some percentage of that current.

$$\mathrm{L} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L,PEAK} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

If FCCM light load operation is selected, make sure the inductance value is high enough to avoid reverse current limit is been triggered just under steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Selecting low loss ferrite materials is recommended.

Inductor Design Example

Consider a typical design for a buck converter providing 3.3V_{OUT} at 8A from 12V_{IN}, operating at 600kHz and using target inductor ripple current (ΔI_L) of 40% or 3.2A.

First, determine the approximate inductance value:

$$L = \frac{3.3V \times (12V - 3.3V)}{12V \times 600kHz \times 3.2A} = 1.246\mu H$$

Next, select the nearest standard inductance value, in this case 1.5µH, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{3.3V \times (12V - 3.3V)}{12V \times 600kHz \times 1.5\mu H} = 2.66A$$

$$I_{L,PEAK} = 8A + \frac{2.66A}{2} = 9.33A$$

The resulting 2.66A ripple current is 2.66A/8A is ~33.3%, well within the 20% ~ 40% target.

$$I_{L,PEAK,RVS} = \frac{2.66A}{2} = 1.33A < I_{LMT,RVS}$$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 9.33A.

Output Capacitor Selection

The buck converter provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Steady State Output Ripple

Steady state output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,\ ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,\ CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 2.66A using three 22µF ceramic capacitors, each with an ESR of ~6mΩ for parallel total of 66µF and 2mΩ ESR.

$$V_{RIPPLE,\ ESR} = 2.66A \times 2m\Omega = 5.32mV$$

$$V_{RIPPLE,\ CAP} = \frac{2.66A}{8 \times 66\mu F \times 600kHz} = 8.40mV$$

Total ripple = 13.72mV. The actual capacitive ripple may be higher than calculated value because the capacitance decreases with the voltage on the capacitor.

Using a 150µF 40mΩ POS cap, the above result is

$$V_{RIPPLE,\ ESR} = 2.66A \times 40m\Omega = 106.40mV$$

$$V_{RIPPLE,\ CAP} = \frac{2.66A}{8 \times 150\mu F \times 600kHz} = 3.69mV$$

Total ripple = 110.09mV

Output Transient Undershoot/Overshoot

If very fast load transient must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions, however, for good performance specific considerations must be addressed, especially when using small ceramic capacitors which have low capacitance at low output voltages, which results in insufficient stored energy for load transients. Output transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as

$$V_{ESR} = \Delta I_{OUT} \times ESR$$

Using the ceramic capacitor example above and a fast load transient of ± 4A, V_{ESR} = ± 4A × 2mΩ = ± 8mV. The POS capacitor result with the same load transient, V_{ESR} = ± 4A × 40mΩ = ± 160mV.

Capacitive undershoot (load increasing) is a function of the output capacitance, the load step, the inductor value and the input-output voltage difference and the maximum duty cycle factor. During a fast load transient, the maximum duty cycle of the buck converter is a function of t_{ON} and the $t_{OFF,MIN}$, as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{ON} pulses in this case. The maximum duty factor D_{MAX} may be calculated by

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated by

$$V_{UNDERSHOOT,CAP} = -\frac{L \times \Delta I^2{}_{OUT}}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 4A load increase using the ceramic capacitor case when V_{IN} = 12V.At V_{OUT} = 3.3V, the result is t_{ON} = 458ns, $t_{OFF,MIN}$ = 150ns, D_{MAX} = 458 / (458 + 150) = 0.753 and

$$V_{UNDERSHOOT,CAP} = -\frac{1.5\mu H \times (4A)^2}{2 \times 66\mu F \times (12V \times 0.753 - 3.3V)} = -31.7mV$$

Using the POS capacitor case, the above result is

$$V_{UNDERSHOOT,CAP} = -\frac{1.5\mu H \times (4A)^2}{2 \times 150\mu F \times (12V \times 0.753 - 3.3V)} = -13.95mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L \times \Delta I^2{}_{OUT}}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 4A load decrease using the ceramic capacitor case above. At V_{OUT} = 3.3V the result is

$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (4A)^2}{2 \times 66\mu F \times 3.3V} = 55.1mV$$

Using the POS capacitor case, the above result is

$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (4A)^2}{2 \times 150\mu F \times 3.3V} = 24.2mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application. If the system requirements are not met, recalculate with a different configuration.

Load Transient Considerations

The device uses the COT ripple-based control strategy to achieve good stability and fast transient response. In applications with high step load current, adding an RC network R_{FF} and C_{FF} between the OUT capacitors and the FB pin may further speed up the load transient response. R_{FF} = 1kΩ and C_{FF} = 220pF have been shown to perform well in most applications. Increasing C_{FF} will speed up the load transient response if there is no stability issue.

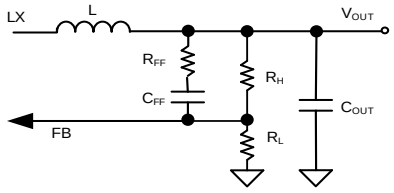


Figure14. Feedforward Network

Note: For C_{OUT} > 500μF and when the minimum load current is low, use feedforward values of R_{FF} = 1kΩ and C_{FF} = 2.2nF to provide sufficient ripple to FB node for low output ripple and good transient behavior.

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the device package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}}$$

Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125℃. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN2.5×2.5-16 package the thermal resistance θ_{JA} is 33℃/W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz. copper traces connected to each IC pin and very large, unbroken 1-oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the device backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A=25℃ may be calculated by the following formula:

$$P_{D,MAX} = \frac{125℃ - 25℃}{33℃/W} = 3W$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.

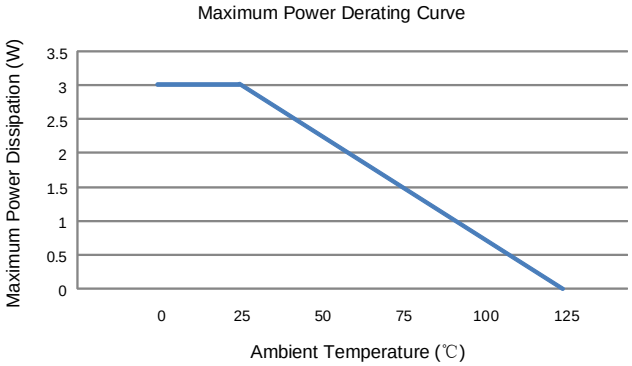


Figure15. Maximum Power Derating Curve

Application Schematic (V_{OUT}=3.3V)

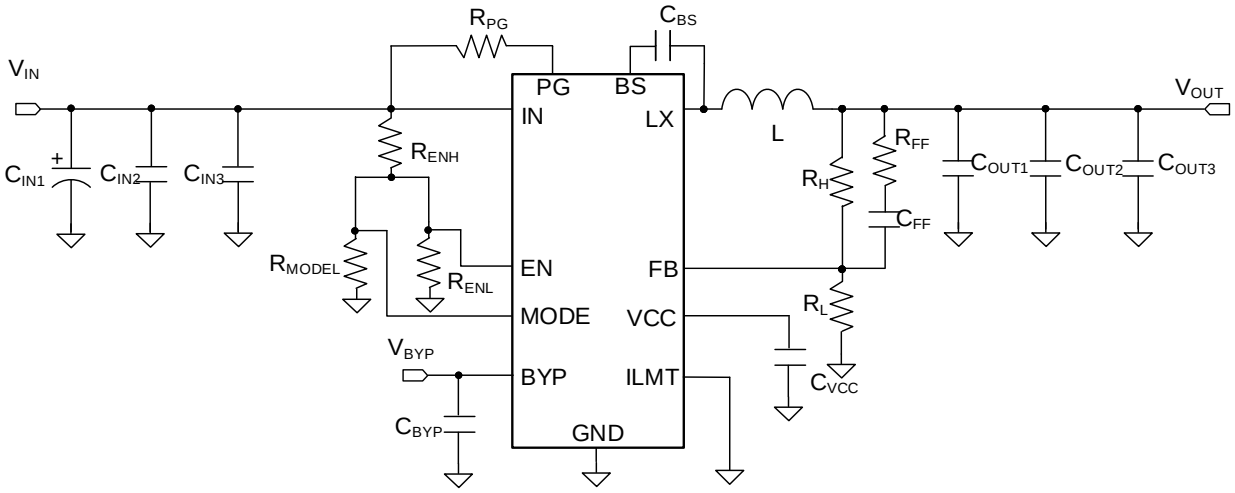


Figure16. Schematic Diagram

BOM List

Designator	Description	Part Number	Manufacturer
C_{IN1}	47μF/50V, Electrolytic Cap		
C_{IN2}	10μF/50V/X5R, 1206	GRM31CR61H106KA12L	mμRata
C_{IN3}, C_{BS}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	mμRata
C_{OUT1}, C_{OUT2}, C_{OUT3}	22μF/16V/X5R, 1206	GRM31CR61C226ME15L	mμRata
C_{VCC}	2.2μF/16V/X5R, 0603	GRM188R61C225KE15D	mμRata
C_{FF}	220pF/50V/C0G, 0603	GRM1885C1H221JA01D	mμRata
C_{BYP}	1.0μF/25V/X5R, 0603	GRM155R61E105KE11D	mμRata
L	1.5μH/16A, inductor	PCMB104T-1R5MS	CYNTEC
R_H, R_{PG}	100kΩ, 1%, 0603		
R_L	22.1kΩ, 1%, 0603		
R_{ENH}	10kΩ, 1%, 0603		
R_{ENL}, R_{MODEL}	1MΩ, 1%, 0603		
R_{FF}	1kΩ, 1%, 0603		

Recommend Components Values for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number
1.2	100	100	220	1.0μH/PCMB104T-1R0MT
1.8	100	49.9	220	1.0μH/PCMB104T-1R0MT
3.3	100	22.1	220	1.5μH/PCMB104T-1R5MS
5	100	13.7	220	1.5μH/PCMB104T-1R5MS

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

Input Capacitors: Place the input capacitor close to IN and GND pins, minimizing the loop formed by these connections. The capacitor should be connected to the IN and GND using a wide copper pour. A 0.1μF input ceramic capacitor is recommended to reduce the high-frequency noise.

Output Capacitors: Ensure that the C_{OUT} negative sides are connected to GND using wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.

VCC Capacitor: Place the VCC capacitor close to VCC using a short, direct copper trace to the nearest GND pin (pin 14).

BYP Capacitor: Place the BYP capacitor close to BYP using a short, direct copper trace to the nearest device GND pin (pin 14) if bypass function is used. It is recommended to make one good RC filter for BYP input if the 3.3V external power ripple is large.

Feedback Network: Place the feedback components (R_H, R_L, R_{FF} and C_{FF}) as close to FB pin as possible. Avoid routing the feedback line near LX, BS or other high frequency signal as it is noise sensitive. Use a Kelvin connection for the feedback sampling point at C_{OUT} rather than the inductor output terminal.

LX Connection: Keep LX area small to prevent excessive EMI, while using a wide copper trace to minimize parasitic resistance and inductance. Wide LX copper trace between pin 5 and pin 15, 16 should be used to improve efficiency.

BS Capacitor: Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX and C_{BS}) as short as possible.

Control Signals: It is not recommended to connect control signals to V_{IN} or another voltage source directly. A resistor in a range of 1kΩ to 1MΩ should be used if they are pulled high.

GND Vias: Place adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected by a larger copper area than its size, place four GND vias on it for heat dissipation.

PCB Board: A four-layer layout with 2-oz copper is strongly recommended to achieve better thermal performance. The top layer and bottom layer should place power IN and GND copper area as wide as possible. Middle1 layer should be used as a GND layer for conducting heat and shielding the middle2 layer signal lines from top layer crosstalk. Place signal lines on middle2 layer instead of the other layers, so that the other layers' GND plane is not cut by signal lines.

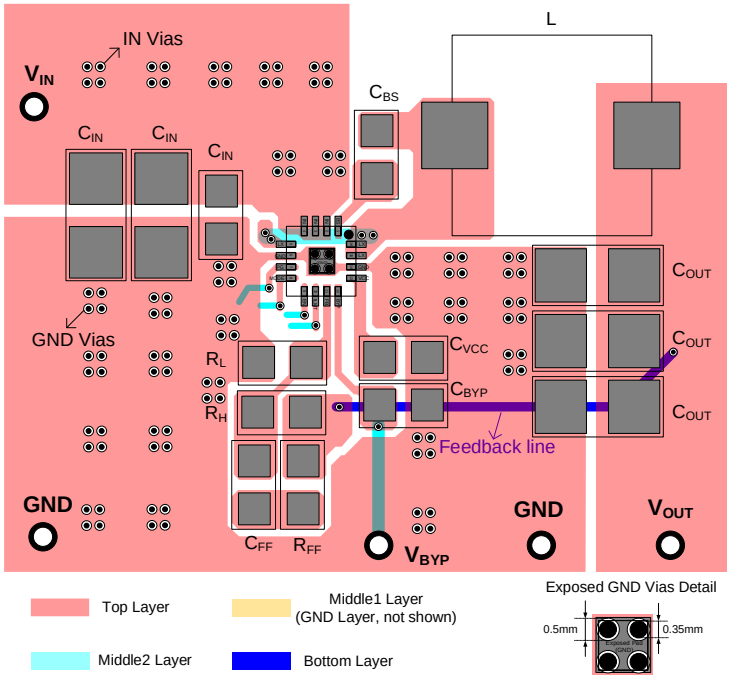
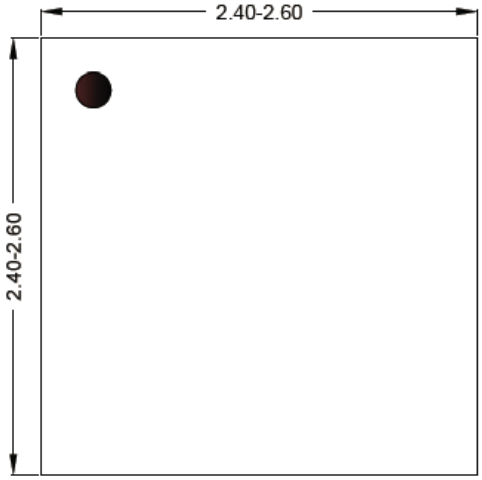
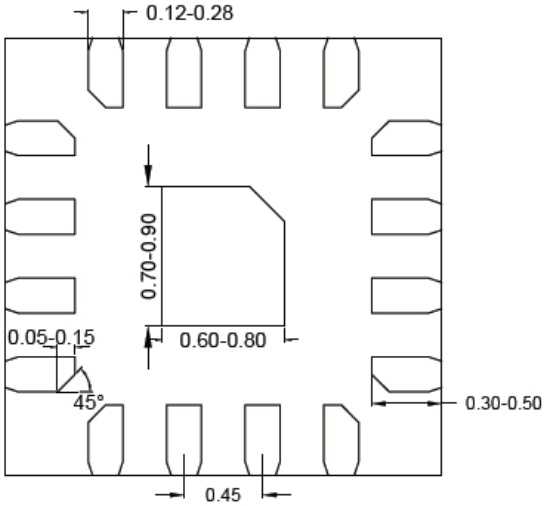


Figure17. PCB Layout Suggestion

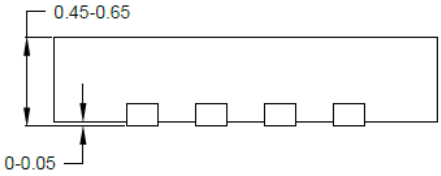
QFN2.5×2.5-16 Package Outline Drawing



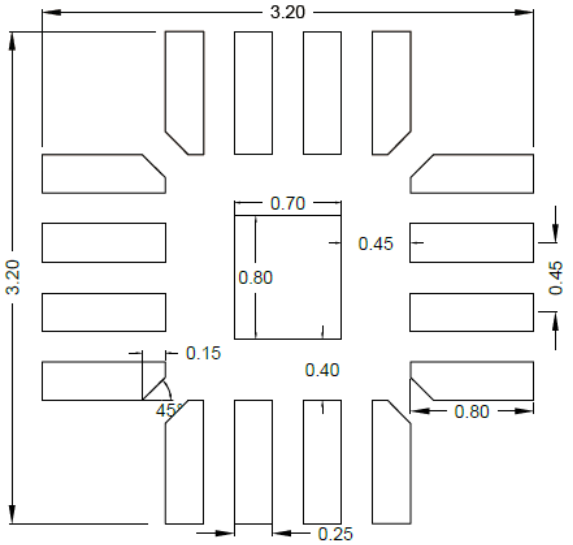
Top view



Bottom view



Side view

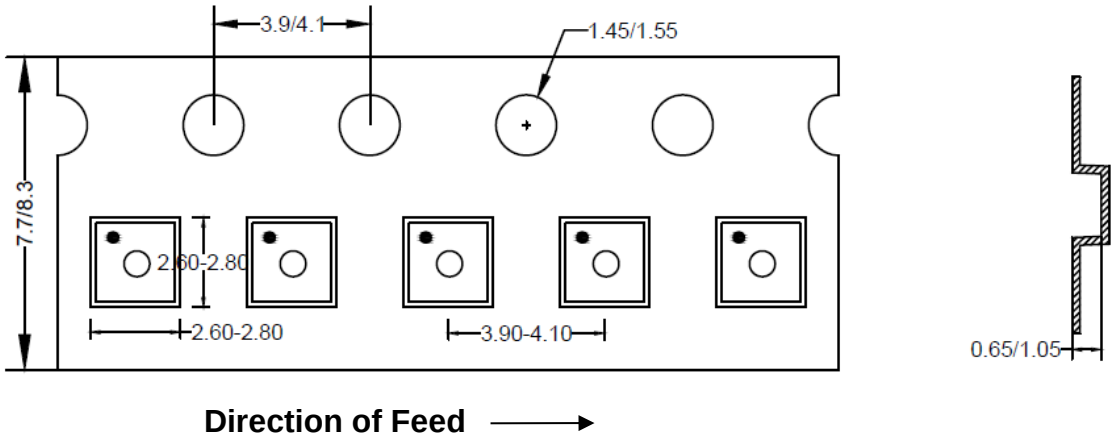


Recommended PCB layout
(Reference only)

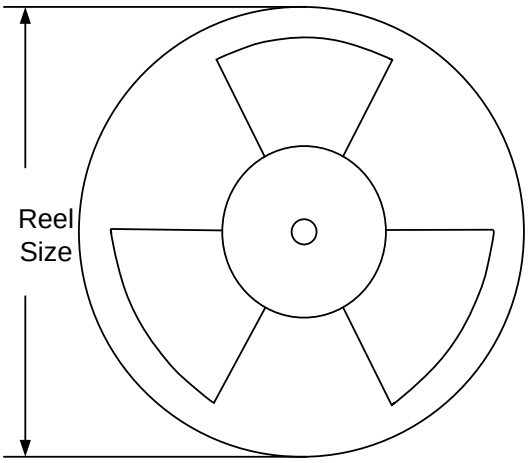
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Tape and Reel Information

1. Tape Dimensions and Pin1 Orientation
QFN2.5×2.5



2. Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2.5×2.5	8	4	7"	400	160	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
July 19, 2024	1.0	Initial Release	-

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