SY21240D

High Efficiency Fast Response, 9A, 28V Input Synchronous Step Down Regulator with VDDQ LDO

General Description

The SY21240D provides a complete power supply with the highest density for DDR3, DDR3L, LPDDR3 and DDR4 memory. It develops one high efficiency synchronous step-down DC/DC regulator VDD2 capable of delivering 9A continuous/12A peak current and one sink/source VDDQ LDO capable of delivering ±1A current. In addition, it operates at 600kHz pseudo constant frequency under continuous conduction mode. The integrated low $R_{DS(ON)}$ switches minimize the conduction loss.

Silergy's proprietary Instant-PWM™ fast-response, constant-on-time (COT) PWM control method supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation and even with low ESR ceramic capacitors.

The SY21240D operates over a wide input voltage range from 4V to 24V. Cycle-by-cycle current limit, input under voltage lock-out, internal soft-start, output under voltage protection and over voltage protection and thermal shutdown provide safe operation in all operating conditions.

Ordering Information

SY21240 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY21240DRAC	QFN3×3-20	--

Features

- Low $R_{DS(ON)}$ for Internal Switches of the Regulator (Top/Bottom): 27/9 mΩ
- 4~24V Input Voltage Range
- Compatible for LPDDR4X Application
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal 450μs Soft-start Limits the Inrush Current
- 600kHz Pseudo-constant Switching Frequency
- PFM/USM Selectable Light Load Operation Mode
- ±1.0% 0.6V VDD2 Reference
- 9A Continuous/12A Peak Output Current Capability of the VDD2 Regulator
- Fixed 0.61V VDDQ Reference
- ±1A Source/Sink Current Capability of the VDDQ LDO
- VDD2 and VDDQ Power Good Indicator
- Support VDDQ LDO High-Z in S3
- Output Discharge Function for Both VDD2 and VDDQ in S4/S5
- Guarantee VDD2 200mV Higher Than VDDQ at Any Operation Condition
- Cycle-by-cycle Valley and Peak Current Limit Protection for VDD2
- Latch-off Mode Output Under Voltage Protection for VDD2
- Latch-off Mode Output Over Voltage Protection for VDD2
- Latch-off Mode Over Temperature Protection for VDD2
- Input UVLO and Bias UVLO
- RoHS Compliant and Halogen Free
- Compact package: QFN3×3-20

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

Typical Applications

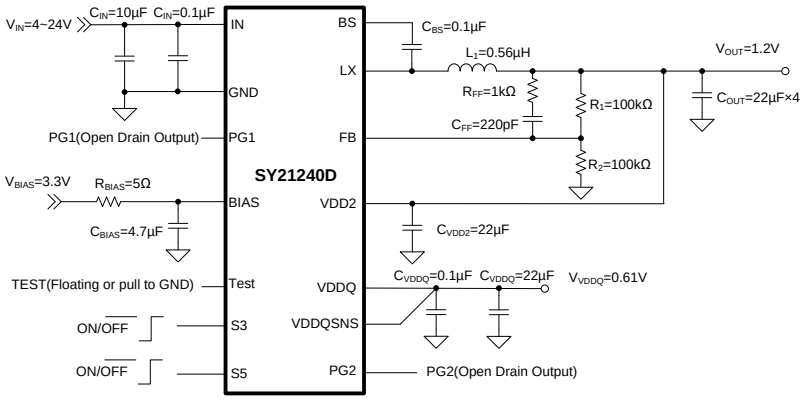


Figure1. Schematic Diagram

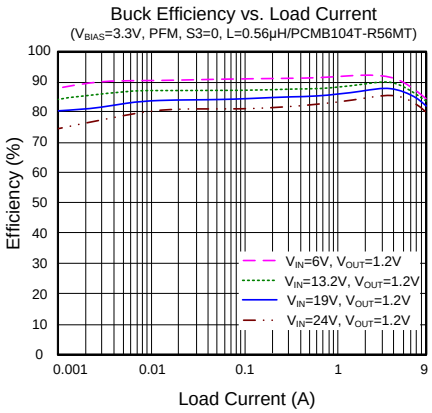
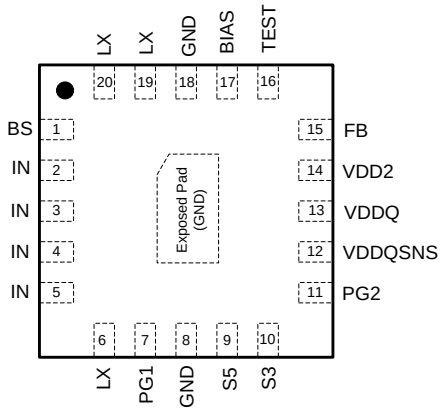


Figure2. Buck Efficiency vs. Load Current

Pinout (Top view)



(QFN3×3-20)

Top Mark: **CUT*xyz***, **(**Device code: CUT, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin.
IN	2, 3, 4, 5	Input pin. Decouple this pin to GND pin with at least 20μF ceramic capacitor.
LX	6, 19, 20	Inductor pin. Connect this pin to the switching node of inductor.
PG1	7	VDD2 power good indicator. Open drain output when the VDD2 output voltage is within 89% to 120% of VDD2 regulation point.
GND	8, 18, EP	Ground pin.
S5	9	S5 signal input. Internally pulled low with ~1MΩ resistor. This pin is also used for controlling operation mode of the regulator under light load condition after the output of Buck regulator is within the regulation range. If the voltage on this pin is lower than 1.6V, the Buck regulator will work under ultra-sonic mode (USM). If the voltage on this pin is greater than 2.2V, the Buck regulator will work under PFM mode.
S3	10	S3 signal input. Internally pulled low with ~1MΩ resistor.
PG2	11	VDDQ power good indicator. Open drain output when the VDDQ output voltage is within 500mV to 750mV.
VDDQSNS	12	VDDQ LDO remote sense input.

VDDQ	13	Power output of VDDQ LDO. Decouple this pin to the GND pin with at least a 22μF ceramic capacitor.
VDD2	14	Power supply for the VDDQ LDO. Connect VDD2 to the output capacitor of the regulator directly with a thick (>30 mil) trace. Do not leave this pin floating.
FB	15	VDD2 Output feedback pin. Connect this pin to the center point of the output resistor divider to program the output voltage: V_{SET}=0.6× (1+R_1/R_2).
TEST	16	For factory use only. Leave this pin floating in application.
BIAS	17	External 3.3V VCC input. Power supply for internal analog circuits and driving circuit. Make one good RC filter circuit between supply source and the BIAS pin.

Block Diagram

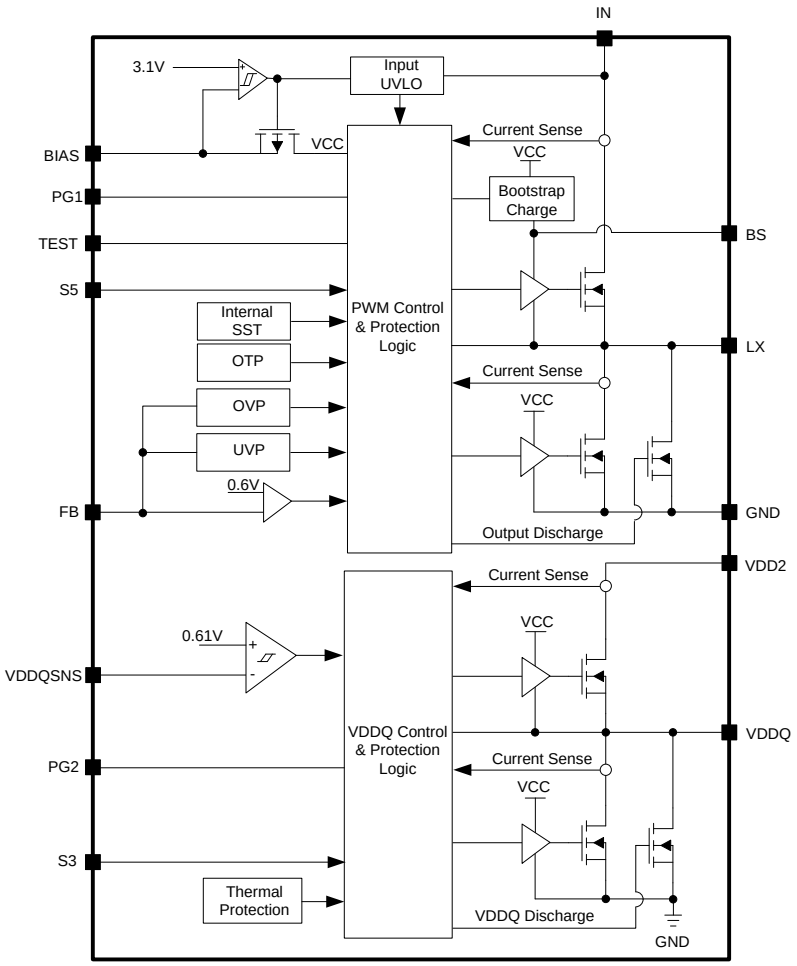


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 28V
IN-LX, LX, PG1, S3, S5, TEST Voltage---------- -0.3V to 26V
BIAS, VDD2, VDDQ, VDDQSNS, PG2, FB, BS-LX Voltage---------- -0.3V to 4V
Maximum Power Dissipation, $P_{D,MAX}$ @ T_A = 25°C QFN3×3-20 ---------- 3.33W
Package Thermal Resistance (Note 2)
θ_{JA}, QFN3×3-20 ---------- 30°C/W
θ_{JC}, QFN3×3-20 ---------- 4.5°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX Voltage in 10ns Duration ---------- -5V to 29V
Dynamic LX Voltage in 20ns Duration ---------- -1V to 27V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4V to 24V
BIAS Supply Voltage ---------- 3.1V to 3.6V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN}= 12V, V_{BIAS}= 3.3V, V_{OUT}=1.2V, C_{OUT}= 100µF, T_A= 25°C, I_{OUT}= 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4		24	V
Input UVLO Threshold	$V_{IN,UVLO}$	V_{IN} rising			3.95	V
Input UVLO Hysteresis	$V_{IN,HYS}$			0.3		V
Bias UVLO Threshold	$V_{BIAS,UVLO}$	V_{BIAS} rising	2.8			V
Bias UVLO Hysteresis	$V_{BIAS,HYS}$			0.2		V
Bias Shutdown Current	$I_{BIAS,SHDN}$	S3=0, S5=0			1	µA
Bias Quiescent Current in S3 State	$I_{BIAS,Q1}$	S3=0, S5=1, I_{OUT}=0A, V_{OUT}=V_{SET}×105%		65	100	µA
Bias Quiescent Current in S0 State	$I_{BIAS,Q2}$	S3=1, S5=1, I_{OUT}=0A, I_{VDDQ}=0A, V_{OUT}=V_{SET}×105%		110	135	µA
VDD2 Input Current in S0 State	I_{VDD2}	S3=1, S5=1, V_{VDD2}=1.2V, I_{VDDQ}=0A		1	5	µA
Feedback Reference Voltage	V_{REF}		0.594	0.6	0.606	V
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			27		mΩ
Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			9		mΩ
VDD2 Output Discharge Current	$I_{DIS,VDD2}$	V_{OUT}=1.2V		70		mA
Top FET Current Limit	$I_{LMT,TOP}$	(Note 4)		20		A
Bottom FET Current Limit	$I_{LMT, BOT}$		13.5	16	18	A
Bottom FET Reverse Current Limit	$I_{LMT, RVS}$	USM mode	2	3.5	5	A
Soft-start Time	t_{SS}	V_{OUT} from 0% to 100%V_{SET}		450		µs
S5/S3 Input Voltage High	$V_{S5/S3,H}$		1			V
S5/S3 Input Voltage Low	$V_{S5/S3,L}$				0.3	V
S3, S5 Internal Resistance	R_S	S3=S5=3.3V	0.5		2	MΩ
S5 Voltage for USM Mode	$V_{S5,USM}$		1		1.6	V
S5 Voltage for PFM Mode	$V_{S5,PFM}$		2.2		V_{IN}	V
Switching Frequency	f_{SW}	V_{OUT}=1.2V, CCM	510	600	690	kHz
Ultra-sonic Mode Frequency	f_{USM}	USM mode, I_{OUT}=0A		27		kHz
Min ON Time	$t_{ON,MIN}$	V_{IN}=V_{INMAX} (Note 4)		50		ns
Min OFF Time	$t_{OFF,MIN}$			210		ns
Output Over Voltage Threshold	V_{OVP}	V_{FB} rising	117	120	123	%V_{REF}
Output Over Voltage Hysteresis	$V_{OVP,HYS}$			5		%V_{REF}
Output OVP Delay	$t_{OVP,DLY}$	(Note 4)		20		µs
Output Under Voltage Protection Threshold	V_{UVP}	V_{FB} falling		33		%V_{REF}
Output UVP Delay	$t_{UVP,DLY}$	(Note 4)		10		µs
VDD2 Power Good Threshold	V_{PG1}	V_{FB} rising (good)	86	89	92	%V_{REF}
VDD2 Power Good Hysteresis	$V_{PG1,HYS}$			6		%V_{REF}
VDD2 Power Good Delay	$t_{PG1,R}$	Low to high (Note 4)		150		µs
	$t_{PG1,F}$	High to low (Note 4)		15		µs
VDD2 Power Good Output Low	$V_{PG1,LOW}$	I_{PG1}=2mA, V_{FB}=0V			0.3	V
VDD2 Input Voltage Range	$V_{VDD2,IN}$		1		2.5	V
VDDQ Output Source Current Limit	$I_{LMT,VDDQ,SOU}$	VDDQ source current	1.6			A
VDDQ Output Sink Current Limit	$I_{LMT,VDDQ,SIN}$	VDDQ sink current	1.6			A

VDDQ Output Error $V_{VDDQ,ERR}$=|V_{VDDQ}-610mV|	$V_{VDDQ,ERR}$	I_{VDDQ}=0A		5	15	mV
		VDDQ source 1A		15	40	mV
		VDDQ sink 1A		15	40	mV
VDDQ Power Good Threshold	V_{PG2}	V_{VDDQ} rising (good)	470	500	530	mV
VDDQ Power Good Hysteresis	$V_{PG2,HYS}$			40		mV
VDDQ Power Good OVP Threshold	$V_{PG2,OVP}$	V_{VDDQ} rising (not good)	710	750	790	mV
VDDQ Power Good OVP Hysteresis	$V_{PG2,OVP,HYS}$			40		mV
VDDQ Power Good Delay	$t_{PG2,R}$	Low to high (Note 4)		3		μs
	$t_{PG2,F}$	High to low (Note 4)		20		μs
VDDQ Power Good Output Low Voltage	$V_{PG2,LOW}$	I_{PG2}=2mA, V_{VDDQ}=0V			0.1	V
Over Temperature Protection Temperature	T_{OTP}	T_J rising (Note 4)		150		℃
Over Temperature Protection Recovery Hysteresis	$T_{OTP,HYS}$	(Note 4)		15		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a 8.5cm×8.5cm size, four-layer Silergy Evaluation Board with 2-oz copper.

Note 3: The device is not guaranteed to function outside its operating conditions.

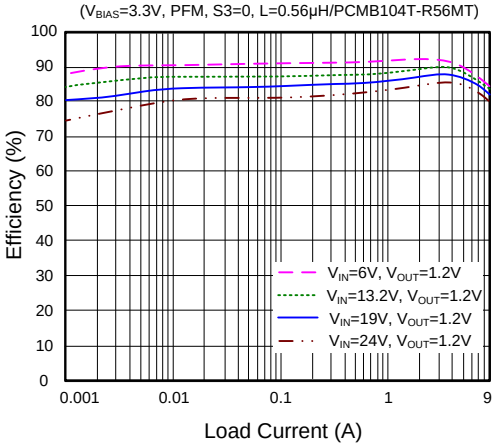
Note 4: Guaranteed by design.

Typical Performance Characteristics

(T_A=25°C, V_{IN}=12V, V_{BIAS}=3.3V, V_{OUT}=1.2V, L=0.56µH, C_{OUT}=88µF, C_{VDDQ}=22µF, unless otherwise noted)

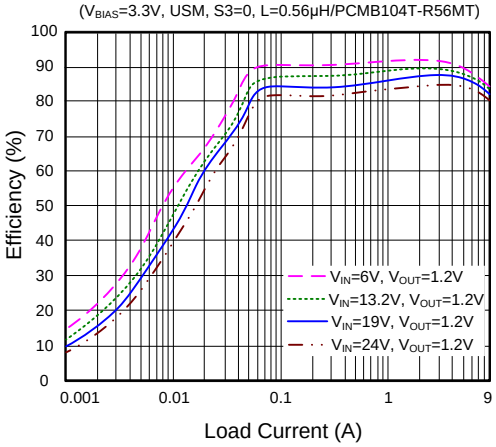
Buck Efficiency vs. Load Current

(V_{BIAS}=3.3V, PFM, S3=0, L=0.56µH/PCMB104T-R56MT)



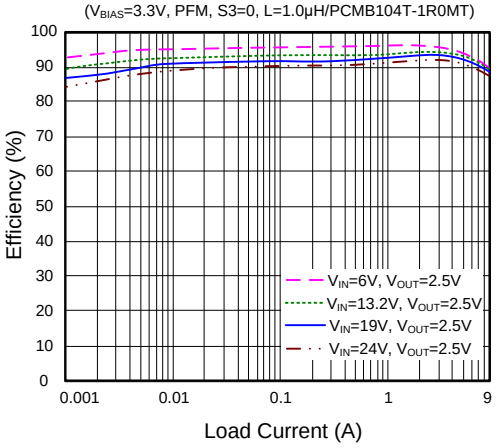
Buck Efficiency vs. Load Current

(V_{BIAS}=3.3V, USM, S3=0, L=0.56µH/PCMB104T-R56MT)



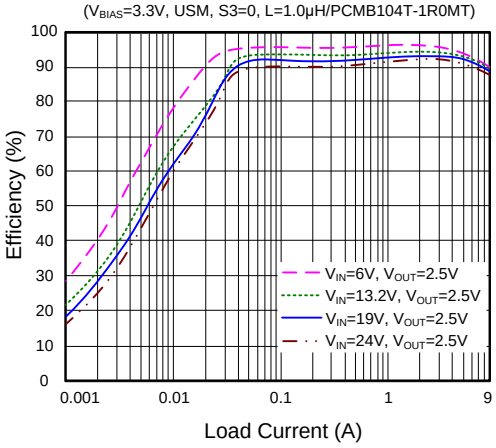
Buck Efficiency vs. Load Current

(V_{BIAS}=3.3V, PFM, S3=0, L=1.0µH/PCMB104T-1R0MT)



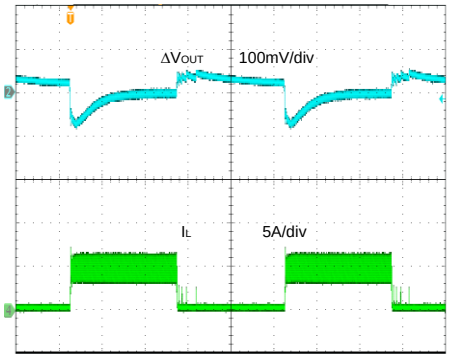
Buck Efficiency vs. Load Current

(V_{BIAS}=3.3V, USM, S3=0, L=1.0µH/PCMB104T-1R0MT)



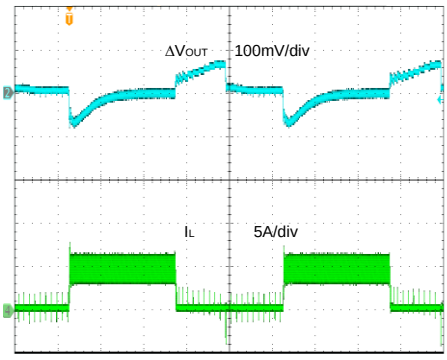
Buck Load Transient

(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0-4.5A, PFM, S3=0)



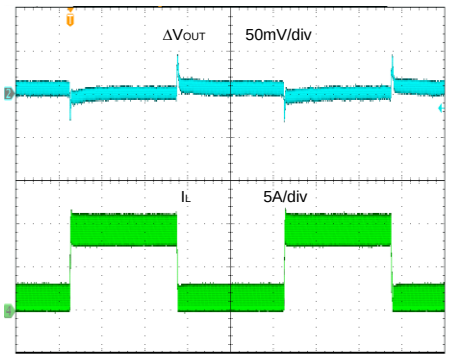
Buck Load Transient

(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0-4.5A, USM, S3=0)



Buck Load Transient

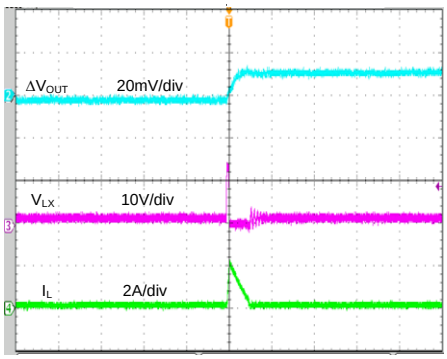
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0.9A-9A, S3=0)



Time (200μs/div)

Buck Output Ripple

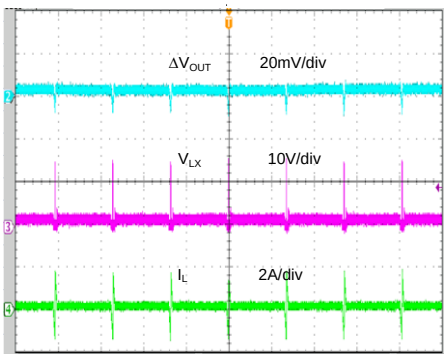
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0A, PFM, S3=0)



Time (2μs/div)

Buck Output Ripple

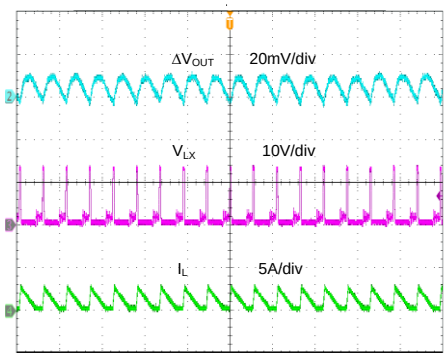
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0A, USM, S3=0)



Time (20μs/div)

Buck Output Ripple

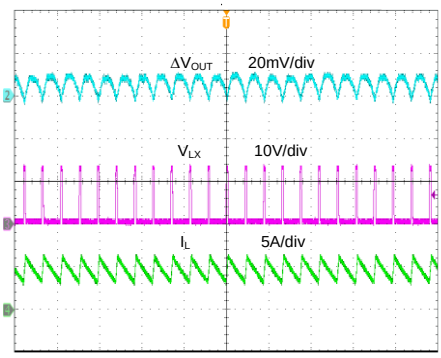
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0.9A, S3=0)



Time (4μs/div)

Buck Output Ripple

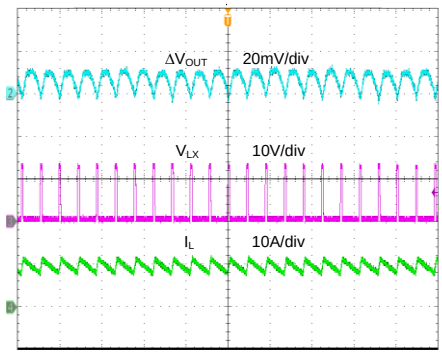
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=4.5A, S3=0)



Time (4μs/div)

Buck Output Ripple

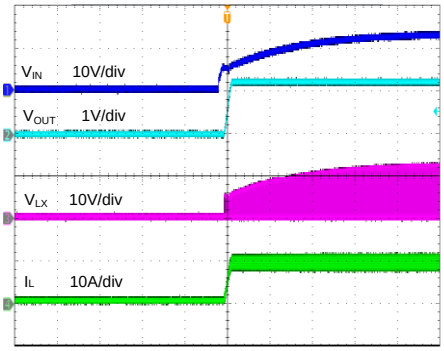
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, S3=0)



Time (4μs/div)

Buck Startup from V_{IN}

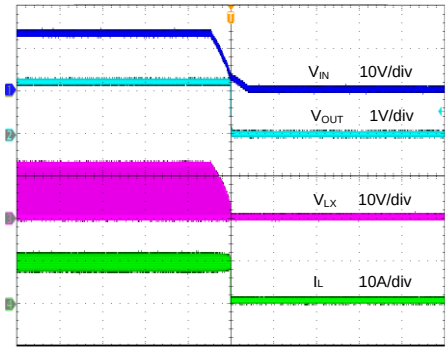
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, S3=0)



Time (2ms/div)

Buck Shutdown from V_{IN}

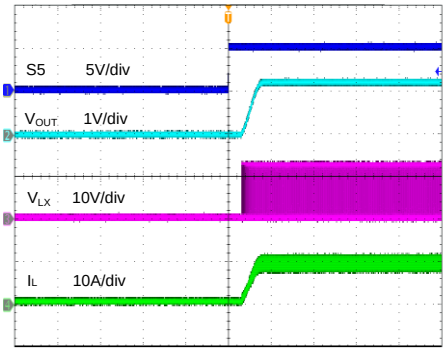
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, S3=0)



Time (2ms/div)

Buck Startup from S5

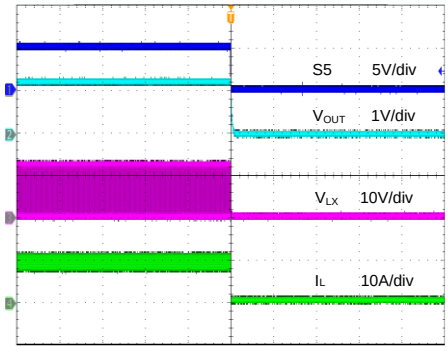
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, S3=0)



Time (800µs/div)

Buck Shutdown from S5

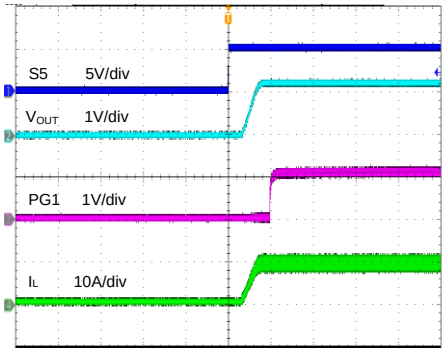
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, S3=0)



Time (800µs/div)

PG1 Test When S5 On

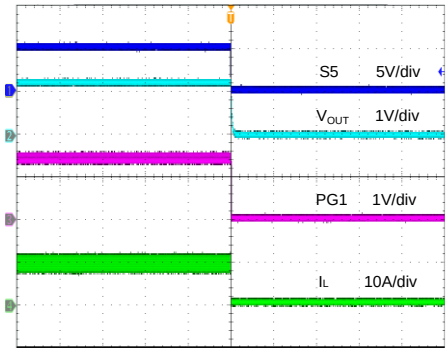
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, S3=0)



Time (800µs/div)

PG1 Test When S5 Off

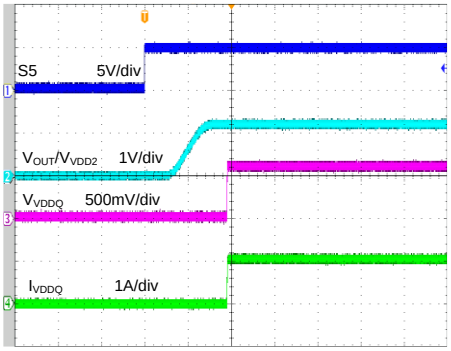
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, S3=0)



Time (800µs/div)

VDDQ Startup from S5

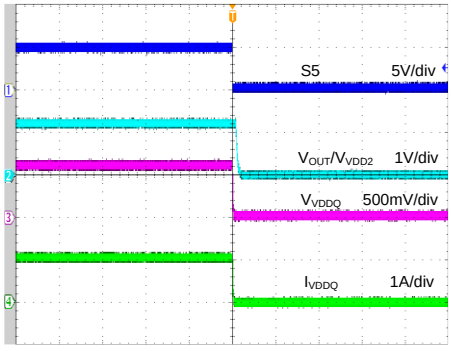
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, I_{VDDQ}=1A, S3=1)



Time (400µs/div)

VDDQ Shutdown from S5

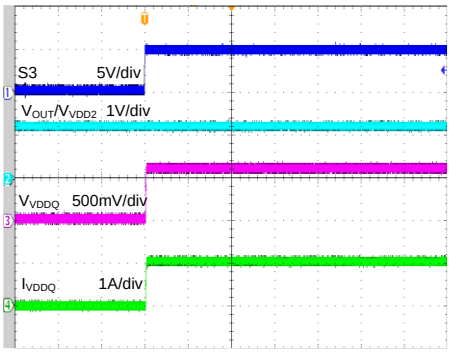
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, I_{VDDQ}=1A, S3=1)



Time (400µs/div)

VDDQ Startup from S3

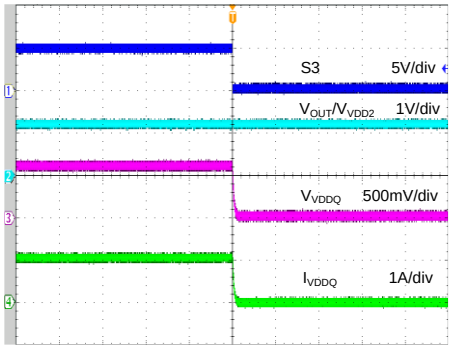
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, I_{VDDQ}=1A, S5=1)



Time (400µs/div)

VDDQ Shutdown from S3

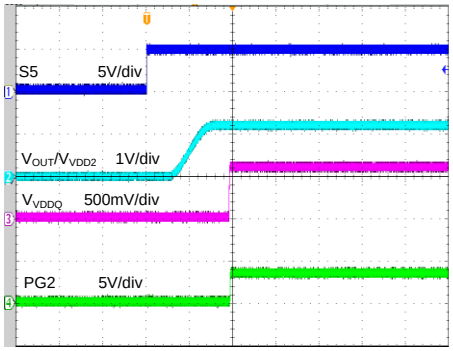
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, I_{VDDQ}=1A, S5=1)



Time (400µs/div)

PG2 Test When S5 On

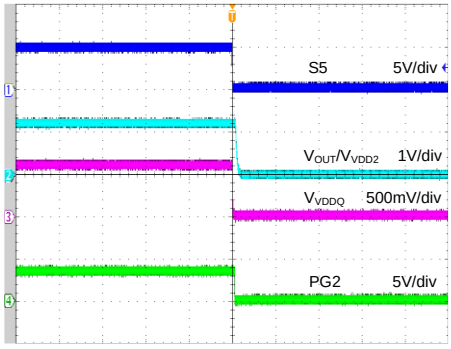
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, I_{VDDQ}=1A, S3=1)



Time (400µs/div)

PG2 Test When S5 Off

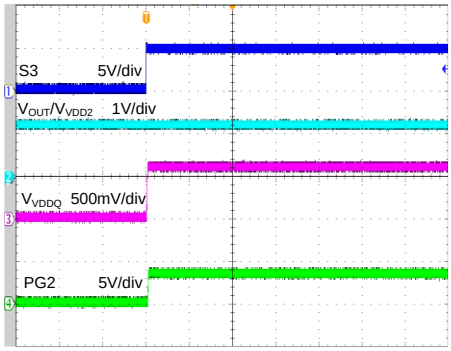
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, I_{VDDQ}=1A, S3=1)



Time (400µs/div)

PG2 Test When S3 On

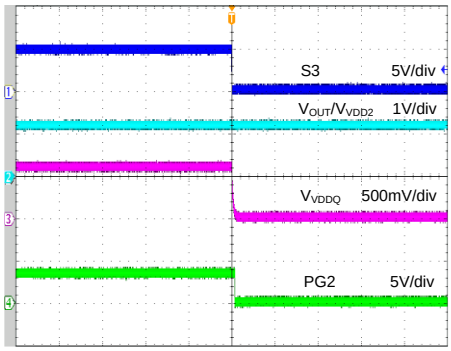
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, I_{VDDQ}=1A, S5=1)



Time (400µs/div)

PG2 Test When S3 Off

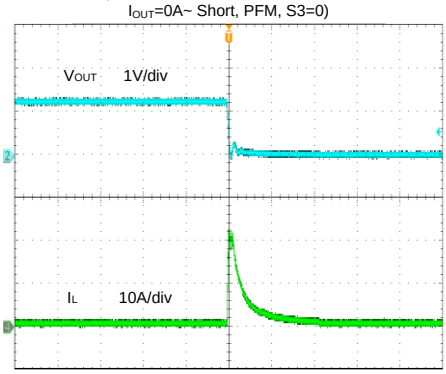
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, I_{VDDQ}=1A, S5=1)



Time (400µs/div)

Buck Output Short Circuit

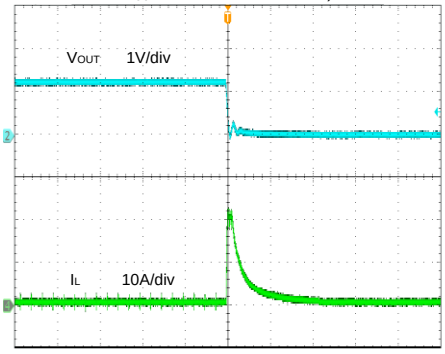
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0A~ Short, PFM, S3=0)



Time (100µs/div)

Buck Output Short Circuit

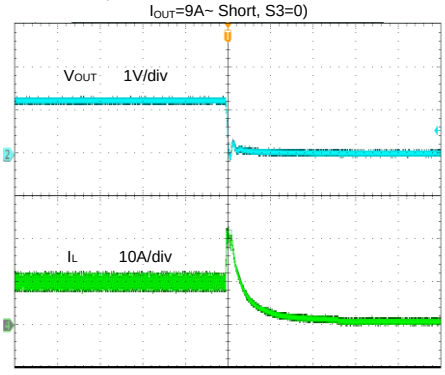
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0A~ Short, USM, S3=0)



Time (100µs/div)

Buck Output Short Circuit

(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A~ Short, S3=0)



Time (100µs/div)

Detailed Description

General Features

Constant-on-time Architecture

Fundamental to any constant-on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the high-side power switch. Each on-time (t_{ON}) is a "fixed" period internally calculated to operate the step down regulator at the desired switching frequency considering the input and output voltage ration, $t_{ON}=(V_{OUT}/V_{IN})\times(1/f_{SW})$. For example, considering that a hypothetical converter targets 1.2V output from a 10V input at 600kHz, the target on-time is (1.2V/10V)×(1/600kHz) = 200ns. Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FB drops below the target value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is less than the target. This approach avoids the making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

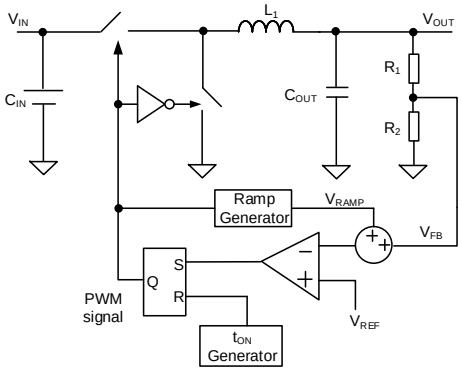
In COT architecture, there is no fixed clock, so the high-side power switch can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramp the inductor current up to meet load requirements with minimal delays. Traditional current mode or voltage mode control methods must simultaneously monitor the feedback voltage, current feedback and internal ramps and compensation signals to determine when to turn off the high-side power switch and turn on the low-side synchronous rectifier. Considering these small signals in a switching environment are difficult to be noise-free after switching large currents, making those architectures difficult to apply in noisy environments and at low duty cycles.

Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for small duty cycle, since at very low duty cycle operation, once the on-time is close to the minimum on time, the switching frequency can be reduced as needed to always ensure a proper operation.

Under T_J=-40℃~125℃ condition, the device can support 2.5V output even the input voltage is as low as 4V.

Instant-PWM Operation



Silergy's instant-PWM control method adds several proprietary improvements to the traditional COT architecture. Whereas most legacies based on COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, instant-PWM control method derives this signal internally. Another improvement optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT regulators may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor maybe become too small to maintain smooth operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum t_{OFF} has been satisfied and the inductor current as measured in the low-side synchronous rectifier is lower than the bottom FET current limit. As the t_{ON} pulse is triggered, the low-side synchronous rectifier turns off and the high-side power switch turns on. Then the inductor current ramps up linearly during the t_{ON} period. At the conclusion of the t_{ON} period, the high-side power switch turns off, the low-side synchronous rectifier turns on and the inductor current ramps down linearly. This action also initiates the minimum t_{OFF} timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum t_{OFF} is relatively short so that during high speed load transient t_{ON} can be retriggered with minimal delay, allowing the inductor current to ramp quickly to provide sufficient energy to the load side.

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between the high-side power switch off and the low-side synchronous rectifier on

period or the low-side synchronous rectifier off and the high-side power switch on period.

Light Load Operation Mode Selection

PFM or USM light load operation is selected by the S5 pin. S5 is not only enable pin but also mode selection pin to control operation mode of the regulator under light load condition after the output of Buck regulator is within the regulation range. If the voltage on this pin is lower than 1.6V and higher than its rising threshold, the Buck regulator will work under ultra-sonic mode (USM). If the voltage on this pin is greater than 2.2V, the Buck regulator will work under pulse-frequency modulation mode (PFM).

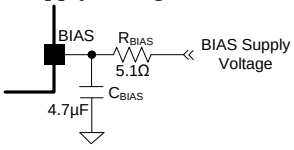
If PFM light load operation is selected, under light load conditions, typically $I_{OUT} < 1/2 \times \Delta I_L$, the current through the low-side synchronous rectifier will ramp to near zero before the next t_{ON} time. When this occurs, the low-side synchronous rectifier turns off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, and the combined feedback and ramp signals remain much greater than the reference voltage, the instant-PWM control loop will not trigger another t_{ON} until needed, so the apparent operating switching frequency will correspondingly drop, further enhancing efficiency. The switching frequency can be lower than audible frequency area under deep light load or null load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle. The device enters CCM once the load current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range. The critical level of the load current is determined with

$$I_{OUT\_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1-D)}{2 \times f_{SW} \times L_1}$$

If USM light load operation is selected, it keeps the switching frequency above an audible frequency area even under deep light load or null load conditions. Once the device detects that both the high-side power switch and the low-side synchronous rectifier turn off for more than one certain time, it forces the low-side synchronous rectifier turn on in advance of one t_{ON} cycle and discharge the output capacitor electric quantity so that the switching frequency is out of audio range. There is also one feedback loop to match the low-side synchronous rectifier forced turn on time with the error amplifier output voltage to avoid output voltage becoming too high.

Bias Input Supply

The SY21240D has no internal linear regulator (VCC) itself; it needs one bias input supply to power the internal gate drivers, PWM logic, analog circuitry, and other blocks. Connect a 4.7μF low ESR ceramic capacitor from BIAS to GND if the supply voltage is one DC source. Connect a 5.1Ω resistor before the capacitor to make the bias voltage AC ripple is small enough if the supply voltage is not one DC source.

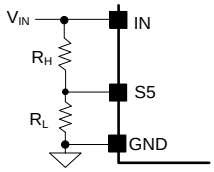


Input and Bias Under Voltage Lock-out (UVLO)

To prevent operation before all internal circuitry is ready and to ensure that the power and synchronous rectifier switches can be sufficiently enhanced, the instant-PWM incorporates two under-voltage lockout protections: input UVLO and bias UVLO.

The device remains in a low current state and all switching actions are inhibited until V_{IN} and V_{BIAS} all exceed their own UVLO (rising) threshold. At that time, if S5 in enabled, the device will start-up by initiating a soft-start ramp. If V_{IN} falls below $V_{IN,UVLO}$ less than the input UVLO hysteresis, or V_{BIAS} falls below $V_{BIAS,UVLO}$ less than the bias UVLO hysteresis, switching actions will again be suppressed.

If the input UVLO threshold is low for some high input UVLO threshold requirement applications, use S5 to adjust the input UVLO by adopting two external divided resistors.



S5/S3 Control

The SY21240D has two enable pins to control the synchronous Buck regulator output VDD2 and VDDQ LDO. When the input voltage and the bias voltage both exceed their own UVLO (rising) threshold, S5 and S3 linked voltage are not allowed to be 2V higher than the input voltage at the same time.

Both VDD2 and VDDQ outputs are turned on under S0 state (S5 = S3 = high). Under S3 state (S3 = low, S5 = high), only VDD2 output is turned on while VDDQ output is turned off and left at a high-impedance state (high Z). The VDDQ output floats and does not sink or source current under this state. Under S4/S5 state (S5 = S3 = low), both VDD2 and

VDDQ outputs are turned off and work under discharge state. VDDQ outputs discharge quickly before VDD2 discharges after entering S4/S5 state. See S5/S3 control logic details in below table.

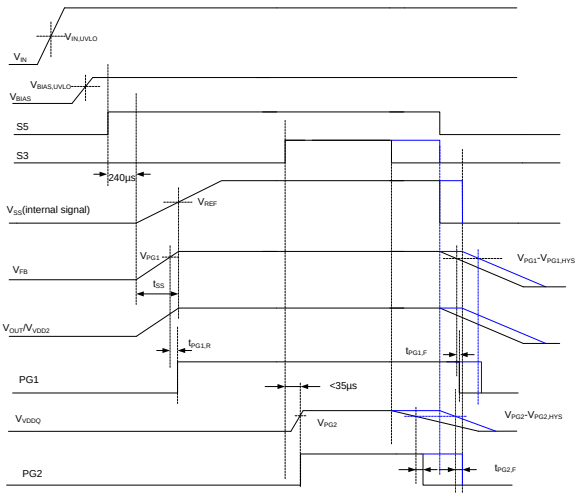
S3	S5	STATE	BUCK(VDD2)	VDDQ
High	High	S0	On	On
Low	High	S3	On	Off (High-Z)
Low	Low	S4/S5	Off (Discharge)	Off (Discharge)

The S5/S3 input is a high-voltage capable input with logic-compatible threshold. When S5/S3 is driven above 1V normal device operation will be enabled. When driven < 0.3V the device will be shut down, reducing bias input current to < 1.0μA.

It is not recommended to connect S5, S3 and IN directly. A resistor in a range of 1kΩ to 1MΩ should be used if S5, S3 is pulled high by IN.

Startup and Shutdown

The SY21240D incorporates an internal soft-start circuit to smoothly ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 450μs, which avoids high current flow and transients during startup. The startup and shutdown sequence is shown below.



If the output is pre-biased to a certain voltage before start-up, the device disables the switching of both the high-side power switch and the low-side synchronous rectifier until the voltage on the internal reference exceeds the sensed output voltage at the FB node.

Buck Output Discharge and VDDQ Discharge

The SY21240D discharges Buck output and VDDQ voltage when the converter shuts down from V_{IN} or S5, or thermal shutdown, so that output voltage can be discharged in a minimal time, even load current is zero. The Buck discharge FET in parallel with the low-side synchronous rectifier turns on after the low-side synchronous rectifier turns off when shut down logic is triggered. The output discharge current is typically 70mA.

When the device detects it enters into discharge status, the VDDQ discharge FET is turned on firstly and discharge VDDQ voltage quickly, when the VDDQ power good is turned low, then the Buck discharge FET is turned on to discharge Buck output voltage. Note that all discharge actions are not active beyond these shutdown conditions.

VDDQ Output

The SY21240D integrates high performance, low drop-out linear regulators VDDQ to provide complete LPDDR4X power solutions.

The VDDQ is one LDO output with 1A source/sink current capability. The VDDQ reference voltage is fixed 0.61V. A minimum 22μF low ESR ceramic capacitor must be connected close to the VDDQ terminal. The VDDQSNS should make one Kelvin connection with the positive node of VDDQ output capacitor.

In order to avoid LDO shoot-through, ±5mV offset voltage is added with the reference voltage of VDDQ sink/source MOSFET, so that the VDD2 input current is small when VDDQ output current is zero even under state S3.

Buck Output Power Good Indicator PG1

The Buck power good indicator is an open drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is greater than V_{PG1} and less than V_{OVP} for at least the PG1 power good delay time (low to high), PG1 will be high-impedance.

PG1 should be connected to BIAS or another voltage source through a resistor (e.g. 100kΩ). After the input voltage and bias voltage exceed their own UVLO (rising) threshold, the PG1 FET is turned on so that PG1 is pulled to GND before output voltage is ready. After feedback voltage V_{FB} reaches V_{PG1}, PG1 is pulled high (after one delay time typical 150 μs). When V_{FB} drops to V_{PG1} less than one $V_{PG1,HYS}$, or rises to V_{OVP} for one OVP delay time, PG1 is pulled low (after one delay time typical 15 μs).

VDDQ Power Good Indicator PG2

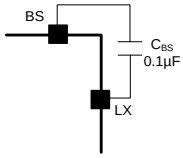
The VDDQ good indicator is an open drain output controlled by a window comparator connected to the VDDQ feedback signal. If VDDQSNS voltage is

greater than V_{PG2} and less than $V_{PG2,OVP}$ for at least the PG2 power good delay time (low to high), PG2 will be high-impedance.

PG2 should be connected to BIAS or another voltage source through a resistor (e.g. 100kΩ). After the input voltage and bias voltage exceed their own UVLO (rising) threshold, the PG2 FET is turned on so that PG2 is pulled to GND before output voltage is ready. After VDDQSNS voltage reaches V_{PG2}, PG2 is pulled high (after one delay time typical 3μs). When VDDQSNS voltage drops to V_{PG2} less than one $V_{PG2,HYS}$, or rises to $V_{PG2,OVP}$ for one PG2 high to low delay time, PG2 is pulled low (after one delay time typical 20 μs).

External Bootstrap Capacitor Connection

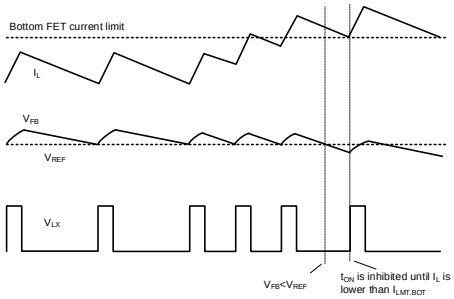
This device integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 0.1μF low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel MOSFET power switch.



Fault Protection Modes

Buck Output Current Limit

Instant-PWM incorporates a cycle-by-cycle "valley" current limit. Inductor current is measured in the low-side synchronous rectifier when it turns on and as the inductor current ramps down. If the current exceeds the bottom FET current limit threshold, t_{ON} is inhibited until the current returns back to the limit threshold or lower.



When the valley current limit occurs, the output current limit value is $I_{LMT,OUT}=I_{LMT,BOT}+\Delta I_L/2$,

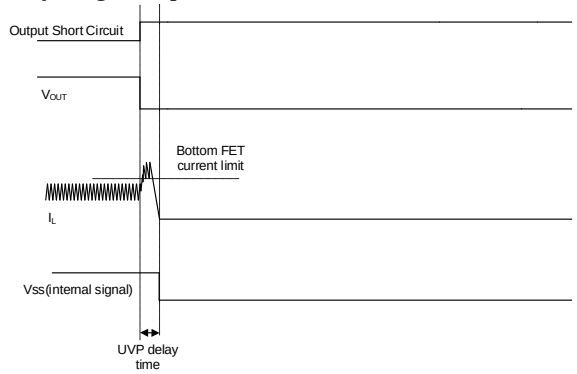
$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

The over current limit protection limits the inductor current but the OCP itself is one non-latch protection. When the load current is higher than the bottom FET current limit threshold by one half of the peak-to-peak inductor ripple current, the output voltage starts to drop. Once the feedback voltage falls lower than the under voltage protection (UVP) threshold and continues for one UVP delay time, the device will UVP latch off. On the other hand, over temperature protection may also be triggered under an over current condition and the device will OTP latch off.

The Buck regulator also features cycle-by-cycle "peak" current limit (top FET current limit). During t_{ON} time, the high-side power switch current is monitored. If the monitored current exceeds the top FET current limit, the high-side power switch is turned off, the low-side synchronous rectifier is turned on and then t_{ON} is inhibited. t_{ON} can be not inhibited any more once low-side synchronous rectifier current is lower than the bottom FET current limit value.

Buck Output Under Voltage Protection (UVP)

If V_{OUT} < ~33% of the set point for approximately 10μs occurring when the output short circuit or the load current is heavier than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the device will latch off. Recycling S5 input to re-enable the device.



Buck Output Over Voltage Protection (OVP)

This device includes Buck output over voltage protection (OVP). If the output voltage rises above the feedback regulation level, the high-side power switch naturally remains off and different actions are adopted in different operation mode.

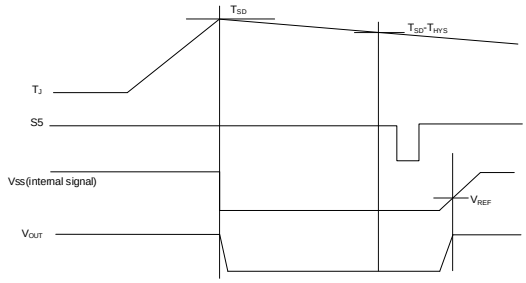
When operating in PFM light load mode, if the output voltage remains high, the low-side synchronous rectifier remains on until the inductor current reaches zero and the switching actions are suppressed. If the output voltage doesn't exceed over voltage protection threshold, the switching actions will be recovered once the combined feedback and ramp signals become lower than the reference voltage. If the output

voltage exceeds over voltage protection threshold and lingers for one OVP delay time, the output over voltage protection (OVP) will be triggered, and the device will latch off. Recycling S5 input to re-enable the device.

When operating in USM light load mode, if the output voltage remains high, the low-side synchronous rectifier forced turn on time will be longer and inductor current average value becomes more and more negative until the reverse current limit is triggered, trying to make output voltage lower. If the output voltage continues to rise and exceeds the output over voltage threshold for more than OVP delay time, the output over voltage protection (OVP) will be triggered, and the device will latch off. Recycling S5 input to re-enable the device. False OVP may happen under USM light load condition if the inductance is chosen too small and reverse current limit is triggered.

Buck Over Temperature Protection (OTP)

Instant-PWM includes Buck over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. When the Buck thermal sensor detects that the buck junction temperature exceeds 150°C, the over temperature protection (OTP) will be triggered, and the device will latch off. Recycling S5 input to re-enable the device after the junction temperature cools down about 15°C.

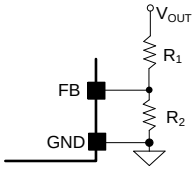


Design Procedure

Feedback Resistor Selection

Choose R_1 and R_2 to program the proper Buck output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is strongly recommended for both resistors. If V_{SET} is 1.2V, R_1 = 100kΩ is chosen, then using following equation, R_2 can be calculated to be 100kΩ.

$$R_2 = \frac{0.6V}{V_{SET}-0.6V} \times R_1$$



Buck Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

Instant-PWM operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost and size for a particular application. Selecting a low inductor value will help reduce size and cost and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low value inductors may help reduce DC losses and increase efficiency. On the other hand, higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) about 20% ~ 50% of the desired full output load current. Start by calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$) and estimating a ΔI_L as some percentage of that current.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

And $I_{L,PEAK} = I_{OUT,MAX} + \Delta I_L/2$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

If USM light load operation is selected, make sure the inductor value is high enough to avoid reverse current limit is been triggered just under steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Low loss ferrite materials should be considered.

Buck Inductor Design Example

Consider a typical design for a device providing 1.2V_{OUT} at 9A from 20V_{IN}, operating at 600kHz and using target inductor ripple current (ΔI_L) of 40% or

3.6A. Determine the approximate inductance value at first:

$$L_1 = \frac{1.2V \times (20V - 1.2V)}{20V \times 600kHz \times 3.6A} = 0.52\mu H$$

Next, select the nearest standard inductance value, in this case 0.56µH, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{1.2V \times (20V - 1.2V)}{20V \times 600kHz \times 0.56\mu H} = 3.36A$$

$I_{L,PEAK}$ = 9A + 3.36A/2 = 10.68A

The resulting 3.36A ripple current is 3.36A/9A is ~37.3%, well within the 20% ~ 50% target.

$I_{L,PEAK,RVS}$ = 3.36A/2 = 1.68A < $I_{LIM,RVS}$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 10.68A.

Buck Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current,

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

On the other hand, the input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1\text{-}D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications two 10µF X5R capacitors are sufficient. Take care to locate the ceramic input capacitor as close to the device IN and GND pin as possible.

Buck Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Buck Output Ripple

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 3.36A using four 22µF ceramic capacitors, each with an ESR of ~6mΩ for parallel total of 88µF and 1.5mΩ ESR.

$$V_{RIPPLE,ESR} = 3.36A \times 1.5m\Omega = 5.04mV$$

$$V_{RIPPLE,CAP} = \frac{3.36A}{8 \times 88\mu F \times 600kHz} = 7.95mV$$

Total ripple = 12.99mV. The actual capacitive ripple may be higher than calculated value because the capacitance decreases with the voltage on the capacitor.

Using a 150µF 40mΩ POS cap, the above result is

$$V_{RIPPLE,ESR} = 3.36A \times 40m\Omega = 134.4mV$$

$$V_{RIPPLE,CAP} = \frac{3.36A}{8 \times 150\mu F \times 600kHz} = 4.67mV$$

Total ripple = 139.07mV

Buck Output Transient Undershoot/Overshoot

If very fast load transient must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions,

however, some considerations must be needed, especially when using small ceramic capacitors which have low capacitance at low output voltages which results in insufficient stored energy for load transient. Output transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as $V_{ESR} = \Delta I_{OUT} \times ESR$. Using the ceramic capacitor example above and a fast load transient of ± 4.5A, $V_{ESR} = \pm 4.5A \times 1.5m\Omega = \pm 6.75mV$. The POS capacitor result with the same load transient, $V_{ESR} = \pm 4.5A \times 40m\Omega = \pm 180mV$.

Capacitive undershoot (load increasing) is a function of the output capacitance, the load step, the inductor value and the input-output voltage difference and the maximum duty factor. During a fast load transient, the maximum duty factor of instant-PWM is a function of t_{ON} and the minimum t_{OFF} as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{ON} pulses in this case. The maximum duty factor D_{MAX} may be calculated by

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated by

$$V_{UNDERSHOOT,CAP} = -\frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 5A load increase using the ceramic capacitor case when V_{IN} = 20V.At V_{OUT} = 1.2V, the result is t_{ON} = 100ns, $t_{OFF,MIN}$ = 210ns, D_{MAX} = 100 / (100 + 210) = 0.323 and

$$V_{UNDERSHOOT,CAP} = -\frac{0.56\mu H \times (4.5A)^2}{2 \times 88\mu F \times (20V \times 0.323 - 1.2V)} = -12.25mV$$

Using the POS capacitor case, the above result is

$$V_{UNDERSHOOT,CAP} = -\frac{0.56\mu H \times (4.5A)^2}{2 \times 150\mu F \times (20V \times 0.323 - 1.2V)} = -7.19mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 4.5A load decrease using the ceramic capacitor case above. At V_{OUT} = 1.2V the result is

$$V_{OVERSHOOT,CAP} = \frac{0.56\mu H \times (4.5A)^2}{2 \times 88\mu F \times 1.2V} = 53.69mV$$

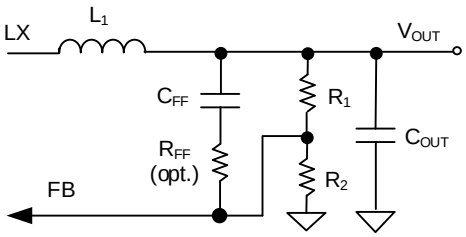
Using the POS capacitor case, the above result is

$$V_{OVERSHOOT,CAP} = \frac{0.56\mu H \times (4.5A)^2}{2 \times 150\mu F \times 1.2V} = 31.5mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

Buck Feed-forward Compensation (R_{FF}, C_{FF})

The SY21240D is internally compensated and optimized for low duty cycle applications. However, in some applications, especially where V_{OUT} > 1.2V, the feedback divider attenuates the AC component of the output. In these cases, transient response may be improved by adding feed-forward compensation. R_{FF} = 1kΩ and C_{FF} = 220pF have been shown to perform well in most applications.



Note that when C_{OUT} > 500µF and minimum load current is low, set feed-forward values as R_{FF} = 1kΩ and C_{FF} = 2.2nF to provide sufficient ripple to FB for small output ripple and good transient behavior.

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the IC package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

$P_{D,MAX} = (T_{J,MAX} - T_A) / \theta_{JA}$

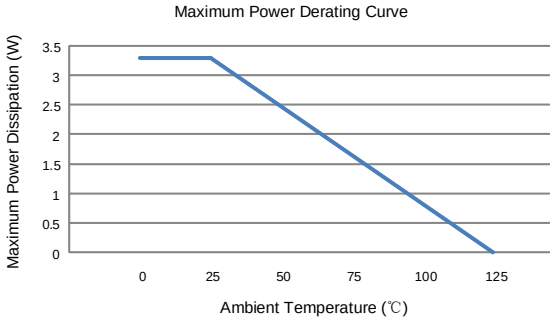
Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125℃. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN3×3-20 package the thermal resistance θ_{JA} is 30 ℃/W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz. copper traces connected to each IC pin and very large, unbroken 1-oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A=25℃ may be calculated by the following formula:
$P_{D,MAX}$ = (125℃ − 25℃) / (30℃/W) = 3.33W

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.



Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

Buck Input Capacitors: Place the input capacitor very near IN and GND, minimizing the loop formed by these connections. And the input capacitor should be connected to the IN and GND by wide copper plane.

Buck Output Capacitors: Guarantee the C_{OUT} negative sides are connected with GND pin by wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.

BIAS Capacitor or RC Filter: Place the BIAS capacitor close to BIAS using short, direct copper trace to one nearest device GND pin (pin 18). Connect a 5Ω resistor before the capacitor if the supply voltage is not one DC source.

VDD2 Capacitor and VDD2 Line: Place the VDD2 capacitor close to VDD2 using short, direct copper trace to one nearest device GND pin (pin 18). Connect VDD2 capacitor positive side to the output capacitor of the regulator directly with a thick (>30 mil) trace to avoid a voltage drop on the input of VDDQ LDO.

VDDQ Capacitors: Place VDDQ output capacitor C_{VDDQ} very near VDDQ and GND, minimizing the loop formed by these connections to achieve better stability and load transient response of VDDQ LDO.

VDDQ Sense Feedback: VDDQSNS should make one kelvin connection with the positive side of VDDQ output capacitor.

Buck Feedback Network: Place the feedback components (R_{FF} and C_{FF}) as close to FF pin as possible. Avoid routing the feedback line near LX, BS or other high frequency signal as it is noise sensitive. Make the feedback sampling point Kelvin connect with C_{OUT} rather than the inductor output terminal.

LX Connection: Keep LX area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Wide LX copper trace between pin 6 and pin 19, 20 should be adopted to improve efficiency.

BS Capacitor: Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX and C_{BS}) as short as possible.

Control Signals: It is not recommended to connect control signals and IN directly. A resistor in a range of 1kΩ to 1MΩ should be used if they are pulled high by IN.

GND Vias: Place adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected by a larger copper area than its size, place five GND vias on it for heat dissipation.

PCB Board: A four-layer layout with 2-oz copper is strongly recommended to achieve better thermal performance. The top layer and bottom layer should place power IN and GND copper plane as wide as possible. Middle1 layer should place all GND layer for conducting heat and shielding middle2 layer signal line from top layer crosstalk. Place signal lines on middle2 layer instead of the other layers, so that the other layers' GND plane not be cut apart by these signal lines.

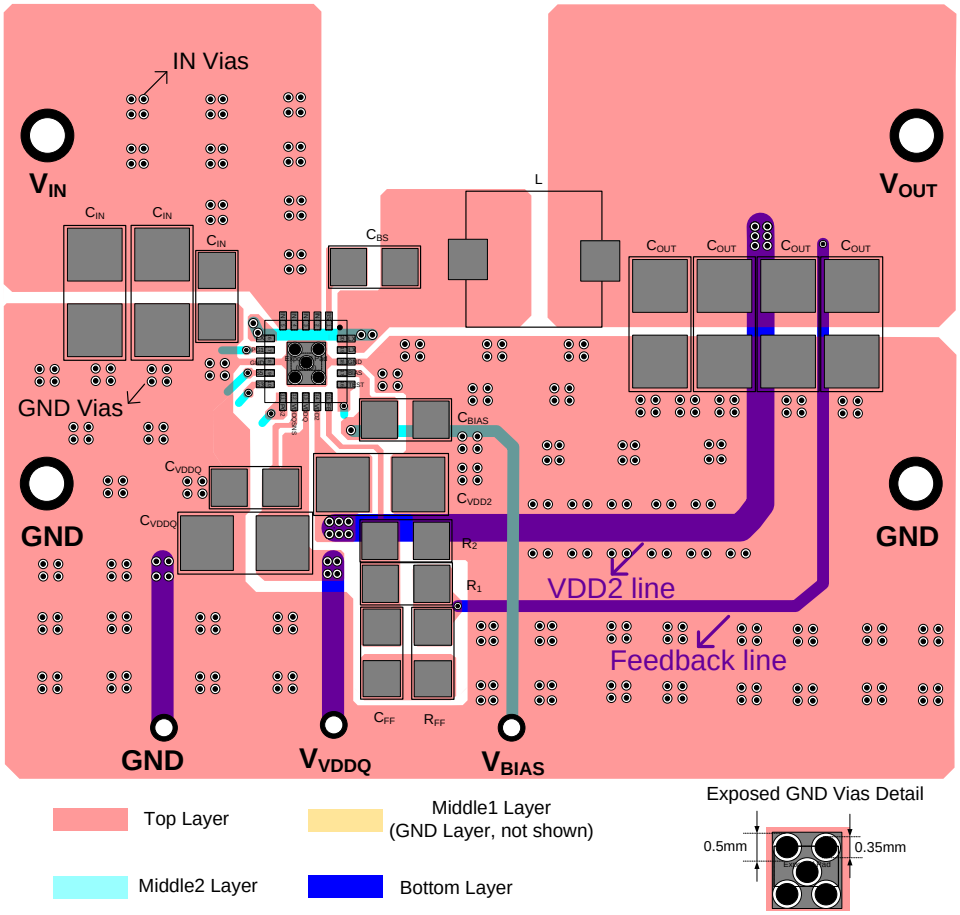
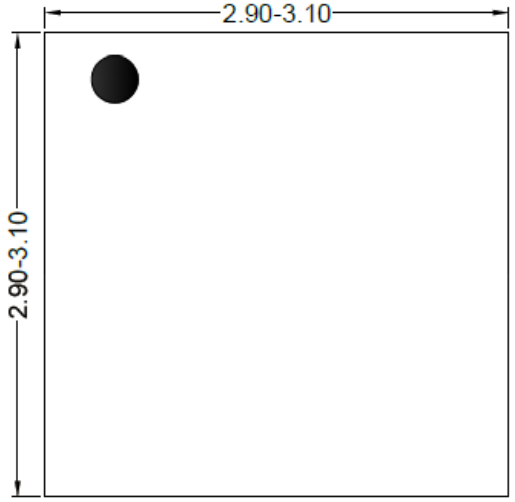
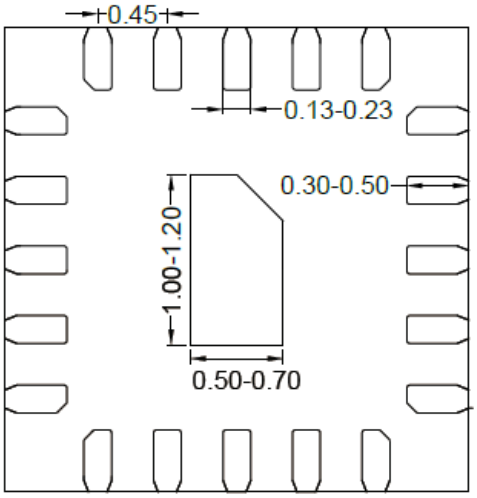


Figure4. PCB Layout Suggestion

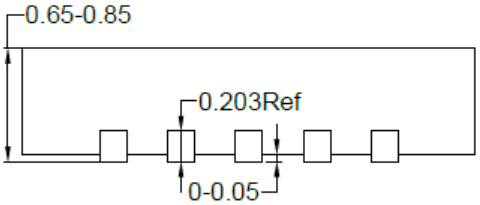
QFN3×3-20 Package Outline



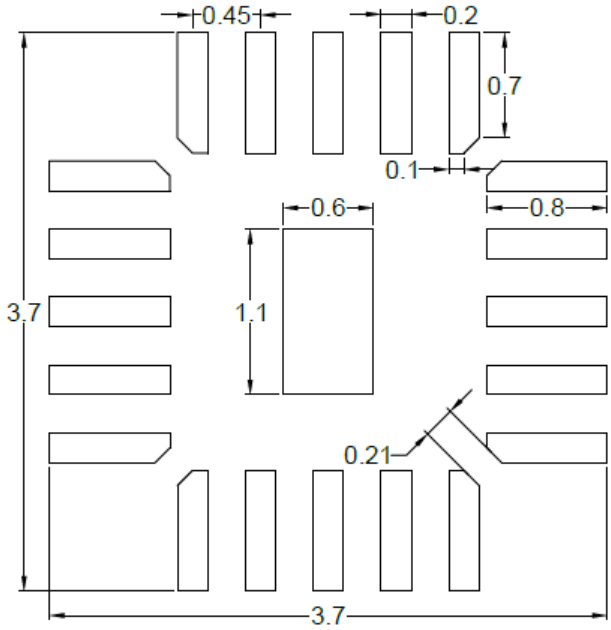
Top view



Bottom view



Side view

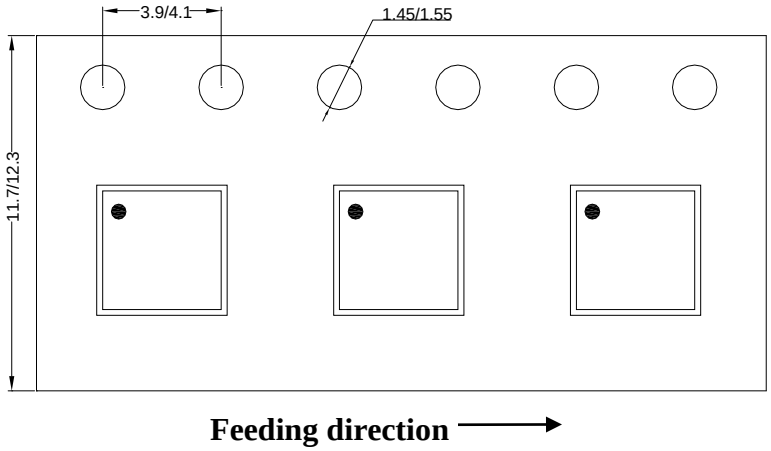


Recommended PCB layout
(Reference only)

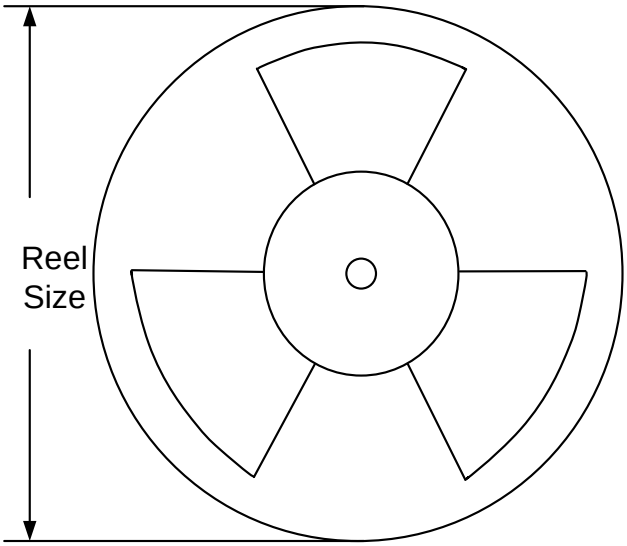
Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

1. QFN3×3-20 taping orientation



2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Jan.14, 2020	Revision 0.9A	Add (IN-LX) voltage in Absolute Maximum Ratings (page 4)
Sep.02, 2020	Revision 0.9	Initial Release

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