

MOSFET - Power, Single N-Channel, STD Gate, TOLL

80 V, 0.89 mΩ, 435 A

NTBLS0D9N08X

Features

- Enhanced Unclamped Inductive Switching (UIS) Capability
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driving Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Supply Unit
- Battery Management System
- Motor Drive
- ORing FET
- Protection FET

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

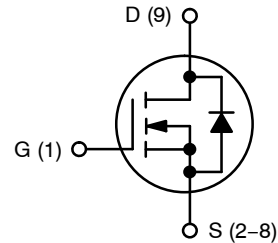
Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	80	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	435	A
	$T_C = 100\text{ }^{\circ}\text{C}$		307	
Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	319	W
Pulsed Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$, $t_p = 100\text{ }\mu\text{s}$	I_{DM}	2691	A
Pulsed Source Current (Body Diode)		I_{SM}	2691	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	$^{\circ}\text{C}$
Continuous Source-Drain Current (Body Diode)	$T_C = 25\text{ }^{\circ}\text{C}$, $V_{GS} = 0\text{ V}$	I_S	430	A
Single Pulse Avalanche Energy ($I_{PK} = 103\text{ A}$)		E_{AS}	530	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- Actual continuous current will be limited by thermal & electromechanical application board design.
- E_{AS} of 530 mJ is based on started $T_J = 25^\circ\text{C}$, $I_{AS} = 103 \text{ A}$, $V_{DD} = 64 \text{ V}$, $V_{GS} = 10 \text{ V}$, 100% avalanche tested.

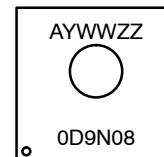
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
80 V	0.89 mΩ @ $V_{GS} = 10 \text{ V}$	435 A

N-CHANNEL MOSFET



H-PSOF8L
CASE 100CU

MARKING DIAGRAM



- A = Assembly Location
 Y = Year
 WW = Work Week
 ZZ = Assembly Lot Code
 0D9N08 = Specific Device Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

NTBLS0D9N08X

THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.47	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	43	

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25\text{ }^{\circ}\text{C}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$, Referenced to $25\text{ }^{\circ}\text{C}$		30		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{ V}, T_J = 25\text{ }^{\circ}\text{C}$			2.0	μA
		$V_{DS} = 80\text{ V}, T_J = 125\text{ }^{\circ}\text{C}$			250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 80\text{ A}, T_J = 25\text{ }^{\circ}\text{C}$		0.7	0.89	m Ω
		$V_{GS} = 6\text{ V}, I_D = 71\text{ A}, T_J = 25\text{ }^{\circ}\text{C}$		1.0	1.4	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 690\text{ }\mu\text{A}, T_J = 25\text{ }^{\circ}\text{C}$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 690\text{ }\mu\text{A}$		-7.5		mV/°C
Forward Transconductance	g_{FS}	$V_{DS} = 10\text{ V}, I_D = 80\text{ A}$		325		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		12620		pF
Output Capacitance	C_{OSS}			3630		
Reverse Transfer Capacitance	C_{RSS}			54		
Output Charge	Q_{OSS}	$V_{DD} = 40\text{ V}, I_D = 80\text{ A}, V_{GS} = 6\text{ V}$ $V_{DD} = 40\text{ V}, I_D = 80\text{ A}, V_{GS} = 10\text{ V}$		259		nC
Total Gate Charge	$Q_{G(TOT)}$			109		
				177		
Threshold Gate Charge	$Q_{G(TH)}$			39		
Gate-to-Source Charge	Q_{GS}			57		
Gate-to-Drain Charge	Q_{GD}			28		
Gate Plateau Voltage	V_{GP}			4.6		
Gate Resistance	R_G	$f = 1\text{ MHz}$		0.5		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(on)}$	Resistive Load, $V_{GS} = 0/10\text{ V}$, $V_{DD} = 40\text{ V}, I_D = 80\text{ A}, R_G = 2.5\text{ }\Omega$		48		ns
Rise Time	t_r			14		
Turn-Off Delay Time	$t_{d(off)}$			75		
Fall Time	t_f			13		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$I_S = 80\text{ A}, V_{GS} = 0\text{ V}, T_J = 25\text{ }^{\circ}\text{C}$		0.8	1.2	V
		$I_S = 80\text{ A}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^{\circ}\text{C}$		0.6		
Reverse Recovery Time	t_{rr}	$V_{GS} = 0\text{ V}, I_S = 80\text{ A}$, $di/dt = 1000\text{ A}/\mu\text{s}, V_{DD} = 40\text{ V}$		37		ns
Charge Time	t_a			21		
Discharge Time	t_b			16		
Reverse Recovery Charge	Q_{RR}			399		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



TYPICAL CHARACTERISTICS

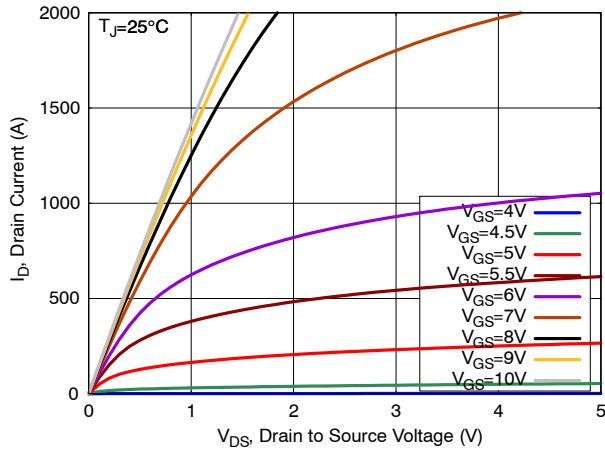


Figure 1. On-Region Characteristics

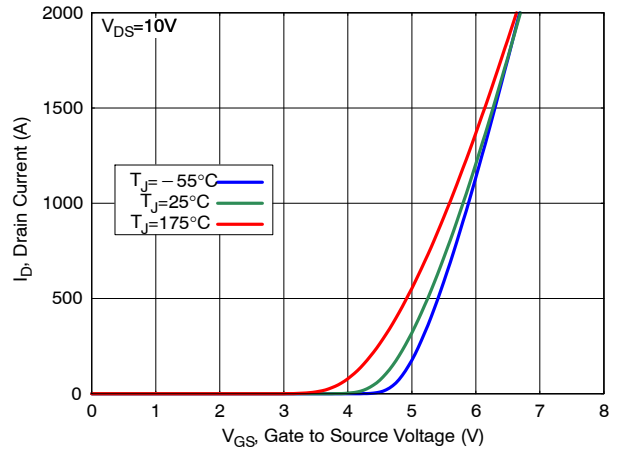


Figure 2. Transfer Characteristics

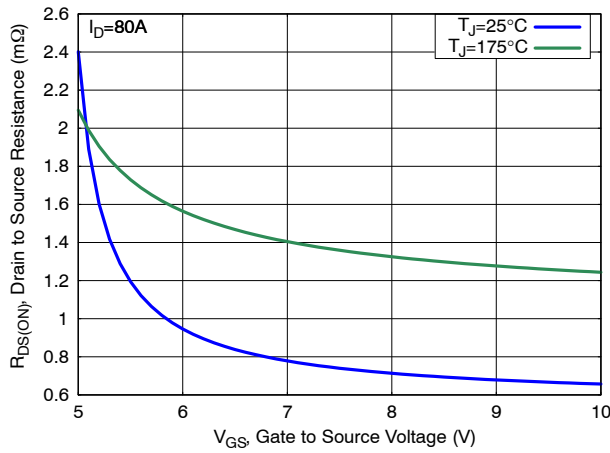


Figure 3. On-Resistance vs. Gate Voltage

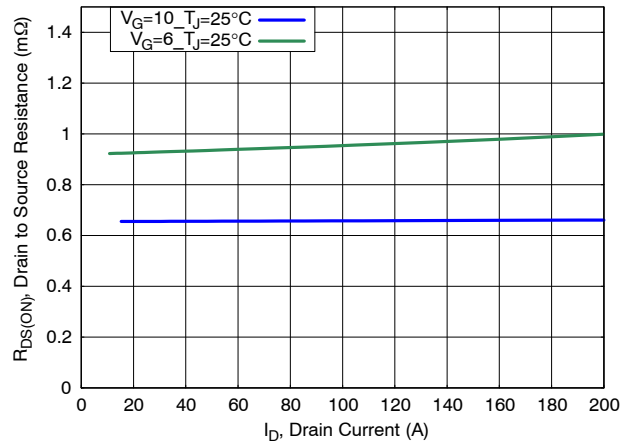


Figure 4. On-Resistance vs. Drain Current

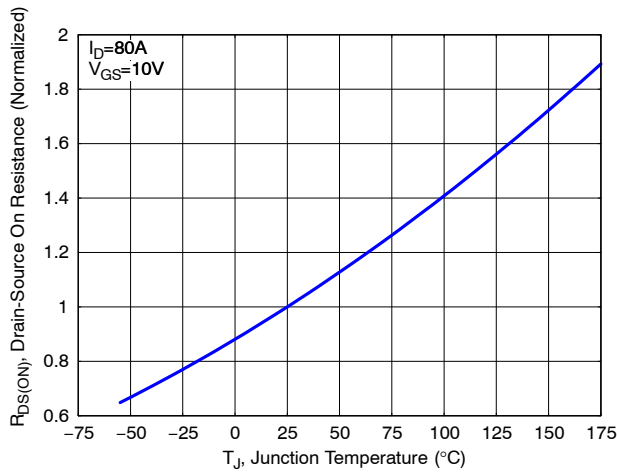


Figure 5. Normalized On-Resistance vs. Junction Temperature

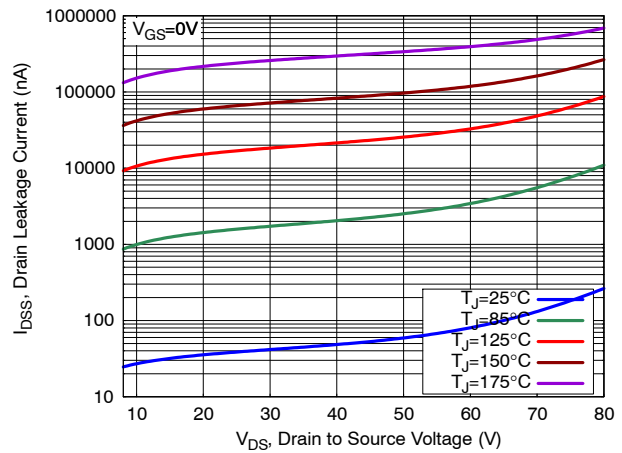


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS

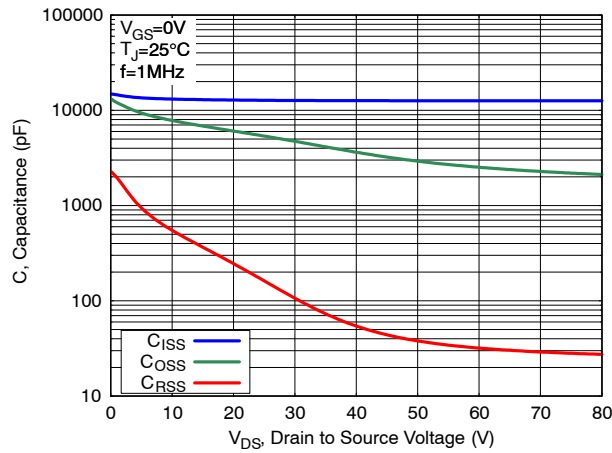


Figure 7. Capacitance Characteristics

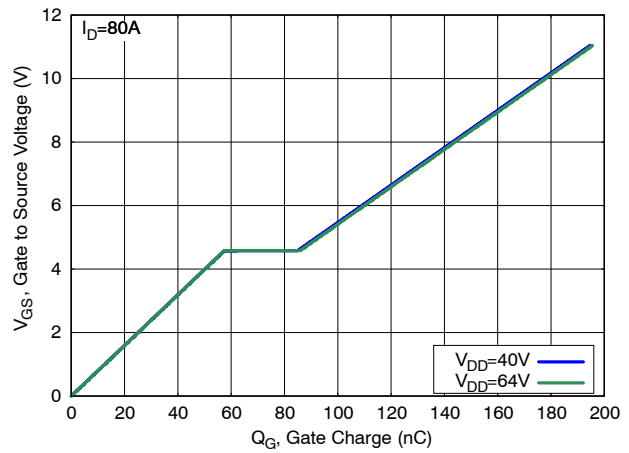


Figure 8. Gate Charge Characteristics

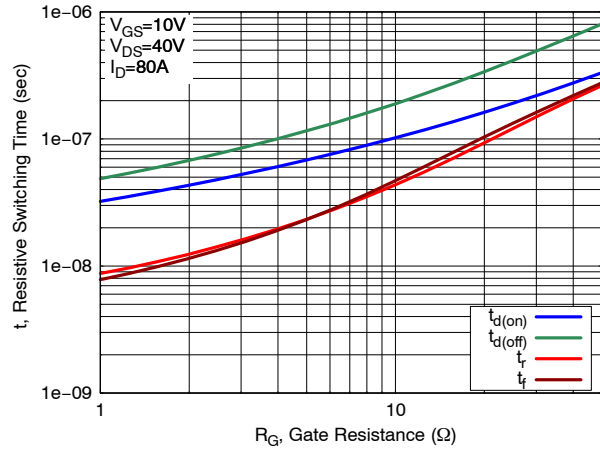


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

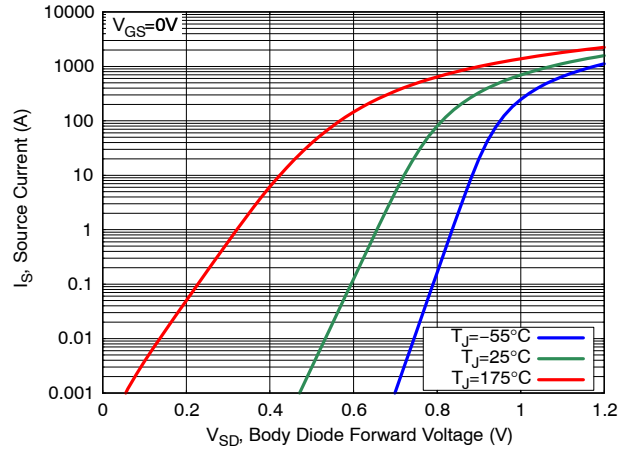


Figure 10. Diode Forward Characteristics

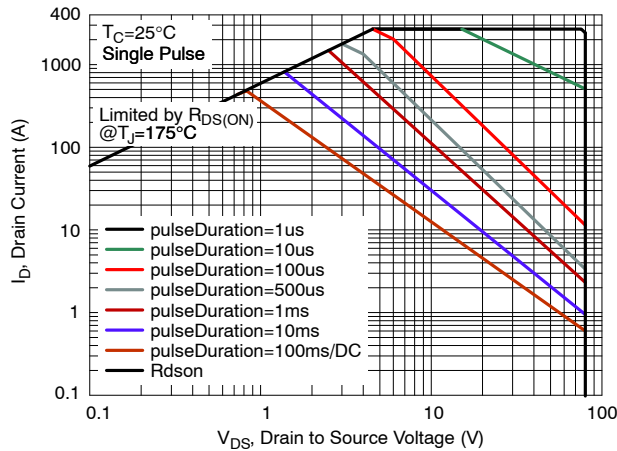


Figure 11. Safe Operating Area (SOA)

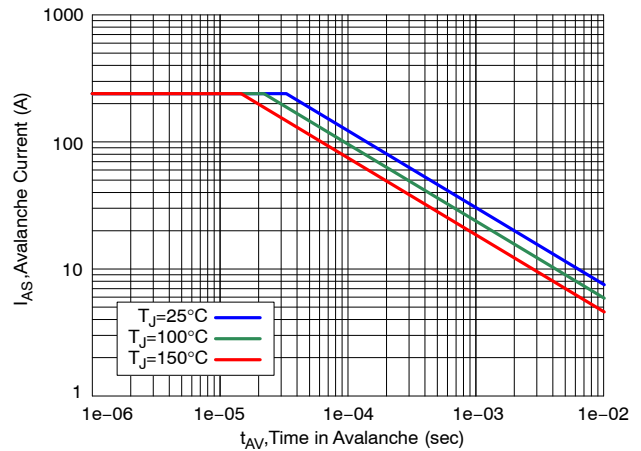


Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS

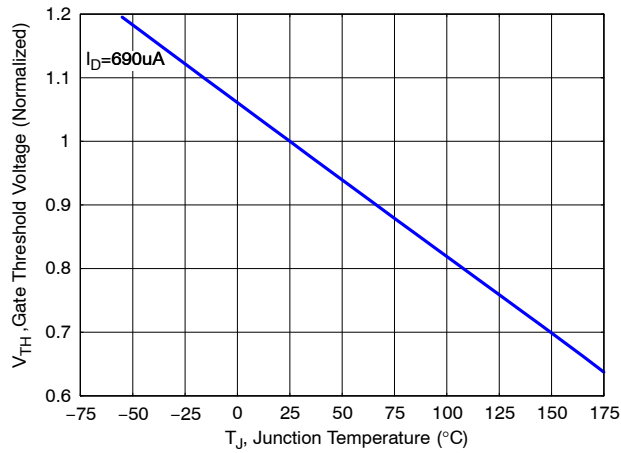


Figure 13. Gate Threshold Voltage vs. Junction Temperature

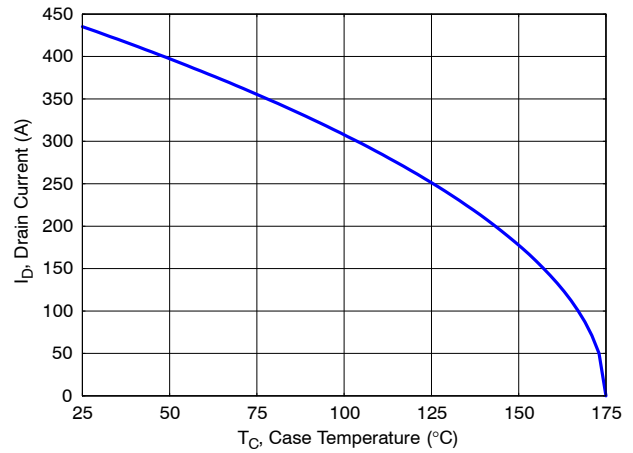


Figure 14. Maximum Current vs. Case Temperature

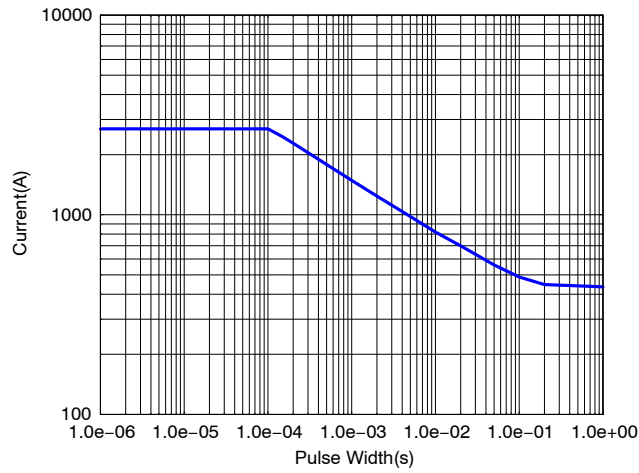


Figure 15. IDM vs. Pulse Width

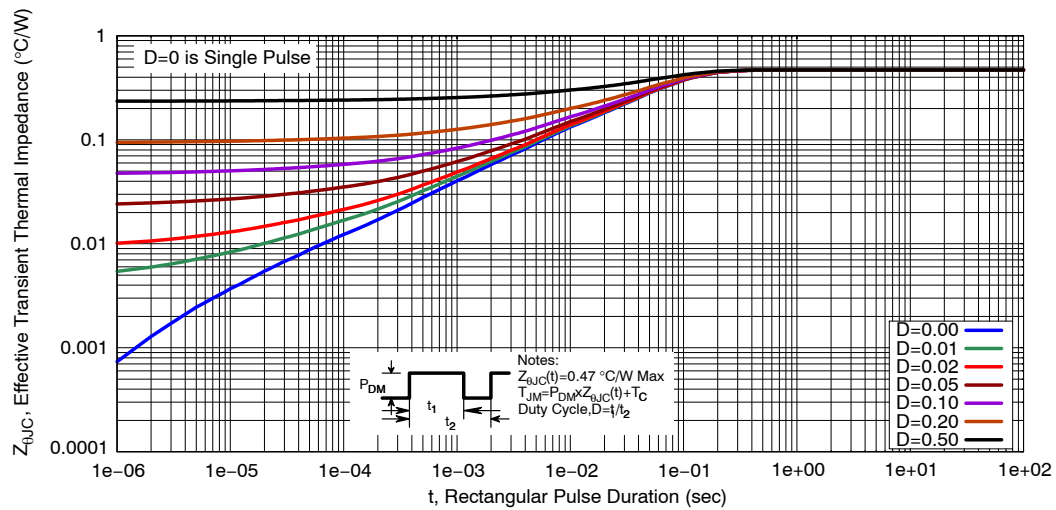


Figure 16. Transient Thermal Response

NTBLS0D9N08X

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTBLS0D9N08XTXG	0D9N08	H-PSOF8L (Pb-Free)	2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



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REVISION HISTORY

Revision	Description of Changes	Date
P0	Initial Preliminary Document release.	1/12/2026
0	Remove preliminary status	1/13/2026

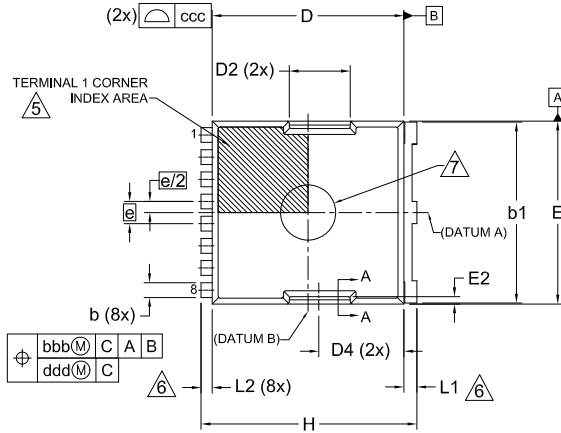
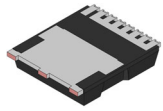


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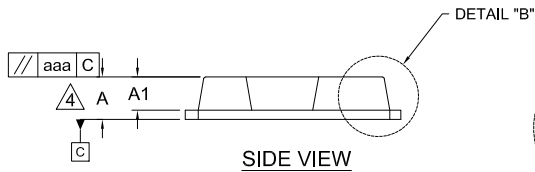
PACKAGE DIMENSIONS

H-PSOF8L 11.68x9.80x2.30, 1.20P
CASE 100CU
ISSUE F

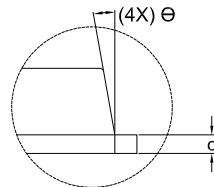
DATE 30 JUL 2024



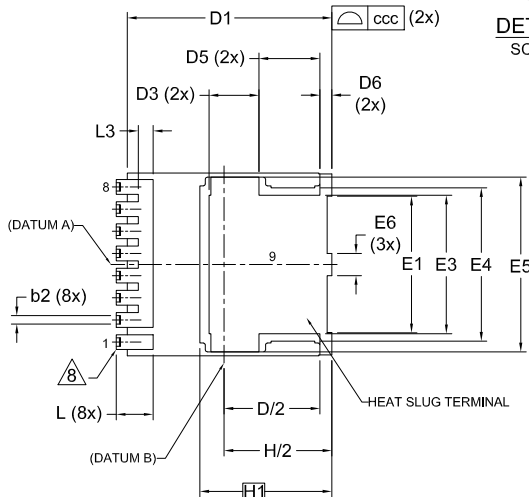
TOP VIEW



SIDE VIEW



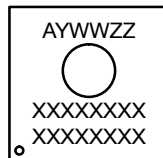
DETAIL "B"
SCALE: 2X



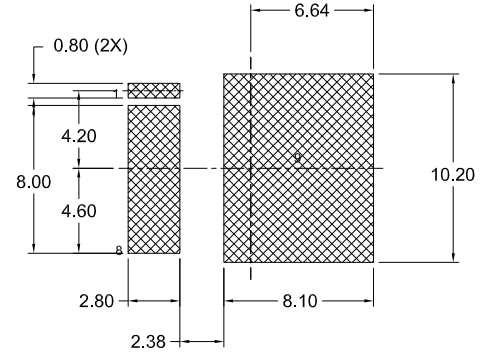
BOTTOM VIEW

GENERIC MARKING DIAGRAM*

A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g., EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1, L1, L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
Θ	10° REF		
Θ1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

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