RICHTEK®

RTQ4554-QT

Automotive Display 4-Channel LED Backlight Driver with I²C Interface

1 General Description

The RTQ4554-QT is a 4-channel LED driver capable of delivering 170mA for each channel with a DC-DC controller. The current-mode switching DC-DC controller supports boost or SEPIC topologies and operates in the 300kHz to 2.2MHz frequency range. The device accepts a wide 3V to 40V input voltage range and withstands direct automotive cold crank and load-dump events. The internal current sinks support a maximum of 3.5% current accuracy and mismatching for excellent brightness uniformity in each string of LEDs.

The RTQ4554-QT automatically detects and disconnects any unconnected and/or broken strings during operation from the control loop to prevent VLED from overvoltage. To provide enough headroom for current sink operation, the boost controller monitors the minimum voltage of the LEDx pins and regulates an optimized output voltage for power efficiency.

The RTQ4554-QT has a standard I²C digital interface for functional settings. Moreover, the boost switching and PWMO frequency can be programmed by the I²C interface. Comprehensive diagnostic information is also available through the I²C interface. When an abnormal situation occurs, a status signal will be sent to the system.

The RTQ4554-QT is available in a 24-pin WQFN package and operates within a temperature range of –40°C to 125°C.

2 Applications

- Automotive Infotainment Displays
- Automotive Instrument Clusters
- Heads-Up Displays

3 Features

- **Wide Operating Input Voltage: 5V to 40V**
  - **Support Cold Crank Down to 3V Supply After Start-Up**
- **High Output Voltage: Up to 45V**
- **NMOS or PMOS Input Protection Switch**
- **Integrated Boost and SEPIC Controller for LED Driver**
  - **Switching Frequency: 300kHz to 2.2MHz**
  - **Spread Spectrum for Reduced EMI**
  - **Automatic Output Voltage Discharged When Controller Is Disabled**
- **4-Channel Current Sinks with 30mA to 170mA per Channel**
- **Channel Current Regulation with Accuracy ±3.5% and Matching 3.5%**
- **Up to 16-Bit Dimming Resolution with I²C or PWM Input**
- **Programmable Multi-Dimming Operation Mode**
  - **Up to 16-Bit PWM and Mixed Dimming Resolution**
  - **Up to 12-Bit DC Dimming Resolution**
- **Dimming Ratio 32000:1 in PWM Mode Using a 152Hz Output PWM Frequency**
- **Dimming Ratio 4000:1 in DC Mode**
- **Advanced Slope Function for Smooth Dimming**
- **Phase-Shift PWM Mode Reduces Audible Noise**
- **Adaptive Headroom Control Method to Optimize Output Voltage for Power Efficiency**
- **Protections**
  - **LED Open and Short Fault**
  - **Boost OCP, OVP, and UVP Protection**
  - **VIN OVP, OCP, and UVLO Fault**
  - **Warming and Over-Temperature Protection**
  - **Extensive Fault Diagnostics and Fault Indicator Signal Output**
- **Embedded Memory with MTP**
- **AEC-Q100 Grade 1 Qualified**
- **Ambient Temperature Range: –40°C to 125°C**
- **Junction Temperature Range: –40°C to 150°C**

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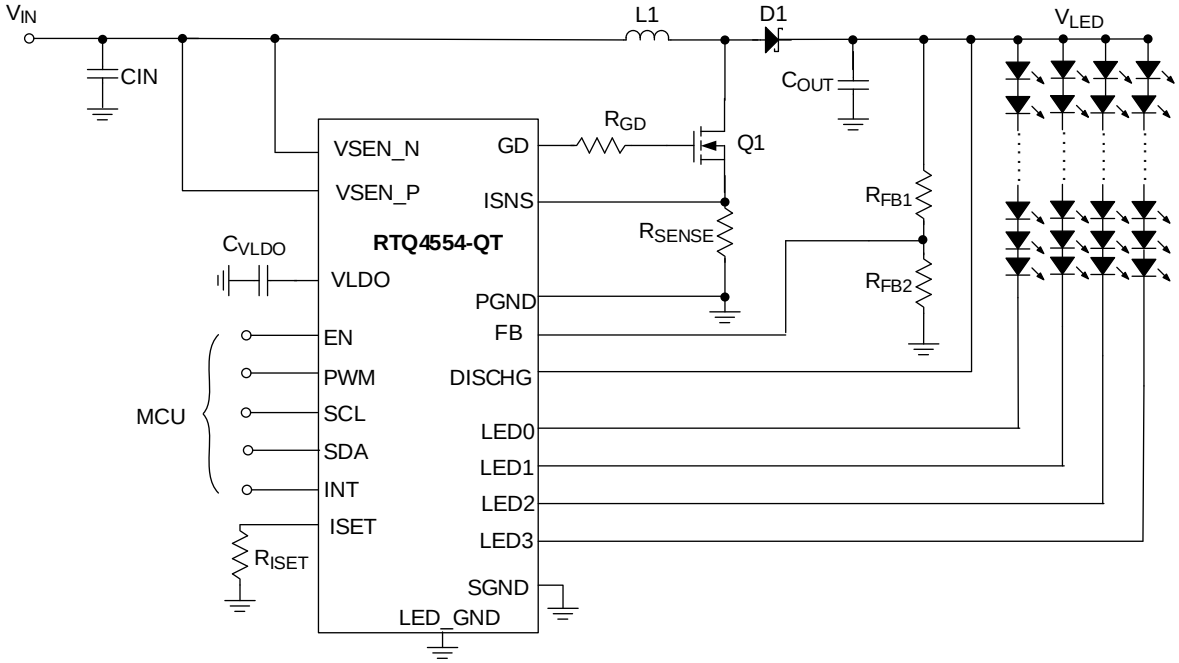
4 Simplified Application Circuit



5 Ordering Information

RTQ4554 □-QT □

Packing
A: Standard

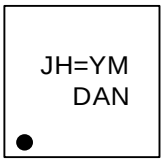
Grade
QT: AECQ100 Qualified

Package Type(1)
N: WQFN-24SL 4x4 (W-Type)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information



JH=: Product Code
YMDAN: Date Code

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Table of Contents

1 General Description ---- 1
2 Applications ---- 1
3 Features ---- 1
4 Simplified Application Circuit ---- 2
5 Ordering Information ---- 2
6 Marking Information ---- 2
7 Pin Configuration ---- 4
8 Functional Pin Description ---- 4
9 Functional Block Diagram ---- 5
10 Absolute Maximum Ratings ---- 6
11 Recommended Operating Conditions ---- 6
12 Electrical Characteristics ---- 7
12.1 System Characteristics ---- 9
13 Typical Application Circuit ---- 13
14 Timing Diagram ---- 17
14.1 Power Sequence ---- 17
15 Typical Operating Characteristics ---- 19
16 Application Information ---- 22
16.1 LED Output Current Setting ---- 22
16.2 ISET Setting Curve ---- 22
16.3 LED Dimming Frequency Setting ---- 23
16.4 Boost Switching Frequency Setting ---- 23
16.5 Dimming Mode ---- 24
16.6 Brightness Control by I2C Interface: ---- 24
16.7 Brightness control by PWM pin: ---- 26
16.8 LED Output String Configuration ---- 28
16.9 LED Current Slope function ---- 28
16.10 Dither Function ---- 29
16.11 LED Headroom and ADHR Function ---- 29
16.12 Spread Spectrum Function ---- 30
16.13 Key Components Selection ---- 30
16.14 Thermal Considerations ---- 37
16.15 Layout Guideline ---- 38
17 Functional Register Description ---- 40
17.1 I^2C Command ---- 40
17.2 MTP Read/Write Function ---- 41
17.3 MTP Program Sequence ---- 43
17.4 MTP Program Application Circuit for Single Chip ---- 43
18 Outline Dimension ---- 71
19 Footprint Information ---- 72
20 Packing Information ---- 73
20.1 Tape and Reel Data ---- 73
20.2 Tape and Reel Packing ---- 74
20.3 Packing Material Anti-ESD Property ---- 75
21 Datasheet Revision History ---- 76

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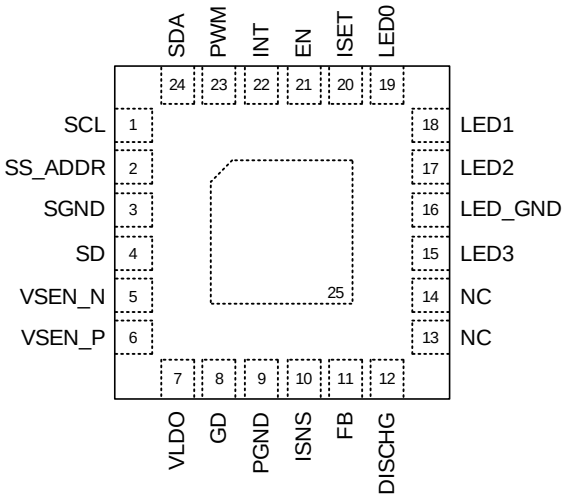
7 Pin Configuration

(TOP VIEW)



WQFN-24SL 4x4

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	SCL	Clock signal pin of the I^2C interface.
2	SS_ADDR	Device Address Select Pin. When SS_ADDRSEL = 0 (Low), the slave address is (0x2Ch). When SS_ADDRSEL = 1 (High), the slave address is (0x3Ch). Set Table 5.
3	SGND	Signal ground.
4	SD	Gate driver output for external power-line N-MOSFET or P-MOSFET control.
5	VSEN_N	Pin for input voltage detection for OVP protection and negative input for input current sense. If input current sensing is not used, connect this pin to the VSEN_P pin.
6	VSEN_P	Pin for input voltage detection for OVP protection and positive input for input current sensing.
7	VLDO	Regulator output for chip internal use only. A 10μF capacitor should be placed on this pin to stabilize the 5V output of the internal regulator.
8	GD	Gate driver output for external power N-MOSFET control.
9	PGND	Power ground.
10	ISNS	Controller current sense positive pin.
11	FB	Controller voltage feedback input.
12	DISCHG	Controller output voltage discharge pin.
13, 14	NC	No internal connection. (Dummy pin which can connect to any level or have the component removed.)
15	LED3	Current sink for LED3. If unused, connect to ground.
16	LED_GND	LED ground.
17	LED2	Current sink for LED2. If unused, connect to ground.

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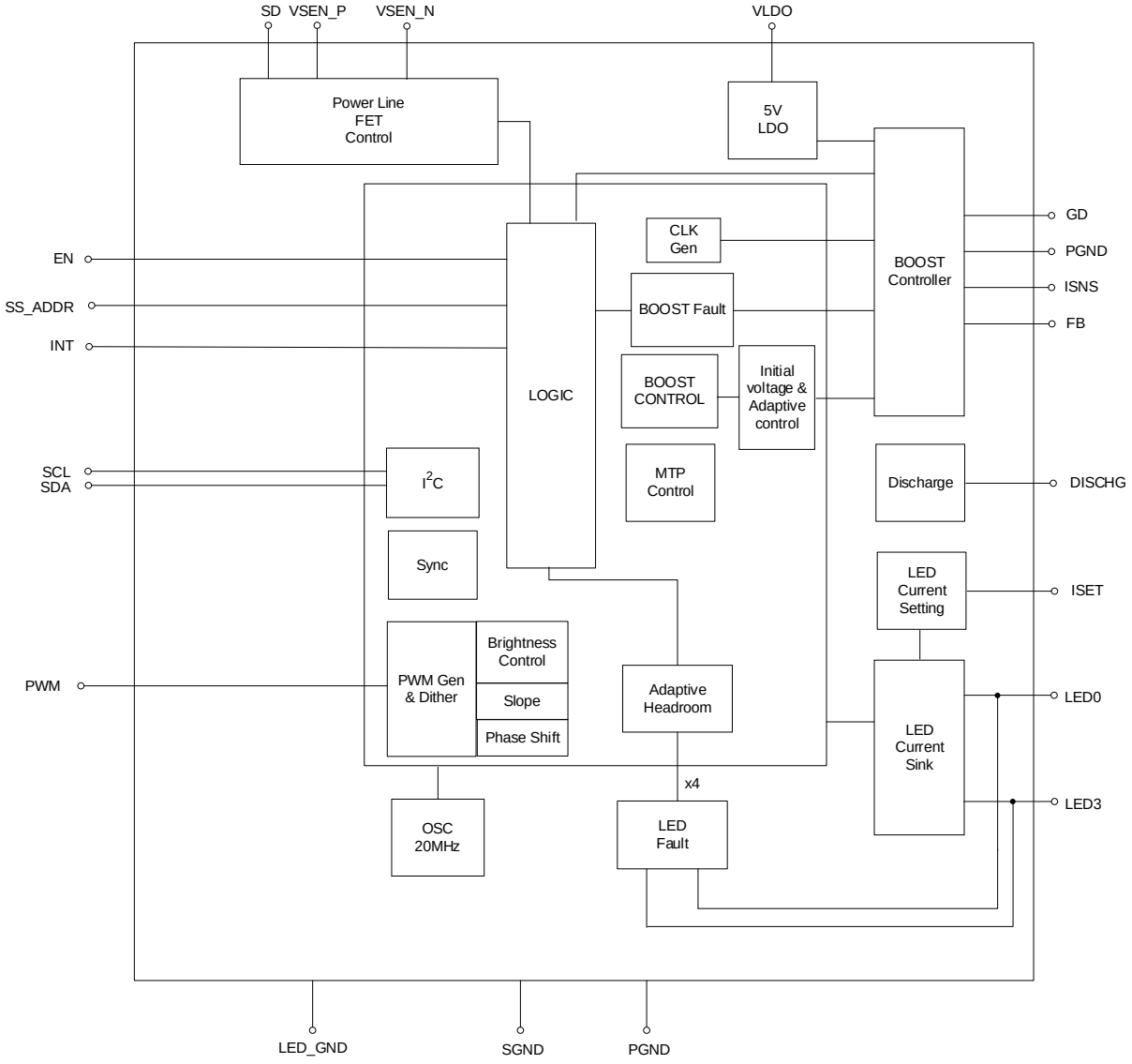
Pin No.	Pin Name	Pin Function
18	LED1	Current sink for LED1. If unused, connect to ground.
19	LED0	Current sink for LED0. If unused, connect to ground.
20	ISET	ILED current setting through an external resistor.
21	EN	Enable input.
22	INT	Status indicator output. This pin will be pulled low if a fault occurs.
23	PWM	PWM input for brightness control.
24	SDA	Data signal pin of the I^2C interface.
25 (Exposed Pad)	GND	The exposed pad must be soldered to a large PCB and connected to the ground for maximum power dissipation.

9 Functional Block Diagram



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10 Absolute Maximum Ratings

(Note 2)

- VSEN_P, VSEN_N, SD, DISCHG, FB, LED0 to LED3 ---------- –0.3V to 49.5V
- EN, PWM, SDA, SCL ---------- –0.3V to 5.5V
- ISNS, VLDO, GD, INT, SS_ADDR, ISET- ---------- –0.3V to 5.5V
- Package Thermal Resistance
- Power Dissipation, P_D @ T_A = 25°C

  WQFN-24SL 4x4 ---------- 2.66W
- Package Thermal Resistance (Note 3)

  WQFN-24SL 4x4, θ_{JA} ---------- 37.57°C/W

  WQFN-24SL 4x4, θ_{JC} ---------- 1.02°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  Human Body Model (HBM), per AEC Q100-002 (Note 5) ---------- ±2kV

  Charged Device Model (CDM), per AECQ100-011

  Corner Pins ---------- ±750V

  Other Pins ---------- ±500V

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

Note 5. AECQ100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

11 Recommended Operating Conditions

(Note 6)

- Ambient Temperature Range ---------- –40°C to 125°C
- Junction Temperature Range ---------- –40°C to 150°C

Note 6. The device is not guaranteed to function outside its operating conditions.

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12 Electrical Characteristics

(V_{IN} = 12V, T_A = T_J = –40°C to 125°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Supply						
VIN Supply Input Voltage	V_{IN}		5	12	40	V
VIN Supply Input Voltage After Start-Up			3	12	40	V
Undervoltage-Lockout Threshold	V_{UVLO_R1}	VIN Rising (Register Setting 1)	3.95	4.3	4.65	V
Undervoltage-Lockout Threshold	V_{UVLO_F1}	VIN Falling (Register Setting 1)	2.35	2.45	2.55	V
Undervoltage-Lockout Threshold	V_{UVLO_R2}	VIN Rising (Register Setting 2)	3.95	4.3	4.65	V
Undervoltage-Lockout Threshold	V_{UVLO_F2}	VIN Falling (Register Setting 2)	3.3	3.45	3.6	V
Undervoltage-Lockout Threshold	V_{UVLO_R3}	VIN Rising (Register Setting 3)	5.1	5.3	5.5	V
Undervoltage-Lockout Threshold	V_{UVLO_F3}	VIN Falling (Register Setting 3)	4.75	4.95	5.15	V
Undervoltage-Lockout Threshold	V_{UVLO_R4}	VIN Rising (Register Setting 4)	7.0	7.3	7.6	V
Undervoltage-Lockout Threshold	V_{UVLO_F4}	VIN Falling (Register Setting 4)	6.65	6.95	7.25	V
Overvoltage Protection Threshold	V_{OVP}	VIN Rising	40.8	43	45.2	V
Overvoltage Protection Threshold Hysteresis	V_{OVP_HYS}		2.0	2.35	2.7	V
Overcurrent Protection Threshold Voltage (Level-I)	V_{TH_OCP1}	RISENSE = 20mΩ IOCP = 11A	187	220	253	mV
Shutdown Current	I_{SHDN}	EN = L	--	1	5	μA
Quiescent Current	I_Q	EN = H, LX no switching, PWM = 0%	6	7	8	mA
Interface Characteristic						
EN, PWM, SS_ADDR, SDA, SCL Input Voltage	V_{IH}		1.2	--	--	V
	V_{IL}		--	--	0.4	V
Internal Pull Low Resistor for EN	R_{PULL_LOW}		0.8	1	1.2	MΩ
INT Pin Output Low Level	V_{OL_INT}	IINT = 3 mA	--	0.3	0.5	V
INT Pin Output Leakage Current	I_{OLK_INT}		--	--	1	μA
Output Leakage Current for SDA	I_{SDA_LK}	SDA Pin Voltage = 3.3V	--	--	1	μA
Boost Controller						
Switching Frequency Accuracy	f_{SW_ACC}	PWM Duty = 100%	–10	--	10	%
Switching Frequency	f_{SW}		303	--	2200	kHz

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Duty Cycle	D	BST_Fsw = 300kHz to 500kHz	88	--	90	%
		BST_Fsw = 1800kHz to 2200kHz	86	--	88	
Inductor Overcurrent Protection Threshold	I_{OCP}	RSENSE = 20mΩ	9	10	11	A
VISNS Threshold	V_{ISNS}	RSENSE= 15 to 50mΩ	180	200	220	mV
Minimum On-Time	t_{ON_MIN}		55	80	105	ns
Overvoltage Protection Threshold (Level-I)	V_{OVP1}	Boost OVP low threshold at the FB pin	1.41	1.43	1.45	V
Overvoltage Protection Threshold (Level-II)	V_{OVP2}	Boost OVP high threshold at the FB pin	1.73	1.76	1.79	V
Overvoltage Protection Threshold (Level-III)	V_{OVP3}	Boost OVP high threshold at the DIS pin	48	50	52	V
Undervoltage Protection Threshold	V_{UVP}	Boost UVP threshold at the FB pin	0.84	0.875	0.91	V
GD Pin Pull-Low Impedance	R_{L_GD}		80	100	120	kΩ
DIS Pin Discharge current	I_{DISCHG}	EN = L	29	33.5	38	mA
Feedback Reference Voltage	V_{REF}		1.17	1.21	1.25	V
LED Current						
Logic Input Leakage Current	I_{ILK}	V_{LEDx} = 48V at LED0~3 pins when EN=0	--	0.1	2.5	μA
Maximum LED Current Setting	I_{LED_MAX}	LED 100% setting at the ISET pin	30	--	170	mA
LED Current Accuracy	$I_{LED_ACC_100\%}$	I_{LEDx} = 150mA, PWM Duty = 100%, All Dimming Mode	–3.5	--	3.5	%
LED Current Matching	$I_{LED_MATCH_100\%}$	I_{LEDx} = 150mA, PWM Duty = 100%, All Dimming Mode	--	--	3.5	%
ISET Pin Undervoltage Protection Threshold	V_{UVP_ISET}	LED_CURRENT[11:0] is written to 0x3FF. Total LED current limited to 70 mA.	0.96	0.99	1.02	V
LED Sink Headroom	$V_{HEADROOM}$	Settings by the Register	0.35	--	0.7	V
LED Sink Headroom Hysteresis	$V_{HEADROOM_HYST}$	Settings by the Register	0.05	--	0.5	V
Saturation Voltage	V_{SAT}	I_{LEDx} = 170 mA, the LED current has dropped by 10% from the value measured at 1V (the LED sink headroom setting 0.7V)	0.25	0.6	0.95	V
ISET Pin Threshold Voltage	V_{ISET}		1.17	1.21	1.25	V
LED Short Detection Threshold	V_{SHORT_LED}		2.6	--	6	V
LED Open Detection Threshold	V_{OPEN_LED}		0.35	--	0.7	V
Power-Line FET and RISENSE Electrical Characteristics						
Current Limit	I_{LIM}	RISENSE = 20mΩ Vsense = 220mV	9.35	11	12.65	A

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VSEN_P Pin Leakage Current	$I_{LEAK_VSEN_P}$	VSEN_P = 40V	--	1	2.5	μA
VSEN_N Pin Leakage Current	$I_{LEAK_VSEN_N}$	VSEN_N = 40V	--	1	2.5	μA
SD Pin Leakage Current	I_{ILK_SD}	VSD = 40V	--	1	--	μA
SD Pull-down current	I_{PD_SD}	RSD = 20kΩ	325	--	450	μA
Gate Driver and GD Current						
High-Side Switch On-Resistance	R_{ON_HS}	Source, VGD/(GDRDSON + total resistance to gate input of SW FET) must not be higher than 2.5A. Source Current= 10mA	1	1.5	2	Ω
Low-Side Switch On-Resistance	R_{ON_LS}	Sink, VGD/(GDRDSON + total resistance to gate input of SW FET) must not be higher than 2.5A. Sink Current= 10mA	0.1	1	1.5	Ω
VLDO Electrical Characteristics						
LDO Output Voltage	V_{LDO}	No LOAD	4.8	5	5.2	V
		I_{LOAD} = 100mA	4.7	5	5.3	
VLDO Source Current	I_{VLDO}		--	--	100	mA
Dropout Voltage	V_{DROP}	I_{LOAD} = 100mA	--	--	800	mV
Current Limit			120	140	160	mA
Spread Spectrum						
SS Modulation Frequency	f_{SS}	Programmable	11	--	30	kHz
SS Frequency Jittering Range	f_{SS_JIT}	Programmable	±3.68	--	±7.13	%
PWM Generator						
LED PWM Output Frequency	f_{PWM_OUT}		0.152	--	19.531	kHz
LED Output Dimming Frequency Accuracy	f_{DIM_ACC}		–10	--	10	%

12.1 System Characteristics

The following specifications are guaranteed by design and are not performed in production testing.

(V_{IN} = 12V, T_A = T_J =-40°C to 125°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Supply						
Quiescent Current	I_Q	EN = H, LX switching, PWM = 0%	--	12.5	--	mA
I2C Interface Timing						
SCL Clock Frequency	f_{SCL}		1	--	400	kHz
(Repeated) Start Hold Time	$t_{HD;STA}$		0.6	--	--	μs
SCL Clock Low Period	t_{LOW}		1.3	--	--	μs
SCL Clock High Period	t_{HIGH}		0.6	--	--	μs

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
(Repeated) Start Setup Time	$t_{SU;STA}$		0.6	--	--	µs
SDA Data Hold Time	$t_{HD;DAT}$		0	--	900	ns
SDA Setup Time	$t_{SU;DAT}$		100	--	--	ns
Rise Time of SDA and SCL Signals	t_R		20	--	300	ns
Fall Time of SDA and SCL Signals	t_F		20	--	300	ns
STOP Condition Setup Time	$t_{SU;STO}$		0.6	--	--	µs
Bus Free Time between Stop and Start	t_{BUF}		1.3	--	--	µs
Capacitive Load for I2C Bus	C_b		--	400	--	pF
Pulse Width of Suppressed Spike	t_{SP}		--	85	--	ns
Time out	t_{OUT}		--	500	--	ms
Output Low Level for SDA	V_{OL_SDA}	External Pull High Current = 3mA	--	0.3	0.5	V
Boost Controller						
Output Voltage	V_{OUT}	Boost Mode, $V_{OUT} > V_{IN}+3$	20	--	45	V
		SEPIC Mode	6	--	24	V
Max Conversion Ratio (V_{OUT}/V_{IN})	M_{MAX}	Boost Mode, I_{OUT} = 4 x 170 mA	--	--	5.5	V/V
		Boost Mode, I_{OUT} = 4 x 100 mA	--	--	10	
		SEPIC Mode	--	--	5	
Soft-Start Time	t_{SS}	Delay from the beginning of boost soft-start to when the LED drivers can begin operation	--	50	--	ms
Power Off Discharge Time	t_{DISCHG}	EN = L	360	400	440	ms
Switching Frequency	f_{SW}	Register AUTO_BST_FREQ_SEL = 0h	273	303	333	kHz
		Register AUTO_BST_FREQ_SEL = 1h	360	400	440	
		Register AUTO_BST_FREQ_SEL = 2h	545	606	667	
		Register AUTO_BST_FREQ_SEL = 3h	720	800	880	
		Register AUTO_BST_FREQ_SEL = 4h	900	1000	1100	
		Register AUTO_BST_FREQ_SEL = 5h	1125	1250	1375	
		Register AUTO_BST_FREQ_SEL = 6h	1500	1667	1834	
		Register AUTO_BST_FREQ_SEL = 7h	1980	2200	2420	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LED Current						
Minimum LED Current Setting	I_{LED_MIN}	I_{LEDx} = 30mA, PWM Duty =1%, PWMO = 19.531 kHz	--	300	--	μA
LED Short Detection Threshold	V_{SHORT_LED}	Register LED_SHORT_THR = 0h	2.35	2.6	2.85	V
		Register LED_SHORT_THR = 1h	2.75	3.0	3.25	
		Register LED_SHORT_THR = 2h	3.25	3.4	3.75	
		Register LED_SHORT_THR = 3h	3.55	3.8	4.05	
		Register LED_SHORT_THR = 4h	3.85	4.2	4.35	
		Register LED_SHORT_THR = 5h	4.3	4.8	4.9	
		Register LED_SHORT_THR = 6h	4.9	5.2	5.5	
		Register LED_SHORT_THR = 7h	5.6	6	6.2	
LED Open Detection Threshold	V_{OPEN_LED}	Register LED_HR_THR = 0h	0.33	0.35	0.37	V
		Register LED_HR_THR = 1h	0.38	0.4	0.42	
		Register LED_HR_THR = 2h	0.43	0.45	0.47	
		Register LED_HR_THR = 3h	0.48	0.5	0.52	
		Register LED_HR_THR = 4h	0.53	0.55	0.57	
		Register LED_HR_THR = 5h	0.58	0.6	0.62	
		Register LED_HR_THR = 6h	0.63	0.65	0.67	
		Register LED_HR_THR = 7h	0.68	0.7	0.72	
Power-Line FET and RISENSE Electrical Characteristics						
Soft-Start Time	t_{SS}	Settings by the Register	25	--	50	ms
SD Pin Leakage Current	I_{ILK_SD}	VSD = 40V	--	1	--	μA
OTP						
Over-Temperature Protection Threshold	T_{OTP}		155	165	175	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
WTP						
Warn-Temperature Protection Threshold	T_{WTP}		--	135	--	°C
Warn-Temperature Protection Hysteresis	T_{WTP_HYS}		--	10	--	°C
Input PWM Electrical Characteristics						
Input Frequency	f_{IN}		0.1	--	20	kHz
Input Minimum On-Time	t_{ON_MIN}		--	200	--	ns
DC DAC Resolution	DAC_{RES}	DC Mode	--	12	--	Bit
PWM Input Resolution	$PWMIN_{RES}$	f_{PWM_IN} = 100Hz	--	16	--	Bit
		f_{PWM_IN} = 20kHz	--	10	--	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Generator						
LED Output Minimum On-Time	$t_{LED_ON_MIN}$		--	200	--	ns
Dither Resolution	$DITHER_{RES}$		--	--	4	Bit
Dimming Resolution	$D_{RES_0.152k}$	PWM Freq =152Hz	--	65536	--	Steps
	$D_{RES_1.221k}$	PWM Freq =1.221kHz	--	16384	--	
	$D_{RES_4.883k}$	PWM Freq = 4.883kHz	--	4096	--	
	$D_{RES_19.531k}$	PWM Freq = 19.531 kHz	--	1024	--	
Dimming Ratio	D_{RI}	f_{PWM_OUT} = 152Hz	--	32000:1	--	
		f_{PWM_OUT} = 4.8kHz with Mixed dimming	--	8000:1	--	
		f_{PWM_OUT} = 4.8kHz	--	1000:1	--	
LED Output Dimming Frequency	f_{DIM}	Register AUTO_PWM_FREQ_SEL = 0h	141	152	163	Hz
		Register AUTO_PWM_FREQ_SEL = 1h	283	305	327	
		Register AUTO_PWM_FREQ_SEL = 2h	567	610	653	
		Register AUTO_PWM_FREQ_SEL = 3h	1135	1221	1307	
		Register AUTO_PWM_FREQ_SEL = 4h	2270	2441	2612	
		Register AUTO_PWM_FREQ_SEL = 5h	4541	4883	5225	
		Register AUTO_PWM_FREQ_SEL = 6h	9082	9766	10450	
		Register AUTO_PWM_FREQ_SEL = 7h	18163	19531	20899	

Note 7. The VIN voltage must rise to a level of 2.8V before I^2C operations can write to the MTP.

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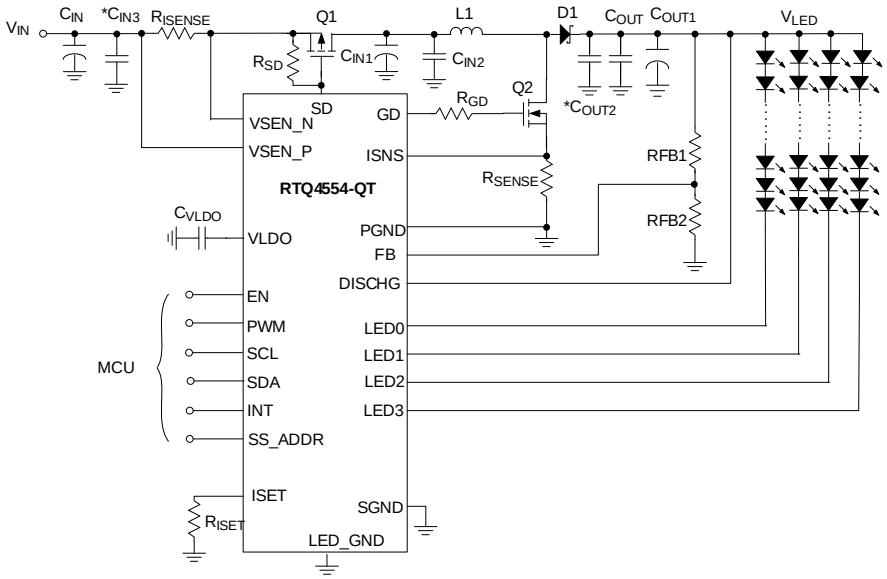
13 Typical Application Circuit

13.1 Boost Controller Mode (P-Type Isolation MOSFET)



Parameter	Description
R_{ISENSE}/R_{SENSE}	20mΩ/2512
R_{SD}	20kΩ/0603
R_{GD}	10Ω/0603
R_{FB2}	100kΩ/0603
R_{FB1}	910kΩ/0603
R_{ISET}	20.8kΩ/0603
C_{LDO}	10μF/16V/±20%/1206
$C_{IN}//C_{IN1}/C_{OUT1}$	33μF/50V/±20%/EEHZC1J330P/Electrolytic/Panasonic
C_{IN2}/C_{OUT}	2x10μF/75V/±20%/1210/CGA6P1X7R1N106M250AC/TDK
* $C_{IN3}/*C_{OUT2}$ (Note 8)	0.1μF/50V/±20%/0603 (Optional)
L1	22μH/Shielded
D1	100V/10A/Schottky diode
Q2	60V/50A/N-MOS
Q1	60V/52A/P-MOS

Note 8. *C_{IN3} and *C_{OUT2}: Optional components.

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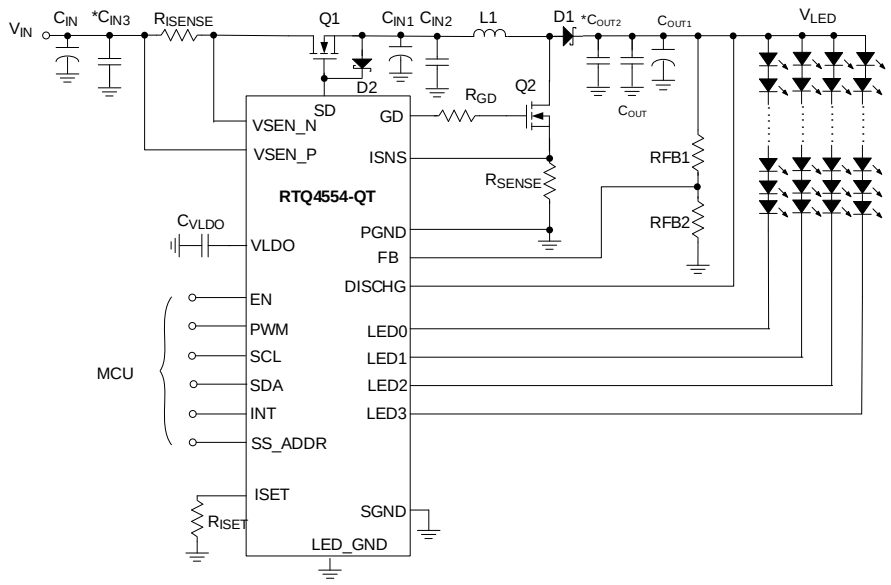
13.2 Boost Controller Mode (N-Type Isolation MOSFET)



Parameter	Description
R_{ISENSE}/R_{SENSE}	20mΩ/2512
R_{SD}	20kΩ/0603
R_{GD}	10Ω/0603
R_{FB2}	100kΩ/0603
R_{FB1}	910kΩ/0603
R_{ISET}	20.8kΩ/0603
C_{LDO}	10μF/16V/±20%/1206
$C_{IN}//C_{IN1}/C_{OUT1}$	33μF/50V/±20%/EEHZC1J330P/Electrolytic/Panasonic
C_{IN2}/C_{OUT}	2x10μF/75V/±20%/1210/CGA6P1X7R1N106M250AC/TDK
* $C_{IN3}/*C_{OUT2}$ (Note 9)	0.1μF/50V/±20%/0603 (Optional)
L1	22μH/Shielded
D1	100V/10A/Schottky diode
D2	100V/0.15A/General diode
Q1/Q2	60V/50A/N-MOS

Note 9. *C_{IN3} and *C_{OUT2}: Optional components.

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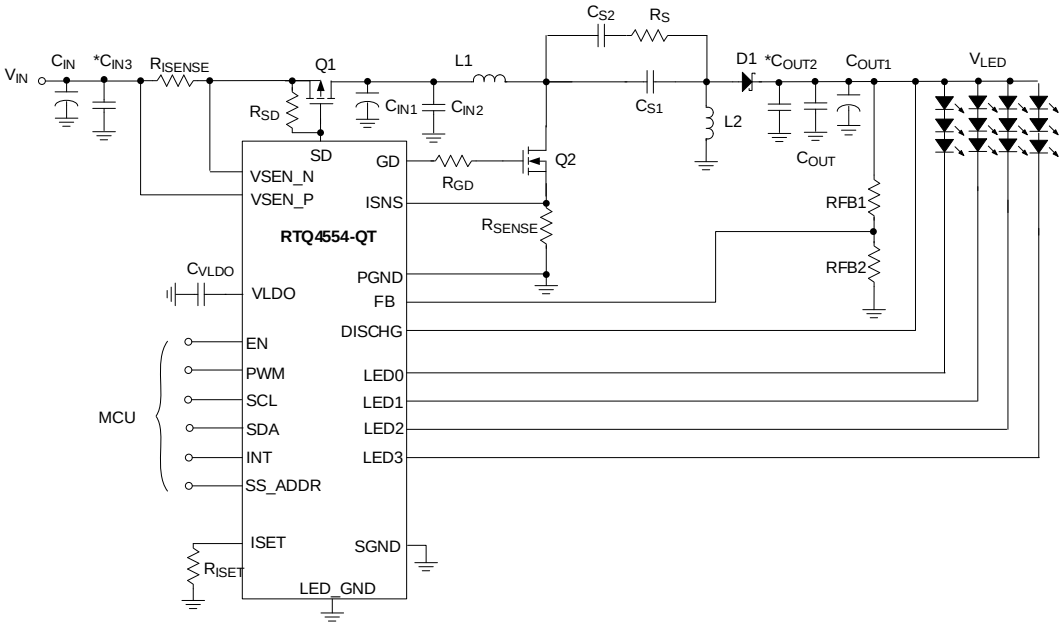
13.3 SEPIC Controller Mode (P-Type Isolation MOSFET)



Parameter	Description
R_{ISENSE}/R_{SENSE}	20mΩ/2512
R_{SD}	20kΩ/0603
R_{GD}	10Ω/0603
R_{FB2}	170kΩ/0603
R_{FB1}	510kΩ/0603
R_{ISET}	20.8kΩ/0603
R_S	2Ω/0603
C_{LDO}	10μF/16V/±20%/1206
$C_{IN}//C_{IN1}/C_{OUT1}/C_{S2}$	33μF/50V/±20%/EEHZC1J330P/Electrolytic/Panasonic
C_{IN2}/C_{OUT}	2x10μF/75V/±20%/1210/CGA6P1X7R1N106M250AC/TDK
* C_{IN3}/*C_{OUT2} (Note 10)	0.1μF/50V/±20%/0603 (Optional)
C_{S1}	10μF/75V/±20%/1210
D1	100V/10A/Schottky diode
Q2	60V/50A/N-MOS
Q1	60V/52A/P-MOS
L1, L2	15μH/Shielded

Note 10. *C_{IN3} and *C_{OUT2}: Optional components.

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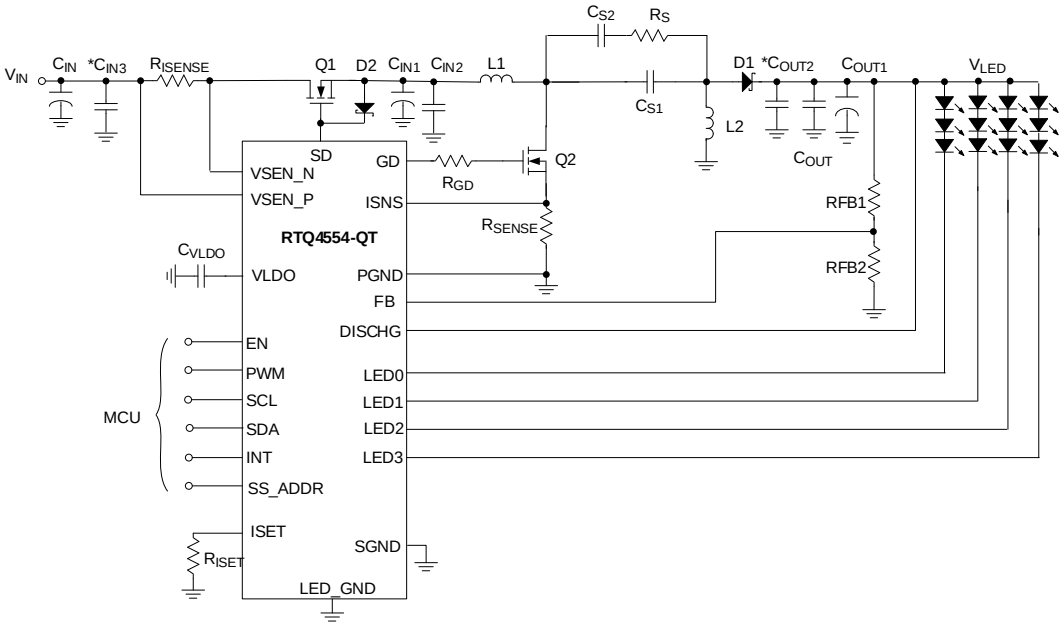
13.4 SEPIC Controller Mode (N-Type Isolation MOSFET)



Parameter	Description
R_{ISENSE}/R_{SENSE}	20mΩ/2512
R_{SD}	20kΩ/0603
R_{GD}	10Ω/0603
R_{FB2}	170kΩ/0603
R_{FB1}	510kΩ/0603
R_{ISET}	20.8kΩ/0603
R_S	2Ω/0603
C_{LDO}	10μF/16V/±20%/1206
C_{IN}//C_{IN1}/C_{OUT1}/C_{S2}	33μF/50V/±20%/EEHZC1J330P/Electrolytic/Panasonic
C_{IN2}/C_{OUT}	2x10μF/75V/±20%/1210/CGA6P1X7R1N106M250AC/TDK
* C_{IN3}/*C_{OUT2} (Note 11)	0.1μF/50V/±20%/0603 (Optional)
C_{S1}	10μF/75V/±20%/1210
D1	100V/10A/Schottky diode
D2	100V/0.15A/General diode
Q1/Q2	60V/50A/N-MOS
L1, L2	15μH/Shielded

Note 11. *C_{IN3} and *C_{OUT2}: Optional components.

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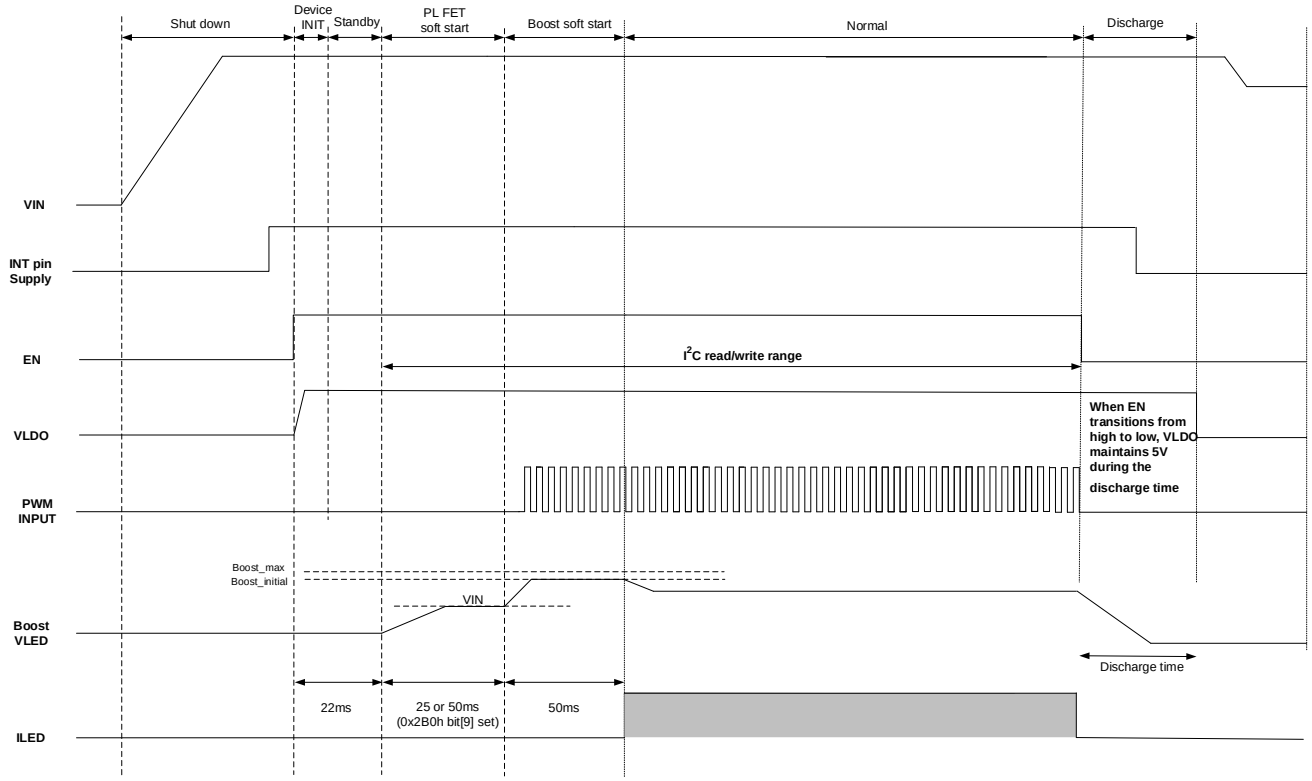
14 Timing Diagram

14.1 Power Sequence



Suggested Power Sequence:

Power On: VIN → INT pin supply → EN → PWM

Power Off: PWM → EN → INT pin supply →VIN

1. Shutdown Mode

When EN is pulled low, the boost (controller), power-line FET, and LED outputs are turned off, and the device tries to discharge the boost output for 50 to 400ms (Register DISCH_SEL can set to disable, 100ms, 200ms, or 400ms). After this period, the device is completely turned off.

2. Device Initialization

When the voltage at the EN pin exceeds VIH and the internal LDO starts up, the device initialization begins after the VLDO voltage surpasses the UVLO rising level. During this state, the EEPROM default and trim configurations are loaded.

3. Standby Mode

Starting from Standby mode, the device can be accessed via I^2C to change any configuration registers. Moreover, when Register SEQ_CTRL = 0, the device remains in standby mode; and when Register SEQ_CTRL = 1, the device transitions to power-line FET soft-start mode.

4. Power-Line FET Soft-Start

The power-line FET is gradually enabled during this 25ms or 50ms long state via the I^2C interface setting in the register PL_TSS. The boost input and output capacitors are charged to the VIN level. VIN faults for OCP, OVP, and UVP are enabled.

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5. Boost Soft-Start

The boost voltage is ramped up to the initial boost voltage level with a reduced current limit for 50ms. All boost faults are now enabled.

6. Normal Mode

The LED drivers are enabled when PWM goes high or the brightness code with I^2C can be accessed. All LED faults are active.

7. Discharge Mode

When EN goes low from normal mode, the boost output voltage is discharged with a 400ms timer. This state exits when VLDO is still above the LDO UVLO threshold voltage.

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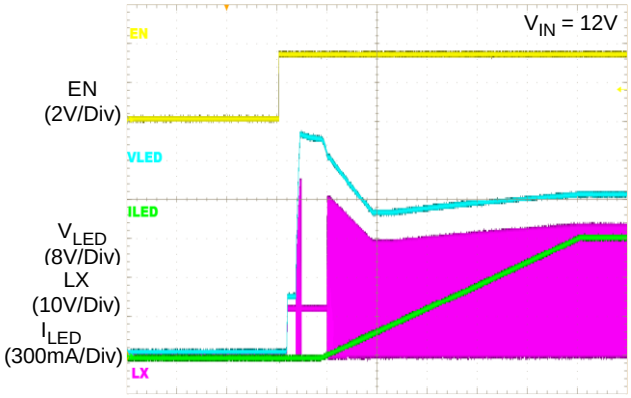
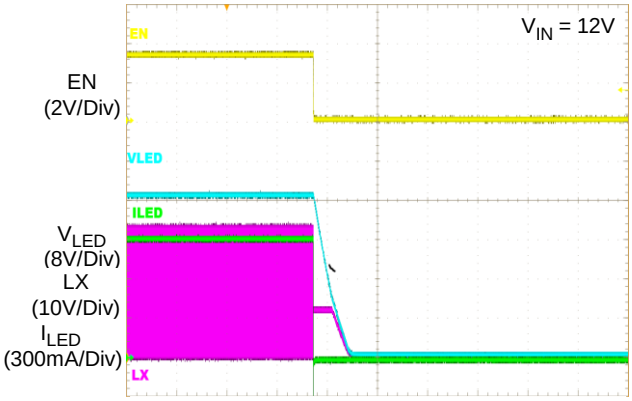
15 Typical Operating Characteristics

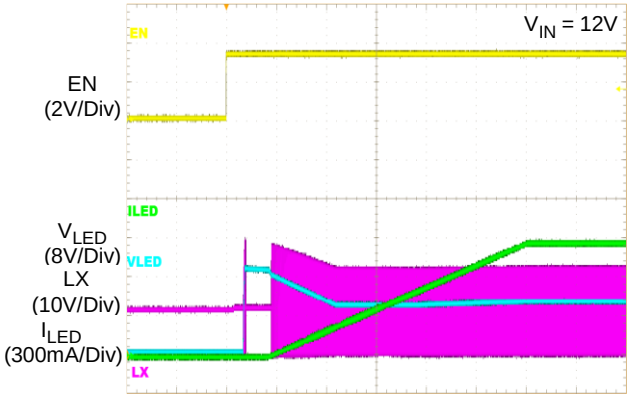
BOOST Power On



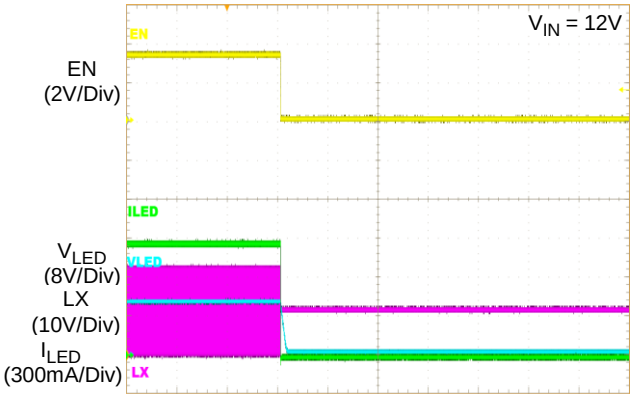
EN BOOST Power Off



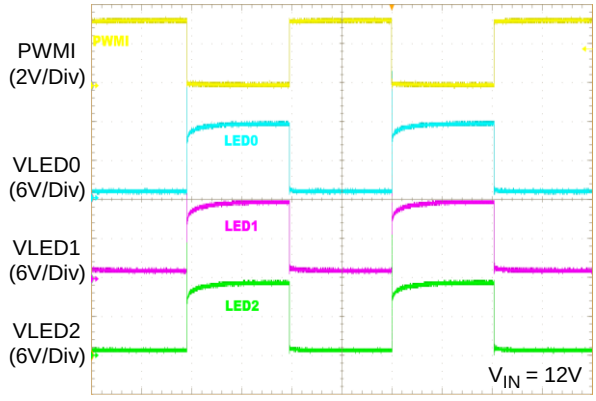
SEPIC Power On



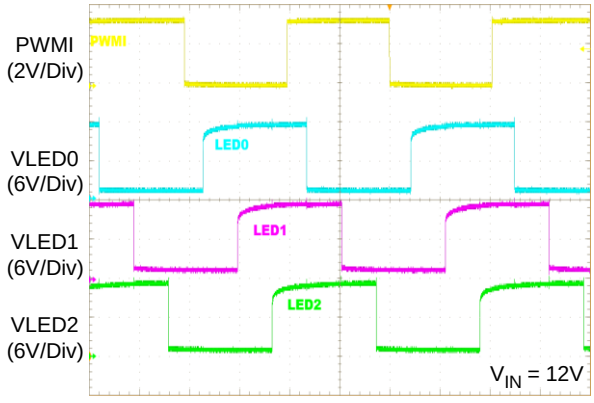
SEPIC Power Off



Direct PWM Mode



Phase Shift PWM Mode



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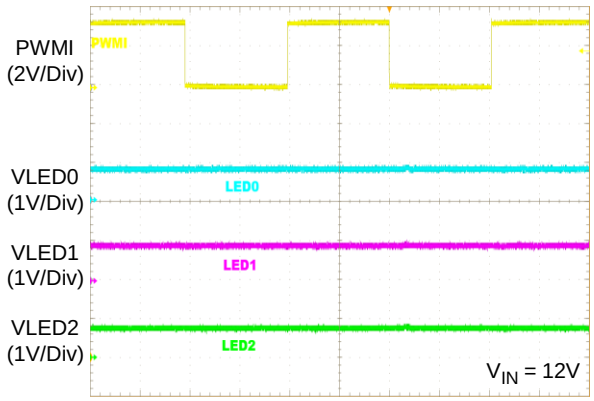
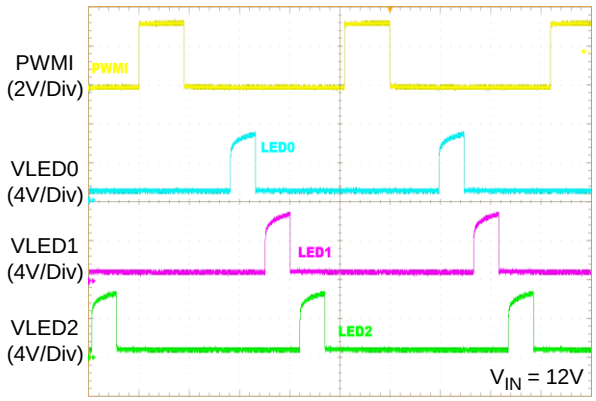
DC Mode



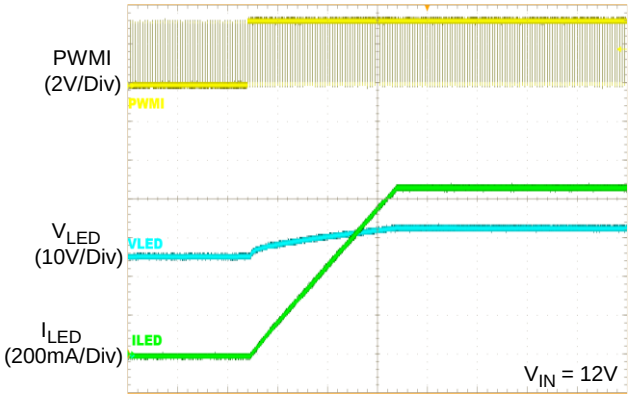
Time (200μs/Div)

Mixed Mode@Duty <25%



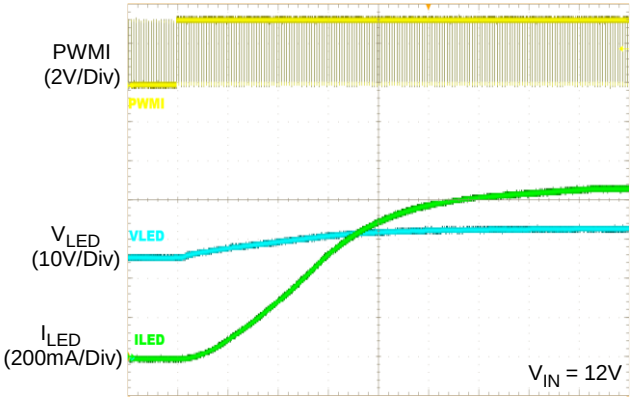
Time (200μs/Div)

Linear Slope



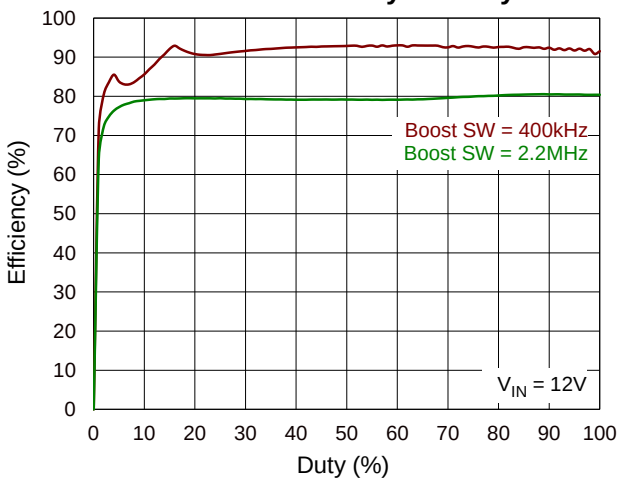
Time (200ms/Div)

Advance Slope

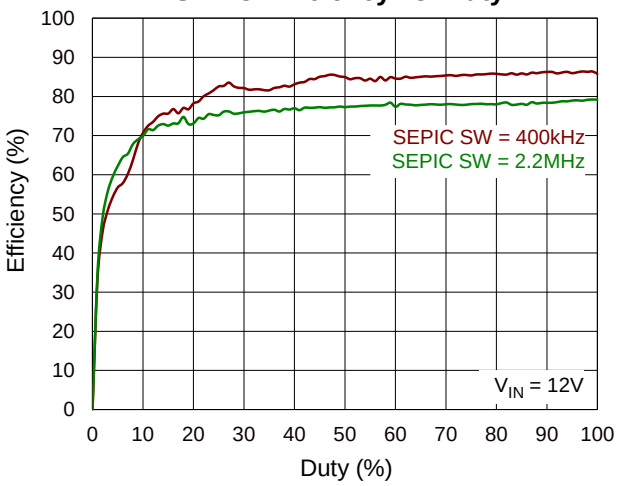


Time (200ms/Div)

BOOST Efficiency vs. Duty



SEPIC Efficiency vs. Duty



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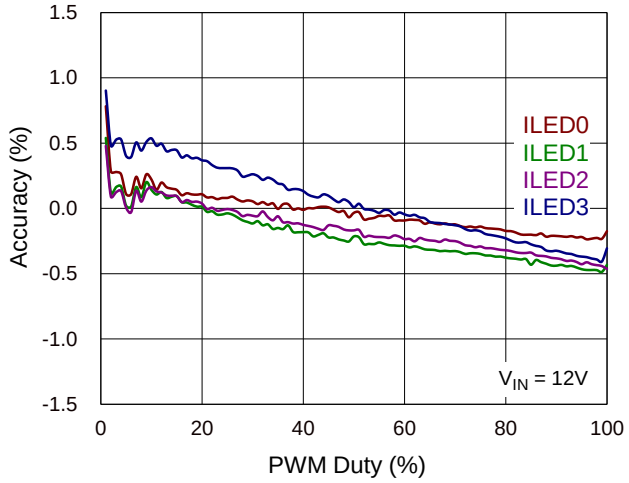
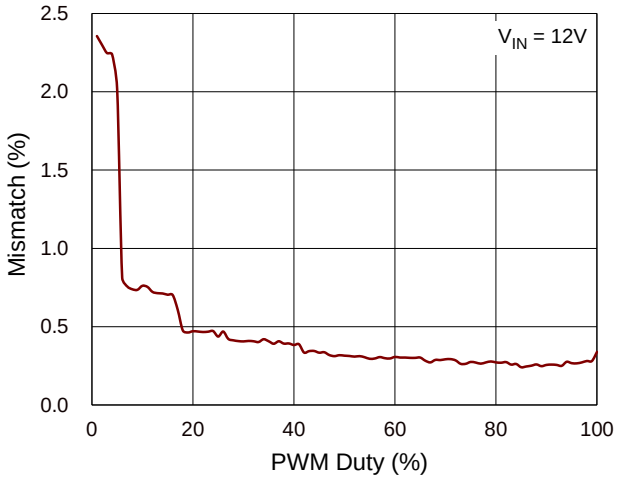
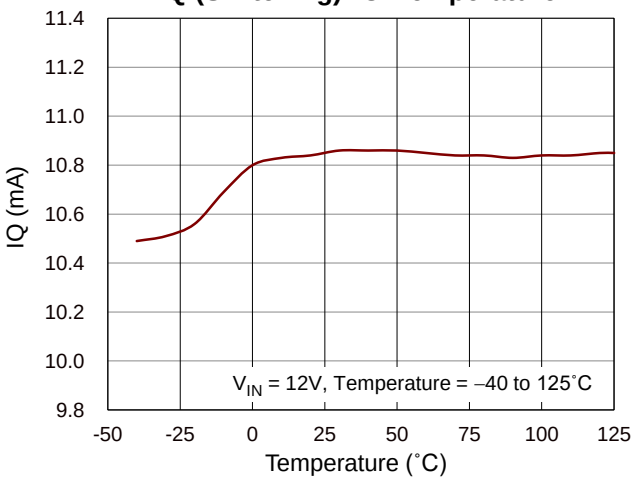
LED Accuracy



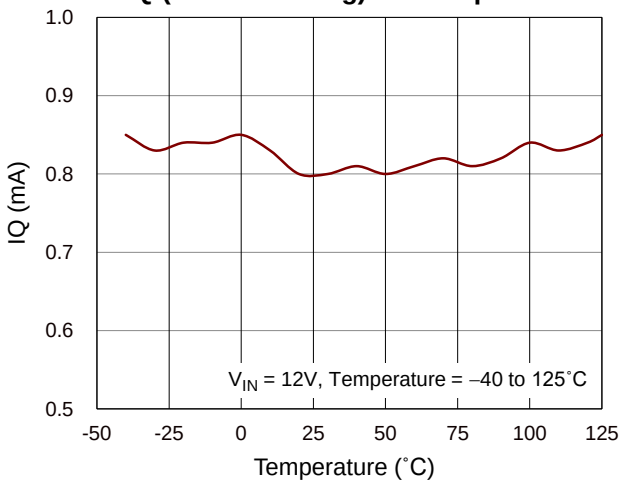
LED Mismatch



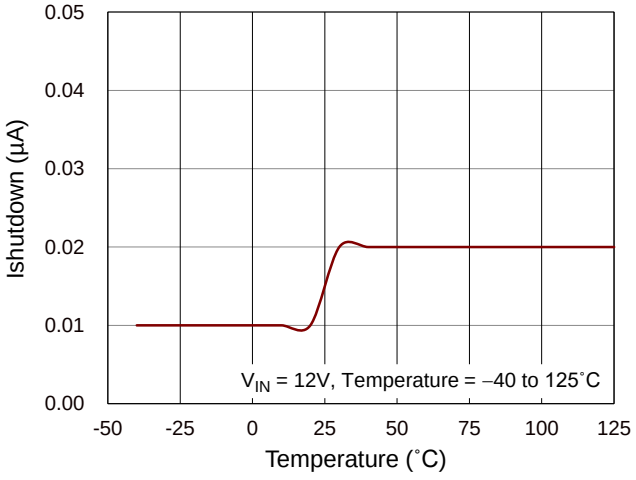
IQ (Switching) vs. Temperature



IQ (Non-switching) vs. Temperature



Ishutdown vs. Temperature



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16 Application Information

(Note 12)

The RTQ4554-QT is designed for automotive applications, with an input voltage VIN intended to be connected to the vehicle battery. Depending on the input voltage, the device can be used in either BOOST mode or SEPIC mode and operates in the 303kHz to 2.2MHz frequency range. The integrated spread spectrum feature helps to reduce EMI. Moreover, the device operates in the -40°C to 125°C temperature range. The internal current sinks support a maximum of 3.5% current mismatching for excellent brightness uniformity in each string of LEDs. LED brightness can be controlled globally through the I^2C interface or PWM input. The boost controller has adaptive output voltage control based on the headroom voltages of the LED current sinks. This feature minimizes the power consumption by adjusting the boost voltage to the lowest sufficient level in all conditions. The RTQ4554-QT supports built-in Direct PWM, Mixed, Phase shift PWM, and DC dimming. The device also embeds a high-resolution architecture to ensure good contrast performance of the display, with a dimming ratio of up to 32000:1 at 152Hz.

16.1 LED Output Current Setting

The maximum output LED current is set by an external resistor value. For the application only using the external resistor RISET to set the maximum LED current for each string, the following equation is used to calculate the current setting of all strings:

$$I_{SET}=\frac{V_{ISET}}{R_{ISET}}\times Gain$$

Where, V_{ISET}=1.21V, Gain = 2580.

The LED_CURRENT[11:0] registers can also be used to adjust strings current down from this maximum. The default value for LED_CURRENT[11:0] registers is the maximum 0xFFF(4095). The following equation is used to calculate the current setting:

$$I_{LED}=\frac{1.21}{R_{ISET}}\times 2580\times \frac{LED_CURRENT[11:0]}{4095}$$

For high accuracy of LED current, it is recommended to set the ILED current in the range from 30mA to 170mA. Therefore, the RISET value is in the range from 18.4kΩ to 104kΩ.

16.2 ISET Setting Curve

The four LED current drivers provide up to 170mA per output and can be tied together to support higher current LEDs. The maximum output current of the LED drivers is set with the ISET resistor and can be optionally scaled by the LEDx_CURRENT[11:0] register bits with an I^2C interface. For high accuracy of LED current, it is recommended to set the ILED current in the range from 30 mA to 170mA. So, the RISET value is in the range from 18.4kΩ to 104kΩ. In order to avoid incorrect resistance or ISET shorting to GND causing larger LED current, the RTQ4554-QT has an ISET current limit protected function to avoid unusual LED current. If the ISET pin resistor is lower than 11.15kΩ or shorts to GND during operation, the maximum current for each LED channel can be calculated by the following equation. The LED_CURRENT[11:0] register will be automatically modified to 1/4 of the latest programmed data. If the ISET pin voltage returns to above 1V, the LED_CURRENT[11:0] register data automatically returns to the latest programmed data.

$$ILED_max\ limit = \left(\left(\frac{1.21}{R_{ISET}}\times 2580\right)\times\left(\frac{LED_current[11:0]}{4095}\right)\right)\times\frac{1}{4}$$

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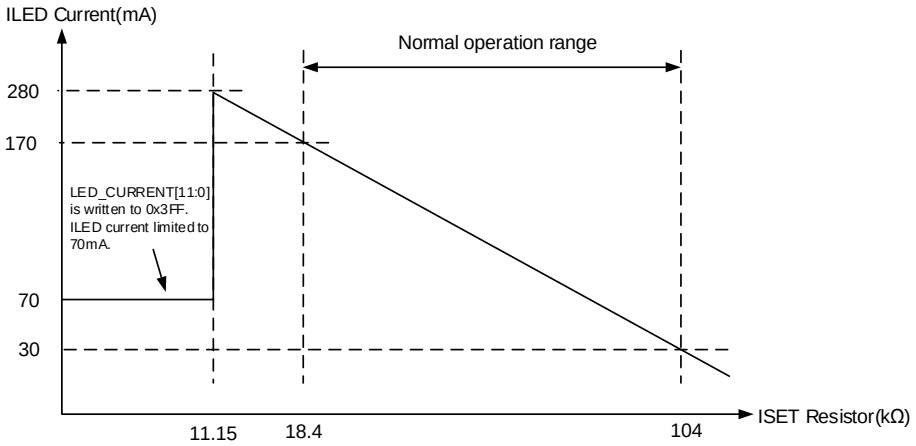

16.3 LED Dimming Frequency Setting

The LED dimming frequency is asynchronous from the input PWM frequency for phase-shift PWM mode and mixed mode. The LED dimming frequency is generated from the internal 20MHz oscillator and can be set to eight discrete frequencies from 152 Hz to 19.531 kHz. The register PWM_FREQ_SEL[8:6] can be used to control the ILED PWM Output frequency. There are two ways to set the PWM frequency:

1. When 0x02B0 PWM_FSET_SEL[1] = 0, the LED PWM frequency will default to 305Hz.
2. When 0x02B0 PWM_FSET_SEL [1] = 1, the PWM output frequency setting will be determined by the user's settings (Table 1).

Table 1

PWM_FREQ_SEL[8:6]	LED PWM Frequency (Hz)
0h	152
1h	305
2h	610
3h	1221
4h	2441
5h	4883
6h	9766
7h	19531

16.4 Boost Switching Frequency Setting

The BST_FREQ_SEL[5:3] can be used to control the boost switching frequency. There are two ways to set the boost switching frequency:

1. When 0x02B0 BST_FSET_SEL[0] = 0, the boost switching frequency will default to 400kHz.
2. When 0x02B0 BST_FSET_SEL [0] = 1, the boost switching frequency setting will be determined by the user's setting (Table 2).

Table 2

BST_FSET_SEL[5:3]	Switching frequency (kHz)
0h	303
1h	400
2h	606
3h	800
4h	1000
5h	1250
6h	1667
7h	2200

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16.5 Dimming Mode

The DIMMING_MODE[1:0] register bits control the performance of dimming, including Phase Shift PWM, Mixed, Direct PWM and DC modes.

16.5.1 Phase Shift PWM Mode

To reduce inrush current and eliminate audible noise during PWM dimming, the LED channels' current source is phase-shifted when the IC is in PWM mode. The shifted phase depends on the number of LED channels in use. The phase shift can be estimated with the equation:

$$\text{Phase}(^\circ) = \frac{360}{n}$$

where n is the number of LED channels being used.

16.5.2 Mixed Mode

Mixed mode combines PWM and DC modes for controlling the brightness. Under heavy and middle load conditions, with PWM Duty ≧ 12.5% or 25%, the dimming changes the DC amplitude performance to avoid flicker and noise issues. Under light load conditions, with PWM Duty < 12.5% or 25%, the PWM dimming provides both high accuracy brightness and low color distortion. By using Mix PWM dimming, the dimming ratio will be increased by 4 or 8 times, which is determined by 0x 2B2h LED_PWM_ISW_THR[8]. And LED_PWM_ISW_THR[8] controls 12.5% or 25 % PWM performance in Mixed PWM mode.

1. For 25% ≦ PWM Duty ≦ 100%, DC dimming benefits the low power requirement and increases the power-to-brightness transformation efficiency. In addition, for PWM Duty < 25%, each current sink turn-on duty will be increased by 4 times at the translated duty cycle and the same frequency to the input PWM, with the LED on-duty current regulated at 25% of the full scale.
2. For 12.5% ≦ PWM Duty ≦ 100%, DC dimming benefits the low power requirement and increases the power-to-brightness transformation efficiency. In addition, for PWM Duty < 12.5%, each current sink turn-on duty will be increased by 8 times at the translated duty cycle and the same frequency to the input PWM, with the LED on-duty current regulated at 12.5% of the full scale.

16.5.3 Direct PWM Mode

Direct PWM mode is the traditional way of controlling the brightness using PWM of the outputs with the same LED current across the entire brightness range. Brightness control is achieved by varying the duty cycle proportional to the input PWM. In Direct PWM mode, the PWM dimming frequency is equal to the PWM input signal. The ON/OFF switching of the current source is synchronized to the PWM signal.

16.5.4 DC Mode

DC mode features pure analog dimming all over the brightness range at full-scale LED current. DC dimming can provide potentially low power requirements for the same WLED brightness output because of the low voltage drop across each LED when the current is low. In DC mode, brightness control is achieved by changing the LED current proportionally from the maximum value to the minimum value across the entire brightness range.

The RTQ4554-QT provides two ways of brightness control for flexible system design, one is the I^2C control interface, and the other is the PWM input signal.

- Brightness Control by I^2C Control Interface:

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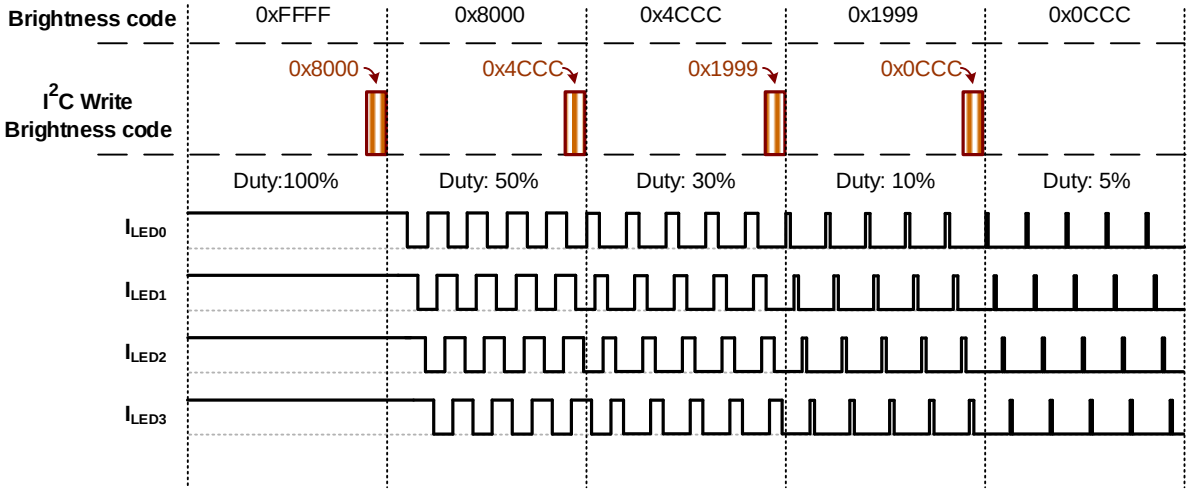
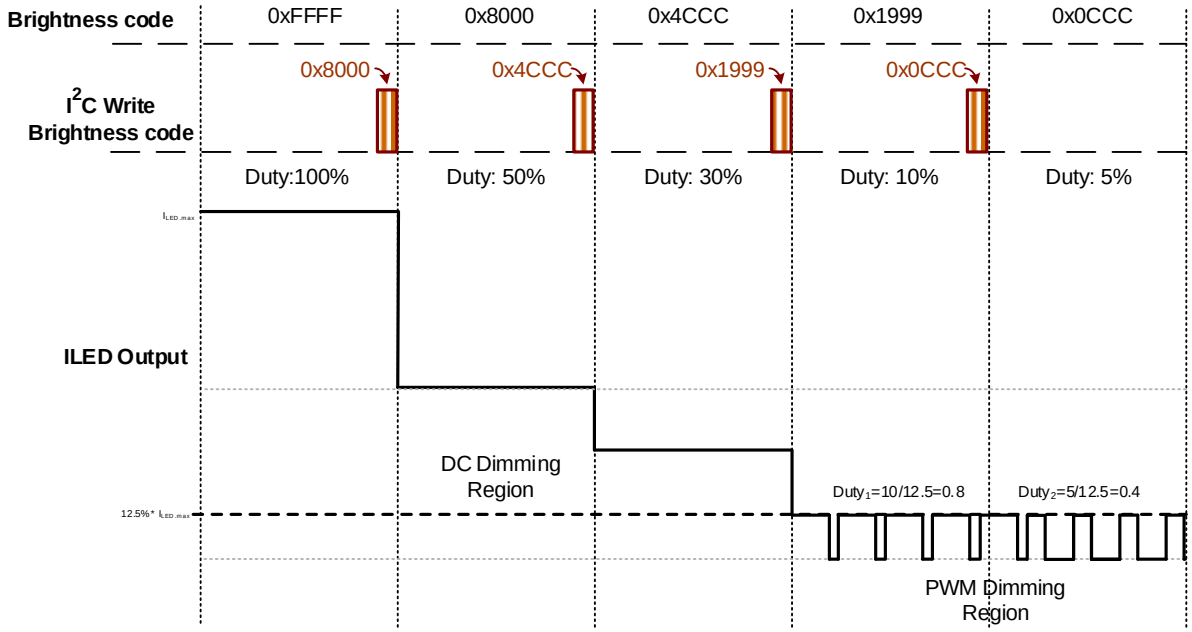
1. Phase Shift PWM Mode



2. Mixed Mode



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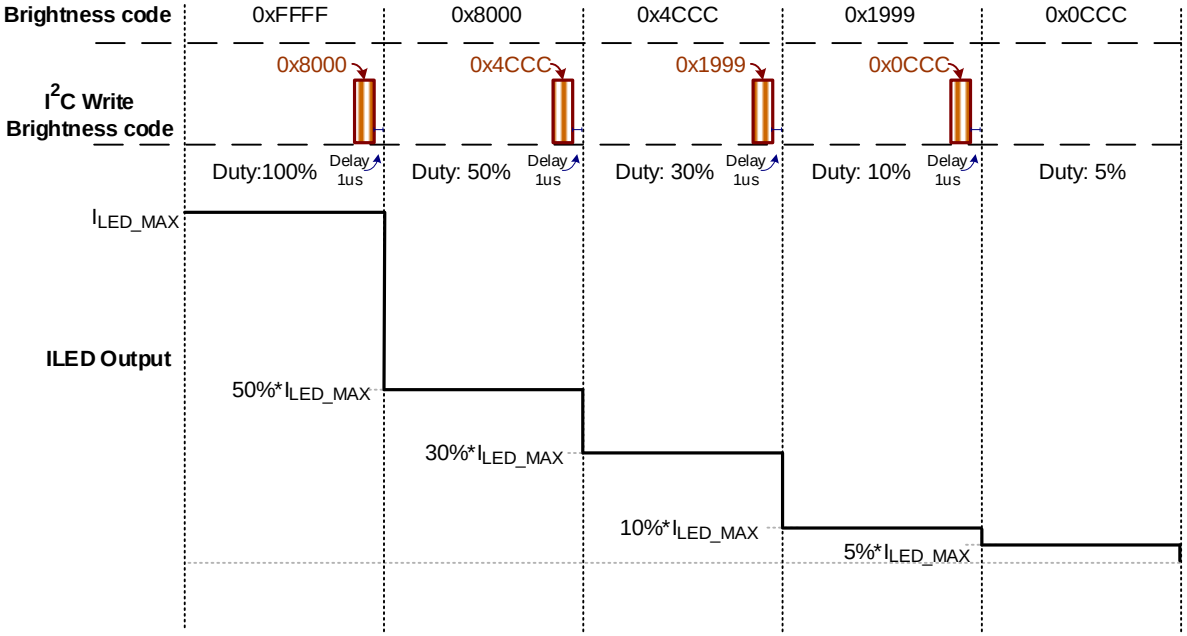
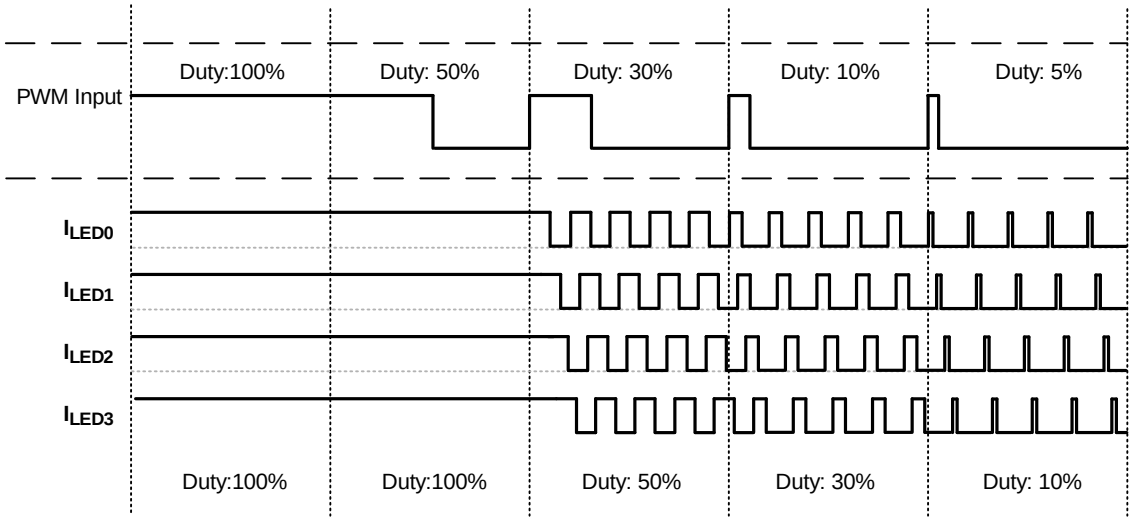
3. DC Mode



- Brightness Control by PWM Input Signal:

1. Phase Shift PWM Mode



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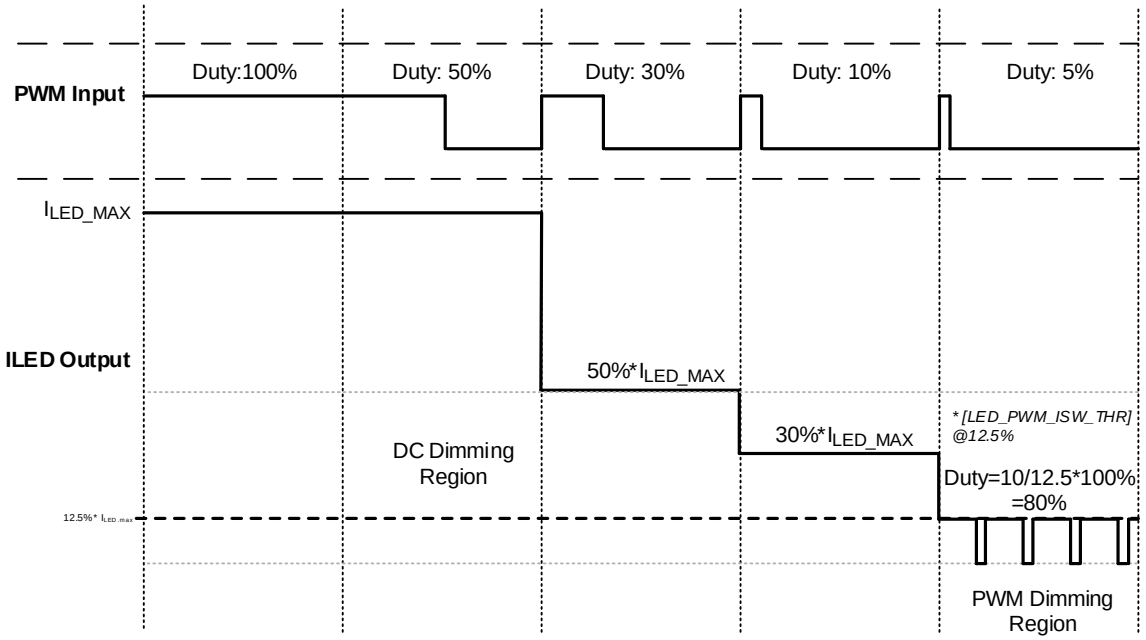
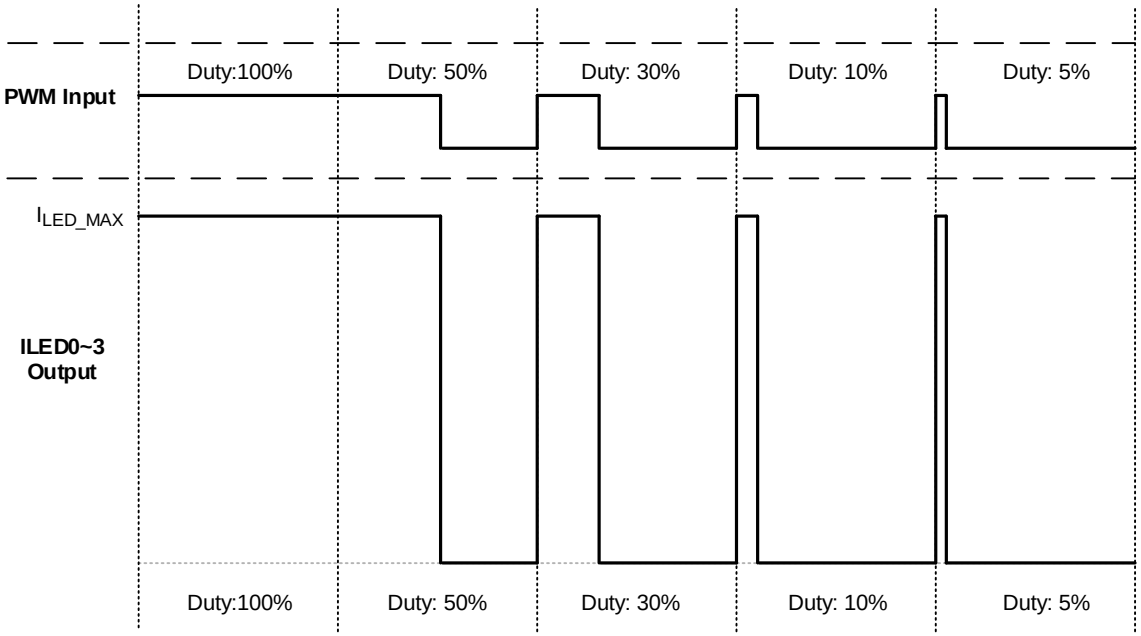
2. Mixed Mode



3. Direct PWM mode



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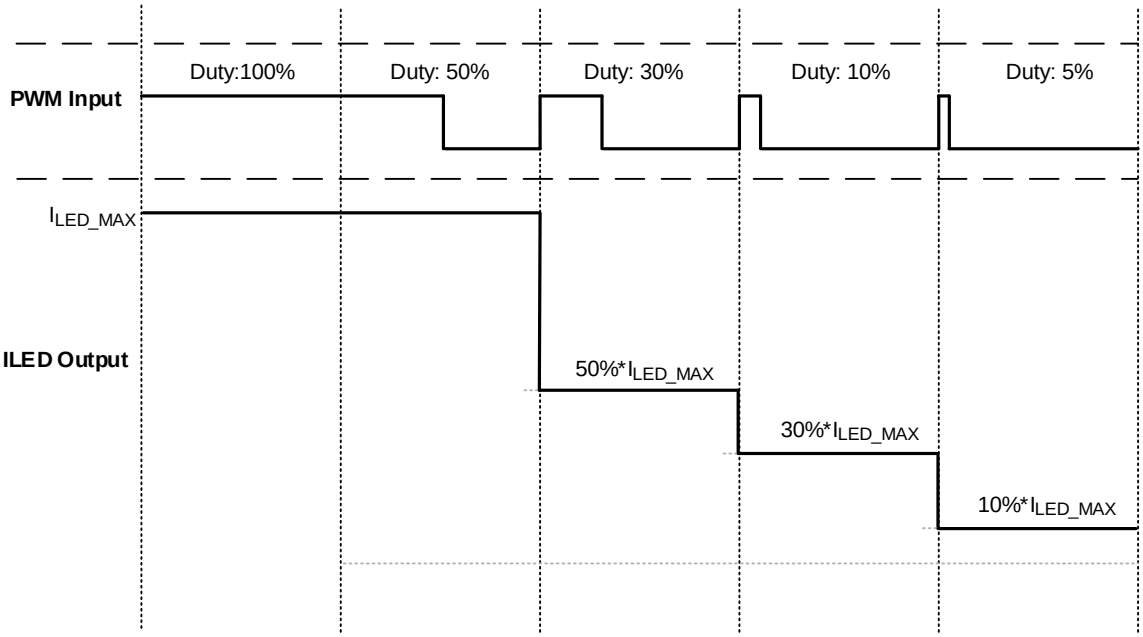
4. DC mode



16.6 LED Output String Configuration

LED_STRING_CFG[2:0] can be controlled using the output channel number. The RTQ4554-QT is a 4-channel LED driver designed for automotive backlighting. It operates by phase shifting the LED outputs based on the number of strings connected, with a 90° phase shift for 4 strings and a 180° phase shift for 2 strings. This design helps to reduce output ripple and increase the load frequency to move potential capacitor noise above the audible band.

LED_STRING_CFG	LED0 (mA)	LED1 (mA)	LED2 (mA)	LED3 (mA)	Automatic Phase Shift
2h: 4 Channel	170	170	170	170	360/4 = 90º
3h: 3 Channel	170	170	170	Tied to GND	360/3 = 120º
4h: 2 Channel	170	170	Tied to GND	Tied to GND	360/2 = 180º

16.7 LED Current Slope function

The RTQ4554-QT has an optional slope function that makes the transition from one brightness value to another optically smooth. The transition time between two brightness values (A and B) is programmed with the SLOPE_SEL[2:0] bits, as shown in the following figure. The SLOPE_EN register controls whether linear or advanced sloping is used. With advanced slope enabled, the brightness changes are further smoothed to be more pleasing to the human eye.

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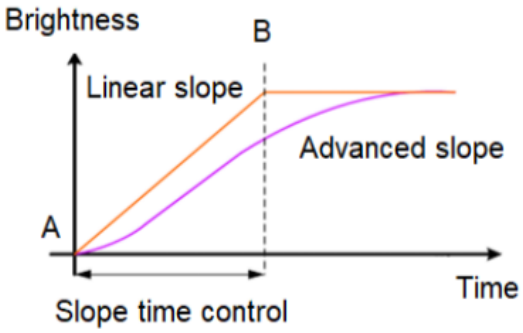
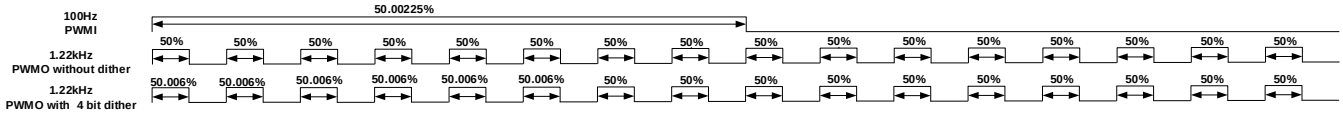


16.8 Dither Function

The PWM duty cycle dither function increases the number of brightness dimming steps beyond this oscillator clock limitation. The dither function modulates the LED driver output duty cycle over time to create more possible average brightness levels. The DITHER_SEL[3:0] register bits control the level of dither, with options to disable it or to set it to 1, 2, 3, or 4 bits.



16.9 LED Headroom and ADHR Function

LED headroom is the voltage difference between the LED forward voltage and the LED driver output voltage. It is an important parameter that affects the performance and efficiency of an LED driver circuit. Setting different LED headroom values can provide various benefits, depending on the requirements of the application.

The figure below shows the behavior of the system during the adaptive control process. The system includes an adaptive control feature that adjusts the control parameters of the system based on measurements of the output voltage from LED0 to LED3 of the system.

During the adjustment process, if the minimum LED channel voltage of the system reaches the [LED_HYS_THR+ LED_HR_THR] setting voltage, the adaptive control stops adjusting the control parameters of the system. However, if the LED channel voltage is greater than the [LED_HYS_THR+ LED_HR_THR] setting, the control adjusts downwards to the [LED_HYS_THR+ LED_HR_THR] voltage. Similarly, if the LED channel voltage is less than the [LED_HYS_THR+ LED_HR_THR] setting, the control adjusts upwards to the [LED_HYS_THR+ LED_HR_THR] voltage.

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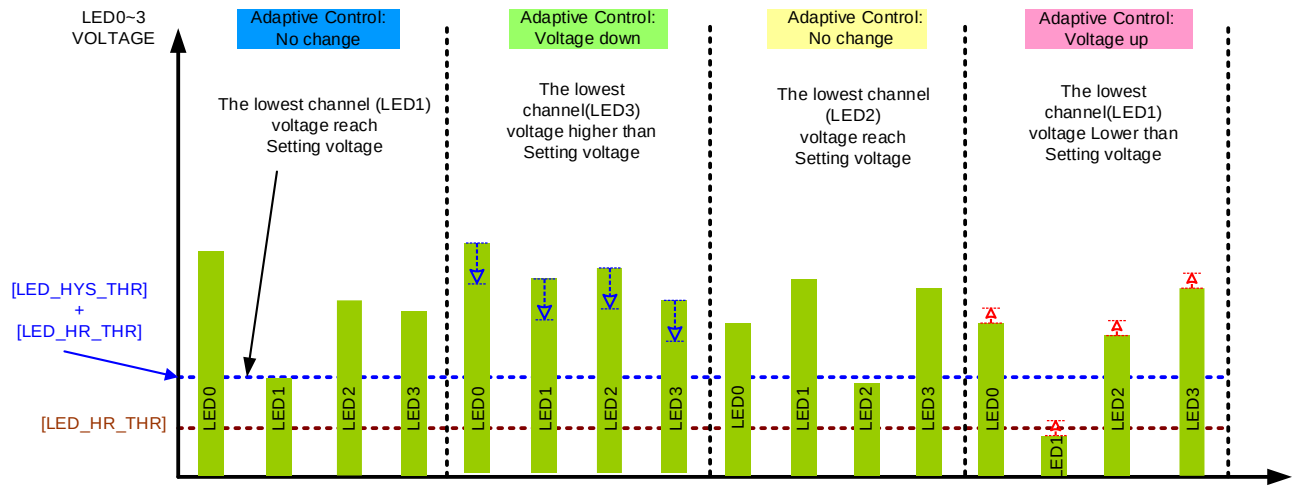

16.10 Spread Spectrum Function

The basic principle behind spread spectrum is to reduce the effects of EMI by converting a narrowband signal into a wideband signal, which will spread energy across multiple frequencies. Conservation of energy requires the total energy to remain constant; however, by distributing this energy across multiple frequency bands, peak energy is minimized. The device embeds an MRSS spread spectrum function to satisfy CISPR25 Class5 Certification requirements. The internal spread spectrum function modulates the boost frequency by ±3.68% to 7.13% from the central frequency, with a 11kHz to 30kHz modulation frequency. The switching frequency variation is programmable via the UM_MRSS_RANGE register, and the modulation frequency is programmable via the UM_MRSS_FREQ register.

16.11 Key Components Selection for Boost Topology

16.11.1 Maximum Output Current

Calculating the maximum current is crucial to determine the inductor ripple current. The switch current limit in the RTQ4554-QT protects the IC and circuit from damage due to overcurrent. It clamps the peak inductor current. Therefore, the current ripple in a boost converter can be subtracted from the maximum current. Also, the maximum output current assists in selecting the appropriate inductor component. The following equation shows the calculation with the related factors of the current:

$$\Delta I_L = \frac{V_{IN} \times D}{f_{SW} \times L} = \frac{(V_{OUT} - V_{IN}) \times (1 - D)}{f_{SW} \times L}$$

V_{IN} = Input Voltage

V_{OUT} = Output Voltage

D = Duty Ratio

f_{SW} = Switch Frequency

L = Selected Inductor Value

After determining the change in the inductor current, we can calculate the maximum output current that the RTQ4554-QT can deliver.

$$I_{MAXOUT} = (I_{OCP} - \frac{\Delta I_L}{2}) \times (1 - D)$$

I_{OCP} = Switching Current Limitation

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ΔI_L = Inductor Ripple Current

D = Duty Ratio

The output current required by the system must be less than the calculated value. It represents the maximum current that the integrated power switch in the RTQ4554-QT can withstand. If the maximum value is only slightly smaller than the required one, it can be solved by using an inductor component with higher inductance. The higher inductance reduces the ripple current and increases the maximum output current.

16.11.2 Inductor Selection

The inductor plays an important role in the switching controller. It influences steady-state operation, transient response, and stability. We must consider inductor specifications, such as inductor value, DC resistance, and saturation current when choosing the inductor component. The value of an inductor determines its ripple current. Higher inductance leads to a higher maximum current due to reduced ripple current. The lower inductance allows the use of a smaller-sized inductor. It is recommended that the ripple current is set to 20% to 40% of the output DC current.

Inductor values commonly have a ±20% tolerance with no current bias. When the inductor current approaches the saturation level, its inductance may decrease 20% to 35%. In addition, inductors with low DCR values provide more output current and higher conversion efficiency. The equation below provides an estimation for the inductor. Table 3 shows recommended inductor values for each frequency.

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{\Delta I_L \times f_{SW} \times V_{OUT}}$$

V_{IN} = Input Voltage

V_{OUT} = Output Voltage

ΔI_L = Inductor Ripple Current

f_{SW} = Switch Frequency

Table 3. Inductance Values for Boost Switching Frequencies

SW Frequency (kHz)	Inductance (μH)
300	22
400	22
600	15
800	15
1000	10
1250	10
1667	10
2200	10

The inductor must be selected with a saturated current rating that is greater than the peak current. It is recommended that the inductor's current rating be 25% higher than the peak current for optimal performance. Additionally, considering efficiency in the selection process is preferable. The calculation for the maximum current is provided by the following equation:

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$$I_{PEAK} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} + \frac{V_{IN} \times D}{2 \times f_{SW} \times L}$$

I_{OUT} = Output Current

V_{OUT} = Output Voltage

D = Duty Ratio

f_{SW} = Switch Frequency

η = Efficiency of the Controller

L = Selected Inductor Value

16.11.3 Diode Selection

The Schottky diode is a good choice for boost converters due to the small forward voltage and fast switching speed. However, when selecting a Schottky diode, important parameters such as reverse voltage rating, and peak current must all be taken into consideration. A suitable Schottky diode's reverse voltage rating must be greater than the maximum output voltage; a rating that is at least 25% higher is recommended. Also, its average rating must be at least 25% higher than the average output current. To increase efficiency, the forward voltage should be as low as possible, ideally less than 0.5V.

16.11.4 Input Capacitor Selection

Low ESR ceramic capacitors are recommended for input capacitor applications. A low ESR will effectively reduce the input voltage ripple caused by the switching operation. The voltage rating of the input capacitor must be greater than the maximum input voltage to ensure the enough filtering ability.

16.11.5 Output Capacitor Selection

Output ripple voltage and boost stability play important roles in estimating the performance. This portion is formed by charging and discharging process of output capacitor. The DC-bias effect can impact on the capacitance and reduce the effective value significantly up to 80%. According to the selection, we recommend using a 33μF electrolytic capacitor in parallel with two 10μF ceramic capacitors to lower the ripple, increase stability, and reduce the ESR effect. The voltage rating of the output capacitor must be 50% greater than the maximum output voltage to ensure the enough filtering ability.

16.11.6 Switching MOSFET

The switching MOSFET is a crucial component of the boost converter. Its power efficiency is determined by its voltage, current rating, R_{DSON}, power dissipation, and rising and falling time. The voltage rating of the N-type MOSFET must be 25% greater than the maximum output voltage. The current rating should be higher than the inductor current. The value of R_{DSON} is recommended to be less than 20mΩ. Besides, adding the resistor between the GD pin and the gate of the MOSFET can help to reduce the peak current. Also, this gate resistor can adjust the rising and falling time to improve the CISPR25 compliance.

16.11.7 Power-Line MOSFET

The power-line MOSFET isolates the input power away from the boost converter for fear that the overcurrent event causes IC damage. Due to the power controller design, the P-type and N-type MOSFETs are used in the application circuit. To turn on the MOSFET completely, the voltage rating must be 25% greater than the maximum input voltage. The current rating should be 25% higher than the input peak current. A lower R_{DSON} can reduce power loss and enhance efficiency. We recommend using an R_{DSON} of less than 20mΩ for optimal performance. If a P-type MOSFET is used, the minimum Gate-to-Source voltage (VGS) required to fully turn on the transistor

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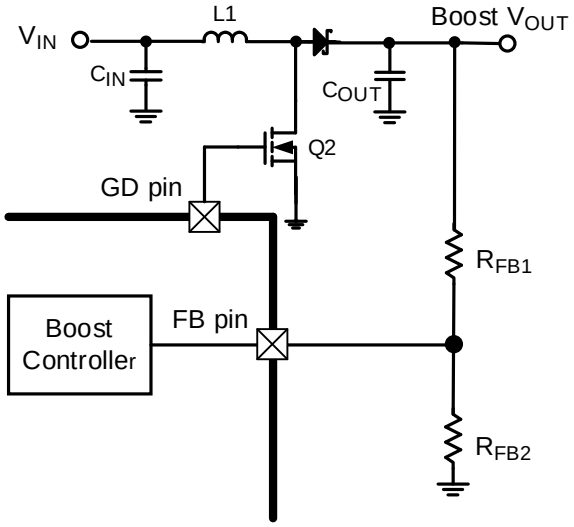
should be less than the minimum input voltage. A 20kΩ resistor should be used between the gate and source. If an N-type MOSFET is used, the Gate-to-Source voltage should be clamped, and an IN4148 should be used between the gate and source.

16.11.8 Input Current Sense Resistor

The current sense resistor in front of the converter detects the input current to prevent overflow and protect the circuit. When the voltage across the sense resistor reaches 220mV, it triggers the VIN OCP protection procedure to shut down the circuit. The value of the sense resistor can be adjusted to the input current limit. Typically, a 20mΩ resistor is used to withstand an 11A current for the specified value. Due to the high power flowing through the sense resistor, it is recommended to choose the power rating of at least 3W and a 2512 package size.

16.11.9 Feedback Resistor Divider

The boost generates the LED supply voltage for best power efficiency. The feedback function (FB pin) of the RTQ4554-QT is connected to the output voltage resistor divider. The feedback mechanism in the power supply is sensed with a resistive voltage divider. The boost output voltage and the feedback resistances, RFB1 and RFB2, can be calculated by the following equation:



$$Boost_max = 38.7 \times 10^{-6} \times R_{FB1} + \left(\frac{R_{FB1}}{R_{FB2}} + 1\right) \times 1.21$$

V_{BOOST_max} = Maximum Boost Voltage

V_{FB} = 1.21V

R_{FB1}/R_{FB2} = 7~10

The recommended value for R_{FB2} is 100kΩ for boost operation.

The minimum boost voltage must be less than the minimum LED string voltage. The minimum boost voltage is calculated using the following equation:

$$Boost_min = \left(\frac{R_{FB1}}{R_{FB2}} + 1\right) \times 1.21$$

V_{FB} = 1.21V

When the boost OVP_LOW level is reached, the boost controller stops switching the boost FET, and the BSTOVPL_STATUS bit is set. The LED drivers are still active during this condition, and the boost resumes normal switching operation once the boost output level falls. The boost OVP low voltage threshold is calculated using the following equation:

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$$Boost_OVP_Low = Boost + \left(\frac{R_{FB1}}{R_{FB2}}+1\right) \times (V_{OVPL} - V_{FB})$$

V_{OVPL} = 1.423V

The boost value also changes dynamically with the current boost voltage.

When the boost OVP_HIGH level is reached, the boost controller enters fault recovery mode, and the BSTOVPH_STATUS bit is set. The boost OVP high-voltage threshold is calculated using the following equation:

$$Boost_OVPH = Boost + \left(\frac{R_{FB1}}{R_{FB2}}+1\right) \times (V_{OVPH} - V_{FB})$$

V_{OVPH} = 1.76V

The boost value also changes dynamically with the current boost voltage.

When the boost UVP level is reached, the boost controller starts a 100-ms OCP counter. The RTQ4554-QT device enters the fault recovery mode and sets the BSTOCP_STATUS bit if the boost voltage does not rise above the UVP threshold before the timer expires. The boost UVP voltage when adaptive voltage control is at the maximum output voltage is calculated using the following equation:

$$Boost_UVP = Boost - \left(\frac{R_{FB1}}{R_{FB2}}+1\right) \times (V_{FB} - V_{UVP})$$

V_{UVP} = 0.886V

I_{SEL} = 38.7μA

The boost value also changes dynamically with the current boost voltage.

16.11.10 LED Output Current Setting Resistor

The maximum output LED current is set by an external resistor value. The 0x1C2h LED_CURRENT[11:0] registers can also be used to individually adjust each string's current down from this maximum. The default value for all the LED_CURRENT[11:0] registers is the maximum (4095). The following equation is used to calculate the current setting of an individual string:

$$ILED = \left(\frac{1.21}{R_{ISET}} x2580\right) \times \left(\frac{LED_current[11:0]}{4095}\right)$$

16.12 Key Components Selection for SEPIC Topology:

16.12.1 Inductor Selection

The inductance values for both inductors are shown in Table 4 for each frequency. The inductance should be 20% to 35% higher than the peak current. The ripple current is estimated to be 20% to 40% of the maximum output DC current. The following equation calculates the inductor peak current.

$$I_{PEAK(L1)} = I_{OUT} \times \frac{(V_{OUT}+V_D)}{V_{IN}} \times \left(1+\frac{40\%}{2}\right)$$

V_{IN} = Input Voltage

V_{OUT} = Output Voltage

V_D = Diode Forward Voltage

$I_{PEAK(L1)}$ = Peak Current for Inductor 1

I_{OUT} = Output Current

Table 4. Inductance Values for Sepic Switching Frequencies

SW Frequency (kHz)	Inductance (μH)
300	15

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400	15
600	10
800	10
1000	6.8
1250	6.8
1667	4.7
2200	4.7

$$I_{PEAK(L2)} = I_{OUT} \times (1+\frac{40\%}{2})$$

$I_{PEAK(L2)}$ = Peak Current for Inductor 2

I_{OUT} = Output Current

$$\Delta I_L = I_{IN} \times 40\% = I_{OUT} \times \frac{V_{OUT}}{V_{IN}} \times 40\%$$

V_{IN} = Input Voltage

V_{OUT} = Output Voltage

I_{IN} = Input Current

I_{OUT} = Output Current

ΔI_L = Inductor Ripple Current

16.12.2 Coupled Capacitor Selection

The coupled capacitor is used to protect against a shorted load between the input and the output. The RMS current, calculated using the following equation, affects the coupled capacitor significantly. The voltage rating of the coupled capacitor must be greater than the input voltage. It is recommended to use a 10μF ceramic capacitor in series with a 2Ω resistor, in parallel with a 33μF electrolytic capacitor.

$$I_{Cs_RMS} = I_{OUT} \times \sqrt{\frac{(V_{OUT} + V_D)}{V_{IN}}}$$

V_{IN} = Input Voltage

V_{OUT} = Output Voltage

V_D = Diode Forward Voltage

I_{Cs_RMS} = RMS Current of Cs Capacitor

I_{OUT} = Output Current

16.12.3 Feedback Resistor Divider

The SEPIC generates the LED supply voltage for best power efficiency. The feedback function (FB pin) of the RTQ4554-QT connects to its output voltage resistor divider. The feedback in the power supply is sensed through a resistive voltage divider. The boost output voltage and the feedback resistances, R_{FB1} and R_{FB2}, can be calculated using the following equation:

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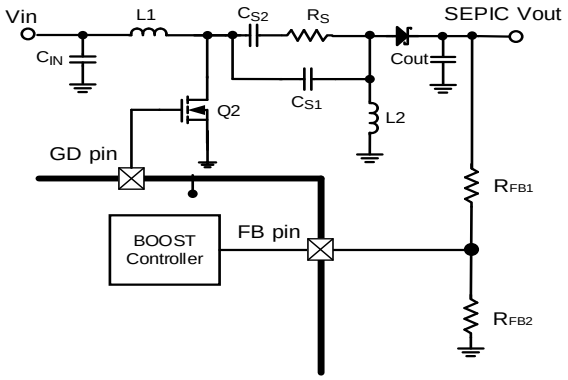

$$SEPIC_max = 38.7 \times 10^{-6} \times R_{FB1} + \left(\frac{R_{FB1}}{R_{FB2}} + 1\right) \times 1.21$$

V_{SEPIC_max} = Maximum SEPIC Voltage

V_{FB} = 1.21V

R_{FB1}/R_{FB2} = 3~6

The recommended value of R_{FB2} is 170 kΩ for SEPIC operation.

The minimum SEPIC voltage must be lower than the minimum LED string voltage. The minimum SEPIC voltage is calculated using the following equation:

$$SEPIC_min = \left(\frac{R_{FB1}}{R_{FB2}} + 1\right) \times 1.21$$

V_{FB} = 1.21V

When the SEPIC OVP_LOW level is reached, the SEPIC controller stops switching the boost FET, and the BSTOVPL_STATUS bit is set. The LED drivers are still active during this condition, and the SEPIC resumes normal switching operation once the SEPIC output level falls. The boost OVP low voltage threshold is calculated using the following equation:

$$SEPIC_OVP_Low = SEPIC + \left(\frac{R_{FB1}}{R_{FB2}} + 1\right) \times (V_{OVPL} - V_{FB})$$

V_{OVPL} = 1.423V

The SEPIC also dynamically adjusts to the current SEPIC voltage.

When the boost OVP_HIGH level is reached, the SEPIC controller enters fault recovery mode, and the BSTOVPH_STATUS bit is set. The boost OVP high-voltage threshold is calculated using the following equation:

$$SEPIC_OVPH = SEPIC + \left(\frac{R_{FB1}}{R_{FB2}} + 1\right) \times (V_{OVPH} - V_{FB})$$

V_{OVPH} = 1.76V

The SEPIC also dynamically adjusts to the current SEPIC voltage.

When the boost UVP level is reached, the SEPIC controller starts a 100-ms OCP counter. The RTQ4554-QT device enters the fault recovery mode and sets the BSTOCP_STATUS bit if the SEPIC voltage does not rise above the UVP threshold before the timer expires. The boost UVP voltage, when adaptive voltage control is at the maximum output voltage, is calculated using the following equation:

$$SEPIC_UVP = SEPIC - \left(\frac{R_{FB1}}{R_{FB2}} + 1\right) \times (V_{FB} - V_{UVP})$$

V_{UVP} = 0.886V

The SEPIC also dynamically adjusts to the current SEPIC voltage.

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16.13 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-24SL 4x4 package, the thermal resistance, θ_{JA}, is 37.57°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C – 25°C) / (37.57°C/W) = 2.66W for a WQFN-24SL 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

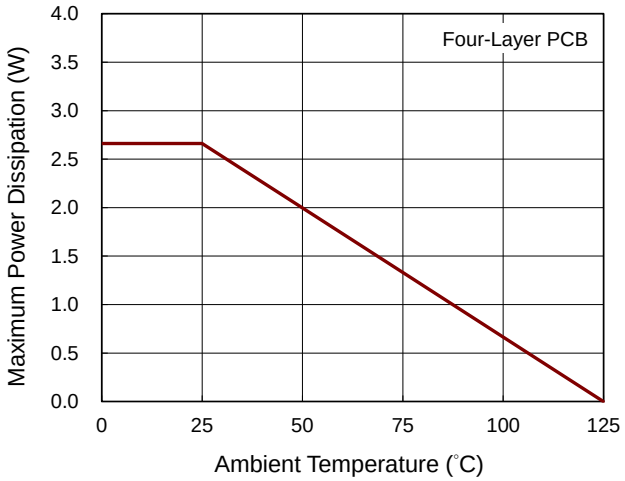

Figure 1. Derating Curve of Maximum Power Dissipation

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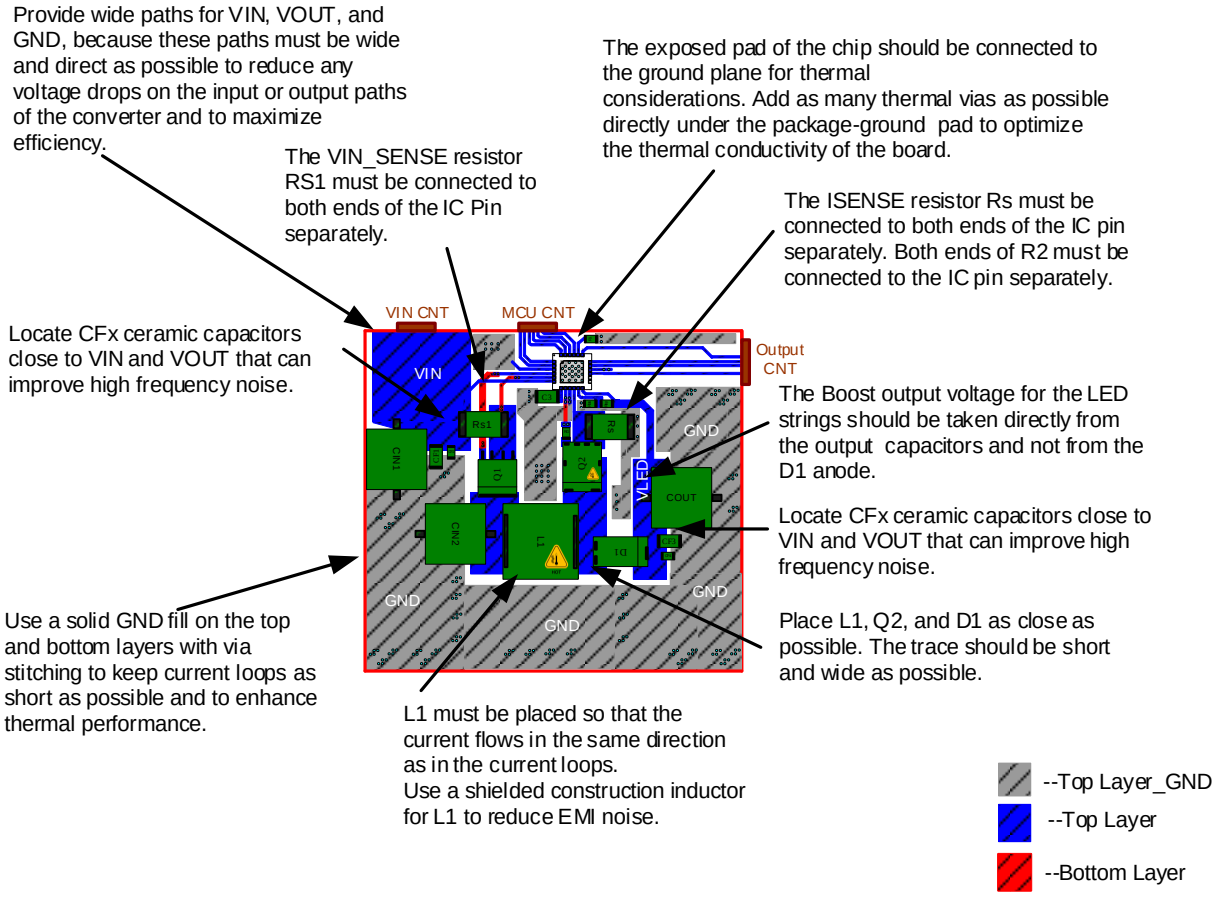
16.14 Layout Guideline

PCB layout is very important to design power switching circuits. The following layout guidelines should be strictly followed for the best performance of the RTQ4554-QT.

Boost Topology:



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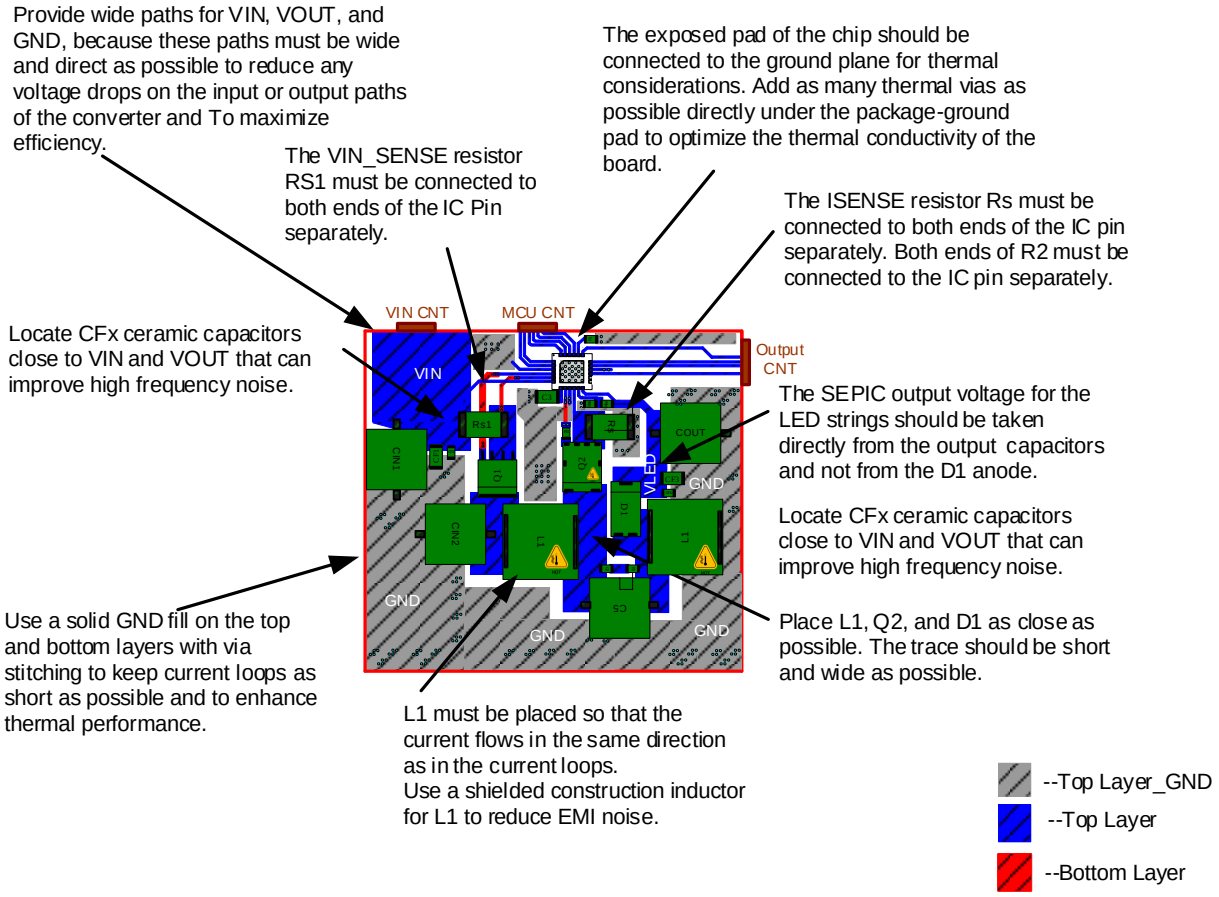
Topology:



Note 12. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

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17 Functional Register Description

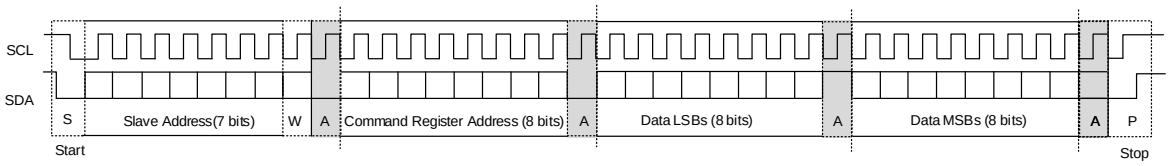
17.1 I²C Command

The RTQ4554-QT supports the I²C interface to access and change the configuration. The 7-bit base slave address is 0x2C or 0x3C. The address can be configured through the resistor settings of the SS_ADDR pin. The IC uses a 10-bit register address space. The 10-bit register address space is accessed as three separate 8-bit address spaces. Three different slave addresses are used to access each of the three 8-bit address register spaces.

Table 5. I²C Address Registers Selection

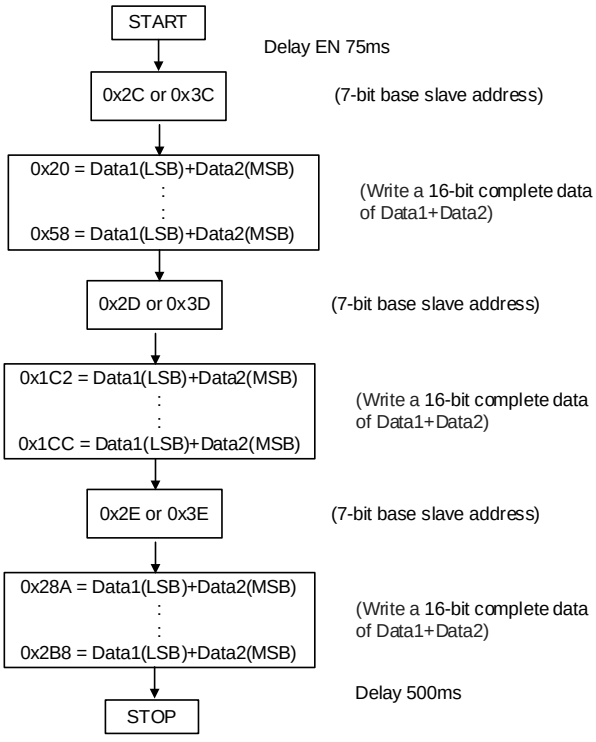
SS_ADDR PIN	7-Bit Base Address	7-Bit Slave Address	Accessible 10-Bit Registers
GND	0x2C	0x2C	0x000 to 0x0FF
		0x2D	0x100 to 0x1FF
		0x2E	0x200 to 0x2FF
VLDO	0x3C	0x3C	0x000 to 0x0FF
		0x3D	0x100 to 0x1FF
		0x3E	0x200 to 0x2FF

The RTQ4554-QT supports the I²C interface to access and change the configuration. The 7-bit base slave address is 0x2C or 0x3C. The address can be configured through the resistor settings of the SS_ADDR pin. The IC uses a 10-bit register address space. The 10-bit register address space is accessed as three separate 8-bit address spaces. Three different slave addresses are used to access each of the three 8-bit address register spaces.



I²C Write

Write DAC Flowchart



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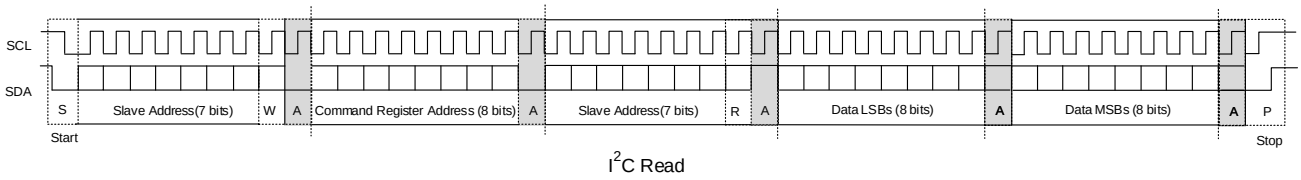
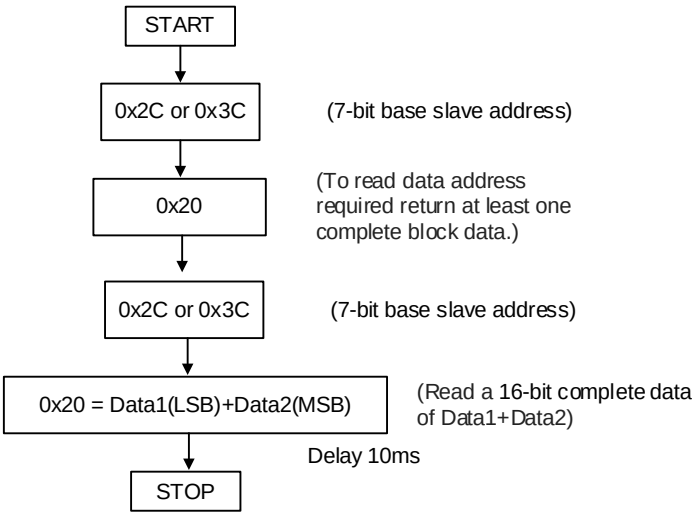
Read I2C transactions are made up of five bytes. The first byte includes the 7-bit slave address and the Write bit. The 7-bit slave address selects the IC slave address and one of three 8-bit register address sections. The second byte includes 8 LSB bits of the 10-bit register address. The third byte includes the 7-bit slave address and the Read bit. The last two bytes are the 16-bit register value returned from the slave.



I2C Read

Read DAC Flowchart



17.2 MTP Read/Write Function

Writes and reads can be made directly to the DAC register to control and monitor the position without any nonvolatile memory changes. The nonvolatile memory stores the power-on value. When powered on, the contents of the memory are transferred to the DAC register. Then, set the write data bit once all desired data are addressed after power-on. To write a new value to the memory, set a new power-on position and load the same value into the DAC register. When writing to address 0xFEh and the data register 8000h, the I2C interface will write all DAC register data into EEPROM.

Table 6

Address	Bit	Name	Default Value	Description	R/W
FEh	8	MTP Read	0h	MTP Read 0h: I2C read data from DAC 1h: I2C read data from MTP	R/W
FEh	15	MTP Programming	0h	MTP Programming 0h: Normal operation 1h: Start MTP programming sequence	R/W

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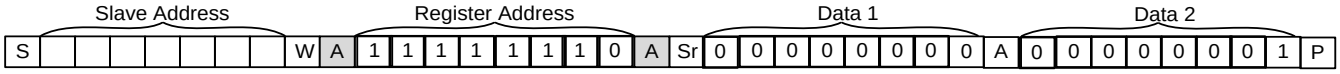
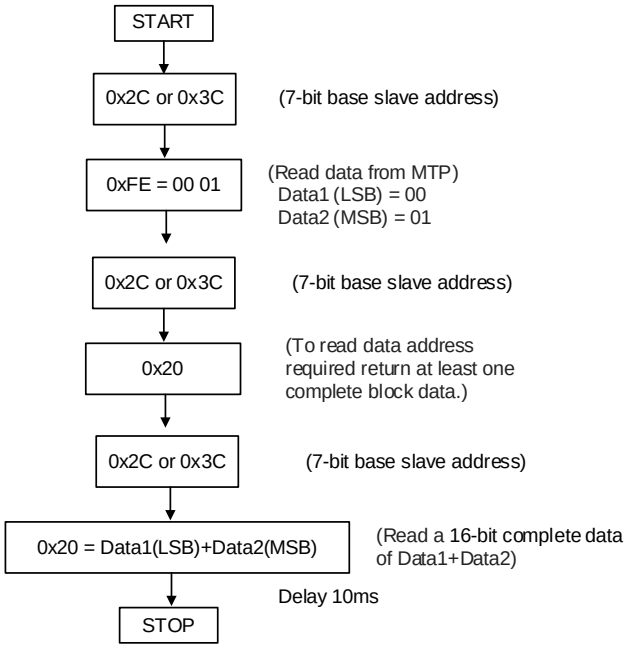
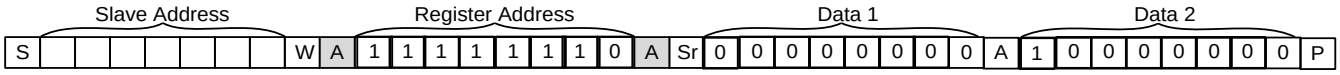
Read from MTP



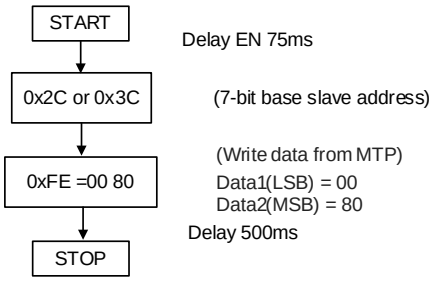
Read MTP Flowchart



Write to MTP



Write MTP Flowchart



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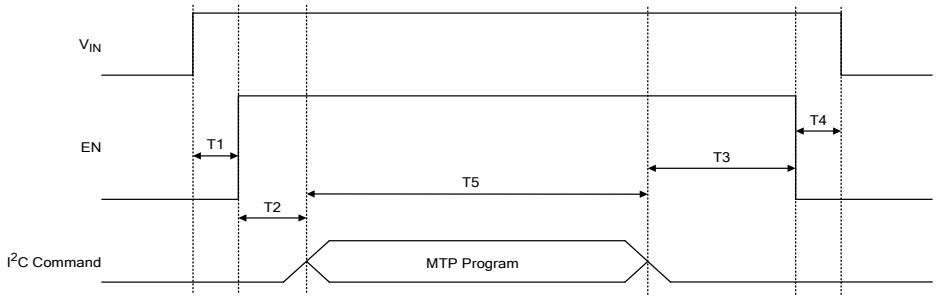
17.3 MTP Program Sequence



Write:

T1 = 30ms, T2 = 75ms, T3 = 500ms, T4 = 100ms, T5= 120ms

Read

T1 = 30ms, T2 = 75ms, T3 = 10ms, T4 = 100ms, T5= 80μs

f_{SCL} = 400kHz

17.4 MTP Program Application Circuit for Single Chip

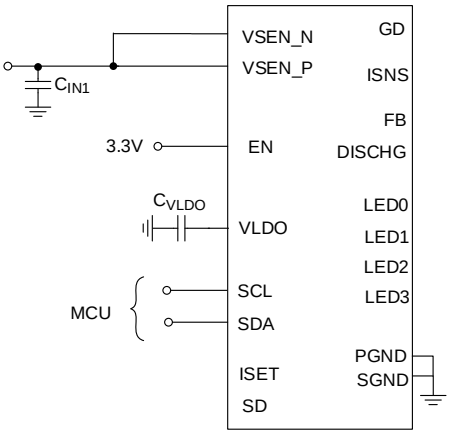


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Table 7. Protection Table

Channel	Fault Name	Threshold	Condition	Action	Trigger Fault State	Enter Fault Recovery	Trigger INT pin
Vin	VIN UVLO	2.8V/3.8V/5.3V/7.3V	Vin fall voltage	The device goes to standby and then attempts to restart once the input voltage rises above threshold.	V	X	V
	VIN OVP	43V	VIN voltage rises above 43V.	The device goes to standby and waits until input voltage falls below threshold before restarting.	V	X	V
	VIN OCP	0.22V	Voltage across RISENSE exceeds 220mV.	The device goes to Fault Recovery and then attempts to restart 100 ms after fault occurs.	V	V	V
Boost	Boost OVP High	1.76V or DIS pin≧ 49.5V	The FB pin voltage rises above the VFB_OVPH level, or the DISCHARGE pin voltage (Vout) rises above VBST_OVPH.	The device goes to Fault Recovery and waits until output voltage falls below threshold before restarting.	V	V	V
	Boost OVP Low	1.423V	The FB pin voltage rises above the VFB_OVPL level.	Boost stops switching until boost voltage level falls. The device remains in normal mode with LED drivers operational.	X	X	X
	Boost OCP	cycle by cycle current limit drop below VFB UVP:0.886V for 110ms.	The FB pin voltage falls below the VUVP level.	1. The boost cycle-by-cycle current limit is to protect the DC/DC components (inductor, Schottky diode, and switching MOSFET) in normal scenario, avoiding current running over their maximum limit. The normal scenario means when loading has sharp change or input voltage has sharp change. It will not trigger any device fault. However, if OCP continues to occur and then VOUT drops to trigger the UVP level, the device goes to fault recovery and then attempts to start 100ms after fault occurs. 2. The Boost OCP fault recovery state is entered, and a fault interrupt is generated.	V	V	V

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Channel	Fault Name	Threshold	Condition	Action	Trigger Fault State	Enter Fault Recovery	Trigger INT pin
LED	Open LED String	LED_DRV_HEADROOM ≤0.35V~0.7V	The headroom voltage on one or more channels is below minimum level for LED filter time or LED global filter time when boost has adapted to maximum level.	The faulted LED string is disabled and removed from the adaptive boost control loop. The string is re-enabled in the next power cycle.	V	X	V
	LED Internal Short	2.6~6V	The headroom voltage on one or more channels is above the SHORTED_LED_THRESHOLD for > cycle time while the headroom of at least one channel is still inside the normal headroom operation window.	The faulted LED string is disabled and removed from the adaptive boost control loop. String is re-enabled next power cycle.	V	X	V
VLDO	LDO_UVP	LDO_VOUT<3.5V	LDO_VOUT<3.5V	The device goes to Fault Recovery and then attempts to restart 100 ms after fault occurs.	V	V	V
OTP	Over-Temperature Protection	165°C	Junction temperature rises above Over-Temperature Protection threshold. (Hysteresis = 20°C)	The device goes to standby and then attempts to restart once the die temperature falls below the threshold.	V	X	V
I^2C	I^2C Timeout	STOP Signal for 500ms	The device receives the I^2C command without a STOP signal for 500ms.	1. Device functions normally and waits for the next I2C command. 2. If the chip receives an I2C command without a STOP signal for 500 ms, the I2C communication block auto resets and waits for the next command.	V	X	V
	CRC Error	CRC Error	The factory default configuration for registers, options, and trim bits are not correctly loaded from memory.	1.MTP CRC: If the MTP load down fails, the IC waits for a clear bit or restart. 2.DAC CRC: If the chip receives an I^2C command error, the I^2C communication block auto resets and waits for the next command.	V	X	X
Setting Miss	ISET Resistor Fault		The ISET pin voltage is pulled below 0.99V due to the ISET pin resistor shorted to GND. If the ISET pin voltage returns to above 1.1 V, the LED_CURRENT[11:0] register data automatically returns to the latest programmed data.	The LED_CURRENT[11:0] is written to 0x3FF, and the total LED current is limited to 70 mA.	V	X	V

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The following table summarizes the registers and their default values.

Table 8. Register Map

Slave Address	Data Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Default Value	Type
0x2Ch/3Ch	0x20h	Reserved								Reserved						BRT_MODE		0000h	R/W
	0x28h	DP_BRT																FFFFh	R/W
	0x40h	DITHER_SEL				Reserved				SLOPE_SEL		SLOPE_EN		Reserved		DIMMING_MODE		00B0h	R/W
	0x42h	PWM_MIN_LIM_EN	Reserved															0000h	R/W
	0x4Eh	Reserved		VINOCP_INT_EN		ISET_INT_EN		BIST_INT_EN		Reserved		MTP CRC_INT_EN		VINOVP_INT_EN		VINUVP_INT_EN		280Ah	R/W
	0x50h	GLOBAL_INT_EN		BSTOVPH_INT_EN		LDO_UV_INT_EN		I2C_TIMEOUT_INT_EN		Reserved		BSTOCP_INT_EN		Reserved		TSD_INT_EN		AA22h	R/W
	0x52h	Reserved								LED_INT_EN		Reserved						0080h	R/W
	0x54h	BSTOVPH_STAT	BSTOVPH_CLR	ISET_STAT	ISET_CLR	LDO_UV_STAT	LDO_UV_CLR	I2C_TIMEOUT_STAT	I2C_TIMEOUT_CLR	BSTOVPL_STAT	BSTOVPL_CLR	BSTOCP_STAT	BSTOCP_CLR	BIST_STAT	BIST_CLR	TSD_STAT	TSD_CLR	0000h	R/W

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	0x56h	Reserved	Reserved	LED3_FAULT	LED2_FAULT	LED1_FAULT	LED0_FAULT	OPEN_LED_STAT	INTERNAL SHORT_LED_STAT	LED_STAT	LED_CLR	Reserved	Reserved	MTP_CRC_STAT	MTP_CRC_CLR	DAC_CRC_STAT	DAC_CRC_CLR	0000h	R/W
	0x58h	Reserved	Reserved	VINOCP_STAT	VINOCP_CLR	Reserved	Reserved	INT_PIN_STAT	INT_PIN_CLR	Reserved	Reserved	Reserved	Reserved	VINOVP_STAT	VINOVP_CLR	VINUVP_STAT	VINUVP_CLR	0000h	R/W
	0xE8h	Reserved																0000h	R
	0xECh	Reserved																0000h	R/W
	0xEEh	Reserved																0000h	R/W
0x2Dh/3Dh	0x13Ch	Reserved																0000h	R/W
	0x148h	Reserved																0000h	R/W
	0x154h	Reserved																0000h	R/W
	0x160h	Reserved																0000h	R/W
	0x16Ch	Reserved																0000h	R/W
	0x178h	Reserved																0000h	R/W
	0x1C2h	LED0_SHORT_DIS	Reserved							LED_Current								0FFFh	R/W
	0x1C4h	LED1_SHORT_DIS	Reserved															0000h	R/W

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	0x1C6h	LED2_SHORT_DIS	Reserved											0000h	R/W
	0x1C8h	LED3_SHORT_DIS	Reserved											0000h	R/W
	0x1CAh	Reserved												0000h	R/W
	0x1CCh	Reserved												0000h	R/W
0x2Eh/3Eh	0x288h	Reserved												0000h	R/W
	0x28Ah	Reserved					LED_SHORT_THR			Reserved				0800h	R/W
	0x2A4h	Reserved											FSM_LIVE_STAT	0000h	R
	0x2A6h	PWM_INPUT_STAT												0000h	R
	0x2A8h	LED_PWM_STAT												0000h	R
	0x2AAh	Reserved		ILED_STAT										0000h	R

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| | | |

Table 9

Address: 0x20								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Reserved							
Default	00							
Type	R/W							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved						BRT_MODE	
Default	0						0	
Type	R/W						R/W	

Bit	Name	Description
15:2	Reserved	These bits are reserved.
1:0	BRT_MODE	0h = Brightness controlled by PWM Input 1h = Reserved 2h = Brightness controlled by DISPLAY_BRT Register 3h = Reserved

The BRT_MODE[1:0] selects global brightness control for all LED strings through the PWM input duty cycle on the PWM pin or register control by I²C. An internal 20-MHz clock is used for generating PWM outputs.

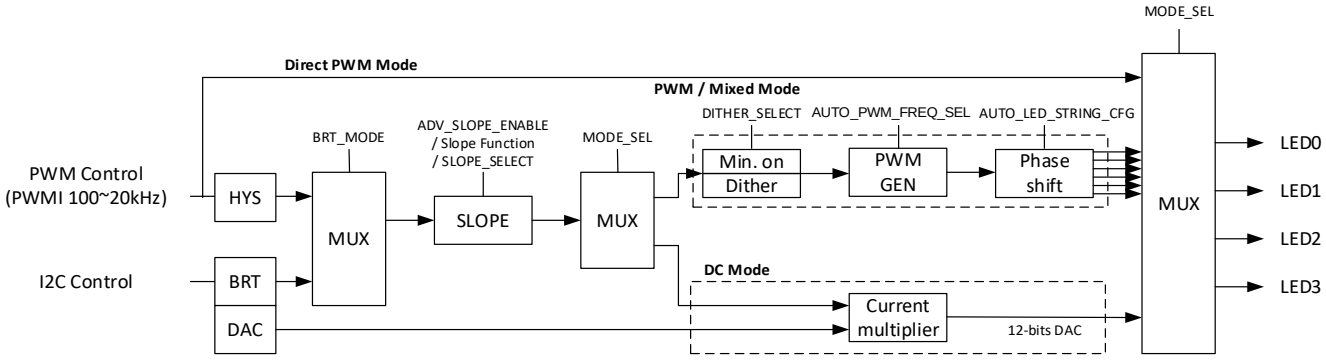

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Table 10

Address: 0x28								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	DP_BRT							
Default	FF							
Type	R/W							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	DP_BRT							
Default	FF							
Type	R/W							

Bit	Name	Description
15:0	DP_BRT	Display Brightness Register

The BRT_MODE register setting is used to select whether the brightness is controlled by the DISP_BRT register or the PWM input pin. The DP BRT register controls 16 bits to adjust the ILED current.

Table 11

Address: 0x40								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	DITHER_SEL			Reserved				
Default	0	0	0	0	0	0	0	0
Type	R/W			R/W				
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	SLOPE_SEL			SLOPE_EN	Reserved		DIMMING_MODE	
Default	1	0	1	1	0	0	0	0
Type	R/W			R/W	R/W		R/W	

Bit	Name	Description
15:13	DITHER_SEL	0h = Dither Disabled 1h = 1-bit Dither 2h = 2-bit Dither 3h = 3-bit Dither 4h = 4-bit Dither 5h = Unused 6h = Unused 7h = Unused
12:8	Reserved	These bits are reserved.
7:5	SLOPE_SEL	0h = 0ms 1h = 1ms 2h = 64ms 3h = 128ms 4h = 256ms 5h = 512ms 6h = 768ms 7h = 1024ms
4	SLOPE_EN	0h = Linear Sloping 1h = Advanced Sloping
3:2	Reserved	These bits are reserved.
1:0	DIMMING_MODE	LED Output Dimming Mode 0h = PWM Mode 1h = Mixed Mode 2h = Direct PWM Mode 3h = 12-bit Constant Current Mode

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The PWM duty cycle dither is a function to increase the number of brightness dimming steps beyond this oscillator clock limitation. The dither function modulates the LED driver output duty to create more average brightness levels. The DITHER_SEL[3:0] register bits control the level of dither, which can be disabled or set to 1, 2, 3, or 4 bits. An optional slope function makes the transition from one brightness value to another optically smooth. The transition time between two brightness values (A and B) is programmed with the SLOPE_SEL[2:0] bits. The SLOPE_EN register controls linear or advanced sloping. With advanced sloping enabled, the brightness changes are further smoothed to be more pleasing to the human eye.

The DIMMING_MODE[1:0] register bits control the performance of dimming, including PWM, Mixed, Direct PWM, and 12 bit Constant Current mode.

Table 12

Address: 0x42								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	PWM_MIN_LIM_EN	Reserved						
Default	0	0	0	0	0	0	0	0
Type	R/W							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved							
Default	00							
Type	R/W							

Bit	**Name**	**Description**
15	PWM_MIN_LIM_EN	Allows PWM pulses to be dithered to reduce lower minimum brightness. When enabled brightness levels that map to less than 200ns pulse width will cause pulses to be skipped. 0h = Disabled 1h = Enabled
14:0	RESERVED	These bits are reserved.

The dither block also has an additional mode at low brightness levels when the LED PWM duty cycle is less than the minimum pulse width. The result is the LED PWM frequency is reduced as more minimum pulses are skipped or dithered out. This function can be enabled using the I^2C interface by programming the PWM_MIN_LIM_EN bit to 1. The result is that the LED PWM frequency is reduced as more minimum pulses are skipped or dithered out.

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Table 13

Address: 0x4E								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	BSTSYNC_INT_EN		VINOCP_INT_EN		ISET_INT_EN		BIST_INT_EN	
Default	0	0	1	0	1	0	0	0
Type	R/W			R/W				
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved		MTP CRC_INT_EN		VINOVP_INT_EN		VINUVP_INT_EN	
Default	0	0	0	0	1	0	1	0
Type	R/W			R/W	R/W		R/W	

Bit	**Name**	**Description**
15:14	BSTSYNC_INT_EN	Boost Sync Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
13:12	VINOCP_INT_EN	VIN Overcurrent Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
11:10	ISET_INT_EN	ISET Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
9:8	BIST_INT_EN	BIST Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
7:6	Reserved	These bits are reserved.
5:4	MTP CRC_INT_EN	MTP CRC Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt

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3:2	VINOVP_INT_EN	VIN Overvoltage Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
1:0	VINUVP_INT_EN	VIN Undervoltage Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt

INTERRUPT_ENABLE_1 is shown in the above figure.

Table 14

Address: 0x50								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	GLOBAL_INT_EN		BSTOVPH_INT_EN		LDO_UV_INT_EN		I2C_TIMEOUT_INT_EN	
Default	1	0	1	0	1	0	1	0
Type	R/W			R/W				
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved		BSTOCP_INT_EN		Reserved		TSD_INT_EN	
Default	0	0	1	0	0	0	1	0
Type	R/W		R/W		R/W		R/W	

Bit	**Name**	**Description**
15:14	GLOBAL_INT_EN	Global Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
13:12	BSTOVPH_INT_EN	Boost OVP High Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
11:10	LDO_UV_INT_EN	LDO UV Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt

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9:8	I2C_TIMEOUT_INT_EN	I2C TIMEOUT Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
7:6	RESERVED	These bits are reserved.
5:4	BSTOCP_INT_EN	Boost Overcurrent Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
3:2	RESERVED	These bits are reserved.
1:0	TSD_INT_EN	Thermal Shutdown Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt

INTERRUPT_ENABLE_2 is shown in the above figure.

Table 15

Address: 0x52								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Reserved							
Default	00							
Type	R/W							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	LED_INT_EN		Reserved					
Default	1	0	0	0	0	0	0	0
Type	R/W		R/W					

Bit	**Name**	**Description**
15:8	Reserved	These bits are reserved.
7:6	LED_INT_EN	LED open/internal short interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
5:0	Reserved	These bits are reserved.

INTERRUPT_ENABLE_3 is shown in the above figure.

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Table 16

Address: 0x54								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	BSTOVPH_STAT	BSTOVPH_CLR	ISET_STAT	ISET_CLR	LDO_UV_STAT	LDO_UV_CLR	I2C_TIMEOUT_STAT	I2C_TIMEOUT_CLR
Default	0	0	0	0	0	0	0	0
Type	R/W			R/W				
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	BSTOVPL_STAT	BSTOVPL_CLR	BSTOCP_STAT	BSTOCP_CLR	BIST_STAT	BIST_CLR	TSD_STAT	TSD_CLR
Default	0	0	0	0	0	0	0	0
Type	R/W			R/W	R/W		R/W	

Bit	Name	Description
15	BSTOVPH_STAT	The FB pin voltage rises above the VFB_OVPH level or the DISCHARGE pin voltage (Vout) rises above VBST_OVPH. Discharge pin - Boost OVP high threshold 50V typical. 0h = No Fault 1h = Fault
14	BSTOVPH_CLR	Boost OVP High Fault Clear Write ’1’ to both Status bit and Clear bit at the same time to clear the interrupt register status and the interrupt pin status.
13	ISET_STAT	The ISET pin voltage is pulled down to below 1V due to the ISET pin resistor being shorted to GND 0h = No Fault 1h = Fault
12	ISET_CLR	ISET Fault Clear Write ‘1’ to both Status bit and Clear bit at the same time to clear the interrupt register status and the interrupt pin status.
11	LDO_UV__STAT	LDO Voltage <3.5V 0h = No Fault 1h = Fault
10	LDO_UV_CLR	LDO UV Fault Clear Write ‘1’ to both Status bit and Clear bit at the same time to clear the interrupt register status and the interrupt pin status.
9	I2C_TIMEOUT_STAT	The device receives an I^2C command without a STOP signal for 500 ms. 0h = No Fault 1h = Fault
8	I2C_TIMEOUT_CLR	I2C Timeout Fault Clear Write ‘1’ to both Status bit and Clear bit at the same time to clear the interrupt register status and the interrupt pin status.
7	BSTOVPL_STAT	Boost OVP Low Status 0h = No Fault 1h = Fault
6	BSTOVPL_CLR	Boost OVP Low Fault Clear Write ‘1’ to both Status bit and Clear bit at the same time to clear the interrupt register status and the interrupt pin status.
5	BSTOCP_STAT	The FB pin voltage falls below the VUVP level of 0.886V for 100 ms.

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		0h = No Fault 1h = Fault
4	BSTOCP_CLR	Boost Overcurrent Fault Clear Write ‘1’ to both Status bit and Clear bit at the same time to clear the interrupt register status and the interrupt pin status.
3	BIST_STAT	BIST Status 0h = No Fault 1h = Fault
2	BIST_CLR	BIST Fault Clear Write ‘1’ to both Status bit and Clear bit at the same time to clear the interrupt register status and the interrupt pin status.
1	TSD_STAT	Thermal Shutdown Status 0h = No Fault 1h = Fault
0	TSD_CLR	Thermal Shutdown Fault Clear Write ‘1’ to both Status bit and Clear bit at the same time to clear the interrupt register status and the interrupt pin status.

INTERRUPT_STATUS_1 is shown in the above figure.

Table 17

Address: 0x56								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Reserved		LED3_FAULT	LED2_FAULT	LED1_FAULT	LED0_FAULT	OPEN_LED_STAT	INTERNAL SHORT_LED_STAT
Default	0	0	0	0	0	0	0	0
Type	R/W			R/W				
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	LED_STAT	LED_CLR	Reserved		MTP_CRC_STAT	MTP_CRC_CLR	DAC_CRC_STAT	DAC_CRC_CLR
Default	0	0	0	0	0	0	0	0
Type	R/W			R/W	R/W		R/W	

Bit	**Name**	**Description**
15:14	Reserved	These bits are reserved.
13	LED3_FAULT	LED3 Status 0h = No Fault 1h = Fault Status is cleared with LED_STATUS bit
12	LED2_FAULT	LED2 Status 0h = No Fault 1h = Fault Status is cleared with LED_STATUS bit
11	LED1_FAULT	LED1 Status 0h = No Fault 1h = Fault Status is cleared with LED_STATUS bit
10	LED0_FAULT	LED0 Status 0h = No Fault 1h = Fault Status is cleared with LED_STATUS bit

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9	OPEN_LED_STAT	LED Open Status 0h = No Fault 1h = Fault Status is cleared with LED_STATUS bit
8	INTERNAL SHORT_LED_STAT	LED Internal Short Status 0h = No Fault 1h = Fault Status is cleared with INTERNAL SHORT bit
7	LED_STAT	LED open/internal short/short to GND fault status 0h = No Fault 1h = Fault
6	LED_CLR	LED open/internal short fault Clear Write '1' to both Status bit and Clear bit at the same time to clear the interrupt register status and the interrupt pin status.
5:4	Reserved	These bits are reserved.
3	MTP_CRC_STAT	MTP CRC Status 0h = No Fault 1h = Fault
2	MTP_CRC_CLR	MTP CRC Clear Write "1" to both Status bit and Clear bit at the same time to clear the interrupt register status and the interrupt pin status.
1	DAC_CRC_STAT	DAC CRC Status 0h = No Fault 1h = Fault
0	DAC_CRC_CLR	DAC CRC Clear Write "1" to both Status bit and Clear bit at the same time to clear the interrupt register status and the interrupt pin status.

INTERRUPT_STATUS_2 is shown in the above figure.

Table 18

Address: 0x58								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Reserved	Reserved	VINOCP_STAT	VINOCP_CLR	Reserved		INT_PIN_STAT	IINT_PIN_CLR
Default	0	0	0	0	0	0	0	0
Type	R/W			R/W				
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved	Reserved	Reserved		VINOVP_STAT	VINOVP_CLR	VINUVP_STAT	VINUVP_CLR
Default	0	0	0	0	0	0	0	0
Type	R/W			R/W	R/W		R/W	

Bit	**Name**	**Description**
15:14	Reserved	These bits are reserved.
13	VINOCP_STAT	Voltage across RISENSE exceeds 220 mV. 0h = No Fault 1h = Fault
12	VINOCP_CLR	VIN Overcurrent Fault Clear. Write "1" to both Status bit and Clear bit at the same time to clear the interrupt register status and the interrupt pin status.
11:10	Reserved	These bits are reserved.
9	INT_PIN_STAT	INT PIN Fault Status 0h = No Fault 1h = Fault

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8	INT_PIN_CLR	INT PIN Fault Fault Clear. Write “1” to both Status bit and Clear bit at the same time to clear the interrupt register status and the interrupt pin status.
7:6	Reserved	These bits are reserved.
5:4	Reserved	These bits are reserved.
3	VINOVP_STAT	VIN voltage rises above 43V 0h = No Fault 1h = Fault
2	VINOVP_CLR	VIN Overvoltage Fault Clear. Write “1” to both Status bit and Clear bit at the same time to clear the interrupt register status and the interrupt pin status.
1	VINUVP_STAT	VIN Undervoltage Fault Status 0h = No Fault 1h = Fault
0	VINUVP_CLR	VIN Undervoltage Fault Clear. Write “1” to both Status bit and Clear bit at the same time to clear the interrupt register status and the interrupt pin status.

INTERRUPT_STATUS_3 is shown in the above figure.

Table 19

Address: 0x1C2								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	LED0_SHORT_DIS	Reserved			LED_Current			
Default	0	0	0	0	1	1	1	1
Type	R/W							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	LED_Current							
Default	FF							
Type	R/W							

Bit	**Name**	**Description**
15	LED0_SHORT_DIS	Short Fault Disable for LED0 0h = Short LED Faults are detected for LED0 output 1h = Short LED Faults are not detected for LED0 output
14:12	Reserved	These bits are reserved.
11:0	LED_Current	LED Current control for LED Output.

The LED_CURRENT[11:0] register can also be used to globally adjust 4 string’s current down from this maximum value. The default value for all the LED_CURRENT[11:0] register is the maximum (4095).

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Table 20

Address: 0x1C4								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	LED1_SHORT_DIS	Reserved						
Default	0	0	0	0	0	0	0	0
Type	R/W							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved							
Default	00							
Type	R/W							

Bit	Name	Description
15	LED1_SHORT_DIS	Short Fault Disable for LED1 0h = Short LED Faults are detected for LED1 output 1h = Short LED Faults are not detected for LED1 output
14:0	Reserved	These bits are reserved.

Table 21

Address: 0x1C6								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	LED2_SHORT_DIS	Reserved						
Default	0	0	0	0	0	0	0	0
Type	R/W							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved							
Default	00							
Type	R/W							

Bit	Name	Description
15	LED2_SHORT_DIS	Short Fault Disable for LED2 0h = Short LED Faults are detected for LED2 output 1h = Short LED Faults are not detected for LED2 output
14:0	Reserved	These bits are reserved.

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Table 22

Address: 0x1C8								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	LED3_SHORT_DIS	Reserved						
Default	0	0	0	0	0	0	0	0
Type	R/W							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved							
Default	00							
Type	R/W							

Bit	Name	Description
15	LED3_SHORT_DIS	Short Fault Disable for LED3 0h = Short LED Faults are detected for LED3 output 1h = Short LED Faults are not detected for LED3 output
14:0	Reserved	These bits are reserved.

Table 23

Address: 0x28A								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Reserved				LED_SHORT_THR			Reserved
Default	0	0	0	0	1	0	0	0
Type	R/W							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved							
Default	00							
Type	R/W							

Bit	Name	Description
15:12	Reserved	These bits are reserved.
11:9	LED_SHORT_THR	Threshold for detecting Shorted LED Fault on LED outputs. Fault is detected when LEDx pin voltage (referenced to ground) exceeds selected threshold when LED driver is enabled. 0h = 2.6V 1h = 3.0V 2h = 3.4V 3h = 3.8V 4h = 4.2V 5h = 4.8V 6h = 5.2V 7h = 6.0V
8:0	Reserved	These bits are reserved.

A shorted LED fault is detected if one or more LED outputs are above the LED_SHORT_THR[11:9] setting.

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Table 24

Address: 0x2A4								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Reserved							
Default	00							
Type	R							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved			FSM_LIVE_STAT				
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
15:5	Reserved	These bits are reserved.
4:0	Reserved	Current status of Device state machine. 1h = LDO_STARTUP 2h = EEPROM_READ 3h = STANDBY 4h - Ch = BOOST_START Dh = NORMAL Eh = DISCHARGE Fh = SHUTDOWN 10h = FAULT_RECOVERY 11h = ALL_LED_FAULT

FSM_LIVE_STAT[4:0] can be read with the serial interface for debugging or to obtain additional device information.

Table 25

Address: 0x2A6								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	PWM_INPUT_STAT							
Default	00							
Type	R							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PWM_INPUT_STAT							
Default	00							
Type	R							

Bit	Name	Description
15:0	PWM_INPUT_STAT	16-bit value for detected duty cycle of PWM input signal.

PWM_INPUT_STAT[15:0] can be read to obtain the duty cycle of the PWM pin information.

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Table 26

Address: 0x2A8								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	LED_PWM_STAT							
Default	00							
Type	R							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	LED_PWM_STAT							
Default	00							
Type	R							

Bit	Name	Description
15:0	LED_PWM_STAT	16-bit PWM Duty Code that Brightness path is driving to LED0 output.

LED_PWM_STATUS[15:0] can be read to obtain the duty cycle of the PWM output information.

Table 27

Address: 0x2AA								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Reserved				ILED_STAT			
Default	0	0	0	0	0	0	0	0
Type	R							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	ILED_STAT							
Default	00							
Type	R							

Bit	Name	Description
15:12	Reserved	These bits are reserved.
11:0	ILED_STAT	12-bit Current DAC Code that Brightness path is driving to LED0 output.

ILED_STAT[11:0] can be read to obtain the DAC code information for the output current.

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Table 28

Address: 0x2AC								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Reserved					BST_STAT		
Default	0	0	0	0	0	0	0	0
Type	R							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	BST_STAT							
Default	00							
Type	R							

Bit	Name	Description
15:12	Reserved	These bits are reserved.
11:0	BST_STAT	11-bit Boost Voltage Code that Adaptive Voltage Control Loop is sending to Analog Boost Block. Boost Output Voltage = ((R_FB1/R_FB2) x 1.2) + (R_FB1 x 18.75nA x VBOOST_STATUS)

BST_STAT[10:0] can be read to obtain the Boost adaptive headroom DAC code information of the output voltage.

Table 29

Address: 0x2AE								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Reserved							PWM_FREQ_SEL
Default	0	0	0	0	0	0	0	0
Type	R/W							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PWM_FREQ_SEL		BST_FREQ_SEL			LED_STRING_CFG		
Default	0	0	0	0	1	0	1	0
Type	R/W							

Bit	Name	Description
15:9	Reserved	These bits are reserved.
8:6	PWM_FREQ_SEL	PWM Frequency Setting based on I^2C Interface. 0h = 152Hz 1h = 305Hz 2h = 610 Hz 3h = 1.22kHz 4h = 2.44kHz 5h = 4.88kHz 6h = 9.77kHz 7h = 19.53kHz
5:3	BST_FREQ_SEL	Boost Frequency Setting based on I^2C Interface 0h = 303kHz 1h = 400kHz 2h = 606kHz 3h = 800kHz 4h = 1MHz 5h = 1.25 MHz 6h = 1.67MHz 7h = 2.2MHz

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2:0	LED_STRING_CFG	Detected LED string configuration. 2h = 4 separate strings 3h = 3 separate strings 4h = 2 separate strings

Table 30

Address: 0x2B0								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	BYP_BIST	BYP_MTP_CRC	VIN_UVLO		BST_GATE_DRV		PL_TSS	WTP_EN
Default	1	1	0	0	1	1	0	0
Type	R/W		R/W					
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	ILED_RISE_SR		ILED_FALL_SR		Reserved		PWM_FSET_SEL	BST_FSET_SEL
Default	0	0	0	0	0	0	1	1
Type	R/W			R/W	R/W		R/W	

Bit	**Name**	**Description**
15	BYP_BIST	BYPASS BIST Fault 0h = Disable 1h = Enable
14	BYP_MTP_CRC	BYP_MTP_CRC 0h = Disable 1h = Enable
13:12	VIN_UVLO	Vin UVLO control for Input voltage 0h = 2.8V 1h = 3.8V 2h = 5.3V 3h = 7.3V
11:10	BST_GATE_DRV	Boost GD drivers peak current, sourcing/sinking 0h = 0.24/0.36A 1h = 0.48/0.76A 2h = 0.84/1.26A 3h = 1.2/1.8A
9	PL_TSS	Boost PL soft-start time: 0h = 25ms 1h = 50ms
8	WTP_EN	WTP Function 0h = Disable 1h = Enable
7:6	ILED_RISE_SR	LED driver rising slew rate.(10%<ILED90%) 0h = 25ns 1h = 50ns 2h = 100ns 3h= 200ns
5:4	ILED_FALL_SR	LED driver falling slew rate.(10%<ILED90%) 0h = 25ns 1h = 50ns 2h = 100ns 3h = 200ns
3:2	Reserved	These bits are reserved.

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1	PWM_FSET_SEL	PWM_FSET Select: 0h = Default code setting. 1h = Follow MTP Set(0x2AE[8:6], this type is R/W)
0	BST_FSET_SEL	BST_FSET Select: 0h = Default code setting. 1h = Follow MTP Set(0x2AE[5:3], this type is R/W)

The VIN_UVLO[13:12] register can be used to adjust the VIN UVLO setting without adding feedback resistors.

The BST_GATE_DRV[11:10] feature provides the ability to adjust the driver strength of the MOSFET in a Boost converter circuit without the need for external components. This allows for fine-tuning of the switching performance of the MOSFET with respect to various parameters such as efficiency, radiated emissions, diode recovery inductive spikes, and dV/dt turn on, which can be critical in optimizing the performance of the Boost converter circuit.

ILED_RISE_SR[7:6] and ILED_FALL_SR[5:4] can be used to adjust the ILED current rising and falling slew rate without adding external components. Changing the LED slew rate can affect the response time and performance of the LED. The LED slew rate refers to the rate at which the LED output can transition from one voltage level to another.

Table 31

Address: 0x2B2								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	LED_HR_THR			LED_HYS_THR			SEQ_CTRL	LED_PWM_ISW_THR
Default	1	0	1	0	0	0	1	0
Type	R/W			R/W				
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	MRSS_SEL		MRSS_FREQ		MRSS_RANGE		MOS_SEL	RANDOM_SEL
Default	1	0	1	0	1	1	0	0
Type	R/W			R/W	R/W		R/W	
Bit	**Name**			**Description**				
15:13	LED_HR_THR			LOW headroom voltage and initial voltage setting. 0h = 0.35V 1h = 0.4V 2h = 0.45V 3h = 0.5V 4h = 0.55V 5h = 0.6V 6h = 0.65V 7h = 0.7V				
12:10	LED_HYS_THR			MID headroom voltage and initial voltage setting. 0h = 0.05V 1h = 0.1V 2h = 0.15V 3h = 0.2V 4h = 0.25V 5h = 0.3V 6h = 0.4V 7h = 0.5V				
9	SEQ_CTRL			Power sequence control: 0h = Keep in standby mode 1h = Go to power-line FET soft-start mode				
8	LED_PWM_ISW_THR			Switch point from PWM control to current control when Hybrid mode is enabled				

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		0h = 12.5% 1h = 25%
7:6	MRSS_SEL	Boost spread spectrum function select: 0h = Random 1h = Triangular 2h = MRSS(Random+Triangular) 3h = MRSS(Random+Sawtooth)
5:4	MRSS_FREQ	Boost spread spectrum modulation frequency 0h = 11000 Hz 1h = 15000 Hz 2h = 20000 Hz 3h = 30000 Hz
3:2	MRSS_RANGE	OSC_BST spread spectrum range 0h = ±3.68% 1h = ±4.6% 2h = ±5.52% 3h = ±7.13%
1	MOS_SEL	MOSFET_Select 0h:P-MOSFET 1h:N-MOSFET
0	RANDOM_SEL	Boost LX change cycle. 0h = Every 1 cycle to change Frequency. 1h = Every 8 cycle to change Frequency.

LED headroom is the voltage difference between the LED forward voltage and the LED driver output voltage. It is an important parameter that affects the performance and efficiency of an LED driver circuit. Different LED headroom values can provide various benefits, depending on the requirements of the application.

Table 32

Address: 0x2B4								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	SYNC_SEL	SYNC_EN_SS	DAC_CRC_EN	DISCH_SEL		SHORT_FLT_CNT		Reserved
Default	1	1	0	1	1	1	1	0
Type	R/W			R/W				
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	LED_FLTR_TIME_RISE						Reserved	
Default	0	0	1	0	1	1	0	0
Type	R/W			R/W	R/W		R/W	

Bit	**Name**	**Description**
15	SYNC_SEL	SYNC select: 0h: No the function 1h: Setting SYNC_EN_SS bit
14	SYNC_EN_SS	SS function EN when SYNC_SEL=1 0h: Disable SS function 1h: Enable SS function
13	DAC_CRC_EN	DAC CRC enable 0h = Disable 1h = Enable
12:11	DISCH_SEL	Discharge time select 0h = Disable 1h = 100ms

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		2h = 200ms 3h = 400ms
10:9	SHORT_FLT_CNT	SCounter that defines how many count a short condition must be continuous present to trip the LED short and LED string short fault 0h = 2 ms count 1h = 3 ms count 2h = 4 ms count 3h = 5 ms count
8	Reserved	These bits are reserved.
7:2	LED_FLTR_TIME_RISE	Selects the number of clocks the LEDx voltage comparators is filtered (rising edge) before they are used to detect LED/string faults and adjust the adaptive boost voltage. This filter time is for the rising edge of each individual string. 0h = 0 1h = 4 2h = 8 3h = 12 4h = 16 .. 3Fh = 252
1:0	Reserved	These bits are reserved.

LED_SHORT_FLT_CNT[10:9] can offer the detection time from 2ms to 4ms to trigger the LED short fault. When a short fault happens, it needs to keep a period of time and then enters into the protection. Also, the LED strings operating at the low duty may lead to short protection by detecting the wrong statement. Therefore, the register 0x2B6h LED_SHORT_LOW_BRT_DIS[15:8] can set the brightness for LED short detect condition disable. If the brightness at the LED string is smaller than the setting, the short protection will not be triggered and latched. And its enable function is shown in the register 0x2B6h LED_SHORT_LOW_BRT_DIS[7]. When the 0x2B6h LED_SHORT_LOW_BRT_DIS[7] is set to ‘1’, the function about “LED short detect condition disable” will be used according to the register 0x2B6h BRT_LED_SHORT_DIS[15:8].

The individual filter is conducted for each channel to filter the duration programmed by register 0x2B4h LED_FLTR_TIME_RISE[7:2]. The comparators about the detecting level are neglected in the period of filter time. Both of these filters start counting the duration from its own LED PWM rising edge they can be set from 0 to 252 clock cycles of 20MHz.

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Table 33

Address: 0x2B6								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	BRT_LED_SHORT_DIS							
Default	03							
Type	R/W							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	LED_SHORT_LOW_BRT_DIS	Reserved	LED_GLOBAL_FLTR_TIME					
Default	0	0	0	0	0	1	0	0
Type	R/W	R/W	R/W					

Bit	**Name**	**Description**
15:8	BRT_LED_SHORT_DIS	Brightness setting for LED short detect condition disable detect when current brightness ≥ BRT_LED_SHORT_DIS
7	LED_SHORT_LOW_BRT_DIS	To disable LED short condition "dac code = 0, but headroom above HIGH" when BRT setting is less than 0x2B6[15:8] 0h: Disable LED short condition when BRT setting is less than {0x2B6[15:8]} 1h: Enable LED short condition when BRT setting is less than {0x2B6[15:8]}
6	Reserved	These bits are reserved.
5:0	LED_GLOBAL_FLTR_TIME	Selects the number of clocks used for global filtering (rising and falling edge). This is also to select the filter time of the low comparator for each individual string. 0h = 0 1h = 4 2h = 8 3h = 12 4h = 16 .. 3Fh = 252

Similarly, the global filter is conducted for every channels to filter the duration programmed by the register 0x2B6h LED_GLOBAL_FLTR_TIME[5:0]. It starts to count from the PWM rising and falling edges of any other LED channels except its own. The global filter is also able to be set from 0 to 252 clock cycles of 20MHz.

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Table 34

Address: 0x2B8								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Reserved							
Default	00							
Type	R							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved				READ_DEVICE_INF			
Default	0	0	0	0	1	0	1	0
Type	R				R			

Bit	Name	Description
15:4	Reserved	These bits are reserved.
3:0	READ_DEVICE_INF	Read Device information

READ_DEVICE_INF[3:0] can be read to obtain the RTQ4554-QT information(0A).

Table 35

Address: 0xFE								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	MTP Programming	Reserved						MTP Read
Default	0	0	0	0	0	0	0	0
Type	R/W	R/W						R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved							
Default	00							
Type	R/W							

Bit	Name	Description
15	MTP Programming	0h = normal operation 1h = start MTP programming sequence
14:9	Reserved	These bits are reserved.
8	MTP Red	0h = I^2C read data from DAC 1h = I^2C read data from MTP
7:0	Reserved	These bits are reserved.

The RTQ4554-QT has an MTP function for MTP programming and MTP Read. The MTP register stores the default settings. When power-on, the contents of the MTP register are transferred to the I^2C register. Write and read can be made directly to control the I^2C register without any changes to the MTP register. If the MTP default value must be changed, first write all desired data to the I^2C register.

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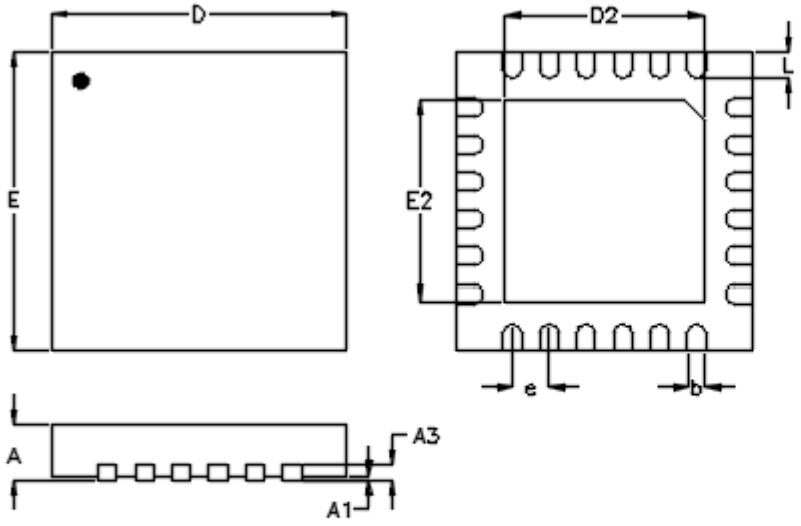
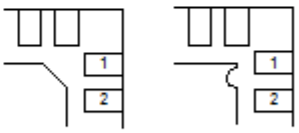
18 Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	3.900	4.100	0.154	0.161
D2	2.650	2.750	0.104	0.108
E	3.900	4.100	0.154	0.161
E2	2.650	2.750	0.104	0.108
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 24SL QFN 4x4 Package

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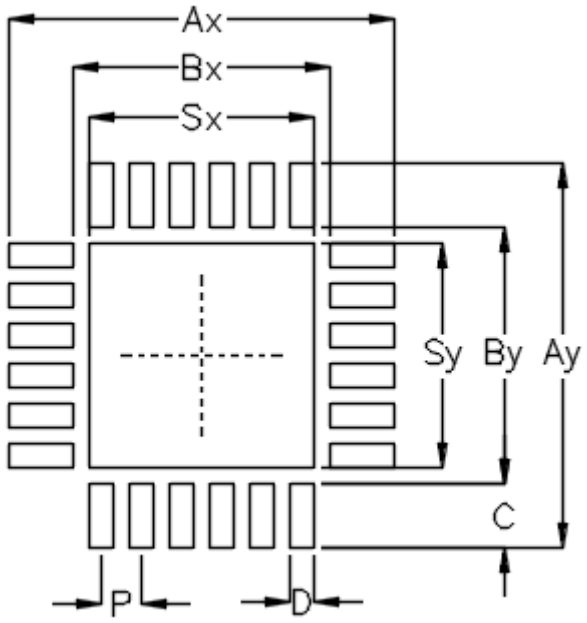
19 Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN4*4-24S	24	0.50	4.80	4.80	3.20	3.20	0.80	0.30	2.80	2.80	±0.05

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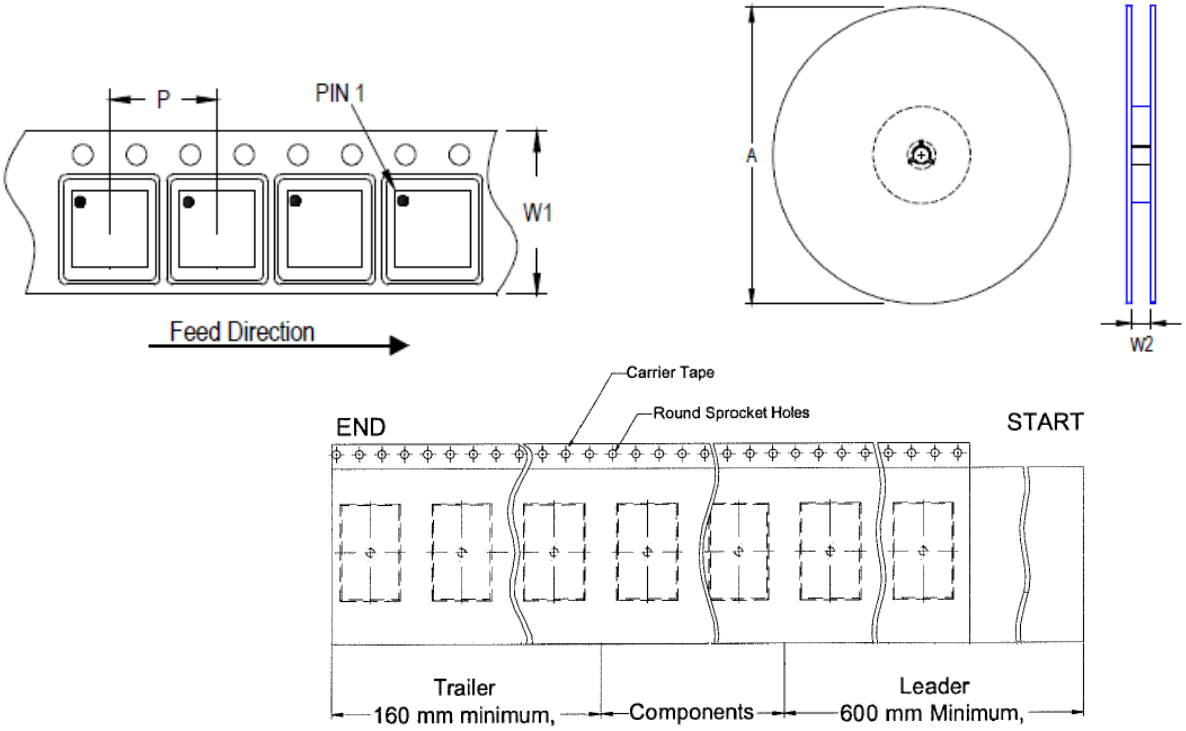
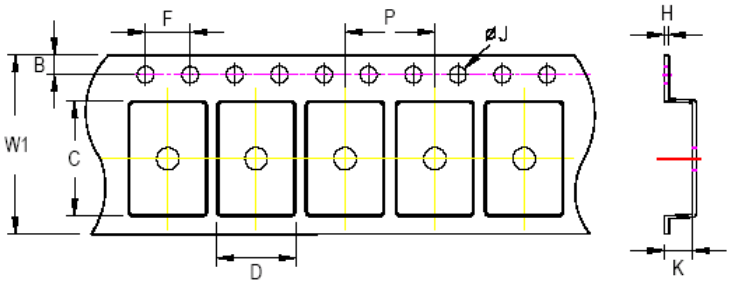
20 Packing Information

20.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 4x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

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20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	Reel 7”	4	3 reels per inner box **Box A**
2	HIC & Desiccant (1 Unit) inside	5	12 inner boxes per outer box
3	Caution label is on backside of Al bag	6	Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN/DFN 4x4	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

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20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
00	2024/10/9	Final	

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