

Power Solution for Wearable AMOLED Products

1 General Description

The RT4733 is a highly integrated power solution with a buck-boost converter and an inverting charge pump to generate negative output voltage. The output voltages can be adjusted via the SWIRE interface protocol. The part maintains high efficiency by utilizing a $-0.5x/-1x$ mode fractional charge pump. With an input voltage range of 2.9V to 5.5V, the RT4733 is optimized for products powered by single-cell batteries and can supply symmetrical output currents up to 150mA. The RT4733 is available in the WL-CSP-21B 1.31x2.91 (BSC) package.

The recommended junction temperature range is -40°C to 125°C , and the ambient temperature range is -40°C to 85°C .

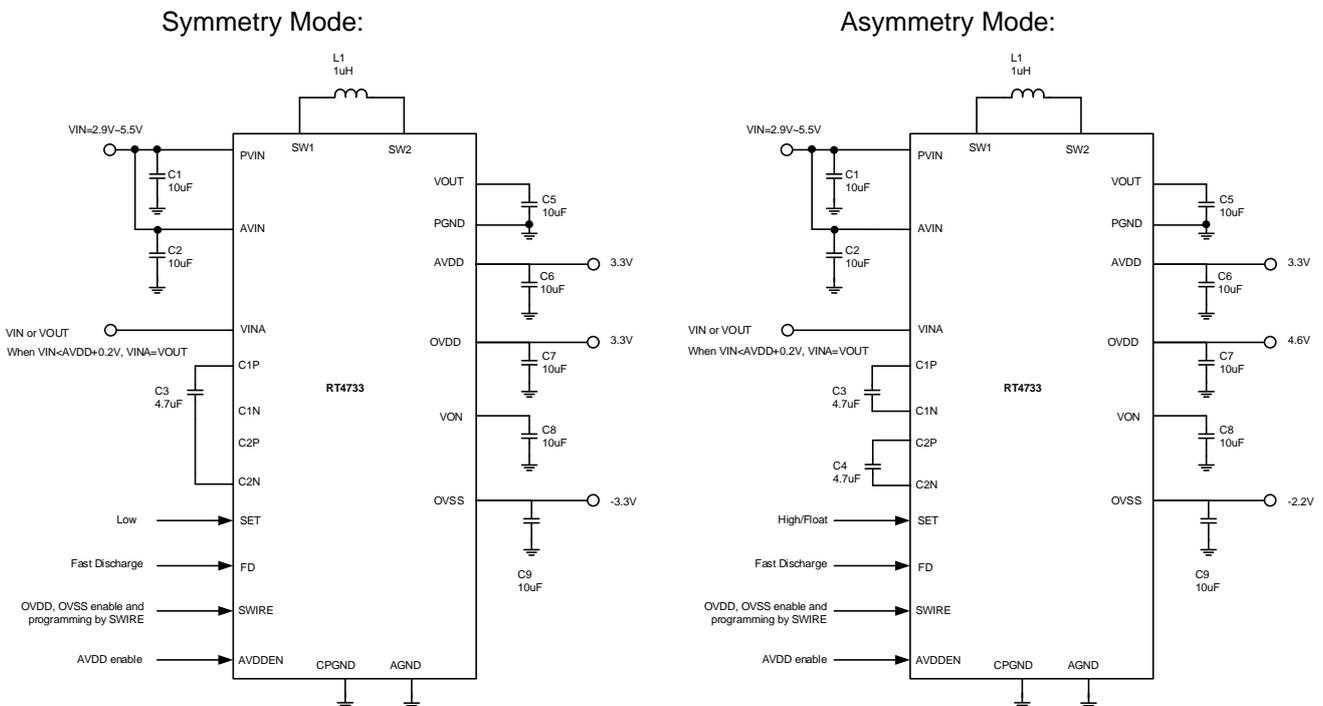
2 Applications

- AMOLED Panels
- Wearable Devices

3 Features

- 2.9V to 5.5V Supply Voltage Range
- Positive OVDD Voltage from 2.8V to 4.6V
- Negative OVSS Voltage from -0.6V to -4.2V
- Positive AVDD Voltage from 2.8V to 3.3V
- $-0.5x/-1x$ VON Negative Charge Pump
- Maximum Output Current up to 150mA for AMOLED Positive & Negative Power Supply in Symmetry Mode
- Maximum Output Current up to 60mA for AMOLED Positive & Negative Power Supply in Asymmetry Mode
- Maximum Output Current up to 30mA for AVDD Output Supply
- Excellent Line and Load Transient/Regulation
- Discharge/Hi-Z Function
- Low Quiescent Current $< 1\mu\text{A}$ in Shutdown Mode
- UVLO, OCP, SCP, OTP Protection
- Available in 21-Ball WL-CSP Package

4 Simplified Application Circuit



Note: C4 is only used when VON: $-0.5x$.

Without head room control (HRC)

5 Ordering Information

RT4733□

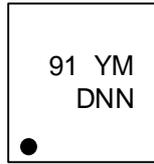
Package Type⁽¹⁾

WSC: WL-CSP-21B 1.31x2.91 (BSC)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with ⁽¹⁾ indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

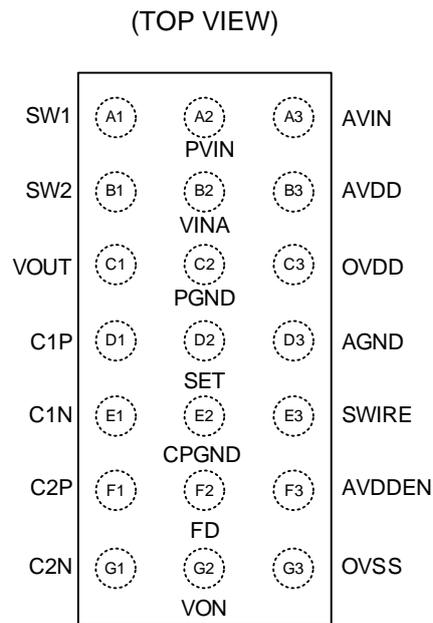


91: Product Code
YMDNN: Date Code

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7 Pin Configuration



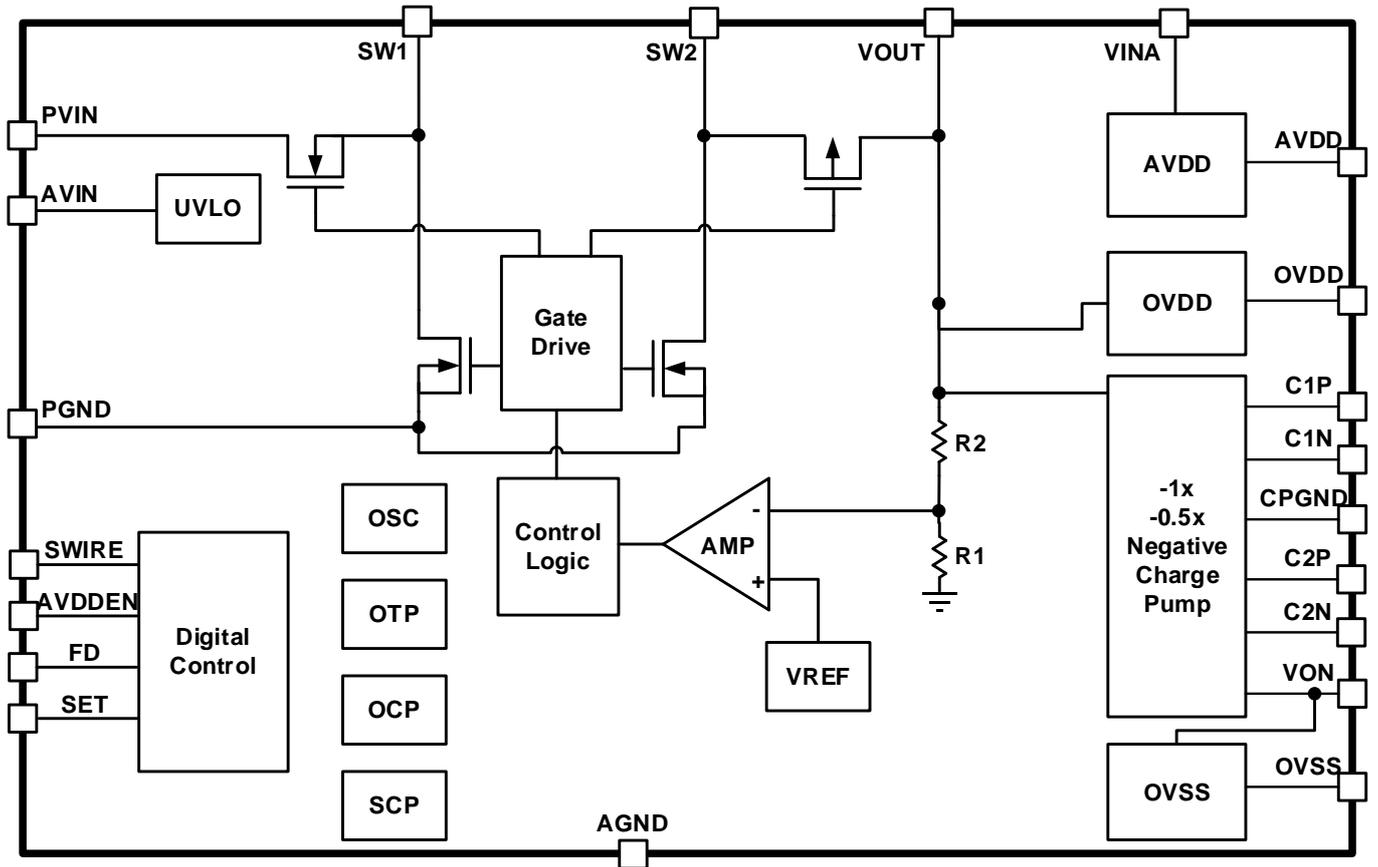
WL-CSP-21B 1.31x2.91 (BSC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	SW1	SW1 switching node for buck-boost converter.
A2	PVIN	Power input for buck-boost converter.
A3	AVIN	Analog power input for IC.
B1	SW2	SW2 Switching node for buck-boost converter.
B2	VINA	Power input for AVDD.
B3	AVDD	AVDD LDO output.
C1	VOUT	VOUT Buck-boost converter output.
C2	PGND	Power ground.
C3	OVDD	OVDD LDO output.
D1	C1P	Flying capacitor 1 positive connection.
D2	SET	Select pin for symmetry or asymmetry power. SET pin = L: symmetry mode; SET pin = H or floating: asymmetry mode.
D3	AGND	Analog ground.
E1	C1N	Flying capacitor 1 negative connection.
E2	CPGND	Charge pump ground.
E3	SWIRE	Enable for OVDD and OVSS. SWIRE control interface.
F1	C2P	Flying capacitor 2 positive connection.
F2	FD	Enable for fast discharge function. FD pin = L: disable; FD pin = H or floating: enable.
F3	AVDDEN	Enable for AVDD.

Pin No.	Pin Name	Pin Function
G1	C2N	Flying capacitor 2 negative connection.
G2	VON	VON charge pump output.
G3	OVSS	OVSS LDO output.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, PVIN, AVIN, VINA to AGND ----- -0.3V to 6V
- VOUT, AVDD, OVDD, SWIRE, AVDDEN, SET, FD to AGND ----- -0.3V to 6V
- VON, OVSS, to AGND ----- -6V to 0.3V
- SW1, SW2, C1P, C2P to PGND ----- -0.3V to 6V
- C1N, C2N to PGND ----- -6V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
 - WL-CSP-21B 1.31x2.91 (BSC) ----- 2.99W
- Package Thermal Resistance (Note 3)
 - WL-CSP-21B 1.31x2.91 (BSC), θ_{JA} ----- 33.4°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 4)
 - HBM (Human Body Model) ----- 2kV
 - CDM (Charge Device Model) ----- 500V

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage Range----- 2.9V to 5.5V
- Ambient Temperature Range ----- -40°C to 85°C
- Junction Temperature Range ----- -40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

($V_{IN} = 3.7V$, $VOVDD = 3.3V$, $VOVSS = -3.3V$, $VAVDD = 3.3V$, $C_{IN} = 10\mu F$, $COVDD = COVSS = CAVDD = 10\mu F$, $L = 1\mu H$, $T_A = 25^\circ C$, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
General						
VIN Supply Input Voltage	V_{IN}		2.9	3.7	5.5	V
Quiescent Current	$I_{Q_VIN_SW_VON_N1x}$	$V_{IN} = 3.7V$, no load, SET = L, AVDDEN = H, SWIRE = H (pulse = 97 default), bypass mode	--	270	--	μA
		$V_{IN} = 3.7V$, no load, SET = L, AVDDEN = H, SWIRE = H (pulse = 95), bypass mode	--	170	--	
	$I_{Q_VIN_SW_VON_N0.5x}$	$V_{IN} = 3.7V$, no load, SET = H, AVDDEN = H, SWIRE = H (pulse = 97 default)	--	380	--	
		$V_{IN} = 3.7V$, no load, SET = H, AVDDEN = H, SWIRE = H (pulse = 95)	--	230	--	
$I_{Q_VIN_IDLE}$	$V_{IN} = 3.7V$, no load, AVDDEN = H, SWIRE = L	--	70	--		
Shutdown Current	I_{SHDN_VIN}	$V_{IN} = 2.5V$ to $5.5V$, AVDDEN = L, SWIRE = L	--	--	1	μA
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}	VIN rising	--	2.35	--	V
Undervoltage-Lockout Falling Threshold	V_{UVLO_F}	VIN falling	--	2.2	--	V
Over-Temperature Protection	TOTP		--	140	--	$^\circ C$
Over-Temperature Protection Hysteresis	TOTP_HYS		--	15	--	$^\circ C$
SWIRE						
Initial Waiting Time	$t_{WAIT_INT_SWIRE}$	AVDDEN = H	300	--	--	μs
	$t_{WAIT_INT_OVDDEN}$		--	--	300	
SWIRE Input Voltage Logic-High	V_{IH_SWIRE}		1	--	VIN	V
SWIRE Input Voltage Logic-Low	V_{IL_SWIRE}		GND	--	0.4	V
Pull-Down Resistance	R_{PD_SWIRE}		350	500	650	k Ω
Turn-Off Detection Time	t_{OFF_SWIRE}		120	--	150	μs
Signal Stop Indicate Time	t_{STOP_SWIRE}		80	--	100	μs
Rising Time	t_{R_SWIRE}		--	--	200	ns
Falling Time	t_{F_SWIRE}		--	--	200	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clocked SWIRE High	t _{ON_SWIRE}		4	--	20	μs
Clocked SWIRE Low	t _{OFF_SWIRE}		4	--	20	μs
Input Clocked Frequency	f _{CLK_SWIRE}		25	--	125	kHz
Logic Signals (AVDDEN)						
Input Voltage Logic-High	V _{IH_AVDDEN}		1	--	V _{IN}	V
Input Voltage Logic-Low	V _{IL_AVDDEN}		GND	--	0.4	V
Turn-Off Detection Time	t _{OFF_AVDDEN}		120	--	150	μs
Pull-Down Resistance	R _{PD_AVDDEN}		350	500	650	kΩ
Logic Signals (SET, FD)						
Input Voltage Logic-High	V _{IH_SET, FD}		1.0	--	V _{IN}	V
Input Voltage Logic-Low	V _{IL_SET, FD}		GND	--	0.4	V
Pull-Up Resistance	R _{PU_SET, FD}		210	265	340	kΩ
VOUT Buck-Boost Converter						
Output Voltage Range	V _{OUT}	SET = L	3	--	4.8	V
		SET = H	3	--	5.4	
Switching Frequency Accuracy	V _{OUT_ACC_SW}	V _{IN} = 2.9V to 5V, V _{OUT} = 3.55V, V _{OUT} operates in boost or buck mode	1.98	2.2	2.42	MHz
Maximum Output Current Capability	I _{OUT_MAX}	SEL = L, V _{IN} = 2.9V to 5V	300	--	--	mA
		SEL = H, V _{IN} = 2.9V to 5V	150	--	--	
High-Side MOSFET On-Resistance	R _{DS(on)_H_VOUT}	I _{OUT} = 100mA	--	100	--	mΩ
Low-Side MOSFET On-Resistance	R _{DS(on)_L_VOUT}	I _{OUT} = 100mA	--	200	--	mΩ
Current Limit Peak	I _{LIM_PEAK}		1.5	1.75	2	A
Short Circuit Protection Threshold	V _{SCP_VOUT}	V _{IN} = 2.9V to 5V, without hysteresis	75	80	85	%
Short Circuit Protection Delay Time	t _{DLY_SCP_VOUT}	V _{IN} = 2.9V to 5V	0.85	1	1.15	ms
Power-Off Discharge Time	t _{DISCHG_VOUT}	V _{IN} = 2.9V to 5V, AVDDEN = SWIRE = L	3	--	--	ms
VON Charge Pump						
Power-Off Discharge Time	t _{DISCHG_VON}	V _{IN} = 2.9V to 5V, SWIRE = L	3	--	--	ms
AVDD LDO						
Output Voltage Range	V _{AVDD}		2.8	--	3.3	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Default Output Voltage	V _{AVDD_3.3V}	V _{IN} = 2.9V to 5V, V _{INA} = V _{AVDD} + 0.3V, no load	3.2835	3.3	3.3165	V
Output Accuracy	V _{AVDD_ACC}	V _{IN} = 2.9V to 5V, V _{AVDD} = 2.8V to 3.3V, no load, T _A = 25°C	-0.5	--	0.5	%
	V _{AVDD_ACC_3T}	V _{IN} = 2.9V to 5V, V _{AVDD} = 2.8V to 3.3V, no load, T _A = -40 to 85°C	-0.8	--	0.8	
Maximum Output Current Capability	I _{AVDD_MAX}	V _{IN} = 2.9V to 5V, V _{AVDD} = 2.8V to 3.3V	30	--	--	mA
Line Regulation	V _{LINE_REG_AVDD}	V _{IN} = 2.9V to 5V, V _{AVDD} = 2.8V to 3.3V, I _{AVDD} = 0mA to 30mA	--	5	10	mV
Load Regulation	V _{LOAD_REG_AVDD}	V _{IN} = 2.9V to 5V, V _{AVDD} = 2.8V to 3.3V, I _{AVDD} = 0mA to 30mA	--	5	10	mV
Output Voltage Ripple	V _{OUT_RIPPLE_SYM_AVDD}	V _{IN} = 3.7V, SET = L, V _{AVDD} = 3.3V, I _{AVDD} ≤ 10mA, V _{OVDD} = 3.3V, I _{OVDD} ≤ 30mA, V _{OVSS} = -3.3V, I _{OVSS} ≤ 30mA	--	--	Δ10	mV
	V _{OUT_RIPPLE_ASYM_AVDD}	V _{IN} = 3.7V, SET = H, V _{AVDD} = 3.3V, I _{AVDD} ≤ 10mA, V _{OVDD} = 4.6V, I _{OVDD} ≤ 30mA, V _{OVSS} = -2.2V, I _{OVSS} ≤ 30mA	--	--	Δ10	
	V _{OUT_RIPPLE_HB_AVDD}	V _{IN} = 3.7V, SET = L, HRC = Enable, V _{AVDD} = 3.3V, I _{AVDD} ≤ 10mA, V _{OVDD} = 3.3V, I _{OVDD} ≤ 150mA, V _{OVSS} = -4V, I _{OVSS} ≤ 150mA	--	--	Δ10	
Line Transient Response	V _{LINE_TR_SYM_AVDD}	V _{IN} = 2.9V to 5V, ΔV _{IN} = 500mV, t _r = t _f = 10μs, SET = L, V _{AVDD} = 3.3V, I _{AVDD} = 10mA, V _{OVDD} = 3.3V, I _{OVDD} = 30mA, V _{OVSS} = -3.3V, I _{OVSS} = 30mA	-5	--	5	mV
	V _{LINE_TR_ASYM_AVDD}	V _{IN} = 2.9V to 5V, ΔV _{IN} = 500mV, t _r = t _f = 10μs, SET = H, V _{AVDD} = 3.3V, I _{AVDD} = 10mA, V _{OVDD} = 4.6V, I _{OVDD} = 30mA, V _{OVSS} = -2.2V, I _{OVSS} = 30mA	-5	--	5	
	V _{LINE_TR_HB_AVDD}	V _{IN} = 2.9V to 5V, ΔV _{IN} = 500mV, t _r = t _f = 10μs, SET = L, HRC = Enable, V _{AVDD} = 3.3V, I _{AVDD} = 10mA, V _{OVDD} = 3.3V, I _{OVDD} = 150mA, V _{OVSS} = -4V, I _{OVSS} = 150mA	-10	--	10	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Load Transient Response	V _{LOAD_TR SYM_AVDD}	V _{IN} = 3.7V, SET = L, V _{AVDD} = 3.3V, V _{OVDD} = 3.3V, V _{OVSS} = -3.3V, I _{OVDD-OVSS} = 50mA, I _{AVDD} = 0 ↔ 10mA, t _R = t _F = 10μs	-10	--	10	mV
	V _{LOAD_TR SYM_AVDD}	V _{IN} = 3.7V, SET = H, V _{AVDD} = 3.3V, V _{OVDD} = 4.6V, V _{OVSS} = -2.2V, I _{OVDD-OVSS} = 50mA, I _{AVDD} = 0 ↔ 10mA, t _R = t _F = 10μs	-10	--	10	
	V _{LOAD_TR HB_AVDD}	V _{IN} = 3.7V, SET = L, HRC = Enable, V _{AVDD} = 3.3V, V _{OVDD} = 3.3V, V _{OVSS} = -4V, I _{OVDD-OVSS} = 150mA, I _{AVDD} = 0 ↔ 10mA, t _R = t _F = 10μs	-10	--	10	
Current Limit	I _{LIM_AVDD}	V _{IN} = 2.9V to 5V, V _{AVDD} = 2.8V to 3.3V	--	150	--	mA
Short Circuit Protection Threshold	V _{SCP_AVDD}	V _{IN} = 2.9V to 5V, V _{AVDD} = 2.8V to 3.3V	75	80	85	%
Short Circuit Protection Delay Time	t _{DLY SCP_AVDD}	V _{IN} = 2.9V to 5V, V _{AVDD} = 2.8V to 3.3V	0.85	1	1.15	ms
Power-Off Discharge Time	t _{DISCHG_AVDD}	V _{IN} = 2.9V to 5V, V _{AVDD} = 2.8V to 3.3V, AVDDEN = L	--	--	3	ms
OVDD LDO						
Output Voltage Range	V _{OVDD}		2.8	--	4.6	V
Default Output Voltage	V _{OVDD_3.3V}	V _{IN} = 2.9V to 5V, no load, SET = L	3.2835	3.3	3.3165	V
	V _{OVDD_4.6V}	V _{IN} = 2.9V to 5V, no load, SET = H	4.577	4.6	4.623	
Output Accuracy	V _{OVDD_ACC}	V _{IN} = 2.9V to 5V, V _{OVDD} = 2.8V to 4.6V, no load, T _A = 25°C	-0.5	--	0.5	%
	V _{OVDD_ACC_3T}	V _{IN} = 2.9V to 5V, V _{OVDD} = 2.8V to 4.6V, no load, T _A = -40 to 85°C	-0.8	--	0.8	
Maximum Output Current Capability	I _{MAX_OVDD}	V _{IN} = 2.9V to 5V, HRC = Enable, V _{OVDD} = 2.8V to 4.1V	150	--	--	mA
		V _{IN} = 2.9V to 5V, HRC = Disable, V _{OVDD} = 2.8V to 4.6V	60	--	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	V _{LINE_REG_OVDD}	V _{IN} = 2.9V to 5V, HRC = Enable, V _{OVDD} = 2.8V to 4.1V, I _{OVDD} = 0mA to 150mA	--	5	10	mV
		V _{IN} = 2.9V to 5V, HRC = Disable, V _{OVDD} = 2.8V to 4.6V, I _{OVDD} = 0mA to 60mA	--	5	10	
Load Regulation	V _{LOAD_REG_OVDD}	V _{IN} = 2.9V to 5V, HRC = Enable, V _{OVDD} = 2.8V to 4.1V, I _{OVDD} = 0mA to 150mA	--	5	10	mV
		V _{IN} = 2.9V to 5V, HRC = Disable, V _{OVDD} = 2.8V to 4.6V, I _{OVDD} = 0mA to 60mA	--	5	10	
Output Voltage Ripple	V _{OUT_RIPPLE_SYM_OVDD}	V _{IN} = 3.7V, SET = L, V _{AVDD} = 3.3V, I _{AVDD} ≤ 10mA, V _{OVDD} = 3.3V, I _{OVDD} ≤ 30mA, V _{OVSS} = -3.3V, I _{OVSS} ≤ 30mA	--	--	Δ10	mV
	V _{OUT_RIPPLE_ASYM_OVDD}	V _{IN} = 3.7V, SET = H, V _{AVDD} = 3.3V, I _{AVDD} ≤ 10mA, V _{OVDD} = 4.6V, I _{OVDD} ≤ 30mA, V _{OVSS} = -2.2V, I _{OVSS} ≤ 30mA	--	--	Δ10	
	V _{OUT_RIPPLE_HB_OVDD}	V _{IN} = 3.7V, SET = L, HRC = Enable, V _{AVDD} = 3.3V, I _{AVDD} ≤ 10mA, V _{OVDD} = 3.3V, I _{OVDD} ≤ 150mA, V _{OVSS} = -4V, I _{OVSS} ≤ 150mA	--	--	Δ10	
Line Transient Response	V _{LINE_TR_SYM_OVDD}	V _{IN} = 2.9 to 5V, ΔV _{IN} = 500mV, t _r = t _f = 10μs, SET = L, V _{AVDD} = 3.3V, I _{AVDD} = 10mA, V _{OVDD} = 3.3V, I _{OVDD} = 30mA, V _{OVSS} = -3.3V, I _{OVSS} = 30mA	-5	--	5	mV
	V _{LINE_TR_ASYM_OVDD}	V _{IN} = 2.9V to 5V, ΔV _{IN} = 500mV, t _r = t _f = 10μs, SET = H, V _{AVDD} = 3.3V, I _{AVDD} = 10mA, V _{OVDD} = 4.6V, I _{OVDD} = 30mA, V _{OVSS} = -2.2V, I _{OVSS} = 30mA	-5	--	5	
	V _{LINE_TR_HB_AVDD}	V _{IN} = 2.9V to 5V, ΔV _{IN} = 500mV, t _r = t _f = 10μs, SET = L, HRC = Enable, V _{AVDD} = 3.3V, I _{AVDD} = 10mA, V _{OVDD} = 3.3V, I _{OVDD} = 150mA, V _{OVSS} = -4V, I _{OVSS} = 150mA	-10	--	10	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Load Transient Response	V _{LOAD_TR_SYM_OVDD}	V _{IN} = 3.7V, SET = L, V _{AVDD} = 3.3V, V _{OVDD} = 3.3V, V _{OVSS} = -3.3V, I _{AVDD} = 10mA, I _{OVDD-OVSS} = 0 ↔ 50mA, t _R = t _F = 10ms	-10	--	10	mV
	V _{LOAD_TR_ASYM_OVDD}	V _{IN} = 3.7V, SET = H, V _{AVDD} = 3.3V, V _{OVDD} = 4.6V, V _{OVSS} = -2.2V, I _{AVDD} = 10mA, I _{OVDD-OVSS} = 0 ↔ 50mA, t _R = t _F = 10ms	-10	--	10	
	V _{LOAD_TR_HB_OVDD}	V _{IN} = 3.7V, SET = L, HRC = Enable, V _{AVDD} = 3.3V, V _{OVDD} = 3.3V, V _{OVSS} = -4V, I _{AVDD} = 10mA, I _{OVDD-OVSS} = 0 ↔ 150mA, t _R = t _F = 10ms	-10	--	10	
Current Limit	I _{LIM_OVDD}	V _{IN} = 2.9V to 5V, V _{OVDD} = 2.8V to 4.6V	--	250	--	mA
Short Circuit Protection Threshold	V _{SCP_OVDD}	V _{IN} = 2.9V to 5V, V _{OVDD} = 2.8V to 4.6V	75	80	85	%
Short Circuit Protection Delay Time	t _{DLY_SCP_OVDD}	V _{IN} = 2.9V to 5V, V _{OVDD} = 2.8V to 4.6V	0.85	1	1.15	ms
Power-Off Discharge Time	t _{DISCHG_OVDD}	V _{IN} = 2.9V to 5V, V _{OVDD} = 2.8V to 4.6V, SWIRE = L	--	--	3	ms
OVSS LDO						
Output Voltage Range	V _{OVSS}	SET = L	-4.2	--	-0.6	V
		SET = H	-2.4	--	-0.6	
Default Output Voltage	V _{OVSS_N3.3V}	V _{IN} = 2.9V to 5V, no load, SET = L	-3.3165	-3.3	-3.2835	V
	V _{OVSS_N2.2V}	V _{IN} = 2.9V to 5V, no load, SET = H	-2.222	-2.2	-2.178	
Output Voltage Accuracy	V _{OVSS_ACC_N3.3V}	V _{IN} = 2.9V to 5V, SET = L, V _{OVSS} = -3.3V, no load, T _A = 25°C	-0.5	--	0.5	%
	V _{OVSS_ACC_3T_N3.3V}	V _{IN} = 2.9V to 5V, SET = L, V _{OVSS} = -3.3V, no load, T _A = -40°C to 85°C	-0.8	--	0.8	
	V _{OVSS_ACC_N2.2V}	V _{IN} = 2.9V to 5V, SET = H, V _{OVSS} = -2.2V, no load, T _A = 25°C	-1	--	1	
Maximum Output Current Capability	I _{MAX_OVSS}	V _{IN} = 2.9V to 5V, HRC = Enable, V _{OVSS} = -4V to -0.6V,	150	--	--	mA
		V _{IN} = 2.9V to 5V, HRC = Disable, V _{OVSS} = -4.2V to -0.6V	60	--	--	

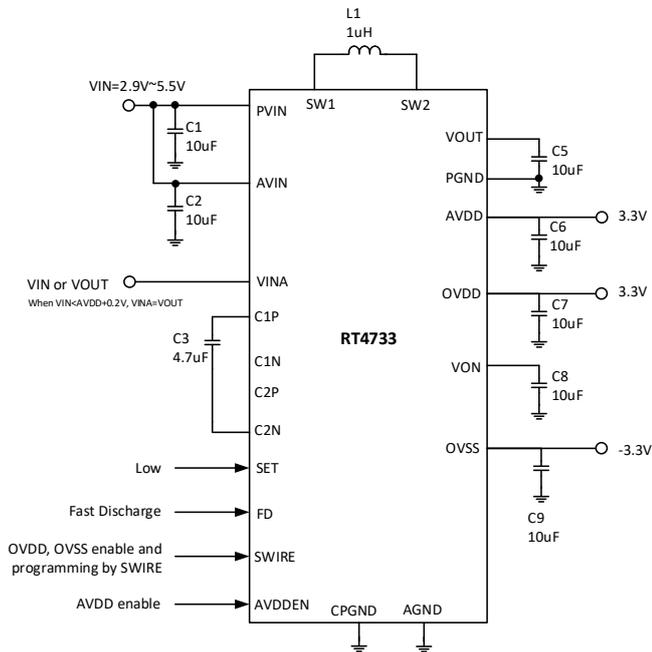
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	V _{LINE_REG_OVSS}	V _{IN} = 2.9V to 5V, HRC = Enable, V _{OVSS} = -4V to -0.6V, I _{OVDD-OVSS} = 0mA to 150mA	--	5	10	mV
		V _{IN} = 2.9V to 5V, HRC = Disable, V _{OVSS} = -4.2V to -0.6V, I _{OVDD-OVSS} = 0mA to 60mA	--	5	10	
Load Regulation	V _{LOAD_REG_OVSS}	V _{IN} = 2.9V to 5V, HRC = Enable, V _{OVSS} = -4V to -0.6V, I _{OVDD-OVSS} = 0mA to 150mA	--	5	10	mV
		V _{IN} = 2.9V to 5V, HRC = Disable, V _{OVSS} = -4.2V to -0.6V, I _{OVDD-OVSS} = 0mA to 60mA	--	5	10	
Output Voltage Ripple	V _{OUT_RIPPLE_SYM_OVSS}	V _{IN} = 3.7V, SET = L, V _{AVDD} = 3.3V, I _{AVDD} ≤ 10mA, V _{OVDD} = 3.3V, I _{OVDD} ≤ 30mA, V _{OVSS} = -3.3V, I _{OVSS} ≤ 30mA	--	--	Δ10	mV
	V _{OUT_RIPPLE_ASYM_OVSS}	V _{IN} = 3.7V, SET = H, V _{AVDD} = 3.3V, I _{AVDD} ≤ 10mA, V _{OVDD} = 4.6V, I _{OVDD} ≤ 30mA, V _{OVSS} = -2.2V, I _{OVSS} ≤ 30mA	--	--	Δ10	
	V _{OUT_RIPPLE_HB_OVSS}	V _{IN} = 3.7V, SET = L, HRC = Enable, V _{AVDD} = 3.3V, I _{AVDD} ≤ 10mA, V _{OVDD} = 3.3V, I _{OVDD} ≤ 150mA, V _{OVSS} = -4V, I _{OVSS} ≤ 150mA	--	--	Δ10	
Line Transient Response	V _{LINE_TR_SYM_OVSS}	V _{IN} = 2.9V to 5V, ΔV _{IN} = 500mV, t _r = t _f = 10μs, SET = L, V _{AVDD} = 3.3V, I _{AVDD} = 10mA, V _{OVDD} = 3.3V, I _{OVDD} = 30mA, V _{OVSS} = -3.3V, I _{OVSS} = 30mA	-5	--	5	mV
	V _{LINE_TR_ASYM_OVSS}	V _{IN} = 2.9V to 5V, ΔV _{IN} = 500mV, t _r = t _f = 10μs, SET = H, V _{AVDD} = 3.3V, I _{AVDD} = 10mA, V _{OVDD} = 4.6V, I _{OVDD} = 30mA, V _{OVSS} = -2.2V, I _{OVSS} = 30mA	-5	--	5	
	V _{LINE_TR_HB_OVSS}	V _{IN} = 2.9V to 5V, ΔV _{IN} = 500mV, t _r = t _f = 10μs, SET = L, HRC = Enable, V _{AVDD} = 3.3V, I _{AVDD} = 10mA, V _{OVDD} = 3.3V, I _{OVDD} = 150mA, V _{OVSS} = -4V, I _{OVSS} = 150mA	-10	--	10	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Load Transient Response	VLOAD_TR_SYM_OVSS	V _{IN} = 3.7V, SET = L, V _{AVDD} = 3.3V, V _{OVDD} = 3.3V, V _{OVSS} = -3.3V, I _{AVDD} = 10mA, I _{OVDD-OVSS} = 0 ↔ 50mA, t _R = t _F = 10ms	-10	--	10	mV
	VLOAD_TR_ASYM_OVSS	V _{IN} = 3.7V, SET = H, V _{AVDD} = 3.3V, V _{OVDD} = 4.6V, V _{OVSS} = -2.2V, I _{AVDD} = 10mA, I _{OVDD-OVSS} = 0 ↔ 50mA, t _R = t _F = 10ms	-10	--	10	
	VLOAD_TR_HB_OVSS	V _{IN} = 3.7V, SET = L, HRC = Enable, V _{AVDD} = 3.3V, V _{OVDD} = 3.3V, V _{OVSS} = -4V, I _{AVDD} = 10mA, I _{OVDD-OVSS} = 0 ↔ 150mA, t _R = t _F = 10ms	-10	--	10	
Current Limit	I _{LIM_OVSS}	V _{IN} = 2.9V to 5V, V _{OVSS} = -4.2V to -0.6V	--	250	--	mA
Short Circuit Protection Threshold	V _{SCP_OVSS}	V _{IN} = 2.9V to 5V, V _{OVSS} = -4.2V to -0.6V	65	80	85	%
Short Circuit Protection Delay Time	t _{DLY_SCP_OVSS}	V _{IN} = 2.9V to 5V, V _{OVSS} = -4.2V to -0.6V	0.85	1	1.15	ms
Power-Off Discharge Time	t _{DISCHG_OVSS}	V _{IN} = 2.9V to 5V, V _{OVSS} = -4.2V to -0.6V, SWIRE = L	--	--	3	ms

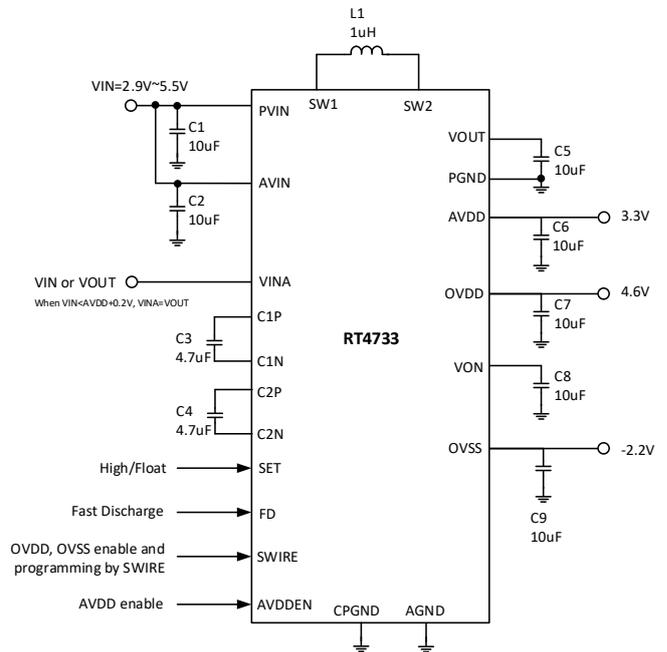
Note 6. Spec. is guaranteed by design.

13 Typical Application Circuit

Symmetry Mode:



Asymmetry Mode:



Note: C4 is only used when VON:-0.5x.
Without head room control (HRC)

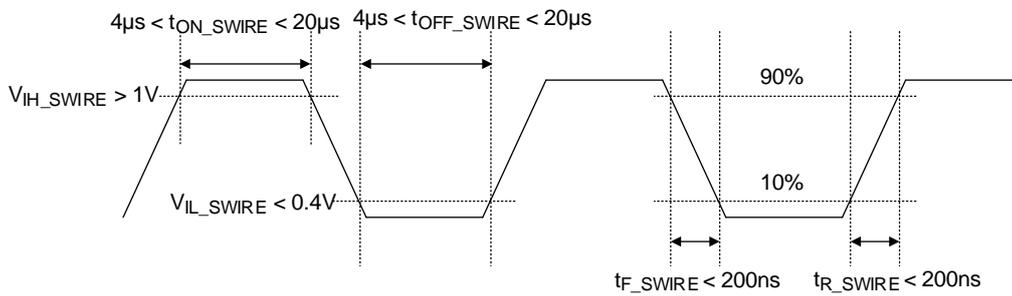
Table 1. Component List of Evaluation Board

Reference	Qty	Part Number	Description	Package	Manufacturer
C1, C2, C5, C6, C7, C8, C9	7	GRM155R61A106ME11 (Note 7)	10μF/10V/X5R	1.0x0.5x0.5mm	muRata
C3, C4	2	GRM155R61A475MEAA (Note 7)	4.7μF/10V/X5R	1.0x0.5x0.5mm	muRata
L1	1	HTTP14120F-1R0MSR	1μH	1.4x1.2x0.6mm	Cyntec

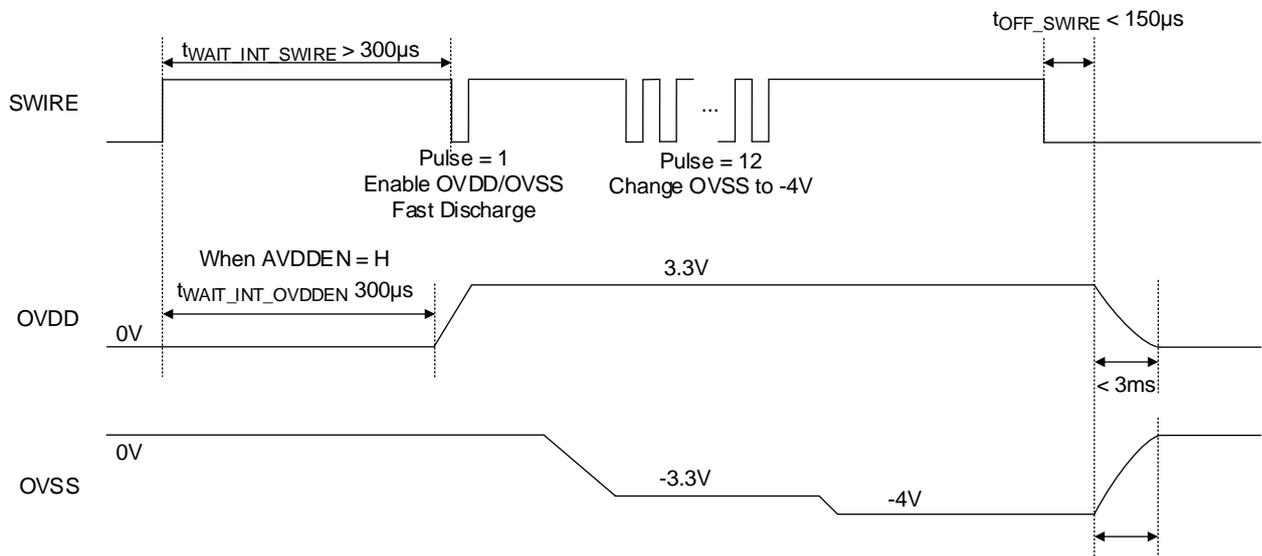
Note 7. If a steady-state temperature-humidity bias life test (85°C/85%RH) is required, it is recommended to use AEC-Q200 qualified capacitors or apply coatings to external components.

14 Timing Diagram

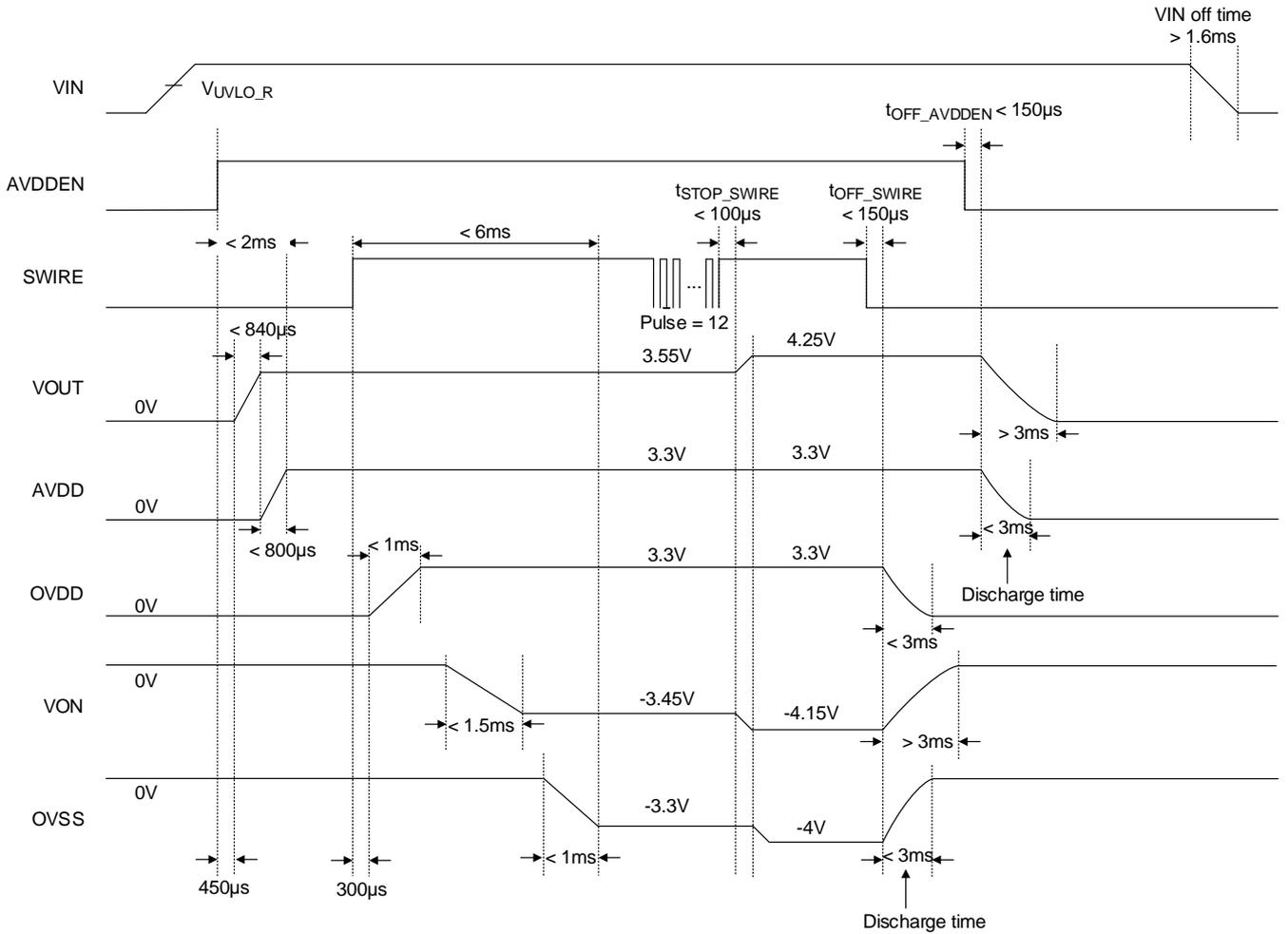
14.1 SWIRE Interface 1



14.2 SWIRE Interface 2



14.3 Power-On/Off Sequence: AVDDEN = On → SWIRE = On → SWIRE = Off → AVDDEN = Off



14.4 Reset by AVDDEN and SWIRE

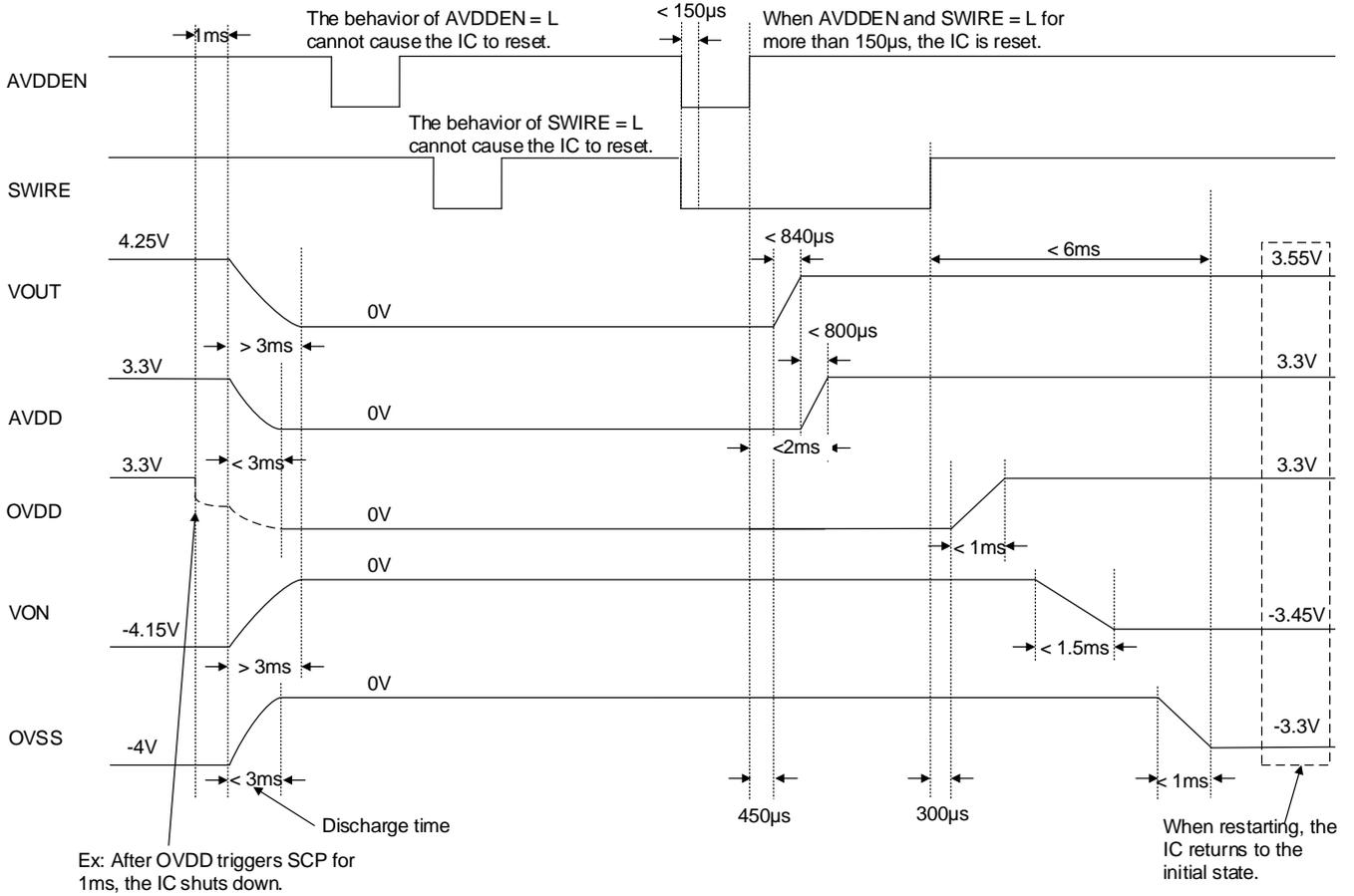


Table 2. Reset Mechanism Table

Protection	Reset to Default
OVDD, OVSS Voltage	SWIRE & AVDDEN both keep low > 150µs
AVDD Voltage	SWIRE & AVDDEN both keep low > 150µs
FD Setting	SWIRE & AVDDEN both keep low > 20ms
SCP_OVDD, OVSS Latch	SWIRE & AVDDEN both keep low > 150µs
SCP3_AVDD Latch	SWIRE & AVDDEN both keep low > 150µs

14.5 Fast Discharge 2: AVDDEN = SWIRE = L > 20ms

14.5.1 Enable Fast Discharge Function by SWRIE = 1 & 3 or FD Pin = H

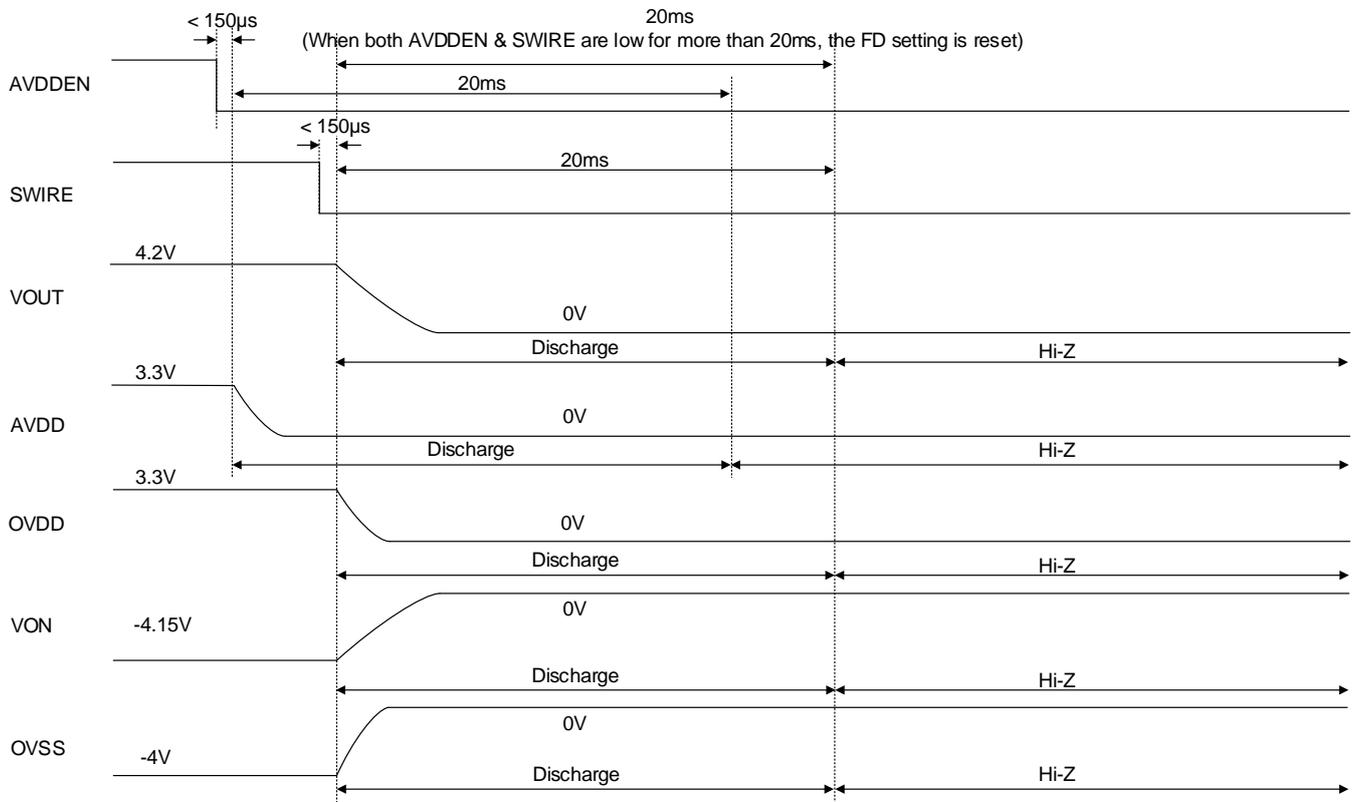


Table 3. Discharge Table for FD Pin = 1

FD pin = 1						
AVDD_EN	SWIRE	AVDD	OVDD	OVSS	VOUT	VON
0	0	FD with 20ms				
0	1	FD with 20ms	--	--	--	--
1	0	--	FD with 20ms	FD with 20ms	--	FD with 20ms
1	1	--	--	--	--	--

Table 4. Discharge Table for FD Pin = 0

FD pin = 0						
AVDD_EN	SWIRE	AVDD	OVDD	OVSS	VOUT	VON
0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	Hi-Z	--	--	--	--
1	0	--	Hi-Z	Hi-Z	--	Hi-Z
1	1	--	--	--	--	--

Table 5. Protection Table

Channel	Protection Name	Function Enable (Note 8)	Latch (O)	Criteria	Behavior	Recovery
			Non Latch (Δ)			
IC	UVLO	VIN > POR (1.6V, typical)	Δ	VIN < VIN_UVLO_F (2.2V, typical)	IC shuts down	VIN > VIN_UVLO_R (2.35V, typical)
	OTP	UVLO & AVDDEN = H or UVLO & SWIRE = H	Δ	IC junction temperature > 140°C (typical)	IC shuts down	Temperature < 125°C (typical)
VOUT Buck-Boost	OCP	UVLO & AVDDEN = H or UVLO & SWIRE = H	Δ	I _{SW12} > 1.75A (typical)	Normal operation: Cycle-by-cycle current limit	Peak value of I _{sw} < OCP
	SCP_80	After soft-start completes	O	VOUT < 80%	Count 1ms then all channels shut down	Condition 1. VIN < VIN_UVLO_F Condition 2. Reset Mechanism
AVDD LDO	OCP	UVLO & AVDDEN = H	Δ	I _{AVDD} > 75mA (typical) soft-start period I _{AVDD} > 150mA (typical) after soft-start completes	Normal operation: Current limit	I _{AVDD} < Current Limit
	SCP_80	After soft-start completes	O	AVDD < 80%	Count 1ms then all channels shut down	Condition 1. VIN < VIN_UVLO_F Condition 2. Reset Mechanism
OVDD LDO	OCP	UVLO & SWIRE = H	Δ	I _{OVDD} > 125mA (typical) soft-start period I _{OVDD} > 250mA (typical) after soft-start completes	Normal operation: Current limit	I _{OVDD} < Current Limit
	SCP_80	After soft-start completes	O	OVDD < 80%	Count 1ms then all channels shut down	Condition 1. VIN < VIN_UVLO_F Condition 2. Reset Mechanism
OVSS LDO	OCP	UVLO & SWIRE = H	Δ	I _{OVSS} > 125mA (typical) soft-start period I _{OVSS} > 250mA (typical) after soft-start completes	Normal operation: Current limit	I _{OVSS} < Current Limit
	SCP_80	After soft-start completes	O	OVSS < 80%	Count 1ms then all channels shut down	Condition 1. VIN < VIN_UVLO_F Condition 2. Reset Mechanism

Note 8. Function Disable: VIN < UVLO_F and AVDDEN = L or VIN < UVLO_F and SWIRE = L

Table 6. Selection Table with SWIRE Pulse

Pulse	Function Description
0	OVDD = 3.3V, OVSS = -3.3V, AVDD = 3.3V(SET = L). OVDD = 4.6V, OVSS = -2.2V, AVDD = 3.3V(SET = H).
1	Fast discharge function on (for OVDD, VON, and OVSS).
2	Fast discharge function off (for OVDD, VON, and OVSS).
3	Fast discharge function on (for AVDD).
4	Fast discharge function off (for AVDD).
5	Force fast discharge on (AVDDEN = SWIRE = L).
6	OVDD = 2.8V, OVSS = -2.8V, AVDD = 2.8V.
7	Enable bypass detection of buck-boost (default).
8	Disable bypass mode, then into switching mode.
9	Reserved.
10~46	SET = L, the OVSS voltage range is -4.2V to -0.6V. SET = H or floating, the OVSS voltage range is -2.4V to -0.6V.
50~55	AVDD setting, 2.8V to 3.3V.
60~78	OVDD setting, 2.8V to 4.6V.
80	OVSS DAC code step time is 25μs (default).
81	OVSS DAC code step time is 200μs.
82	Enable HRC (default).
83	Disable HRC.
84	OVDD turn on (SWIRE = H).
85	VON/OVSS turn on (SWIRE = H).
86	OVDD turn off.
87	VON/OVSS turn off.
88	Exit AOD without soft-start.
89	Reserved.
90	VON: Reference voltage changes at load: 60mA (default).
91	VON: Reference voltage changes at load: 30mA (Note 9).
92	VON-OVSS head room = 0.2V.
93	VON-OVSS head room = 0.15V (default).
94	Force buck-boost always in bypass mode.
95	VON: The minimum frequency is 25kHz.
96	VON: The minimum frequency is 75kHz.
97	VON: The minimum frequency is 150kHz (default) (Note 9).

Note 9. When SET = L, $OVDD - |OVSS| \geq 0.1V$ or $AVDD - |OVSS| \geq 0.1V$. It requires the use of pulse 91 and pulse 97.

Table 7. VOUT Setting with SWIRE Pulse (SET = L)

Pulse	V (OVSS)	Pulse	V (OVSS)	Pulse	V (AVDD)	Pulse	V (OVDD)
10	-4.2	30	-2.2	50	3.3	60	4.6
11	-4.1	31	-2.1	51	3.2	61	4.5
12	-4.0	32	-2.0	52	3.1	62	4.4
13	-3.9	33	-1.9	53	3.0	63	4.3
14	-3.8	34	-1.8	54	2.9	64	4.2
15	-3.7	35	-1.7	55	2.8	65	4.1
16	-3.6	36	-1.6	56	Reserved	66	4.0
17	-3.5	37	-1.5	57	Reserved	67	3.9
18	-3.4	38	-1.4	58	Reserved	68	3.8
19	-3.3	39	-1.3	59	Reserved	69	3.7
20	-3.2	40	-1.2			70	3.6
21	-3.1	41	-1.1			71	3.5
22	-3.0	42	-1.0			72	3.4
23	-2.9	43	-0.9			73	3.3
24	-2.8	44	-0.8			74	3.2
25	-2.7	45	-0.7			75	3.1
26	-2.6	46	-0.6			76	3.0
27	-2.5	47	Reserved			77	2.9
28	-2.4	48	Reserved			78	2.8
29	-2.3	49	Reserved			79	Reserved

Table 8. VOUT Setting with SWIRE Pulse (SET = H)

Pulse	V (OVSS)	Pulse	V (OVSS)	Pulse	V (AVDD)	Pulse	V (OVDD)
10	-2.4	30	-2.2	50	3.3	60	4.6
11	-2.4	31	-2.1	51	3.2	61	4.5
12	-2.4	32	-2.0	52	3.1	62	4.4
13	-2.4	33	-1.9	53	3.0	63	4.3
14	-2.4	34	-1.8	54	2.9	64	4.2
15	-2.4	35	-1.7	55	2.8	65	4.1
16	-2.4	36	-1.6	56	Reserved	66	4.0
17	-2.4	37	-1.5	57	Reserved	67	3.9
18	-2.4	38	-1.4	58	Reserved	68	3.8
19	-2.4	39	-1.3	59	Reserved	69	3.7
20	-2.4	40	-1.2			70	3.6
21	-2.4	41	-1.1			71	3.5
22	-2.4	42	-1.0			72	3.4
23	-2.4	43	-0.9			73	3.3
24	-2.4	44	-0.8			74	3.2
25	-2.4	45	-0.7			75	3.1
26	-2.4	46	-0.6			76	3.0
27	-2.4	47	Reserved			77	2.9
28	-2.4	48	Reserved			78	2.8
29	-2.3	49	Reserved			79	Reserved

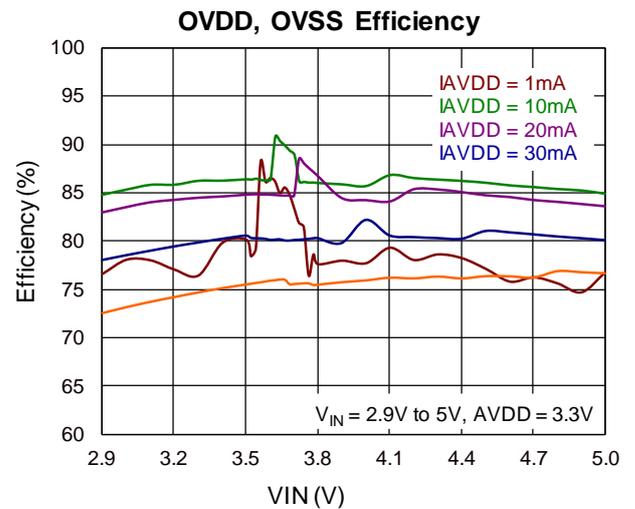
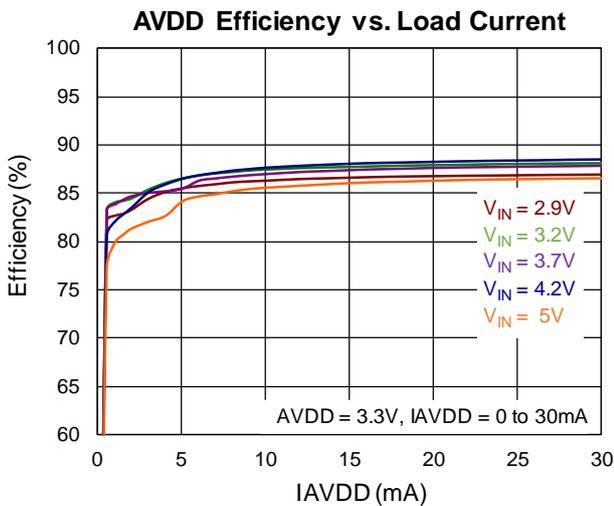
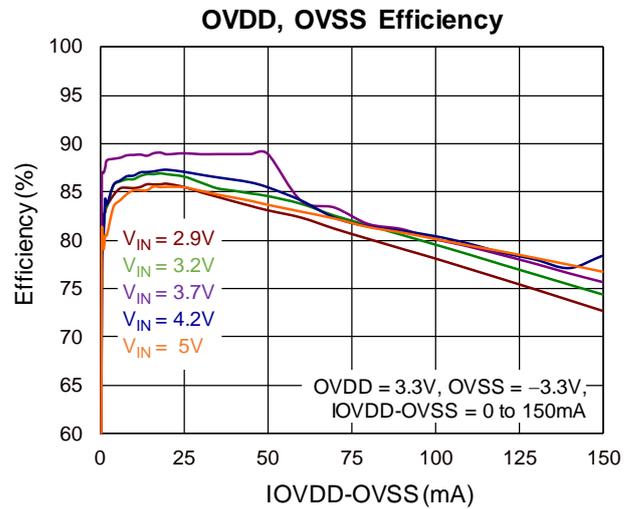
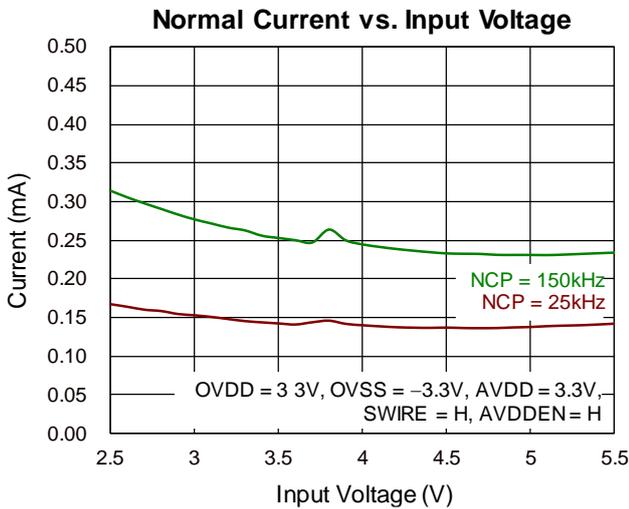
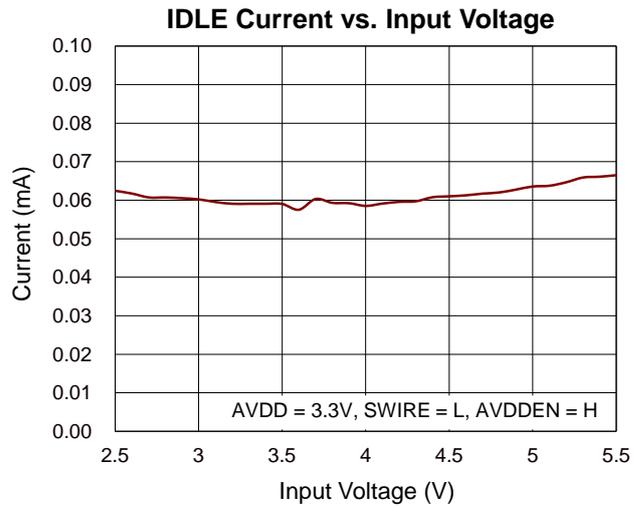
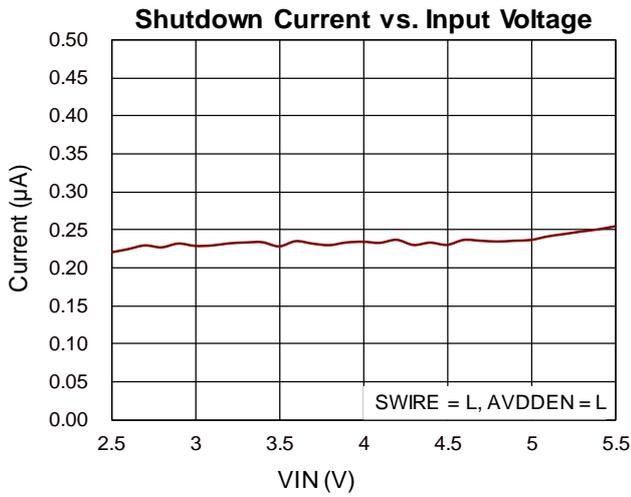
VON: -1x (SET = L)

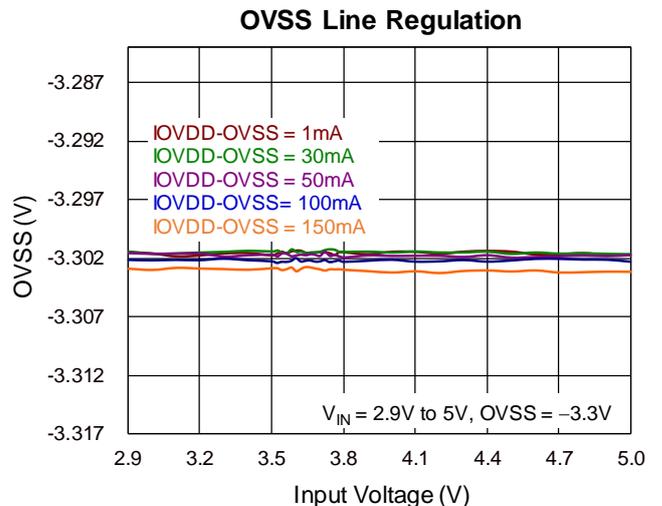
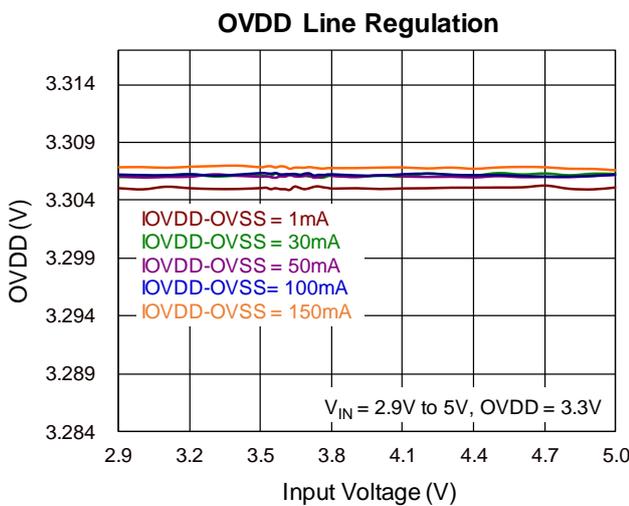
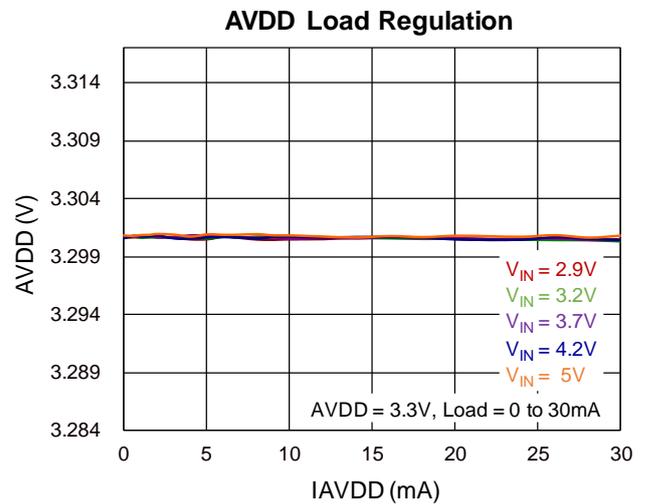
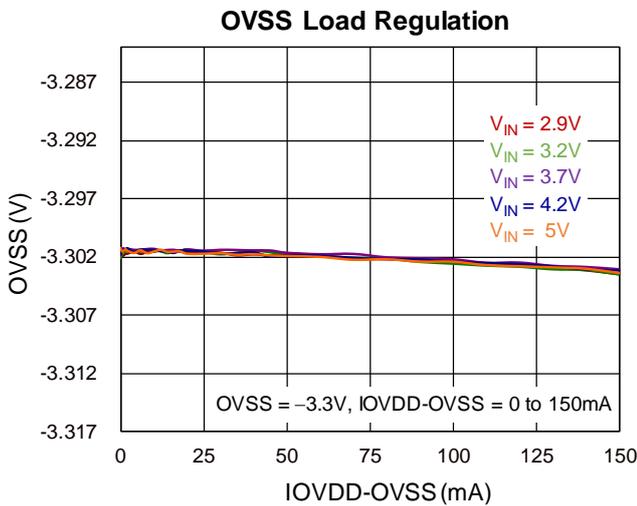
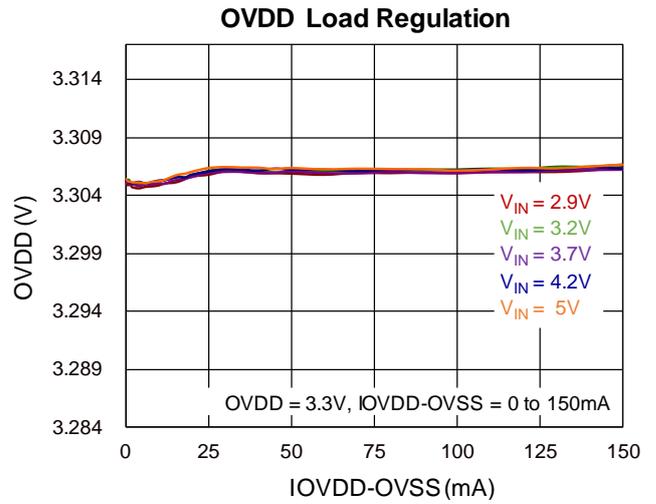
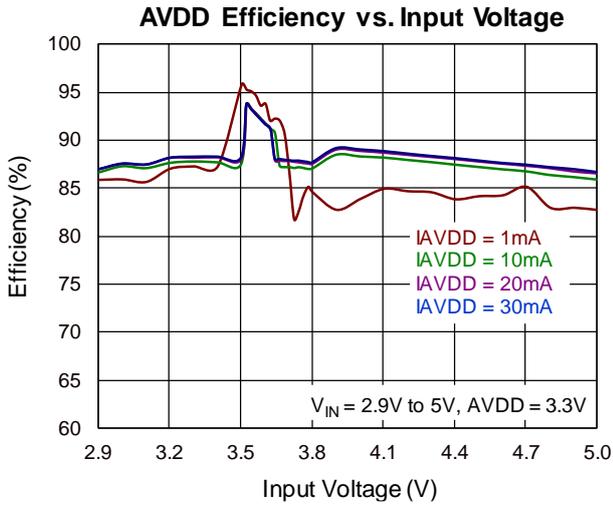
VOUT = Max (AVDD + 0.2V, OVDD + 0.2V, |VON| + 0.1V); VON = |OVSS| + 0.15V (pulse 93) or |OVSS| + 0.2V (pulse 92)

VON: -0.5x (SET = H)

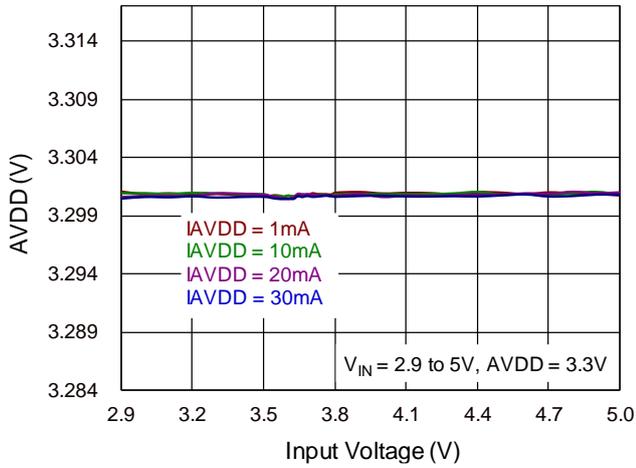
VOUT = Max (AVDD + 0.2V, OVDD + 0.2V, (|VON|+0.1V) x 2); VON = |OVSS| + 0.15V(pulse 93) or |OVSS| + 0.2V (pulse 92)

15 Typical Operating Characteristics

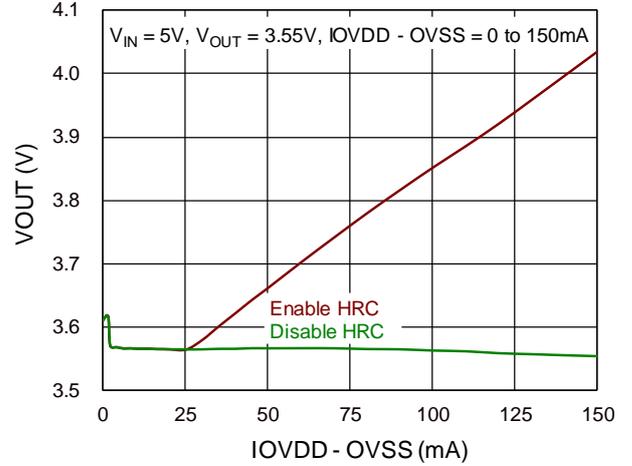




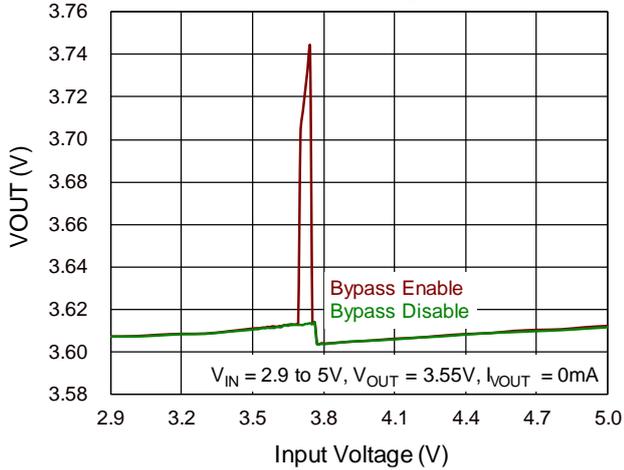
AVDD Line Regulation



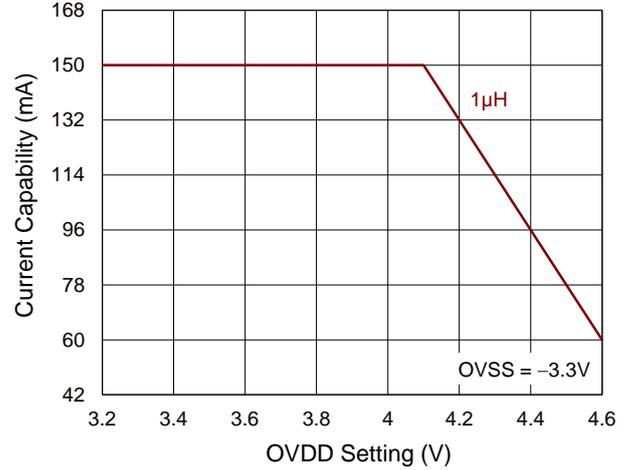
VOUT Load Regulation (Head Room Control)



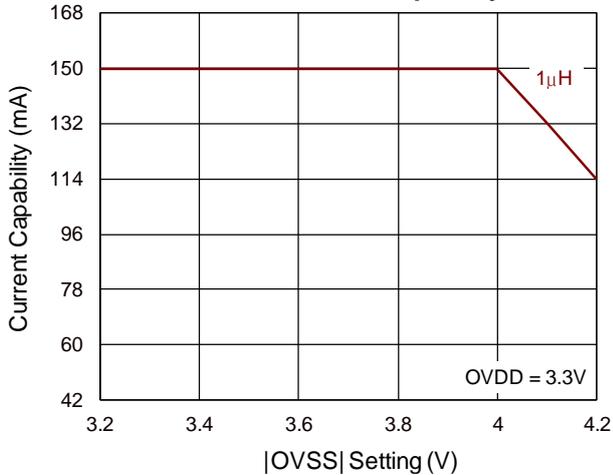
VOUT Line Regulation



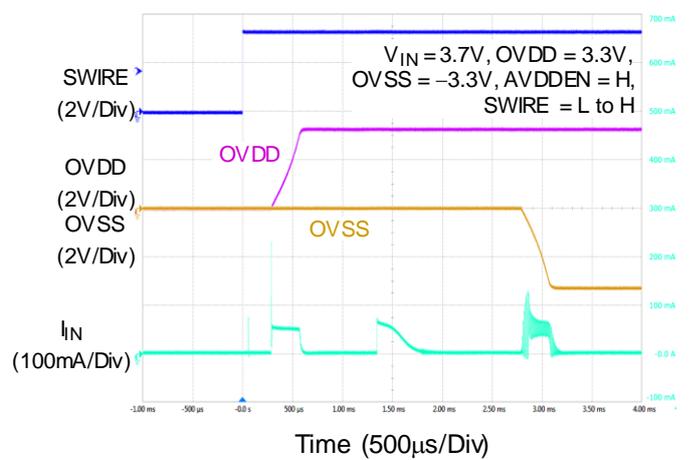
OVDD Current Capability



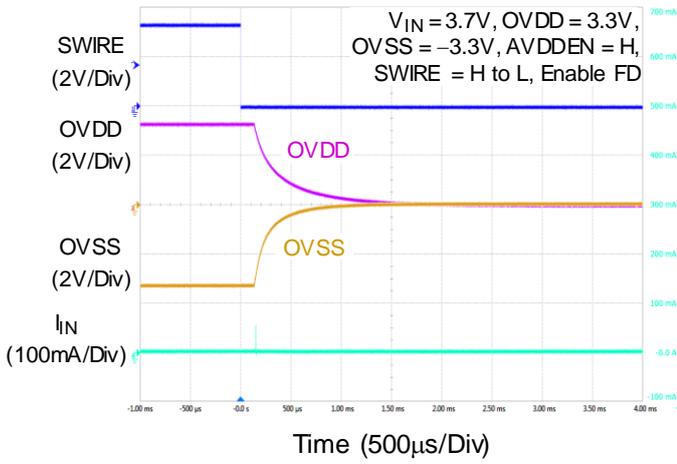
OVSS Current Capability



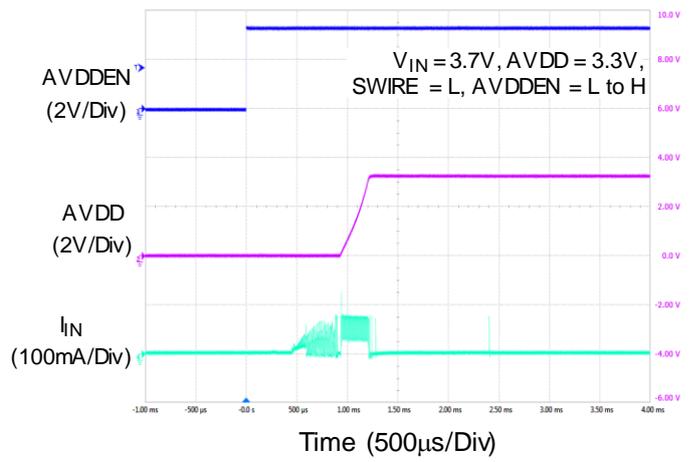
Power On I



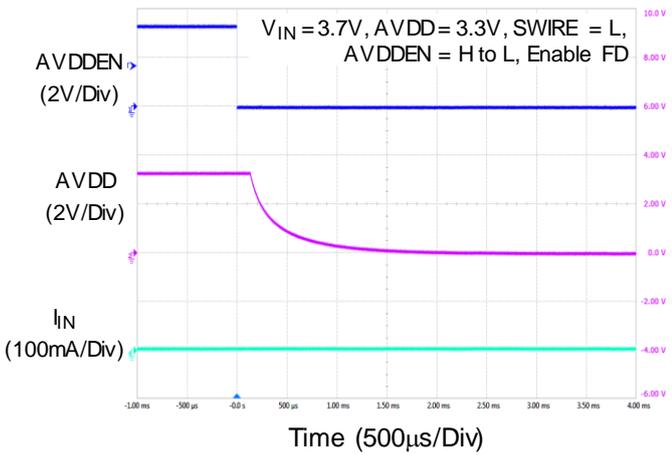
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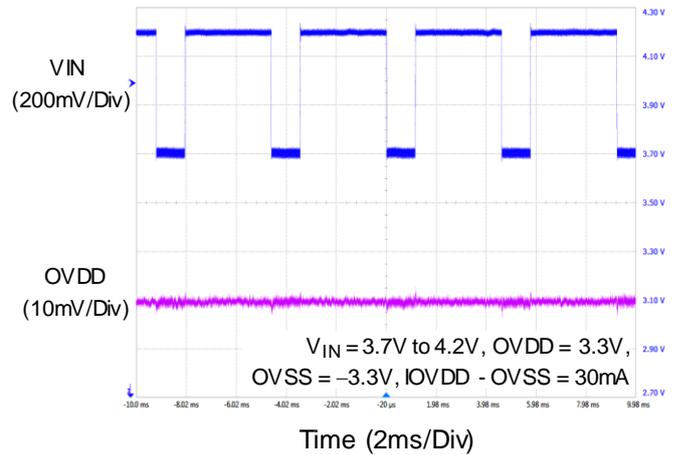
Power On II



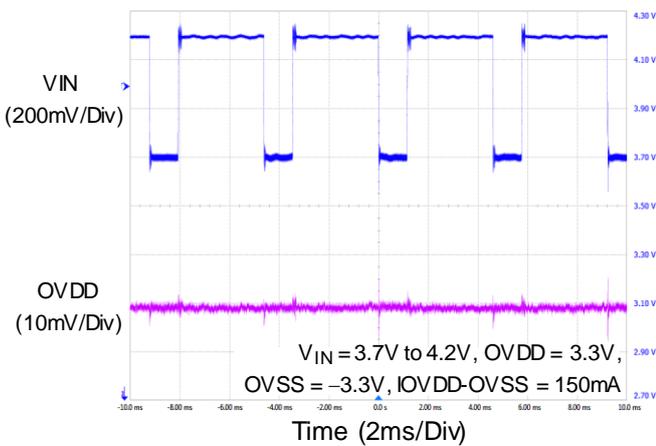
Power Off II



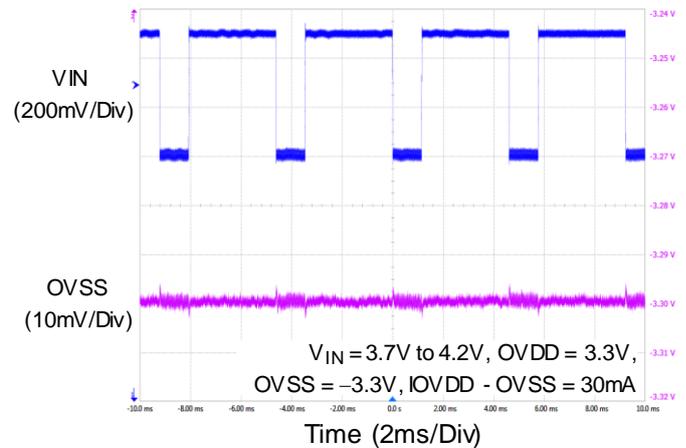
OVDD TDMA

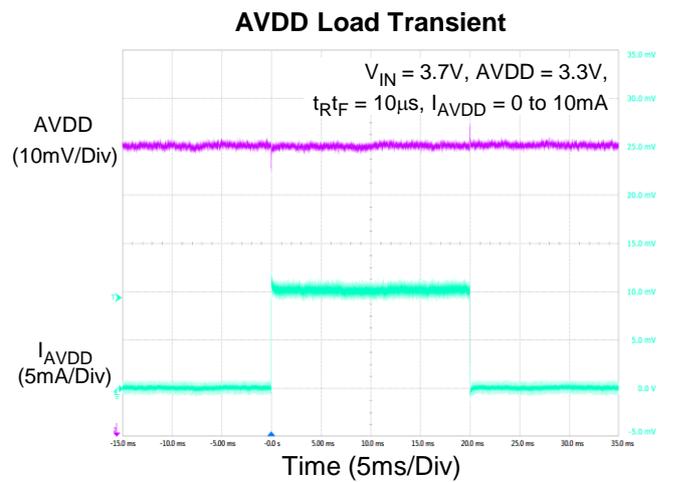
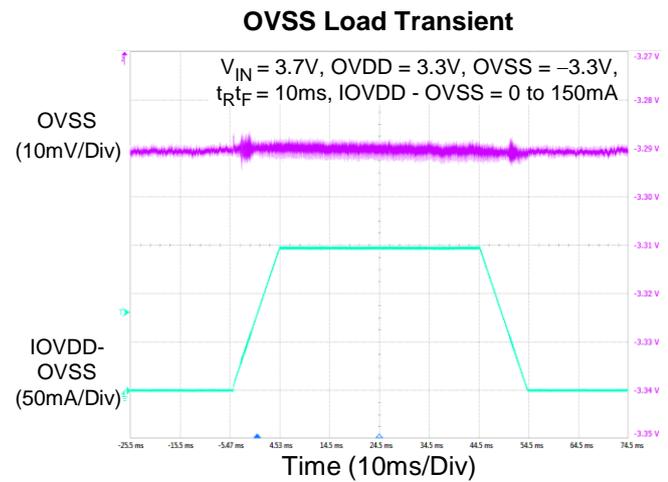
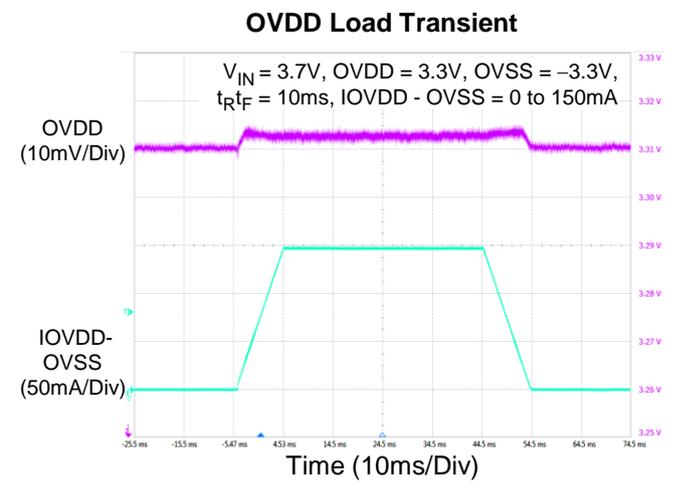
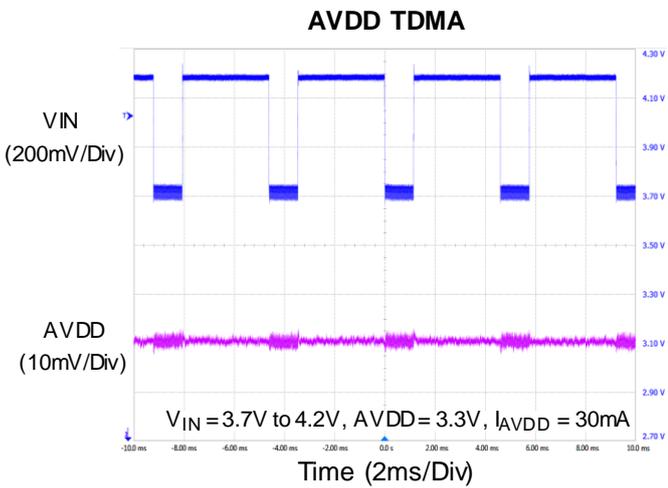
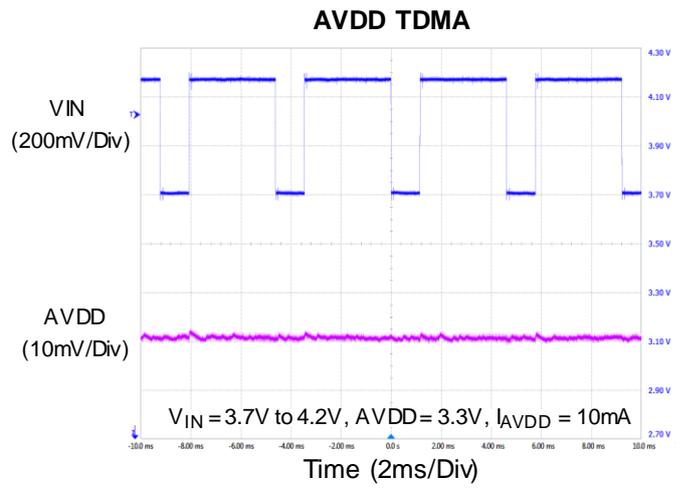
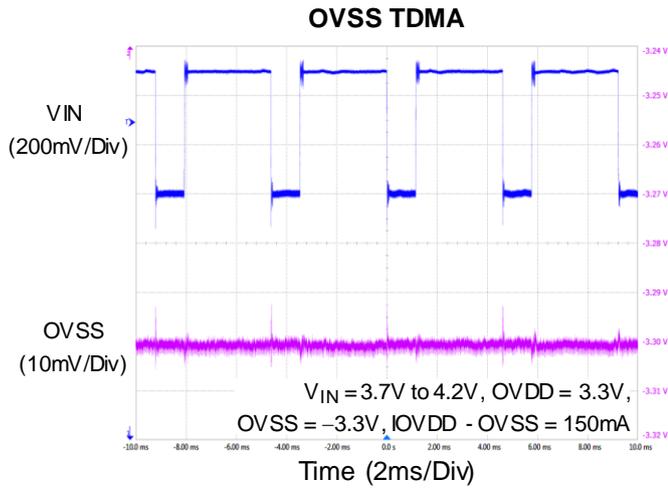


OVDD TDMA



OVSS TDMA





16 Operation

The RT4733 is a highly integrated power solution featuring a buck-boost converter and an inverting charge pump to generate negative output voltage. The output voltages can be adjusted via the SWIRE interface protocol. The OVDD voltage range is from 2.8V to 4.6V, adjustable in 100mV steps. The OVSS voltage ranges from -0.6V to -4.2V, also adjustable in 100mV steps. The AVDD positive output voltage ranges from 2.8V to 3.3V, adjustable in 100mV steps. With an input voltage range of 2.9V to 5.5V, the RT4733 is optimized for products powered by single-cell batteries and can supply symmetrical output currents up to 150mA. The RT4733 provides Over-Temperature Protection (OTP) and Short Circuit Protection (SCP) mechanisms to prevent the device from being damaged during abnormal operations. When the SWIRE and AVDDEN voltages are logic low, the IC will shut down with a low input supply current of less than 1 μ A.

17 Application Information

(Note 10)

The RT4733 is a highly integrated power solution featuring a buck-boost converter and an inverting charge pump to generate both positive and negative output voltages for AMOLED bias. The buck-boost DC-DC converter can operate with a wide input voltage range from 2.9V to 5.5V. The converter feedback loop is internally compensated for both Buck and Boost operations, providing seamless transition between buck and boost modes.

17.1 Undervoltage-Lockout (UVLO)

In addition to the AVDDEN and SWIRE pins, the RT4733 also provides enable control through the VIN pin. If AVDDEN and SWIRE rise above VIH first, switching will still be inhibited until the VIN voltage rises above the UVLO rising threshold (UVLO_R). This ensures that the internal regulator is ready, preventing operation with not-fully-enhanced internal MOSFET switches. If the VIN voltage falls below the UVLO falling threshold (UVLO_F), switching will be inhibited; if the VIN voltage rises above the UVLO rising threshold (UVLO_R), the device will resume switching.

17.2 Soft-Start Function

The RT4733 employs an internal soft-start function to avoid excessive inrush current during startup.

17.3 Fast Discharge Function

The OVDD, OVSS, and AVDD use an embedded discharge function to rapidly discharge the remaining output voltage to 0V, preventing phenomena such as residual images on the display during shutdown.

17.4 Over-Temperature Protection (OTP)

The RT4733 includes an Over-Temperature Protection (OTP) feature to prevent excessive power dissipation and overheating of the device. The OTP will shut down switching operation when the junction temperature exceeds 140°C. Once the junction temperature cools down by approximately 15°C, the converter resumes operation.

To maintain continuous operation, prevent the maximum junction temperature from rising above 125°C.

17.5 Overcurrent Protection (OCP)

The OCP function is implemented by UGATE and LGATE. When the inductor current reaches the UGATE current-limit threshold, the high-side MOSFET will turn off. The low-side MOSFET then turns on to discharge the inductor current until it falls below the LGATE current-limit threshold. After the UGATE current limit is triggered, the maximum inductor current is determined by the inductor current's rising rate and the response delay time of the internal network.

17.6 Short Circuit Protection (SCP)

The RT4733 has an advanced short circuit protection mechanism to prevent damage to the device from unexpected applications. When the output becomes shorted to ground for over 1ms, the device enters shutdown mode. After a reset, the OVDD and OVSS can restart normal operation by triggering the SWIRE pin. The AVDD can only re-start after triggering the AVDDEN pin.

17.7 Input Capacitor Selection

For each channel, input ceramic capacitors with 10 μ F capacitance are suggested. However, to achieve the best performance with the RT4733, larger capacitance values can be used. For better voltage filtering, select ceramic capacitors with low ESR. X5R and X7R types are suitable because of their performance over wider voltage and temperature ranges.

17.8 Inductor Selection

Inductor value selection will affect transient response, ripple, and other performance metrics. The nominal inductance value of the RT4733 is recommended to be 1μH to achieve optimal performance.

The inductor value and operating frequency determine the ripple current based on specific input and output voltages. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{SW} \times L} \right) \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, a reasonable starting point is to set ΔI_L to 30% of I_{MAX}. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f_{SW} \times \Delta I_{L(MAX)}} \right) \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

The inductor's current rating (causing a 40°C temperature rise from a 25°C ambient) should be greater than the maximum load current, and its saturation current should be greater than the short circuit peak current limit.

17.9 Buck-Boost Converter Output Capacitor Selection

The ripple voltage is an important criterion for choosing an output capacitor. This portion consists of two parts. One is the product of the ripple current and the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. The output capacitor is selected according to the output ripple, which is calculated using the equation below.

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{OUT_CAP}$$

$$\Delta V_{ESR} = I_{C_RMS} \times R_{C_ESR}$$

$$\Delta V_{OUT_CAP} = \frac{I_{OUT} \times Duty}{f_{SW} \times C_{MIN}}$$

17.10 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature T_{J(MAX)}, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where T_{J(MAX)} is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-21B 1.31x2.91 (BSC) package, the thermal resistance, θ_{JA}, is 33.4°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (33.4^\circ\text{C/W}) = 2.99\text{W for a WL-CSP-21B 1.31x2.91 (BSC) package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curve in [Figure 1](#) allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

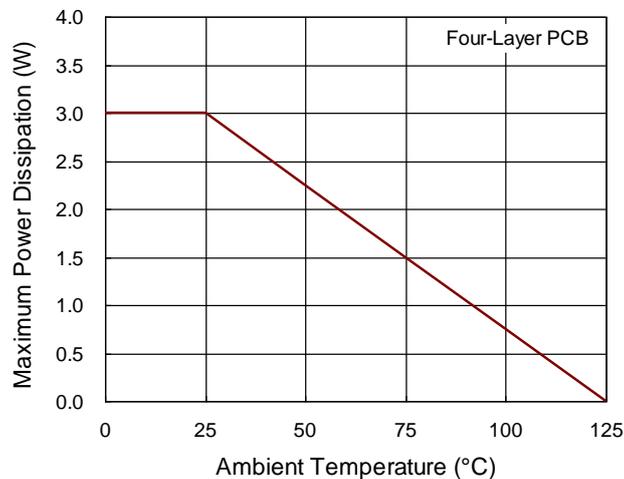


Figure 1. Derating Curve of Maximum Power Dissipation

17.11 Layout Considerations

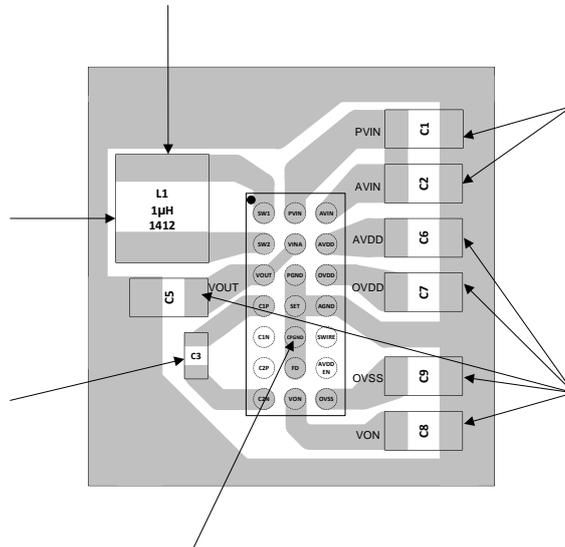
For the best performance of the RT4733, the following PCB layout guidelines should be strictly followed:

- The input bypass capacitor should be placed as close to the IC as possible and connected to the ground plane of the PCB.
- The output bypass capacitor should be placed as close to the IC as possible and connected to the ground plane of the PCB.
- Minimize the size of the SW1 and SW 2 nodes and keep the traces wide and short. Care should be taken to avoid running traces that carry any noise-sensitive signals near SW or high-current traces.
- The inductor should be placed as close to the SW 1 and SW 2 pins to reduce EMI.
- The flying capacitor should be placed as close to the C1P/C2N pin as possible to avoid noise injection.
- Connect AGND, PGND, and CPGND in the top layer.

Minimize the size of the SW1 and SW2 and keep the traces wide and short. Care should be taken to avoid running traces that carry any noise-sensitive signals near SW1 and SW2.

The inductor should be placed as close to SW1 and SW2 pin for reducing EMI.

The flying capacitor should be placed as close to C1P/C2N pin as possible to avoid noise injection.



The input bypass capacitor should be placed as close the IC as possible and connected to the ground plane of the PCB.

The output bypass capacitor should be placed as close the IC as possible and connected to the ground plane of the PCB.

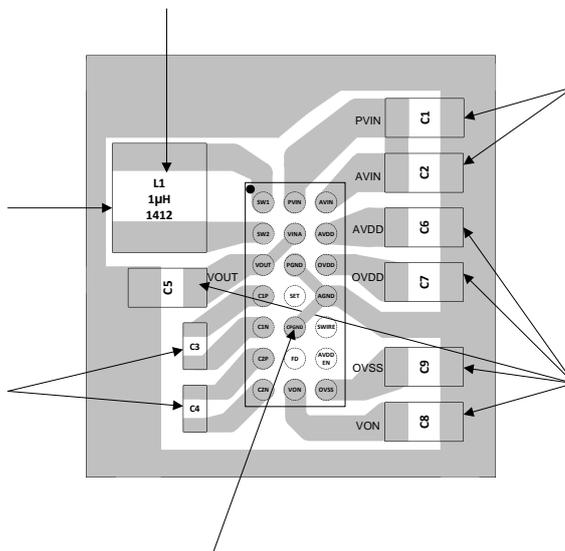
Connect AGND, PGND, and CPGND in the top layer.

Figure 2. PCB Layout Guide-VON: -1x

Minimize the size of the SW1 and SW2 and keep the traces wide and short. Care should be taken to avoid running traces that carry any noise-sensitive signals near SW1 and SW2.

The inductor should be placed as close to SW1 and SW2 pin for reducing EMI.

The flying capacitor should be placed as close to C1P/C1N,C2P/C2N pin as possible to avoid noise injection.



The input bypass capacitor should be placed as close the IC as possible and connected to the ground plane of the PCB.

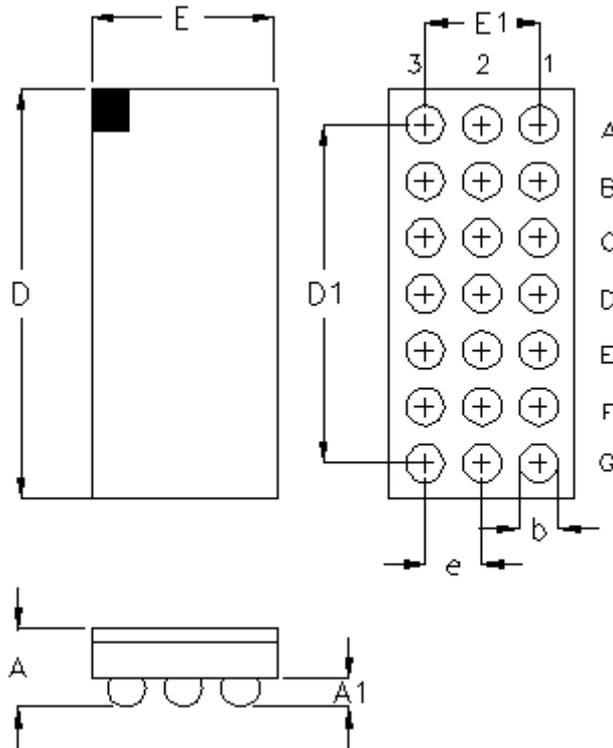
The output bypass capacitor should be placed as close the IC as possible and connected to the ground plane of the PCB.

Connect AGND, PGND, and CPGND in the top layer.

Figure 3. PCB Layout Guide-VON: -0.5x

Note 10. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek’s product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

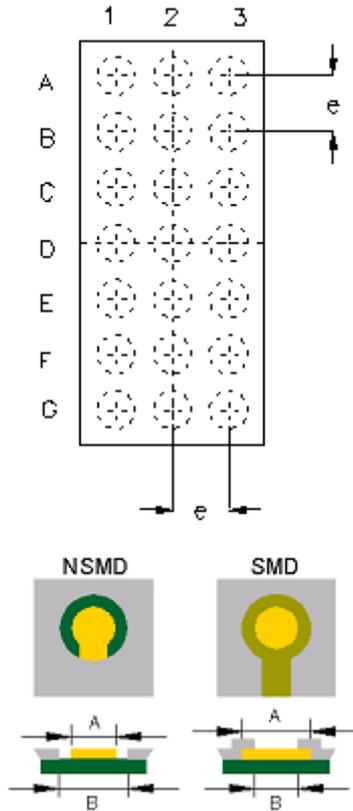
18 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.870	2.950	0.113	0.116
D1	2.400		0.094	
E	1.270	1.350	0.050	0.053
E1	0.800		0.031	
e	0.400		0.016	

21B WL-CSP 1.31x2.91 Package (BSC)

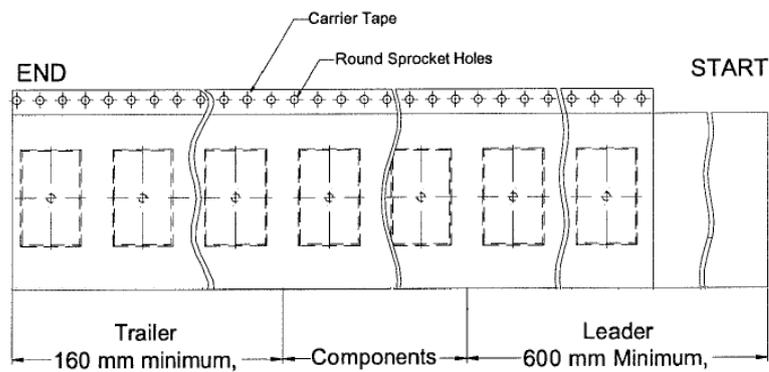
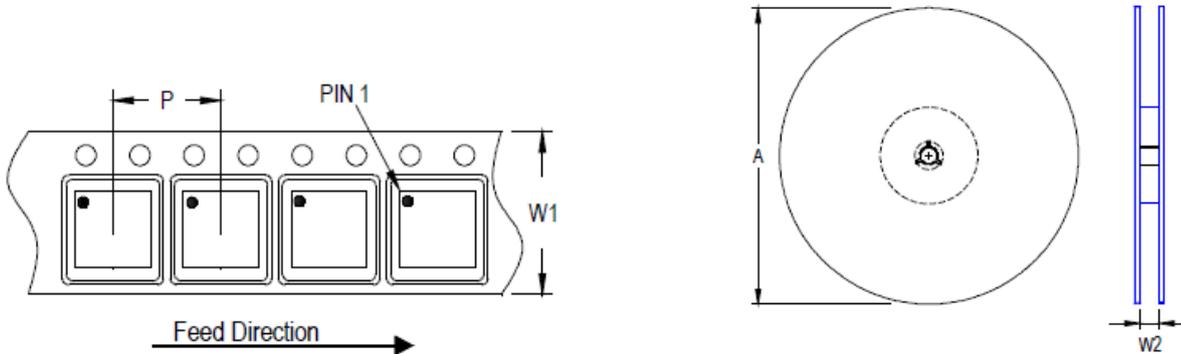
19 Footprint Information



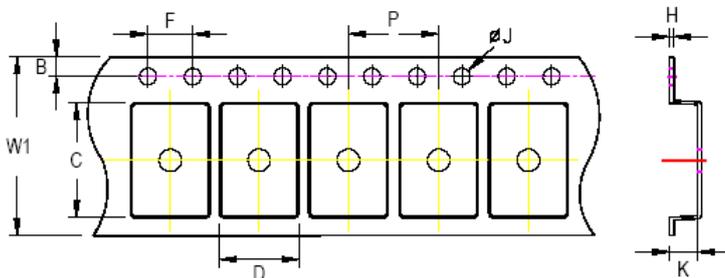
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.31x2.91-21(BSC)	21	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

20 Packing Information

20.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
WL-CSP 1.31x2.91	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size.
The clearance between the components and the cavity is as follows:
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.65mm	0.85mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 <p>Reel 7"</p>	4	 <p>12 inner boxes per outer box</p>
2	 <p>Packing by Anti-Static Bag</p>	5	 <p>Outer box Carton A</p>
3	 <p>3 reels per inner box Box A</p>	6	

Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 1.31x2.91	7"	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}					

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21 Datasheet Revision History

Version	Date	Description	Item
01	2023/12/1	Modify	Features on P1 Simplified Application Circuit on P1 Electrical Characteristics on P4, P5, P6, P9, P11 Time Diagram on P14, P15, P16, P17, P18, P20 Application Information on P26, P28, P29
02	2023/9/27	Modify	Features on P1 Ordering Information on P2 Electrical Characteristics on P5, P6 Typical Application Circuit on P12 Time Diagram on P13, P14, P15, P16, P18 Application Information on P26, P27, P28
03	2024/12/18	Modify	<i>Changed the names of pin A1 to SW1 and pin A2 to SW2.</i> <i>General Description on page 1</i> - Added temperature description <i>Ordering Information on page 2</i> - Updated ordering information and added note <i>Application Information on page 33</i> - Updated declaration <i>Packing Information on page 36, 37</i> - Updated packing information