# Power Management Unit Total Power Solution for SSD

## General Description

The RT5091D is a total power management solution for SSDs (Solid State Drive) with dedicated input supply voltages of 3.3V or 5V. The RT5091D incorporates three high-efficiency synchronous buck regulators and one LDO that deliver several output voltages from a single power source. This provides flexibility to support applications of different VIDs with a regulated power-on sequence.

The RT5091D can provide configurable output voltages to supply ASIC core, DDR, Flash I/O, and PHY. With a dedicated $I^2C$ interface, it supports dynamic voltage scaling (DVS), and PS3.5/PS4 power states for minimized standby power consumption.

## Ordering Information

RT5091D □□

- Package Type
  QW : WQFN-32L 4x4 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

## Applications

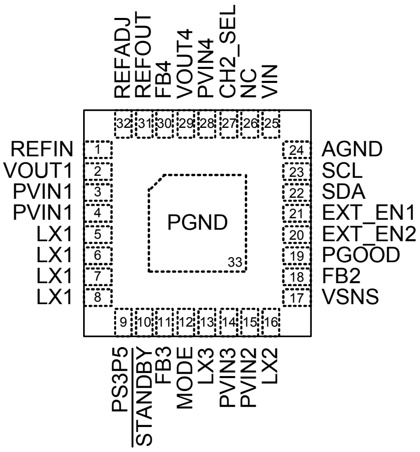
- Solid State Drives

## Features

- **Input Supply Voltage Range : 2.8V to 5.5V**
- **Three High-Efficiency Configurable Low-Voltage Buck Converters at Default Switching Frequency of 2MHz**
  - **CH1 for ASIC Core Power :**
    **Fixed and Adjustable Output by REFIN, Adaptive Voltage 0.7V to 1.3V in 10mV Step by $I^2C$. 4A Max.**
  - **CH2 for DRAM or NAND Core Power :**
    **Buck Mode : Fixed and Adjustable Output by FB2. 2A Max.**
    **Bypass Mode : Load Switch and Soft-Start Control, 4A Max.**
  - **CH3 for Flash I/O Power :**
    **Fixed and Adjustable Output by FB3. 2A Max.**
- **One LDO of Low Quiescent Current**
  - **LDO for Analog and PHY Power :**
    **Fixed and Adjustable Output by FB4. 300mA Max.**
- **Internal Soft-Start and Current Limit Protection for CH1 to CH3 and LDO**
- **$\overline{\text{STANDBY}}$ and PS3P5 Pins for PS3.5 and PS4 Power States Control**
- **Two Output Pins to Control External Regulators/ Switches**
- **One Input Pin to Sense External Regulators/ Switches Output Voltage**
- **High-Speed Mode $I^2C$ Interface for CH1 Output Voltage Programming**
- **PGOOD Indicator for Output Voltages and System Input Brownout Monitor**
- **Power Sequence Control During Start-up**
- **Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), Under-Voltage Lockout (UVLO), and Thermal Shutdown Protection**
- **Small 32-Lead WQFN Package**

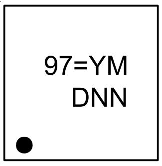
## Pin Configuration

(TOP VIEW)




WQFN-32L 4x4

## Marking Information

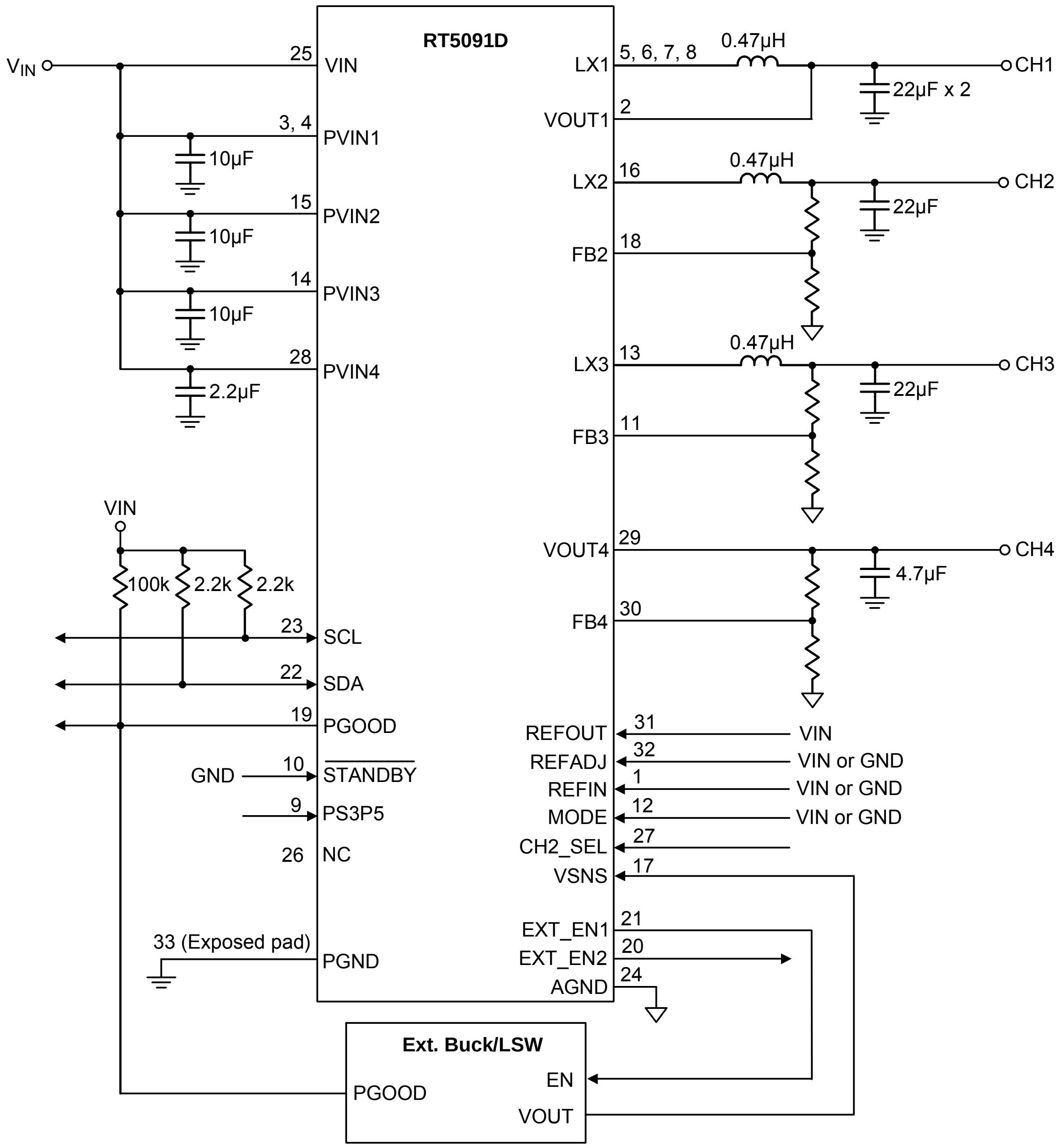



97= : Product Code

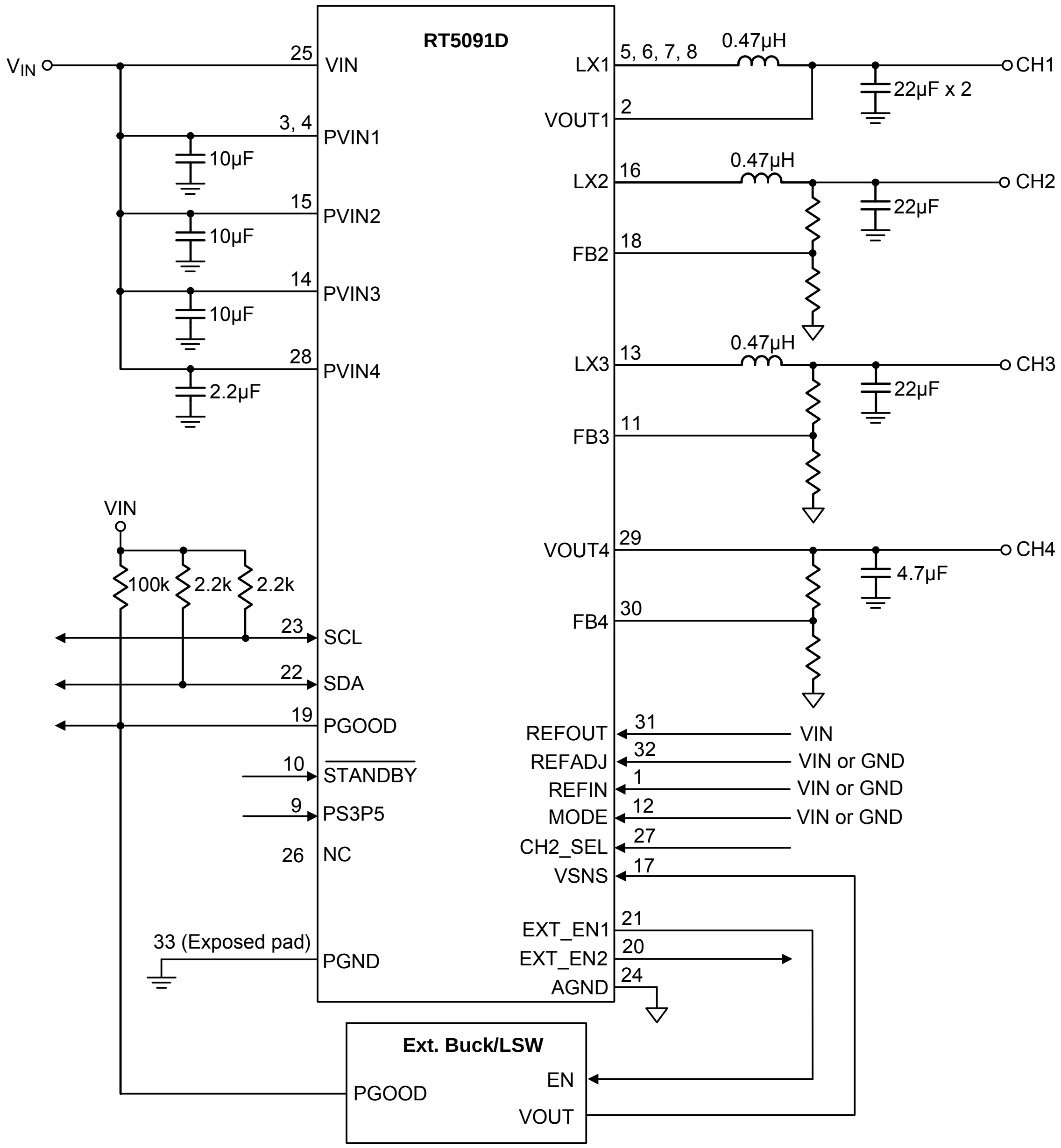
YMDNN : Date Code

## Typical Application Circuit

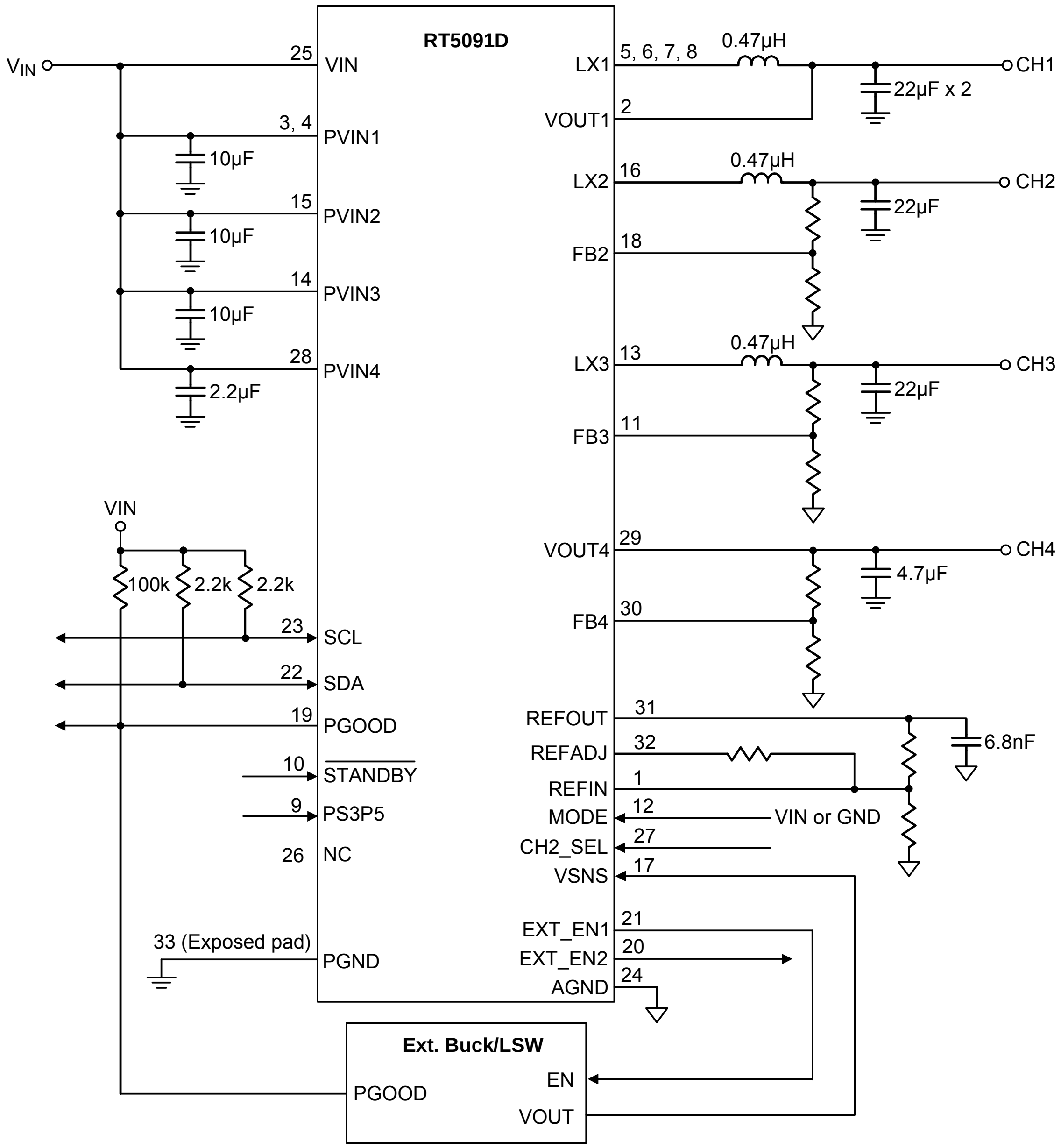
### Power States Operation by I²C & CH1 VOUT DVID by I²C



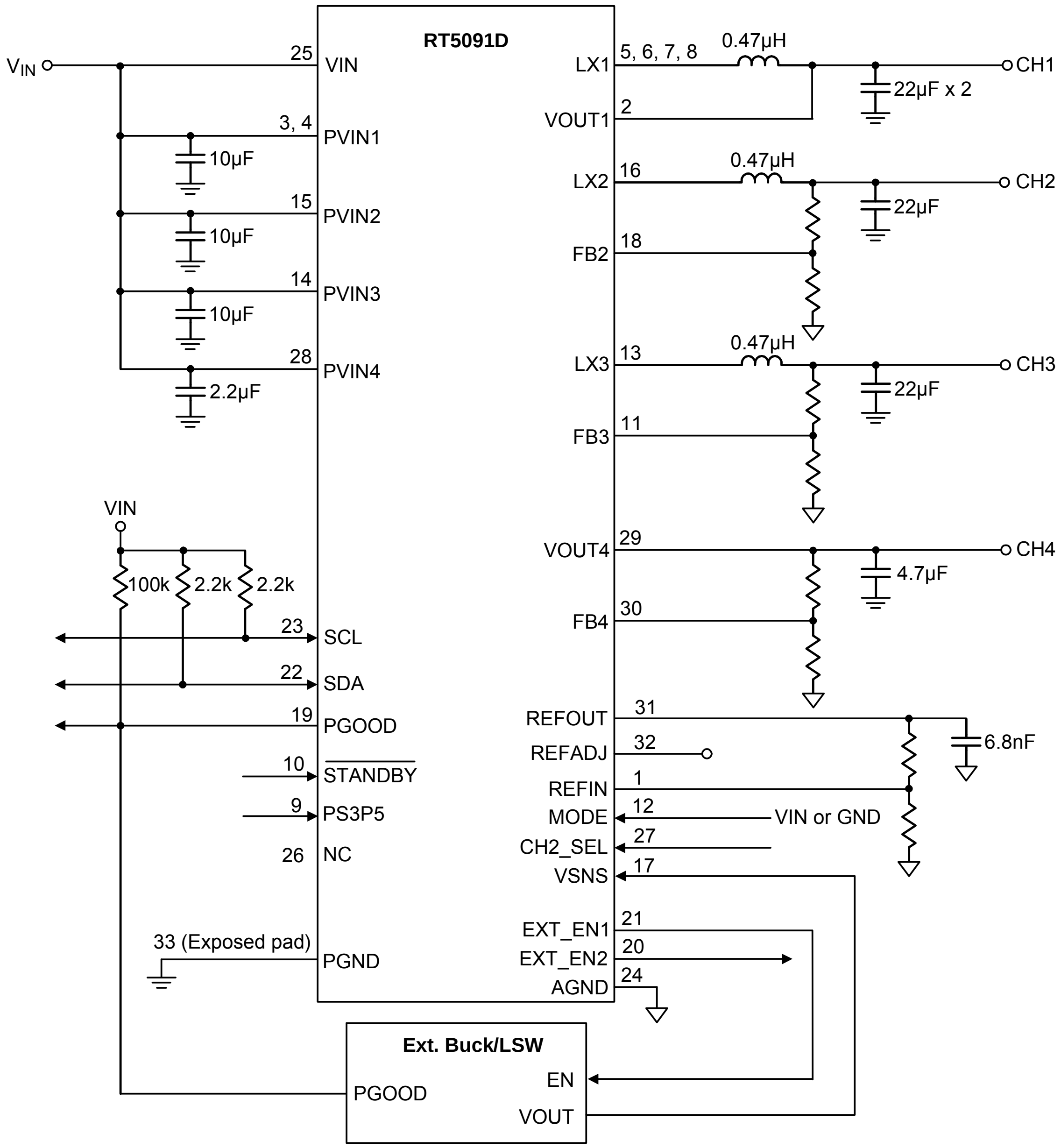
## Power States Operation by $\overline{\text{STANDBY}}$ & CH1 VOUT DVID by $I^2C$



**Power States Operation by $\overline{\text{STANDBY}}$ & CH1 VOUT Adjustment at Sleep Mode & no I²C**



**Power States Operation by $\overline{\text{STANDBY}}$ & CH1 VOUT Adjustment via REFIN & no I[2]C**

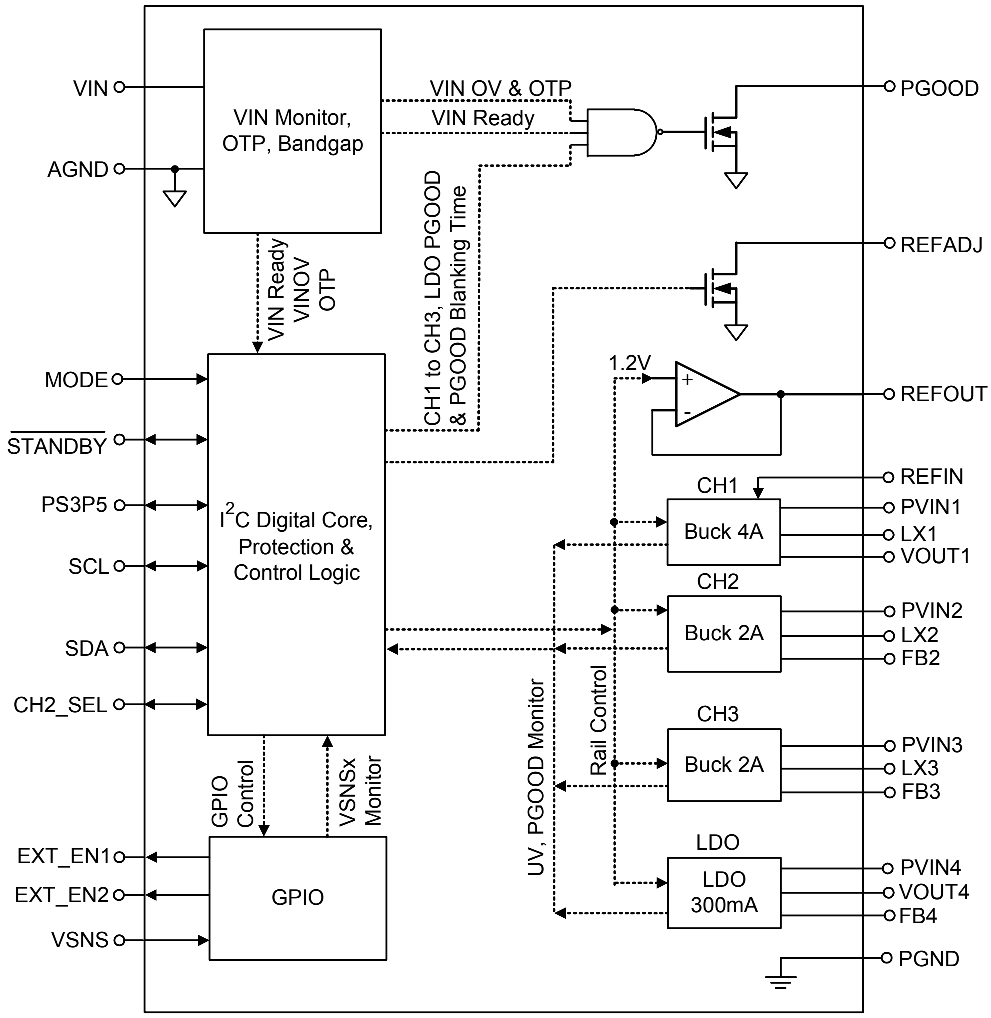


## Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | REFIN | CH1 external reference input. CH1 output voltage is equal to $V_{REFIN}$ x 1.6. |
| 2 | VOUT1 | This pin is CH1 buck feedback input. Connect this pin to CH1 buck output. To disable this rail, connect this pin to VIN. |
| 3, 4 | PVIN1 | CH1 buck converter power input. |
| 5, 6, 7, 8 | LX1 | CH1 buck converter switch node. |
| 9 | PS3P5 | Power state control pin. Refer to PS3P5 control. |
| 10 | $\overline{\text{STANDBY}}$ | Power state control pin. Refer to $\overline{\text{STANDBY}}$ control. Internal pull low by 1μA. |
| 11 | FB3 | This pin is CH3 buck feedback input. Connect this pin to a resistor divider to program CH3 output voltage, or directly to CH3 output node to have a default 1.8V for CH3 output voltage. To disable this rail, connect this pin to VIN. |
| 12 | MODE | SATA 3.3V/5V select. MODE = Low, $V_{IN}$ = 3.3V；MODE = High, $V_{IN}$ = 5V. Internal pull low by 1μA. |
| 13 | LX3 | CH3 buck converter switch node. |
| 14 | PVIN3 | CH3 buck converter power input. |
| 15 | PVIN2 | CH2 buck converter power input. |
| 16 | LX2 | CH2 buck converter switch node. |
| 17 | VSNS | External regulator output sense. If not used, tied to GND. |
| 18 | FB2 | This pin is CH2 buck feedback input. Connect this pin to a resistor divider to program CH2 output voltage, or directly to CH2 output node to have a default 1.2V for CH2 output voltage. To disable this rail, connect this pin to VIN. |
| 19 | PGOOD | This is open drain type. It indicates VIN and all rails output is ready or not. |
| 20 | EXT_EN2 | This pin is used to enable an external regulator/switch. Push-pull output. Should be floated if unused. |
| 21 | EXT_EN1 | This pin is used to enable an external regulator/switch. Push-pull output. Should be floated if unused. |
| 22 | SDA | $I^2C$ interface data signal. Connect to VIN if not used. |
| 23 | SCL | $I^2C$ interface clock signal. Connect to VIN if not used. |
| 24 | AGND | Analog ground pin. |
| 25 | VIN | Power input. |
| 26 | NC | No internal connection. |
| 27 | CH2_SEL | CH2 mode select pin.<br>CH2_SEL=GND, buck mode. CH2_SEL= VIN, bypass mode. |
| 28 | PVIN4 | LDO input. |
| 29 | VOUT4 | LDO output. |
| 30 | FB4 | This pin is LDO feedback input. Connect this pin to a resistor divider to program CH4 output voltage, or set this pin floated to have a default 1.8V for CH4 output voltage. To disable this rail, connect this pin to VIN. |

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 31 | REFOUT | Reference voltage output. It provides 1% high accuracy reference 1.2V with 0.1mA source ability. Bypass to GND with a 6.8nF ceramic capacitor. Series resistors connected to this pin should be lower than 1MΩ. |
| 32 | REFADJ | Reference adjustment output. Refer to PWM-VID Dynamic Voltage Control. If this pin is not used, ties to GND. |
| 33 (Exposed Pad) | PGND | Power ground. The exposed pad must be soldered to a large PCB and connected to PGND for maximum thermal dissipation. |

## Functional Block Diagram



## Operation

The RT5091D provides three high-efficiency synchronous buck regulators and one LDO for the power system of SSD.

### Buck Converter

The RT5091D incorporates three high-efficiency synchronous switching buck converters that deliver programmable output voltages. They feature constant-on-time current mode for low output voltage, quick transient response, and low quiescent current. These buck converters also possess all standard protections.

### Buck Over-Current Limiter (OCL)

The buck converters provides current limiter for over-current protection through detecting low-side MOSFET current, which is known as the valley current limiter behavior. If the sensed inductor current is above the current limit threshold, then current limiter will start to constrain the valley of inductor current to the current limiter threshold until inductor current drops below the current limiter threshold.

### Buck Under-Voltage Protection (UVP)

The output voltages are continuously monitored for under-voltage protection. If the output voltage falls below 62.5% of the reference voltage, under-voltage protection will be triggered and then the high-side and low-side MOSFET will be turned off. The UVP circuit will turn off all rails and latched. The only way to reset the latched behavior is restarting VIN power of the RT5091D.

### Buck Over-Voltage Protection (OVP)

The output voltages are continuously monitored for over-voltage protection. If the output voltage exceeds 125% of the reference voltage, over-voltage protection will be triggered and then the high-side and low-side MOSFET will be turned off. The MOSFET drivers will keep in off-state until the over-voltage protection is released.

### Linear Dropout Regulator (LDO)

The RT5091D includes one high performance linear dropout regulator. The LDO contains an independent current limit and under-voltage protection circuit to prevent unexpected applications. When the path current is above the current limit threshold, the current limit circuit adjusts the gate voltage of power stage to limit the output current. Besides, if the output voltage is lower than 60% of reference voltage, the UVP circuit will turn off all rails and latched. The only way to reset the latched behavior is restarting VIN power of the RT5091D.

### Over-Temperature Protection (OTP)

If chip temperature is higher than 150°C, the OTP circuit will shut down all power rails. PMIC will reboot with power-up sequence after chip temperature cools down lower than 125°C.

### GPIO

The RT5091D includes two external regulators/switches enable signals and one external regulator/switch output voltage sense.

### MODE

MODE is an input pin to select the threshold voltage of VIN for POR. If VIN voltage is above the threshold voltage, PMIC will begin to start up with power-up sequence.

## Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ------------------------------------------------ –0.3V to 6V
- PVIN1, PVIN2, PVIN3, PVIN4 ------------------------------------------------ –0.3V to 6V
- LX1, LX2, LX3 to GND ------------------------------------------------ –0.3V to 6V
  <50ns ------------------------------------------------ –5V to 10V
- Other Pins ------------------------------------------------ –0.3V to 6V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  WQFN-32L 4x4 ------------------------------------------------ 3.59W
- Package Thermal Resistance (Note 2)
  WQFN-32L 4x4, $\theta_{JA}$ ------------------------------------------------ 27.8°C/W
  WQFN-32L 4x4, $\theta_{JC}$ ------------------------------------------------ 7°C/W
- Junction Temperature ------------------------------------------------ 150°C
- Lead Temperature (Soldering, 10 sec.) ------------------------------------------------ 260°C
- Storage Temperature Range ------------------------------------------------ –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ------------------------------------------------ 2kV

## Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ------------------------------------------------ 2.8V to 5.5V
- Other Pins ------------------------------------------------ 0V to 5.5V
- Junction Temperature Range ------------------------------------------------ –40°C to 125°C
- Ambient Temperature Range ------------------------------------------------ –40°C to 85°C

## Electrical Characteristics

($V_{IN}$ = 3.3V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **PMIC** | | | | | | |
| VIN Voltage Range | $V_{VIN}$ | MODE = low | 2.8 | 3.3 | 3.7 | V |
| | | MODE = high | 3.8 | 5 | 5.5 | |
| VIN Supply Current | $I_{VIN}$ | All voltage rails, REFOUT buffer, VSNS GPIO & external MOSFET are disabled. | -- | 20 | -- | μA |
| $\overline{\text{STANDBY}}$ Threshold = High | $V_{\overline{STANDBY}\_H}$ | | 1.2 | -- | -- | V |
| $\overline{\text{STANDBY}}$ Threshold = Low | $V_{\overline{STANDBY}\_L}$ | | -- | -- | 0.4 | V |
| PS3P5 Threshold = High | $V_{PS3P5\_H}$ | | 1.2 | -- | -- | V |
| PS3P5 Threshold = Low | $V_{PS3P5\_L}$ | | -- | -- | 0.4 | V |
| VIN UVLO Threshold | | Falling | 2.1 | 2.2 | 2.3 | V |
| VIN UVLO Threshold Hysteresis | | | -- | 100 | -- | mV |
| Thermal Shutdown Threshold | $T_{SD}$ | (Note 5) | -- | 150 | -- | °C |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal Shutdown Hysteresis | $\Delta T_{SD}$ | (Note 5) | -- | 25 | -- | °C |
| **VIN Monitor** | | | | | | |
| VIN Ready Falling Threshold | $V_{RDY\_L}$ | Program by PGOOD_REG[2:1] via $I^2C$; MODE = low | 2.7 | -- | 3 | V |
| | | Program by PGOOD_VSYS_REG[2:1] via $I^2C$; MODE = high | 3.8 | -- | 4.1 | V |
| VIN Ready Threshold Step Size | | Step size for $I^2C$ programming | -- | 100 | -- | mV |
| VIN Ready Falling Accuracy | | MODE = low; VIN ready falling default threshold | 2.6 | 2.7 | 2.8 | V |
| | | MODE = high; VIN ready falling default threshold | 3.65 | 3.8 | 3.95 | V |
| VIN Ready Hysteresis | | | -- | 150 | -- | mV |
| **CH1 (4A)** | | | | | | |
| **Converter** | | | | | | |
| VIN Quiescent Current | $I_{Q\_VIN}$ | Enable, no switching, other voltage rails off, not include $I_{VIN}$. | -- | 25 | 35 | μA |
| Output Voltage Scaling | $V_{OUT}$ | Controlled by $I^2C$. (Note 6) | 0.7 | -- | 1.3 | V |
| DC Output Voltage Programmable Step | $V_{STEP}$ | | -- | 10 | -- | mV |
| Output Voltage Default | $V_{OUT}$ | REFOUT = REFADJ = REFIN = VIN, refer to configuration for other default voltage | 0.99 | 1 | 1.01 | V |
| Dynamic Voltage Scale Slew Rate | | | -- | 5 | -- | mV/μs |
| Line Regulation | | (Note 5) | -- | 0.5 | -- | %/V |
| Load Regulation | | Force PWM (Note 5) | -- | 0.5 | -- | %/A |
| H/S Switch On Resistance | $R_{DS(ON)\_H}$ | PVIN1 = 5V | -- | 36 | -- | mΩ |
| L/S Switch On Resistance | $R_{DS(ON)\_L}$ | PVIN1 = 5V | -- | 27 | -- | mΩ |
| Current Limit | $I_{LIM}$ | Valley current | 4.1 | 5 | -- | A |
| Switching Frequency | $f_{SW}$ | | 1.8 | 2 | 2.2 | MHz |
| Minimum Off-Time | $t_{OFF\_MIN}$ | | -- | 120 | 160 | ns |
| OVP Trip Threshold | $V_{OVP}$ | OVP detected | 120 | 125 | 130 | % |
| OVP Propagation Delay | $t_{OVPDLY}$ | (Note 5) | -- | 1 | -- | μs |
| UVP Trip Threshold | $V_{UVP}$ | UVP detected | 57.5 | 62.5 | 67.5 | % |
| UVP Propagation Delay | $t_{UVPDLY}$ | (Note 5) | -- | 2 | -- | μs |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PGOOD Trip Threshold | | Falling edge, measured at CH1 VOUT | 80 | 85 | 90 | % |
| PGOOD Trip Hysteresis | | | -- | 5 | -- | % |
| Soft-Start Time | $t_{SS}$ | VOUT1 = 1V | -- | 0.5 | 0.8 | ms |
| Discharge Resistance | $R_{DISCHG}$ | $V_{IN}$ = 5V, discharge from LX1 | -- | 10 | -- | Ω |
| Efficiency | | PVIN1 = 3.3V, VOUT1 = 1V, $I_{OUT}$ = 10mA | 85 | -- | -- | % |
| | | PVIN1 = 3.3V, VOUT1 = 1V, $I_{OUT}$ = 1A | 85 | -- | -- | % |
| **REFOUT Buffer** | | | | | | |
| Quiescent Current | | REFOUT buffer are enabled. | -- | 5 | -- | μA |
| REFADJ Switch On Resistance | | $V_{IN}$ = 5V | -- | 10 | -- | Ω |
| REFOUT Voltage | $V_{REFOUT}$ | Sourcing Current = 0.05mA, with 6.8nF Capacitor | −1% | 1.2 | 1% | V |
| **CH2 (Buck Mode 2A, Bypass Mode 4A)** | | | | | | |
| VIN Quiescent Current | $I_{Q\_IN}$ | Enable, no switching, other voltage rails off, not include $I_{VIN}$. | -- | 25 | 35 | μA |
| Internal Reference Voltage | | Connect FB2 to resistor voltage divider, measure at FB2 pin. | 0.792 | 0.8 | 0.808 | V |
| Output Voltage Default | $V_{OUT}$ | FB2 connected to VOUT2 | -- | 1.2 | -- | V |
| Line Regulation | | (Note 5) | -- | 0.5 | -- | %/V |
| Load Regulation | | Force PWM (Note 5) | -- | 0.5 | -- | %/A |
| H/S Switch On Resistance | $R_{DS(ON)\_H}$ | PVIN2 = 5V | -- | 103 | -- | mΩ |
| L/S Switch On Resistance | $R_{DS(ON)\_L}$ | PVIN2 = 5V | -- | 64 | -- | mΩ |
| Current Limit | $I_{LIM}$ | Buck mode, measure at inductor valley current. | 2.1 | 3 | -- | A |
| Switching Frequency | $f_{SW}$ | | 1.8 | 2 | 2.2 | MHz |
| Minimum Off-Time | $t_{OFF\_MIN}$ | | -- | 120 | 160 | ns |
| OVP Trip Threshold | $V_{OVP}$ | OVP detected | 120 | 125 | 130 | % |
| OVP Propagation Delay | $t_{OVPDLY}$ | (Note 5) | -- | 1 | -- | μs |
| UVP Trip Threshold | $V_{UVP}$ | CH2_SEL = low | 57.5 | 62.5 | 67.5 | % |
| | | CH2_SEL= high, MODE = low | 52 | 57 | 62 | |
| | | CH2_SEL = high, MODE = high | 60 | 65 | 70 | |
| UVP Propagation Delay (Note 5) | $t_{UVPDLY}$ | | -- | 2 | -- | μs |
| PGOOD Trip Threshold (Note 7) | | CH2_SEL = low | 80 | 85 | 90 | % |
| | | CH2_SEL= high, MODE = low | 72.5 | 77.5 | 82.5 | |
| | | CH2_SEL= high, MODE = high | 83.4 | 88.4 | 93.4 | |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PGOOD Trip Hysteresis | | | -- | 5 | -- | % |
| Soft-Start Time | $t_{SS}$ | | -- | 0.5 | 0.8 | ms |
| Discharge Resistance | $R_{DISCHG}$ | $V_{IN}$ = 5V, discharge from LX2 | -- | 10 | -- | Ω |
| Efficiency | | PVIN2 = 3.3V, FB2 = 1.2V, $I_{OUT}$ = 10mA | 85 | -- | -- | % |
| | | PVIN2 = 3.3V, FB2 = 1.2V, $I_{OUT}$ = 0.5A | 85 | -- | -- | % |
| **CH3 (2A)** | | | | | | |
| VIN Quiescent Current | $I_{Q\_IN}$ | Enable, no switching, other voltage rails off, not include $I_{VIN}$. | -- | 25 | 35 | μA |
| Internal Reference Voltage | | Connect FB3 to resistor voltage divider, measure at FB3 pin. | 0.792 | 0.8 | 0.808 | V |
| Output Voltage Default | $V_{OUT}$ | FB3 connected to CH3 VOUT | -- | 1.8 | -- | V |
| Line Regulation | | (Note 5) | -- | 0.5 | -- | %/V |
| Load Regulation | | Force PWM (Note 5) | -- | 0.5 | -- | %/A |
| H/S Switch On Resistance | $R_{DS(ON)\_H}$ | PVIN3 = 5V | -- | 101 | -- | mΩ |
| L/S Switch On Resistance | $R_{DS(ON)\_L}$ | PVIN3 = 5V | -- | 58 | -- | mΩ |
| Current Limit | $I_{LIM}$ | Valley current | 2.1 | 3 | -- | A |
| Switching Frequency | $f_{SW}$ | | 1.8 | 2 | 2.2 | MHz |
| Minimum Off-Time | $t_{OFF\_MIN}$ | | -- | 120 | 160 | ns |
| OVP Trip Threshold | $V_{OVP}$ | OVP detected | 120 | 125 | 130 | % |
| OVP Propagation Delay | $t_{OVPDLY}$ | (Note 5) | -- | 1 | -- | μs |
| UVP Trip Threshold | $V_{UVP}$ | UVP detected | 57.5 | 62.5 | 67.5 | % |
| UVP Propagation Delay | $t_{UVPDLY}$ | (Note 5) | -- | 2 | -- | μs |
| PGOOD Trip Threshold | | Falling edge, measured at CH3 VOUT | 80 | 85 | 90 | % |
| PGOOD Trip Hysteresis | | | -- | 5 | -- | % |
| Soft-Start Time | $t_{SS}$ | | -- | 0.5 | 0.8 | ms |
| Discharge Resistance | $R_{DISCHG}$ | $V_{IN}$ = 5V, discharge from LX3 | -- | 10 | -- | Ω |
| Efficiency | | PVIN3 = 3.3V, FB3 = 1.8V, $I_{OUT}$ = 10mA | 85 | -- | -- | % |
| | | PVIN3 = 3.3V, FB3 = 1.8V, $I_{OUT}$ = 0.5A | 85 | -- | -- | % |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LDO (0.3A)** | | | | | | |
| VIN Quiescent Current | $I_{Q\_IN}$ | Enable, no load, other voltage rails off, not include $I_{VIN}$. | -- | 28 | 38 | μA |
| Internal Reference Voltage | | Connect FB4 to resistor voltage divider, measure at FB4 pin. | 0.4455 | 0.45 | 0.4545 | V |
| Output Voltage Default | | FB4 floating | -- | 1.8 | -- | V |
| Line Regulation | | | -- | 0.5 | -- | %/V |
| Load Regulation | | | -- | 0.5 | -- | %/A |
| Dropout Voltage | $V_{DROP}$ | PVIN4 = 5V, VOUT4 = 3.3V, $I_{OUT}$ =300mA | -- | -- | 100 | mV |
| Current Limit | $I_{LIM}$ | | 0.4 | -- | -- | A |
| UVP Trip Threshold | $V_{UVP}$ | UVP detected | 55 | 60 | 65 | % |
| UVP Propagation Delay | $t_{UVPDLY}$ | (Note 5) | -- | 2 | -- | μs |
| PGOOD Trip Threshold | | Falling edge, measured at VOUT4 | 80 | 85 | 90 | % |
| PGOOD Trip Hysteresis | | | -- | 5 | -- | % |
| Soft-Start Time | $t_{SS}$ | VOUT4 = 1.8V | -- | 0.26 | 0.5 | ms |
| Discharge Resistance | $R_{DISCHG}$ | $V_{IN}$ = 5V, discharge from VOUT4 | -- | 100 | -- | Ω |
| Power Supply Rejection Rate | PSRR | $I_{OUT}$ = 100mA, f = 100Hz | -- | –50 | -- | dB |
| | | $I_{OUT}$ =100mA, f = 100kHz | -- | –28 | -- | |
| **GPIO** | | | | | | |
| **GPIO Input (VSNS)** | | | | | | |
| VSNS Discharge Resistance | $R_{DISCHG}$ | | -- | 10 | -- | Ω |
| **I²C for Fast Mode** | | | | | | |
| SDA, SCL Input Voltage High | | | 1.2 | -- | -- | V |
| SDA, SCL Input Voltage Low | | | -- | -- | 0.4 | V |
| SCL Clock Rate | $f_{SCL}$ | | 100 | -- | 400 | kHz |
| Hold Time for a Repeated START Condition | $t_{HD;STA}$ | After this period, the first clock pulse is generated. | 0.6 | -- | -- | μs |
| Low Period of the SCL Clock | $t_{LOW}$ | | 1.3 | -- | -- | μs |
| High Period of the SCL Clock | $t_{HIGH}$ | | 0.6 | -- | -- | μs |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Set Up Time For a Repeated START Condition | $t_{SU;STA}$ | | 0.6 | -- | -- | μs |
| Data Hold Time | $t_{HD;DAT}$ | | 0 | -- | 0.9 | μs |
| Data Set Up Time | $t_{SU;DAT}$ | | 100 | -- | -- | ns |
| Set Up Time for STOP Condition | $t_{SU;STO}$ | | 0.6 | -- | -- | μs |
| Bus Free Time between a STOP and a START Condition | $t_{BUF}$ | | 1.3 | -- | -- | μs |
| Rising Time of Both SDA/SCL Signals | $t_R$ | | 20 | -- | 300 | ns |
| Falling Time of Both SDA/SCL Signals | $t_F$ | | 20 | -- | 300 | ns |
| SDA Output Low Sink Current | $I_{OL}$ | SDA voltage = 0.4V | 2 | -- | -- | mA |
| **$I^2C$ for High Speed Mode** | | | | | | |
| SDA, SCL Input Voltage High | | | 1.2 | -- | -- | V |
| SDA, SCL Input Voltage Low | | | -- | -- | 0.4 | V |
| SCL Clock Rate | $f_{SCL}$ | | 0.1 | -- | 3.4 | MHz |
| Hold Time for a Repeated START Condition | $t_{HD;STA}$ | After this period, the first clock pulse is generated. | 160 | -- | -- | ns |
| Low Period of the SCL Clock | $t_{LOW}$ | | 160 | -- | -- | ns |
| High Period of the SCL Clock | $t_{HIGH}$ | | 60 | -- | -- | ns |
| Set-Up Time For a Repeated START Condition | $t_{SU;STA}$ | | 60 | -- | -- | ns |
| Data Hold Time | $t_{HD;DAT}$ | | 0 | -- | 70 | ns |
| Data Set-Up Time | $t_{SU;DAT}$ | | 10 | -- | -- | ns |
| Set-Up Time for STOP Condition | $t_{SU;STO}$ | | 160 | -- | -- | ns |
| Rising Time of Both SDA/SCL Signals | $t_R$ | | 10 | -- | 80 | ns |
| Falling Time of Both SDA/SCL Signals | $t_F$ | | 10 | -- | 80 | ns |
| SDA Output Low Sink Current | $I_{OL}$ | SDA voltage = 0.4V | 2 | -- | -- | mA |

**Note 1.** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** $\theta_{JA}$ is measured under natural convection (still air) at $T_A$ = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. $\theta_{JC}$ is measured at the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

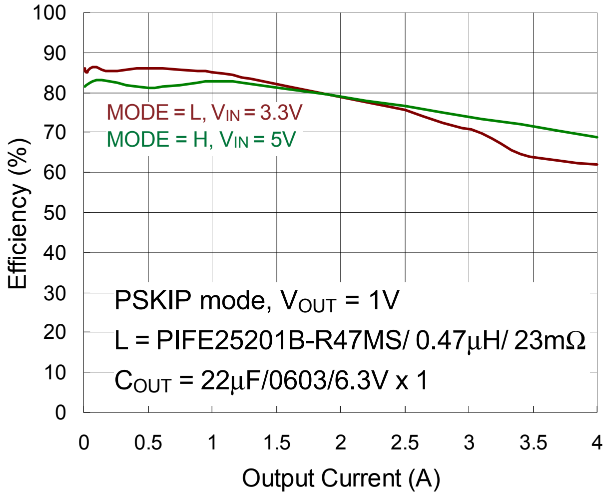
**Note 5.** Guaranteed by design.

**Note 6.** Program CH1 output voltage via $I^2C$ need default output voltage setting during power-up sequence. Please set CH1 buck converter by Table 15.

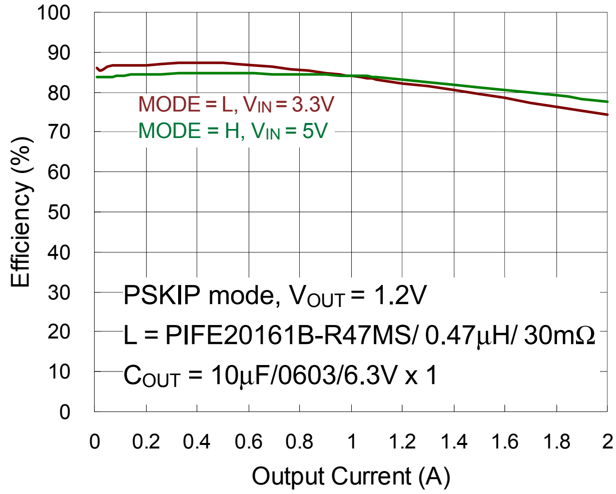
Note 7. Falling edge, measured at CH2 VOUT.

## Typical Operating Characteristics

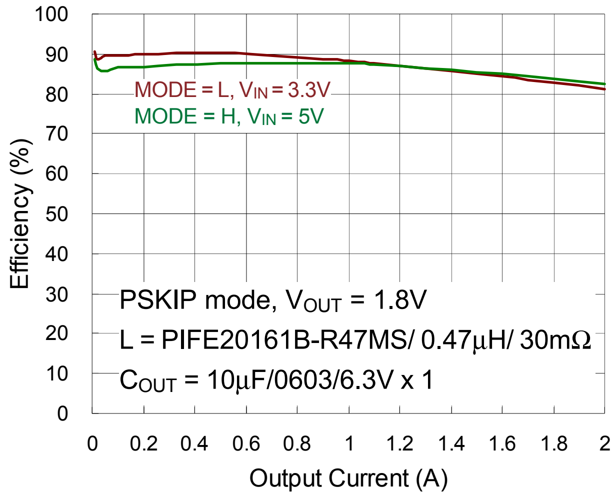
CH1 Efficiency vs. Output Current



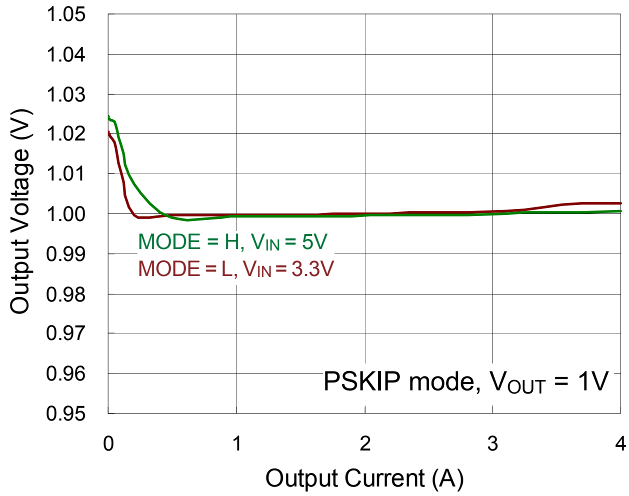

CH2 Efficiency vs. Output Current



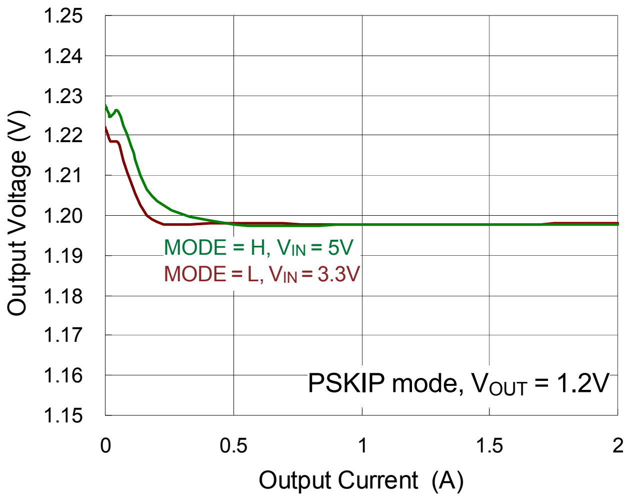

CH3 Efficiency vs. Output Current



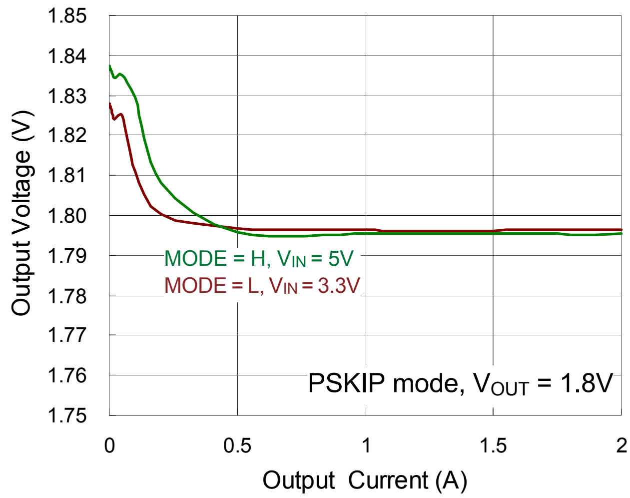

CH1 Output Voltage vs. Output Current

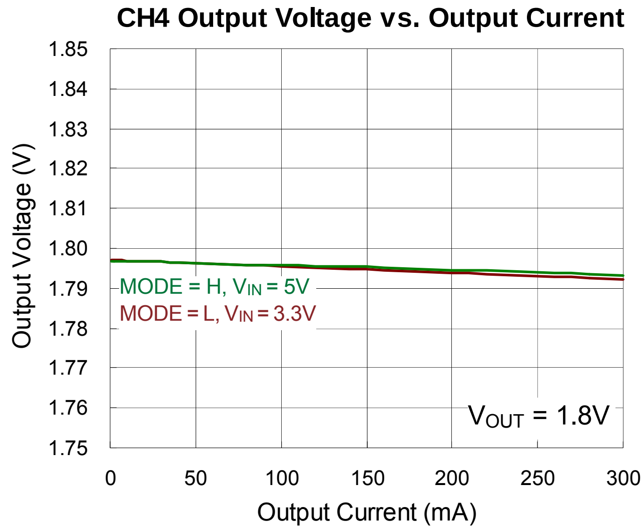


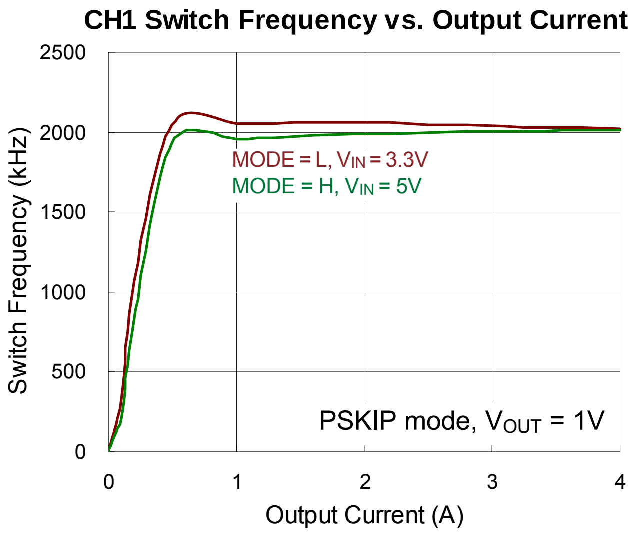

CH2 Output Voltage vs. Output Current

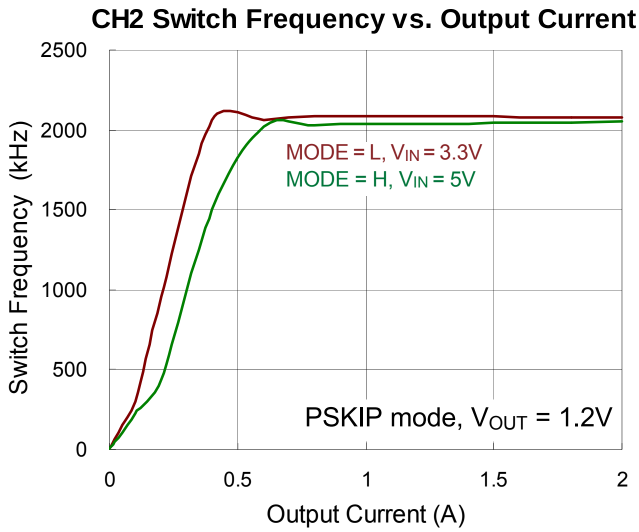


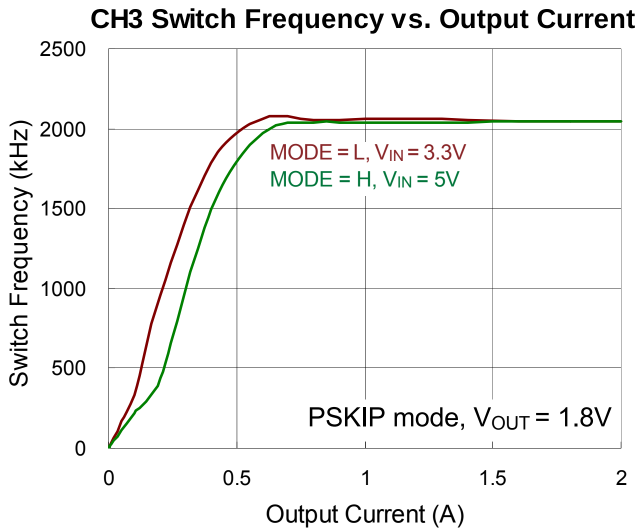

CH3 Output Voltage vs. Output Current

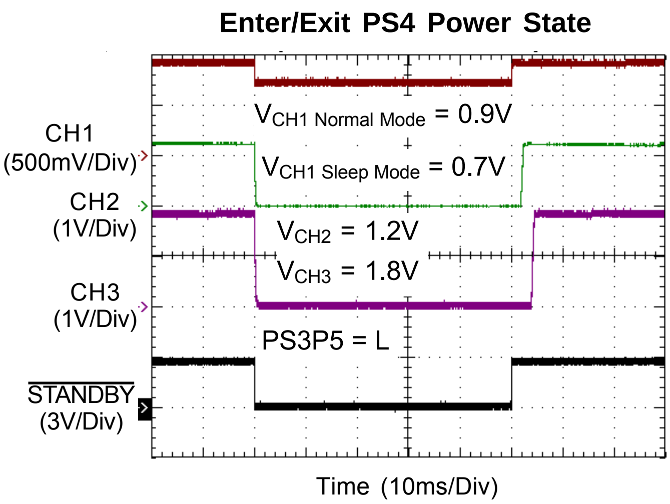


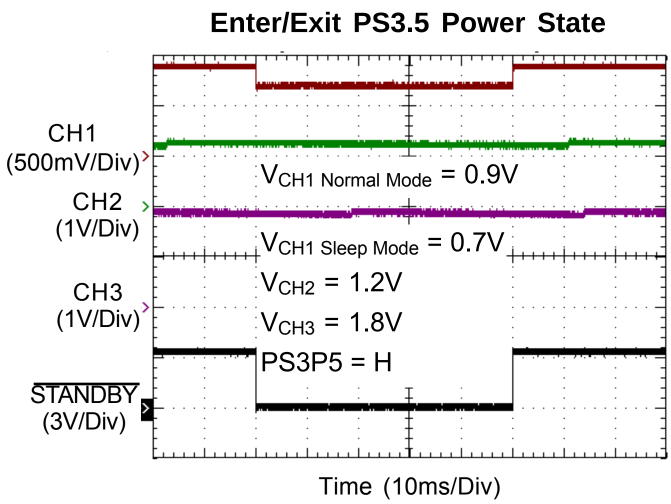

CH4 Output Voltage vs. Output Current
Output Voltage (V)
1.85
1.84
1.83
1.82
1.81
1.80
1.79
1.78
1.77
1.76
1.75
MODE = H, VIN = 5V
MODE = L, VIN = 3.3V
VOUT = 1.8V
0
50
100
150
200
250
300
Output Current (mA)


CH1 Switch Frequency vs. Output Current
Switch Frequency (kHz)
2500
2000
1500
1000
500
0
MODE = L, VIN = 3.3V
MODE = H, VIN = 5V
PSKIP mode, VOUT = 1V
0
1
2
3
4
Output Current (A)

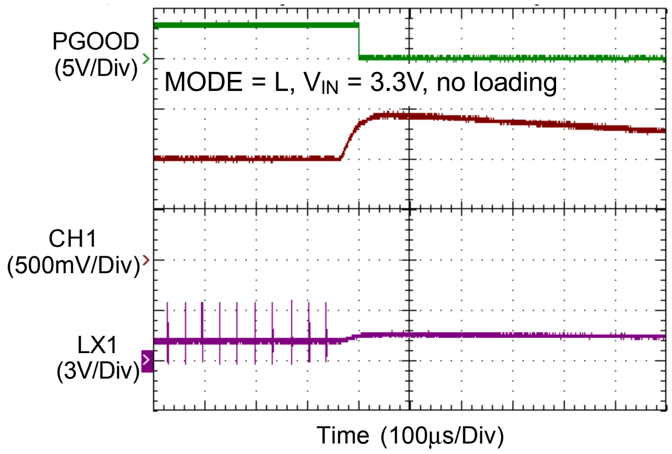

CH2 Switch Frequency vs. Output Current
Switch Frequency (kHz)
2500
2000
1500
1000
500
0
MODE = L, VIN = 3.3V
MODE = H, VIN = 5V
PSKIP mode, VOUT = 1.2V
0
0.5
1
1.5
2
Output Current (A)


CH3 Switch Frequency vs. Output Current
Switch Frequency (kHz)
2500
2000
1500
1000
500
0
MODE = L, VIN = 3.3V
MODE = H, VIN = 5V
PSKIP mode, VOUT = 1.8V
0
0.5
1
1.5
2
Output Current (A)

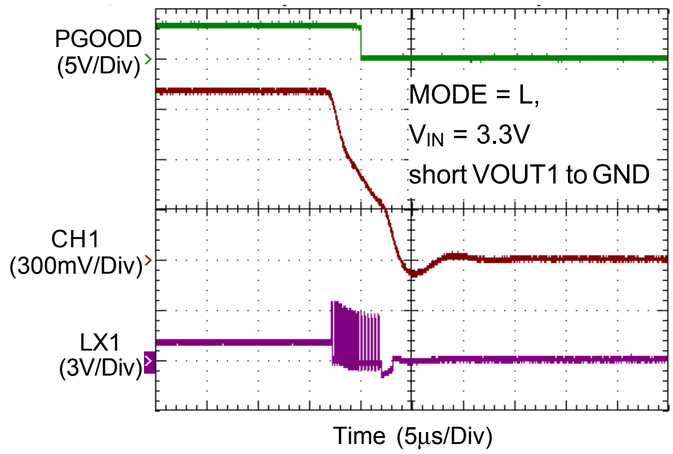

Enter/Exit PS4 Power State
CH1 (500mV/Div)
CH2 (1V/Div)
CH3 (1V/Div)
STANDBY (3V/Div)
VCH1 Normal Mode = 0.9V
VCH1 Sleep Mode = 0.7V
VCH2 = 1.2V
VCH3 = 1.8V
PS3P5 = L
Time (10ms/Div)


Enter/Exit PS3.5 Power State
CH1 (500mV/Div)
CH2 (1V/Div)
CH3 (1V/Div)
STANDBY (3V/Div)
VCH1 Normal Mode = 0.9V
VCH1 Sleep Mode = 0.7V
VCH2 = 1.2V
VCH3 = 1.8V
PS3P5 = H
Time (10ms/Div)

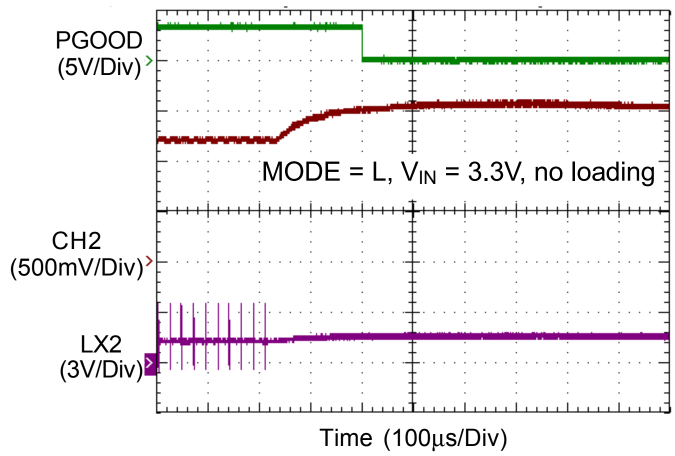
### CH1 Over Voltage Protection



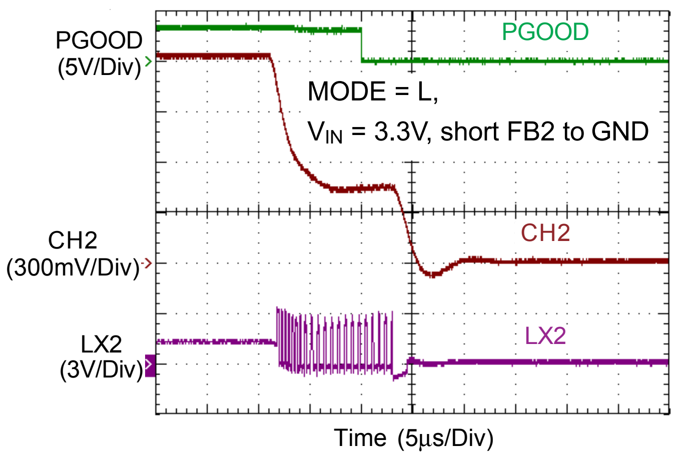

### CH1 Under Voltage Protection



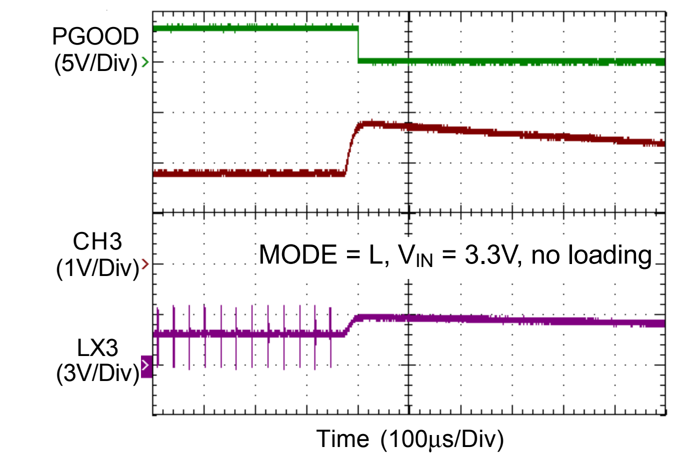

### CH2 Over Voltage Protection



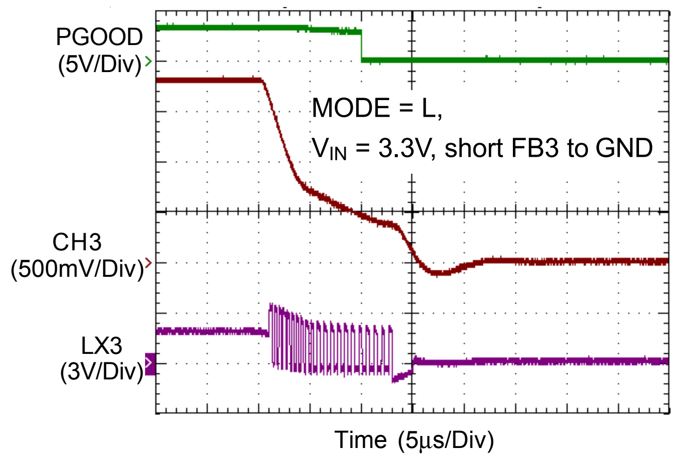

### CH2 Under Voltage Protection



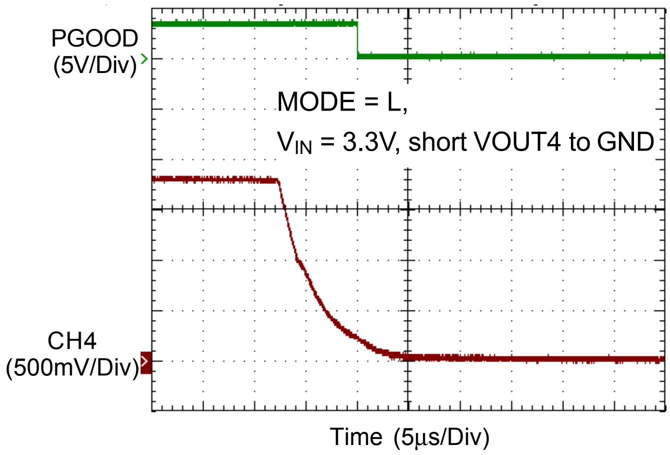

### CH3 Over Voltage Protection



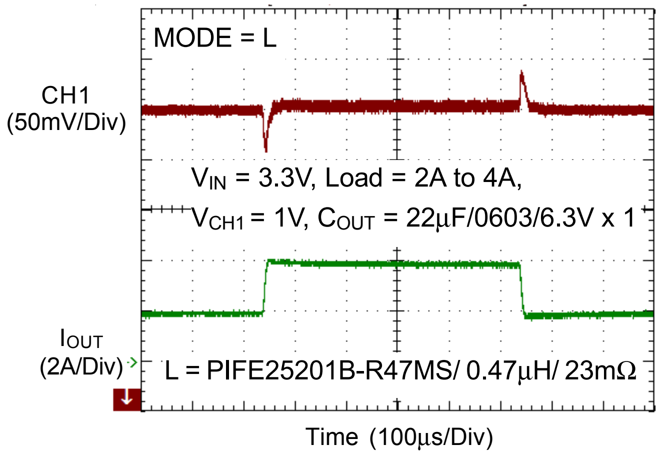

### CH3 Under Voltage Protection



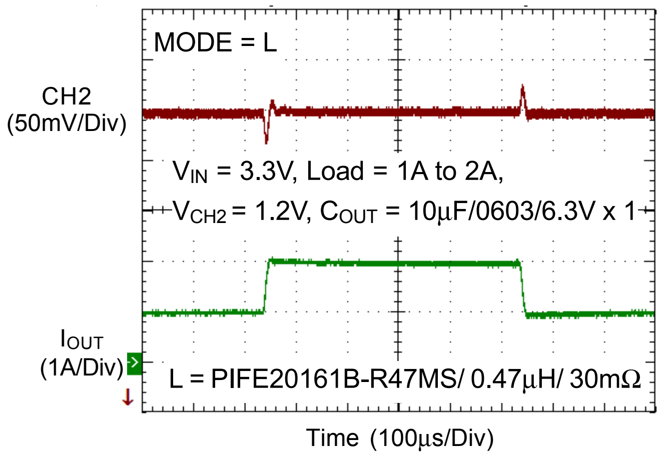
CH4 Under Voltage Protection



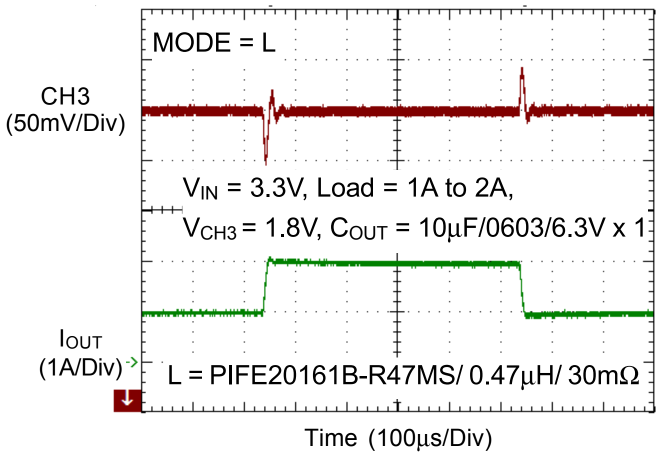

CH1 Transient Response



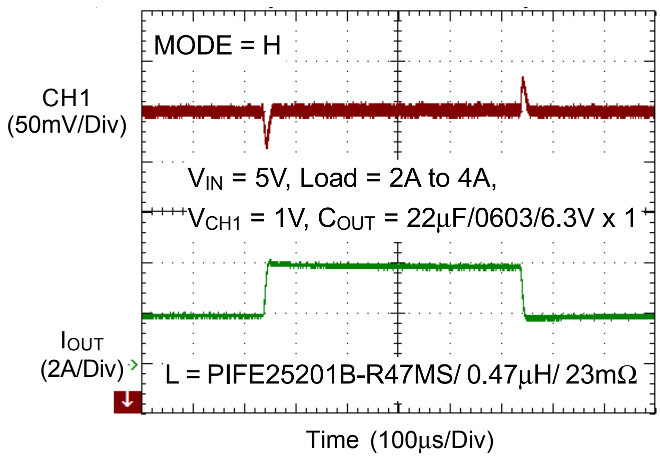

CH2 Transient Response



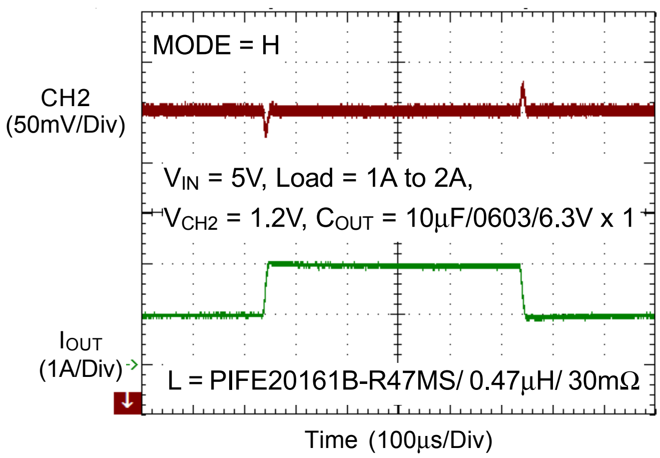

CH3 Transient Response



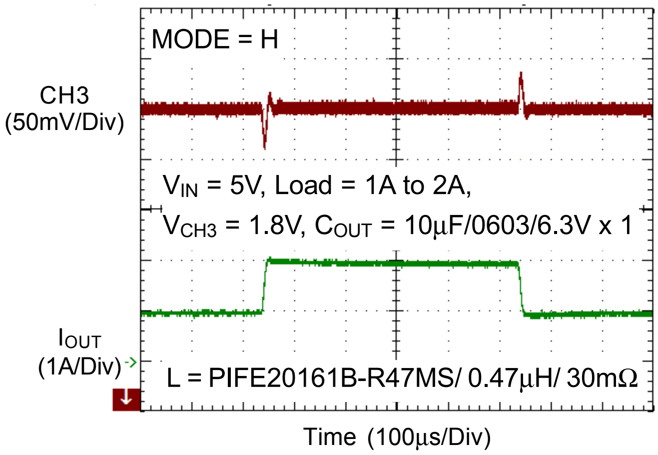

CH1 Transient Response




CH2 Transient Response



CH3 Transient Response



## Functional Register Table

**Table 1. Register Summary**

| Name | Type | Register Reset | Address Offset |
|---|---|---|---|
| STANDBY | R/W | 0x00h | 0x00 |
| PGOOD_ REG | R/W | -- | 0x01 |
| CH1_VID_REG | R/W | -- | 0x02 |
| DCDCCTRL0_REG0 | R/W | 0x00h | 0x03 |
| DCDCCTRL1_REG | R/W | 0x00h | 0x04 |
| CH1/CH2_CONTROL | R/W | 0x56h | 0x05 |
| CH3/LDO_CONTROL | R/W | 0XE1h | 0x06 |
| EXT_EN1/EXT_EN2_CONTROL | R/W | 0x8Ah | 0x07 |
| PRODUCT_ID_REG | R | 0x00h | 0x0A |
| MANUFACTURER_ID_REG | R | 0x00h | 0x0B |
| REVISION_NUMBER_REG | R | 0x00h | 0x0C |
| PROTECT | R | -- | 0x0D |

**Table 2. STANDBY**

**Address :** 0x00
**Description :** PS3.5/PS4 Power State Enable/Disable

| Bits | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| Name | Reserved | | | | | | | STANDBYEN |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/ Write | R | R | R | R | R | R | R | R/W |

| Bits | Name | Description |
|---|---|---|
| 7 : 1 | Reserved | Reserved bit |
| 0 | STANDBYEN | PS3.5/PS4 power state allowed to enter<br>0 : Not allowed<br>1 : Allowed |

Table 3. PGOOD_REG

**Address :** 0x01
**Description :** Power good information register
When voltage rails achieve 90% of VID target, the relative bit will set to 1.

| **Bits** | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | CH1_ PGOOD | CH2_ PGOOD | CH3_ PGOOD | LDO_ PGOOD | MODE | VRDY_TH | | Reserved |
| **Reset Value** | 0 | 0 | 0 | 0 | -- | -- | -- | 1 |
| **Read/ Write** | R | R | R | R | R | R/W | R/W | R/W |

| Bits | Name | Description |
|---|---|---|
| 7 | CH1_PGOOD | Status bit. Indicates power good on CH1 |
| 6 | CH2_PGOOD | Status bit. Indicates power good on CH2 |
| 5 | CH3_PGOOD | Status bit. Indicates power good on CH3 |
| 4 | LDO_PGOOD | Status bit. Indicates power good on CH4 |
| 3 | MODE | MODE = Low, MODE[3] = 0b<br>MODE = High, MODE[3] = 1b |
| 2 : 1 | VRDY_TH | MODE = Low, MODE[3] = 0b :<br>VRDY_TH[2:1] = 00b : 2.7V (default)<br>VRDY_TH[2:1] = 01b : 2.8V<br>VRDY_TH[2:1] = 10b : 2.9V<br>VRDY_TH[2:1] = 11b : 3V<br>MODE = High, MODE[3] = 1b :<br>VRDY_TH[2:1] = 00b : 3.8V (default)<br>VRDY_TH[2:1] = 01b : 3.9V<br>VRDY_TH[2:1] = 10b : 4V<br>VRDY_TH[2:1] = 11b : 4.1V |
| 0 | Reserved | Reserved bit. Keep it always be 1. |

Table 4. CH1_VID_REG

| **Address :** 0x02<br>**Description :** CH1 VID setting register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bits** | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| **Name** | Reserved | | SEL | | | | | |
| **Reset Value** | 0 | 0 | -- | -- | -- | -- | -- | -- |
| **Read/Write** | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

| Bits | Name | Description |
|---|---|---|
| 7 : 6 | Reserved | Reserved bit |
| 5 : 0 | SEL | Supply voltage :<br>SEL[5:0] = 000000b : 0.7V<br>SEL[5:0] = 000001b : 0.71V<br>SEL[5:0] = 000010b : 0.72V<br>SEL[5:0] = 000011b : 0.73V<br>SEL[5:0] = 000100b : 0.74V<br>SEL[5:0] = 000101b : 0.75V<br>SEL[5:0] = 000110b : 0.76V<br>SEL[5:0] = 000111b : 0.77V<br>SEL[5:0] = 001000b : 0.78V<br>SEL[5:0] = 001001b : 0.79V<br>SEL[5:0] = 001010b : 0.8V<br>SEL[5:0] = 001011b : 0.81V<br>SEL[5:0] = 001100b : 0.82V<br>SEL[5:0] = 001101b : 0.83V<br>SEL[5:0] = 001110b : 0.84V<br>SEL[5:0] = 001111b : 0.85V<br>SEL[5:0] = 010000b : 0.86V<br>SEL[5:0] = 010001b : 0.87V<br>SEL[5:0] = 010010b : 0.88V<br>SEL[5:0] = 010011b : 0.89V<br>SEL[5:0] = 010100b : 0.9V<br>SEL[5:0] = 010101b : 0.91V<br>SEL[5:0] = 010110b : 0.92V<br>SEL[5:0] = 010111b : 0.93V<br>SEL[5:0] = 011000b : 0.94V<br>SEL[5:0] = 011001b : 0.95V<br>SEL[5:0] = 011010b : 0.96V<br>SEL[5:0] = 011011b : 0.97V<br>SEL[5:0] = 011100b : 0.98V<br>SEL[5:0] = 011101b : 0.99V<br>SEL[5:0] = 011110b : 1V<br>SEL[5:0] = 011111b : 1.01V<br>SEL[5:0] = 100000b : 1.02V<br>SEL[5:0] = 100001b : 1.03V<br>SEL[5:0] = 100010b : 1.04V<br>SEL[5:0] = 100011b : 1.05V<br>SEL[5:0] = 100100b : 1.06V<br>SEL[5:0] = 100101b : 1.07V |

| Bits | Name | Description |
|---|---|---|
| 5 : 0 | SEL | SEL[5:0] = 100110b : 1.08V<br>SEL[5:0] = 100111b : 1.09V<br>SEL[5:0] = 101000b : 1.1V<br>SEL[5:0] = 101001b : 1.11V<br>SEL[5:0] = 101010b : 1.12V<br>SEL[5:0] = 101011b : 1.13V<br>SEL[5:0] = 101100b : 1.14V<br>SEL[5:0] = 101101b : 1.15V<br>SEL[5:0] = 101110b : 1.16V<br>SEL[5:0] = 101111b : 1.17V<br>SEL[5:0] = 110000b : 1.18V<br>SEL[5:0] = 110001b : 1.19V<br>SEL[5:0] = 110010b : 1.20V<br>SEL[5:0] = 110011b : 1.21V<br>SEL[5:0] = 110100b : 1.22V<br>SEL[5:0] = 110101b : 1.23V<br>SEL[5:0] = 110110b : 1.24V<br>SEL[5:0] = 110111b : 1.25V<br>SEL[5:0] = 111000b : 1.26V<br>SEL[5:0] = 111001b : 1.27V<br>SEL[5:0] = 111010b : 1.28V<br>SEL[5:0] = 111011b : 1.29V<br>SEL[5:0] = 111100b to 111111b : 1.3V |

Table 5. DCDCCTRL0_REG0

**Address :** 0x03
**Description :** Internal enable register

| **Bits** | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | LSW1_ EN | CH1_ EN | CH2_ EN | CH3_ EN | LDO_ EN | EXT_EN1_ EN | EXT_EN2_ EN | Reserved |
| **Reset Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Read/Write** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R |

| **Bits** | **Name** | **Description** |
|---|---|---|
| 7 | LSW1_EN | LSW1_EN[7] = 0b : Disable LSW1<br>LSW1_EN[7] = 1b : Enable LSW1<br>After PMIC powering up, this register value is auto-written to 1b. Power off all rails by setting 0b, PMIC will automatically set this register to 0x00h. Setting to 1b will re-power on all rails in sequence, DO NOT set this register to any value other than 0x80h. In case of rails are forced to be turned on during internal circuits are still doing the auto-calibration and detecting progress. |
| 6 | CH1_EN | CH1_EN[6] = 0b : Disable CH1<br>CH1_EN[6] = 1b : Enable CH1<br>After PMIC powering up, this register value is auto-written to 1b. |
| 5 | CH2_EN | CH2_EN[5] = 0b : Disable CH2<br>CH2_EN[5] = 1b : Enable CH2<br>After PMIC powering up, this register value is auto-written to 1b. |
| 4 | CH3_EN | CH3_EN[4] = 0b : Disable CH3<br>CH3_EN[4] = 1b : Enable CH3<br>After PMIC powering up, this register value is auto-written to 1b. |
| 3 | LDO_EN | LDO_EN[3] = 0b : Disable LDO<br>LDO_EN[3] = 1b : Enable LDO<br>After PMIC powering up, this register value is auto-written to 1b. |
| 2 | EXT_EN1_EN | EXT_EN1_EN[2] = 0b : Disable EXT_EN1<br>EXT_EN2_EN[2] = 1b : Enable EXT_EN1<br>After PMIC powering up, this register value is auto-written to 1b. |
| 1 | EXT_EN2_EN | CH6_EN[1] = 0b : Disable EXT_EN2<br>CH6_EN[1] = 1b : Enable EXT_EN2<br>After PMIC powering up, this register value is auto-written to 1b. |
| 0 | Reserved | Reserved bit |

**Table 6. DCDCCTRL1_REG**

| **Address :** 0x04 **Description :** DCDC PSKIP/PWM mode control register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bits** | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| **Name** | CH1_ PWM | CH2_ PWM | CH3_ PWM | Reserved | | | | |
| **Reset Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Read/Write** | R/W | R/W | R/W | R | R | R | R | R |

| **Bits** | **Name** | **Description** |
|---|---|---|
| 7 | CH1_PWM | CH1_PWM[7] = 0b : PSKIP mode<br>CH1_PWM[7] = 1b : Forced PWM mode |
| 6 | CH2_ PWM | CH2_PWM[6] = 0b : PSKIP mode<br>CH2_PWM[6] = 1b : Forced PWM mode |
| 5 | CH3_ PWM | CH3_PWM[5] = 0b : PSKIP mode<br>CH3_PWM[5] = 1b : Forced PWM mode |
| 4 : 0 | Reserved | Reserved bit |

**Table 7. CH1_CH2_CONTROL**

| **Address :** 0x05 **Description :** CH1/CH2 wake up timing configure register & sleep mode control register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bits** | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| **Name** | CH1_WAKE-UP_TIME | | | CH1_ALIVE | CH2_WAKE-UP_TIME | | | CH2_ALIVE |
| **Reset Value** | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| **Read/Write** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| **Bits** | **Name** | **Description** |
|---|---|---|
| 7 : 5 | CH1_WAKE-UP _TIME | CH1 wake up sequence timing setting<br>[7:5] = 000b : Time slot 0<br>[7:5] = 001b : Time slot 1<br>[7:5] = 010b : Time slot 2<br>[7:5] = 011b : Time slot 3<br>[7:5] = 100b : Time slot 4<br>[7:5] = 101b : Time slot 5<br>[7:5] = 110b : Time slot 6<br>[7:5] = 111b : Time slot 7<br>The duration between wake-up signal and a rail rising edge is :<br>$T_{WAKE\_UP\_DELAY} = 150\mu s + N \times 512\mu s$. $(0 \leq N \leq 7)$ |
| 4 | CH1_ALIVE | When entering sleep mode :<br>CH1_ALIVE[4] = 0b : CH1 turns off<br>CH1_ALIVE[4] = 1b : CH1 keeps alive and enters sleep mode |
| 3 : 1 | CH2_WAKE-UP _TIME | Please refer to “CH1_WAKE-UP_TIME” register description. |
| 0 | CH2_ALIVE | When entering sleep mode:<br>CH2_ALIVE[0] = 0b : CH2 turns off<br>CH2_ALIVE[0] = 1b : CH2 keeps alive and enters sleep mode |

**Table 8. CH3_LDO_CONTROL**

| **Address :** 0x06<br>**Description :** CH3/LDO wake up timing configure register & sleep mode control register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bits** | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| **Name** | CH3_WAKE-UP_TIME | | | CH3_ALIVE | LDO_WAKE-UP_TIME | | | LDO_ALIVE |
| **Reset Value** | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| **Read/Write** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| **Bits** | **Name** | **Description** |
|---|---|---|
| 7 : 5 | CH3_WAKE-UP_TIME | Please refer to "CH1_WAKE-UP_TIME" register description. |
| 4 | CH3_ALIVE | When entering sleep mode :<br>CH3_ALIVE[4] = 0b : CH3 turns off<br>CH3_ALIVE[4] = 1b : CH3 keeps alive and enters sleep mode |
| 3 : 1 | LDO_WAKE-UP_TIME | Please refer to "CH1_WAKE-UP_TIME" register description. |
| 0 | LDO_ALIVE | When entering sleep mode:<br>LDO_ALIVE[0] = 0b : LDO turns off<br>LDO_ALIVE[0] = 1b : LDO keeps alive and enters sleep mode |

**Table 9. EXT_EN1&EXT_EN2_CONTROL**

| **Address :** 0x07<br>**Description :** EXT_EN1/EXT_EN2 wake up timing configure register & sleep mode control register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bits** | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| **Name** | EXT_EN1_WAKE-UP_TIME | | | EXT_EN1_ALIVE | EXT_EN2_WAKE-UP_TIME | | | EXT_EN2_ALIVE |
| **Reset Value** | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| **Read/Write** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| **Bits** | **Name** | **Description** |
|---|---|---|
| 7 : 5 | EXT_EN1_WAKE-UP_TIME | Please refer to "CH1_WAKE-UP_TIME" register description. |
| 4 | EXT_EN1_ALIVE | When entering sleep mode :<br>EXT_EN1_ALIVE[4] = 0b : EXT_EN1 turns off<br>EXT_EN1_ALIVE[4] = 1b : EXT_EN1 keeps alive and enters sleep mode |
| 3 : 1 | EXT_EN2_WAKE-UP_TIME | Please refer to "CH1_WAKE-UP_TIME" register description. |
| 0 | EXT_EN2_ALIVE | When entering sleep mode :<br>EXT_EN2_ALIVE[0] = 0b : EXT_EN2 turns off<br>EXT_EN2_ALIVE[0] = 1b : EXT_EN2 keeps alive and enters sleep mode |

Table 10. PRODUCT_ID_REG

| **Address :** 0x0A<br>**Description :** Product ID number register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bits** | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| **Name** | PRODUCT_ID | | | | | | | |
| **Reset Value** | 0x00h | | | | | | | |
| **Read/Write** | R | R | R | R | R | R | R | R |

| Bits | Name | Description |
|---|---|---|
| 7 : 0 | PRODUCT_ID | Return the product ID number : 0x00h |

Table 11. MANUFACTURER_ID_REG

| **Address :** 0x0B<br>**Description :** Manufacturer ID number register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bits** | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| **Name** | MANUFACTURER_ID | | | | | | | |
| **Reset Value** | 0x00h | | | | | | | |
| **Read/Write** | R | R | R | R | R | R | R | R |

| Bits | Name | Description |
|---|---|---|
| 7 : 0 | MANUFACTURER_ID | Return the manufacturer ID number : 0x00h |

Table 12. REVISION_NUMBER_REG

| **Address :** 0x0C<br>**Description :** Revision number register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bits** | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| **Name** | REVISION_NUMBER | | | | | | | |
| **Reset Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Read/Write** | R | R | R | R | R | R | R | R |

| Bits | Name | Description |
|---|---|---|
| 7 : 0 | REVISION_NUMBER | Return the revision number : 0x00h |

Table 13. PROTECT

| **Address :** 0x0D<br>**Description :** Protect register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bits** | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| **Name** | UV_CH1 | UV_CH2 | UV_CH3 | UV_LDO | OT_IC | OV_VIN | GATE_READY | PORB_VOUT |
| **Reset Value** | -- | -- | -- | -- | -- | -- | 1 | 1 |
| **Read/ Write** | R | R | R | R | R | R | R | R |

| Bits | Name | Description |
|---|---|---|
| 7 | UV_CH1 | Indicator for CH1 under voltage event. |
| 6 | UV_CH2 | Indicator for CH2 under voltage event. |
| 5 | UV_CH3 | Indicator for CH3 under voltage event. |
| 4 | UV_LDO | Indicator for LDO under voltage event. |
| 3 | OT_IC | Indicator for PMIC over temperature event. |
| 2 | OV_VIN | Indicator for VIN over voltage event. |
| 1 | GATE_READY | Internal monitoring signal. (only for vendor) |
| 0 | PORB_VOUT | Internal monitoring signal. (only for vendor) |

## Application Information

The RT5091D is a total power management solution for SSDs (Solid State Drive) with dedicated input supply voltages of 3.3V or 5V. The RT5091D incorporates three high-efficiency synchronous buck regulators and one LDO that deliver several output voltages from a single power source. CH1 buck supports VID programming by either $I^2C$ interface or REFIN pin. And the output voltages of the rest two bucks, CH2 and CH3, can be programmed by resistor dividers or set with default voltage by connecting FB2 pin to VOUT2 node and FB3 pin to VOUT3 node. Output voltage of CH4 (LDO) can also be programmed by resistor divider or set with default voltage by floating FB4 pin.

PS3.5/PS4 power states function is available for both $I^2C$ interface, PS3P5 pin and $\overline{\text{STANDBY}}$ pin. If $I^2C$ interface is applied, PGOOD and UV can be monitored individually.

**Table 14. Detail of Power Rails**

| Resource Name | Type | Voltage Range | Current Rating |
|---|---|---|---|
| CH1 | Buck Converter | 0.7V to 1.3V, 10mV/step via $I^2C$ or Programmable by REFIN Pin | 4000mA |
| CH2 | Buck Converter | Programmable by FB2 Pin | 2000mA |
| CH3 | Buck Converter | Programmable by FB3 Pin | 2000mA |
| CH4 | LDO | Programmable by FB4 Pin | 300mA |

### Buck Converter

The RT5091D incorporates three high-efficiency synchronous switching buck converters that deliver programmable output voltages. They feature constant-on-time current mode for low output voltage, quick transient response, and low quiescent current. These buck converters also possess all standard protections.

Each switching regulator is specially designed for high-efficiency operation throughout the load range. With high switching frequency (2MHz), the external LC filter can be small and keeps very low output voltage ripple.

Additional features include soft-start, discharged, under-voltage protection, over-voltage protection, and over-current limiter. Please note that the PMIC will be latched when any power rail occurs under-voltage protection. The other protections just make the rail output voltage drop and recovery when the faults are reset. With $I^2C$ interface, system is allowed to control the wake up sequences, set rails' on/off states, switch to forced PWM mode/pulse-skipping mode (PSKIP), enter/leave sleep mode, and even directly program CH1 output voltage. Please check the register table for details.

### Buck Output Voltage Setting

The RT5091D provides three synchronous Buck regulators. CH1 buck converter features programmable output voltage by REFIN pin or 0.7V to 1.3V in 10mV/step via $I^2C$. If program CH1 output voltage by REFIN pin, the output voltage can be set by the following equation :

$$V_{CH1} = V_{REFIN} \times 1.6$$

And the $V_{REFIN}$ is setting by the reference resistors; $R_{REFOUT}$, $R_{REFADJ}$ and $R_{REFIN}$ (see Figure 1).

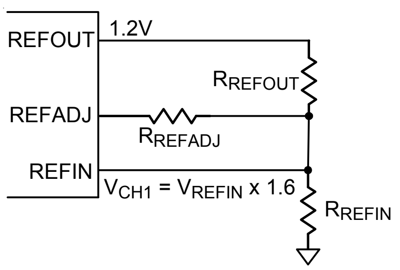



Figure 1. Setting REFIN Voltage with Reference Resistor Divider

When $\overline{\text{STANDBY}}$ goes high, $V_{REFIN}$ which in normal mode would equal to the equation below, where $V_{REFOUT}$ = 1.2V :

$$V_{REFIN} = V_{REFOUT} \times \frac{R_{REFIN}}{R_{REFIN} + R_{REFOUT}}$$

When $\overline{STANDBY}$ goes low, which also means PMIC is entering PS3.5 or PS4 power state, $V_{REFIN}$ which in sleep mode would become following equation :

$$V_{REFIN} = V_{REFOUT} \times \frac{R_{REFIN} // R_{REFADJ}}{(R_{REFIN} // R_{REFADJ}) + R_{REFOUT}}$$

Note that, if wants to keep $V_{REFIN}$ in sleep mode, ties REFADJ pin to GND and removes $R_{REFADJ}$.

If wants to program CH1 output voltage via $I^2C$, PMIC would need default output voltage setting for CH1 buck converter during power-up sequence. Thus following table has four sets of default output voltages for CH1 buck converter.

**Table 15. CH1 Buck Converter $V_{OUT}$ Default Setting**

| REFOUT | REFADJ | REFIN | CH1 $V_{OUT}$ |
|---|---|---|---|
| VIN | GND | GND | 0.9V |
| VIN | GND | VIN | 1.1V |
| VIN | VIN | GND | 1.2V |
| VIN | VIN | VIN | 1.0V |

Other buck converters, CH2 and CH3, feature programmable output voltages through resister divider. Output voltages can be adjusted by setting the feedback resistors, $R_{FB1}$ and $R_{FB2}$, see as Figure 2.

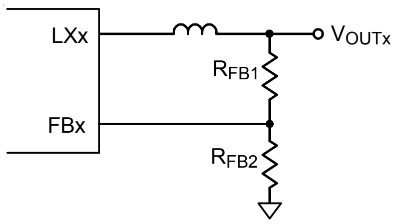



Figure 2. Setting CH2 and CH3 Voltage with Resistor Divider

And the relative equation is shown below, where $V_{FB}$ is 0.8V typically :

$$V_{OUT} = V_{FB} \times \frac{R_{FB1} + R_{FB2}}{R_{FB2}}$$

And please note that equivalent reactance from FB to GND, such as $R_{FB1}$ parallels to $R_{FB2}$, must NOT be less than 20kΩ for the application with external FB resistors.

Directly connect FB2 to CH2 output node to have a default output voltage 1.2V; FB3 to CH3 output node to have a default output voltage 1.8V.

**Buck Over-Current Limiter**

The over-current limit is implemented by using a cycle-by-cycle "valley" current detected control circuit, see as Figure 3. The switching current is monitored by measuring the low-side voltage between the LX pin and GND. The voltage is proportional to the switching current and the on-resistance of the low-side MOSFET.

When high-side MOSFET turn-on ($t_{ON}$), the high-side switching current increases at a linear rate and determines by $V_{IN}$, $V_{OUT}$, $t_{ON}$ and inductance. And when low-side MOSFET turn-on ($t_{OFF}$), the low-side switching current decreases linearly. The average value of the switching current is the output current loading. If the sensing voltage of the low-side MOSFET is above the voltage of current limiter threshold, the converter would keep the low-side turn on until the sensing voltage falls below the voltage of current limiter threshold and then starts a new switching cycle.

For the RT5091D buck converters, the low-side MOSFET are embedded and current limit threshold has defined in electrical characteristics.

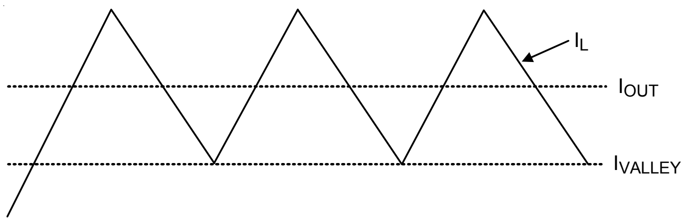



Figure 3. Cycle-By-Cycle "valley" Current Detected Control

**Buck Under-Voltage Protection**

If over-current limiter is activated, output voltage would drop and trigger under-voltage protection when it drops lower than 62.5% of reference voltage. In case of UVP mis-triggering, a de-glitch time is implemented. PMIC will turn off all power rails as long as any UVP is occurred and also pull low PGOOD pin. Note that UVP is a latched function in the RT5091D, thus can only be reset by starting over VIN POR.

### Buck Over-Voltage Protection

If output voltage exceeds 125% of reference voltage, over-voltage protection would be triggered. In case of OVP mis-triggering, a de-glitch time is implemented. PMIC will keep functional but pulling low PGOOD pin. The power rail which is under OVP will turn off its drivers until OVP indicator is released. PGOOD pin will back to high after all OVP indicators are released.

### Over-Temperature Protection

The over-temperature protection function of the RT5091D is built inside the PMIC to prevent overheat damage. If the die temperature is over 150°C, the OTP circuit would be activated and turn off all power rails of the RT5091D. PMIC will re-boot all power rails with power-up sequence after temperature cools down lower than 125°C.

### Linear Dropout Regulator

The RT5091D includes one high performance linear dropout regulator. The LDO has soft-start function. An internal current source charges an internal capacitor to make the soft-start ramp voltage. During the power up procedure, the output voltage tracks the internal voltage ramp for inrush current control.

If VIN UVLO occurs, or the output under-voltage fault latch is set, then the output discharge mode will be activated. During the discharge mode, an internal switch creates a path for discharging the output capacitors' residual charge to GND.

The LDO contains an independent current limiter and under-voltage protection circuit to prevent unexpected applications. The current limit circuit monitors the current from input to output by a current sensing circuit and controls the gate voltage of power stage. When the current is over the current limit threshold, the current limit circuit adjusts the gate voltage to constrain the output current. And if the output voltage is less than 60% of reference voltage, UVP circuit will shut down the LDO and latched. Note that this latched protection can only be reset by starting over VIN POR. The LDO feature programmable output voltage through resister divider. Output voltages can be adjusted by setting the feedback resistors, $R_{FB3}$ and $R_{FB4}$, see as Figure 4.

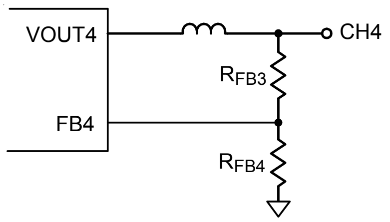



Figure 4. Setting LDO Voltage with Resistor Divider

And the relative equation is shown below, where $V_{FB}$ is 0.45V typically :

$$V_{OUT4} = V_{FB} \times \frac{R_{FB3} + R_{FB4}}{R_{FB4}}$$

Besides, the equivalent resistance from FB to GND must be less than 400kΩ for the application with external FB resistors.

Directly open VOUT4 to CH4 output node to have a default output voltage 1.8V.

### VSNS Discharge

When EXT_EN1 is disabled either through the sequence or through an $I^2C$ command, it activated the discharge resistor is placed between the VSNS and ground. Which means if system wants to discharge external regulator/ switch through VSNS by EXT_EN1, must connect VSNS to the output of external regulation/switch.

### Input OVP Deglitching

In order to prevent input OV is triggered by noise coupling, the RT5091D builds internal deglitching circuit to prevent unexpected triggering of VIN OVP.

If VIN is higher than VIN OVP threshold, where VIN OVP threshold level is selected by MODE pin, PMIC would turn off all power rails and external N-MOSFET to protect PMIC from being damaged by input over voltage.

### MODE

MODE is an input pin to select the threshold voltage of VIN for POR. If VIN voltage is above the threshold voltage, PMIC will begin to start up with power-up sequence. Set MODE = high for 5V VIN applications and MODE = low for 3.3V VIN applications.

## $I^2C$ Interface

The RT5091D $I^2C$ slave address = 0x1b (hex). $I^2C$ interface supports standard slave mode (100kbps), and fast mode (400kbps). The write or read bit stream (N ≥ 1) is shown as Figure 5.

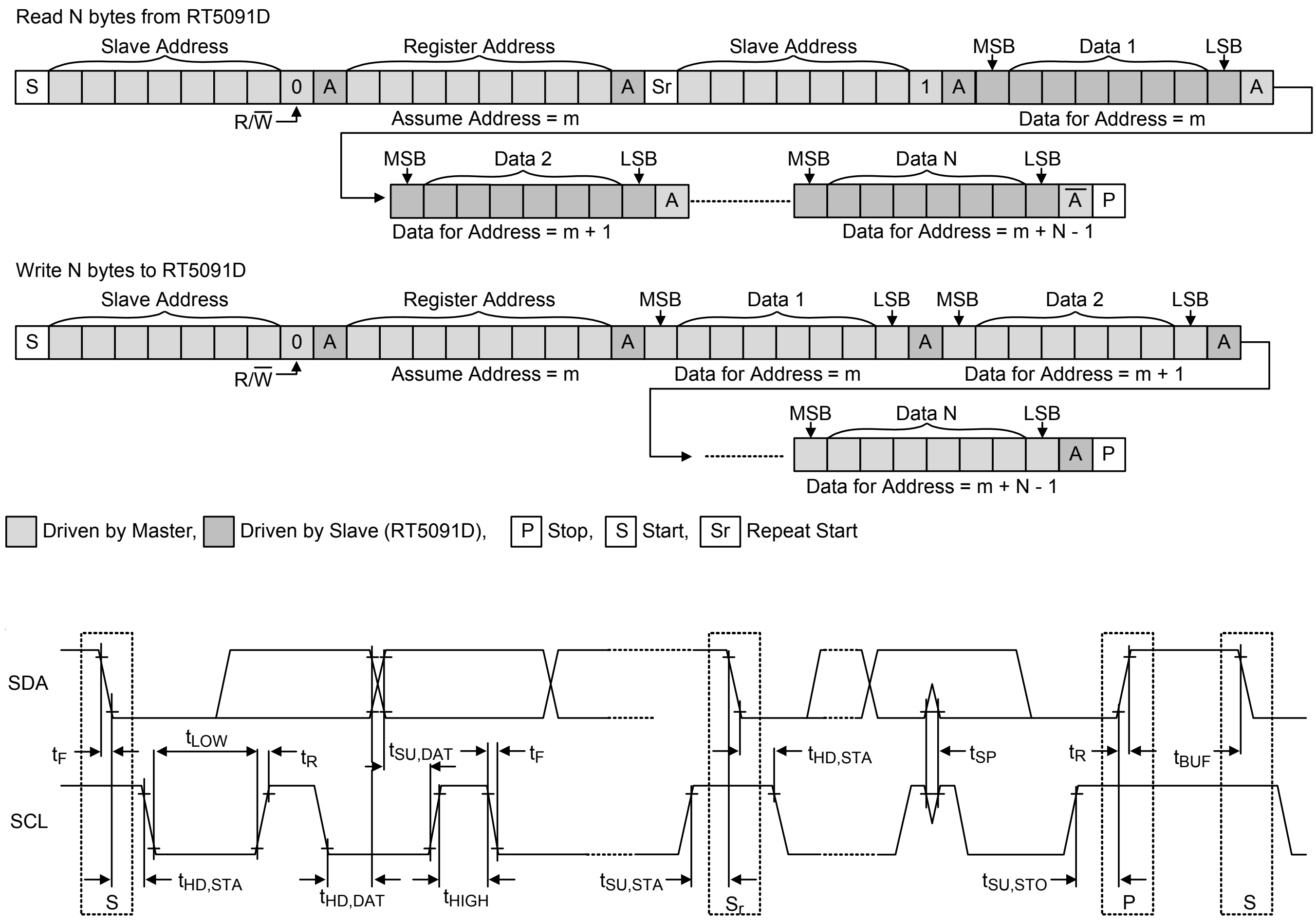



Figure 5. $I^2C$ Read and Write Stream and Timing Diagram

### Inductor Selection

For given input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and operation frequency ($f_{SW}$), the inductor value (L) determines the inductor ripple current ($\Delta I_L$) as shown in equation below :

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times L \times V_{IN}}$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors, but also the output voltage ripple.

A reasonable starting point for selecting the ripple current is $\Delta I_L$ = 0.3 x $I_{MAX}$ to 0.4 x $I_{MAX}$. The largest ripple current occurs at the highest $V_{IN}$. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{f_{SW} \times \Delta I_L \times V_{IN(MAX)}}$$

The current rating of the inductor must be large enough and will not saturate at the peak inductor current ($I_{PEAK}$) :

$$I_{PEAK} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

### $C_{IN}$ and $C_{SYS}$ Selection

The input capacitance of every rail, $C_{IN}$, needs to filter the trapezoidal current at the source of the high-side MOSFET. To prevent large ripple voltage, a low ESR input capacitor for the maximum current should be used. The relation between $C_{IN}$ ripple voltage and current ripple is shown as the Figure 6.

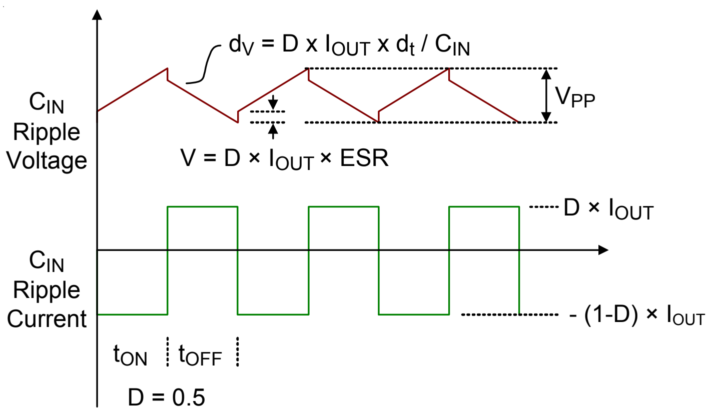



Figure 6. Relationship of $C_{IN}$ Voltage Ripple and Current Ripple

The $C_{IN}$ voltage ripple can use below equations to determine when $f_{SW}$ works at CCM mode.

$$V_{CIN\_PP} = D \times I_{OUT(MAX)} \times (ESR + \frac{(1-D)}{C_{IN} \times f_{SW}}$$

Where D = $V_{OUT}$ / $V_{IN}$. If use MLCC as the input current, the ESR is almost equal to zero. And the minimum input capacitance requirement could be estimate as below :

$$C_{IN(MIN)} = I_{OUT(MAX)} \times \frac{D \times (1-D)}{V_{CIN\_PP} \times f_{SW}}$$

Next, it needs to consider the input bulk capacitance, $C_{SYS}$, to ensure a stable input voltage during large load transient. The input host supply cannot typically provide the enough input current for the converter to respond to a fast transient current. The input bulk capacitor will provide the energy necessary to source current until the host supply fill the demand, as shown as Figure 7.

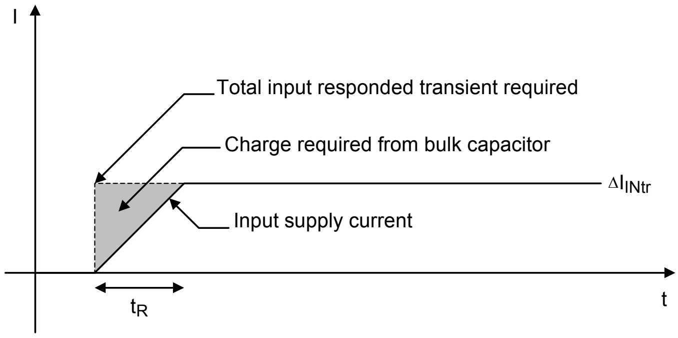



Figure 7. Charge Required from Input Bulk Capacitor During Transient

Figure 8 shows the diagram of every power rail of the RT5091D sharing a single bank of bulk input capacitors. It can calculate the input required transient current using following equation :

$$\Delta I_{INtrL} = \sum_{n=1}^{6} \frac{V_{OUTn} \times \Delta I_{OUTn(MAX)}}{V_{IN} \times \eta_n}$$

Where $\Delta I_{INtr}$ is the total input transient current required. $\Delta I_{OUT}$ is the maximum output transient current. $\eta$ is the efficiency of the Buck at $I_{OUT(MAX)}$.

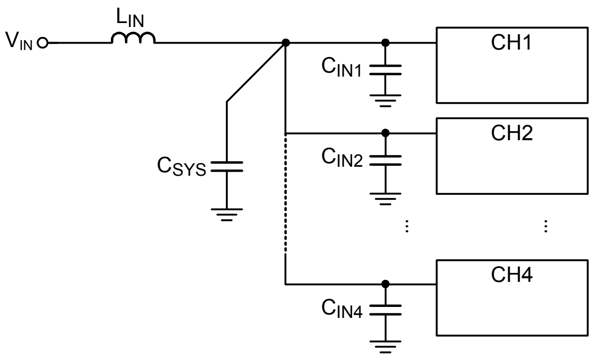



Figure 8. The Location of Bulk Input Capacitance Diagram

When $\Delta I_{INtr}$ is confirmed, the input bulk capacitance, $C_{SYS}$, can be decided with following estimating equation :

$$C_{SYS(MIN)} \cong \frac{1.21 \times \Delta I_{INtr}^2 \times L_{IN}}{\Delta V_{INPP(MAX)}^2}$$

where $\Delta V_{INPP(MAX)}$ is the maximum ac voltage allowable. $L_{IN}$ is the input series filter inductance, if not used, put a reasonable value 50nH due to PCB layout.

### $C_{OUT}$ Selection

The output capacitor and the inductor are used form a low pass filter in the buck topology. In steady state condition, the ripple current flowing into/out of the capacitor results in ripple voltage. The output voltage ripple ($\Delta V_{OUTPP}$) can be calculated by the following equation :

$$\Delta V_{OUTPP} = \Delta I_L \left( ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right)$$

When load transient occurs, the output capacitor supplies the load current before the controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage under-shoot ($V_{SAG}$) can be calculated by the following equation :

$$V_{SAG} = \Delta I_{LOAD} \times ESR$$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore, the ESL contributes to part of the voltage sag. Using a capacitor with low ESL can obtain better transient performance. Generally, using several capacitors connected in parallel can have better transient performance than using a single capacitor for the same total ESR.

Unlike the electrolytic capacitor, the ceramic capacitor has relatively low ESR and can reduce the voltage deviation during load transient. However, the ceramic capacitor can only provide low capacitance value.

Therefore, use a mixed combination of electrolytic capacitor and ceramic capacitor to obtain better transient performance.

### Serial Data Transfer Format in Hs-Mode

Serial data transfer format in Hs-mode meets the Standard-mode $I^2C$-bus specification. Hs-mode can only commence after the following conditions (all of which are in F/S-mode) :

- START condition (S)
- 8-bit master code (00001xxx)
- not-acknowledge bit ( A# )

Figures 8 and Figure 10 show this in more detail. This master code has two main functions :

- It allows arbitration and synchronization between competing masters at F/S-mode speeds, resulting in one winning master.
- It indicates the beginning of an Hs-mode transfer.

Hs-mode master codes are reserved 8-bit codes, which are not used for slave addressing or other purposes.

Furthermore, as each master has its own unique master code, up to eight Hs-mode masters can be present on the one $I^2C$-bus system (although master code 0000 1000 should be reserved for test and diagnostic purposes). The master code for an Hs-mode master device is software programmable and is chosen by the System Designer.

Arbitration and clock synchronization only take place during the transmission of the master code and not-acknowledge bit (A#), after which one winning master remains active. The master code indicates to other devices that an Hs-mode transfer is to begin and the connected devices must meet the Hs-mode specification. As no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge (A#).

After the not-acknowledge bit (A#), and the SCLH line has been pulled-up to a HIGH level, the active master switches to Hs-mode and enables (at time $t_H$, see Figure

10) the current-source pull-up circuit for the SCLH signal. As other devices can delay the serial transfer before $t_H$ by stretching the LOW period of the SCLH signal, the active master will enable its current-source pull-up circuit when all devices have released the SCLH line and the SCLH signal has reached a HIGH level, thus speeding up the last part of the rise time of the SCLH signal.

The active master then sends a repeated START condition (Sr) followed by a 7-bit slave address (or 10-bit slave address) with an R/W bit address, and receives an acknowledge bit (A#) from the selected slave.

After a repeated START condition and after each acknowledge bit (A#) or not-acknowledge bit (A#), the active master disables its current-source pull-up circuit. This enables other devices to delay the serial transfer by stretching the LOW period of the SCLH signal. The active master re-enables its current-source pull-up circuit again.

When all devices have released and the SCLH signal reaches a HIGH level, and so speeds up the last part of the SCLH signal's rise time. Data transfer continues in Hs-mode after the next repeated START (Sr), and only switches back to F/S-mode after a STOP condition (P). To reduce the overhead of the master code, it's possible that a master links a number of Hs-mode transfers, separated by repeated START conditions (Sr).

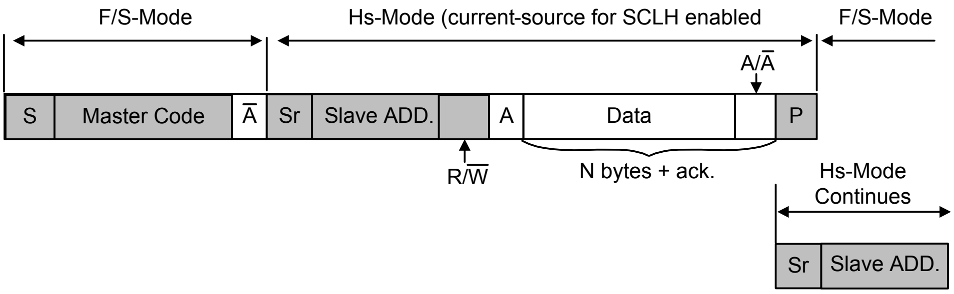



Figure 9. Data Transfer Format in Hs-Mode

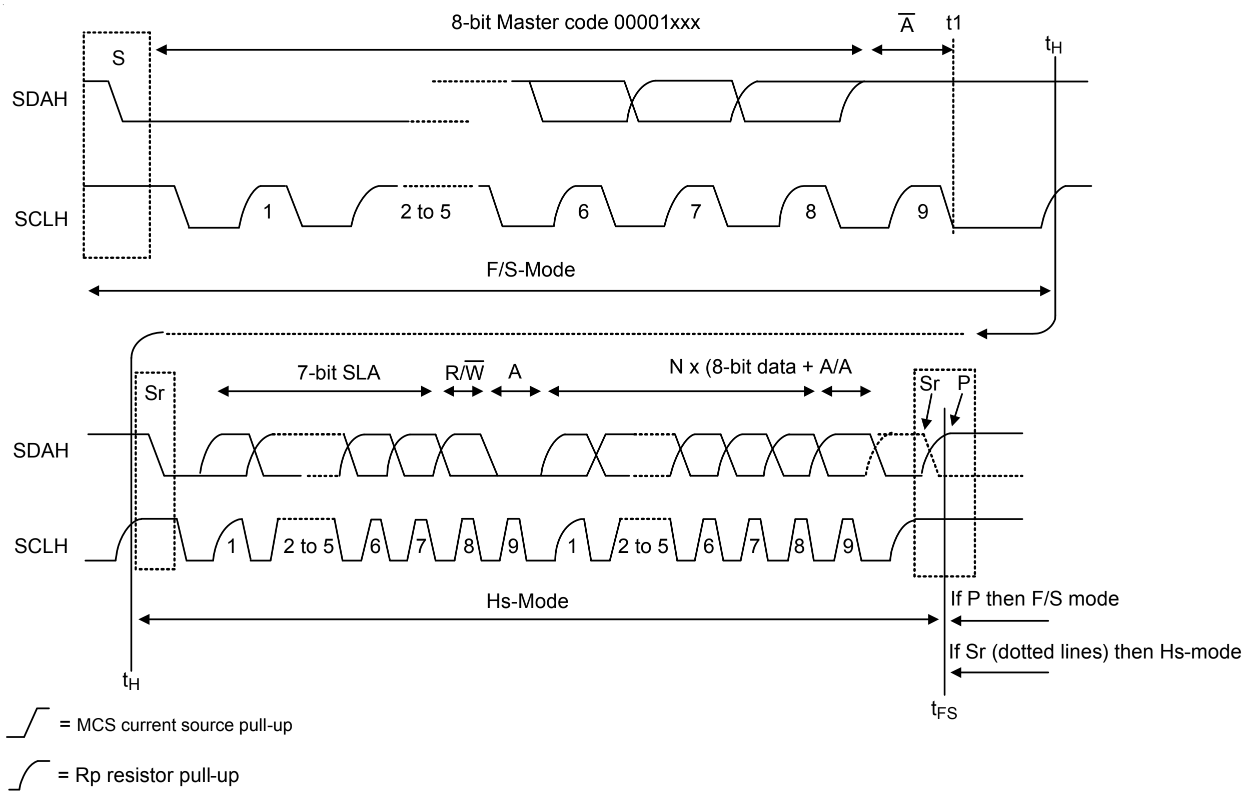



Figure 10. A Complete Hs-Mode Transfer

### Power On/Off Sequence

The RT5091D starts a power up sequence when VIN > RESET rising threshold voltage, and the device shuts down with VIN < UVLO falling threshold voltage. The RT5091D applies PS3.5 and PS4 power states of PMIC to save power consumption with setting the PS3P5 to high for PS3.5 power state or low for PS4 power state before $\overline{\text{STANDBY}}$ goes to low. If the device goes to PS3.5 power state by PS3P5 goes to high then $\overline{\text{STANDBY}}$ to low, almost power rails still alive but CH1 goes to sleep mode form normal mode. If the device goes to PS4 power state by PS3P5 goes to low then $\overline{\text{STANDBY}}$ to low, all power rails set to sleep mode and the alive rails depend on sleep mode control register setting. The power rails will exit from sleep mode to normal mode and wake up with a sequence as the same as the power-up-sequence when $\overline{\text{STANDBY}}$ goes to high. Please note that when PMIC starts a power up sequence, sleep mode operation would not work until 5ms later. The relations of all power rails of the RT5091D and Normal/PS3.5/PS4 power states sequence are shown as Figure 12. The following Table 16 is the power states and active rails mode in each power state.

### Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA}$, is highly package dependent. For a WQFN-32L 4x4 package, the thermal resistance, $\theta_{JA}$, is 27.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A$ = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (27.8°C/W) = 3.59W for a WQFN-32L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA}$. The derating curves in Figure 11 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

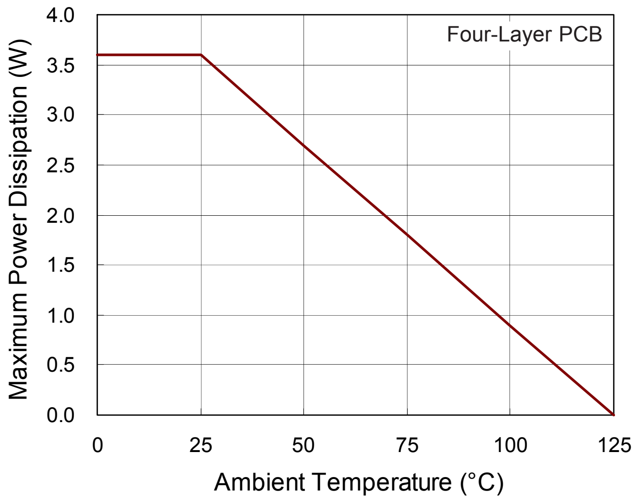



Figure 11. Derating Curve of Maximum Power Dissipation

**Table 16. Power States and Active Rails Mode in Each Power State**

| Power State | Signals to PMIC | | Active Rails Mode in Each Power State | | | | | |
|---|---|---|---|---|---|---|---|---|
| | $\overline{\text{STANDBY}}$ | PS3P5 | CH1 | CH2 | CH3 | CH4 | EXT-EN1 | EXT-EN2 |
| Normal | H | H / L | Normal | Normal | Normal | Normal | Normal | Normal |
| PS3.5 | L | H | Sleep | Normal | Normal | Normal | Normal | Normal |
| PS4 | L | L | Sleep | Off | Off | Normal | Off | Off |

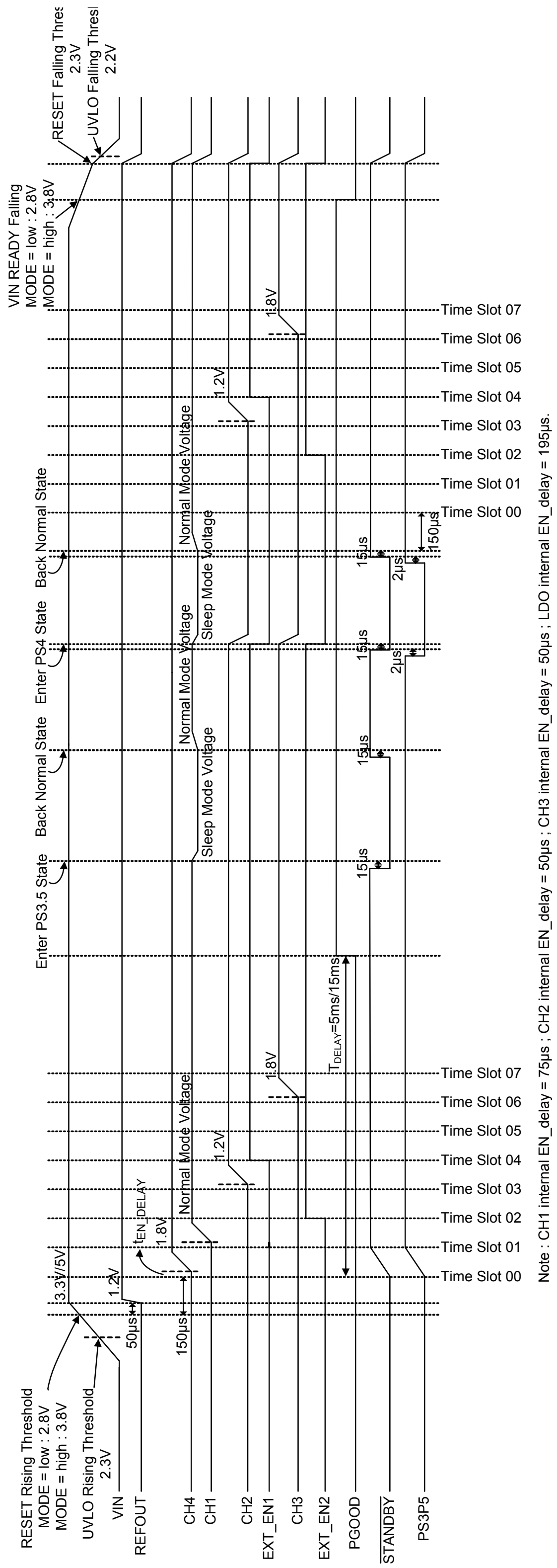
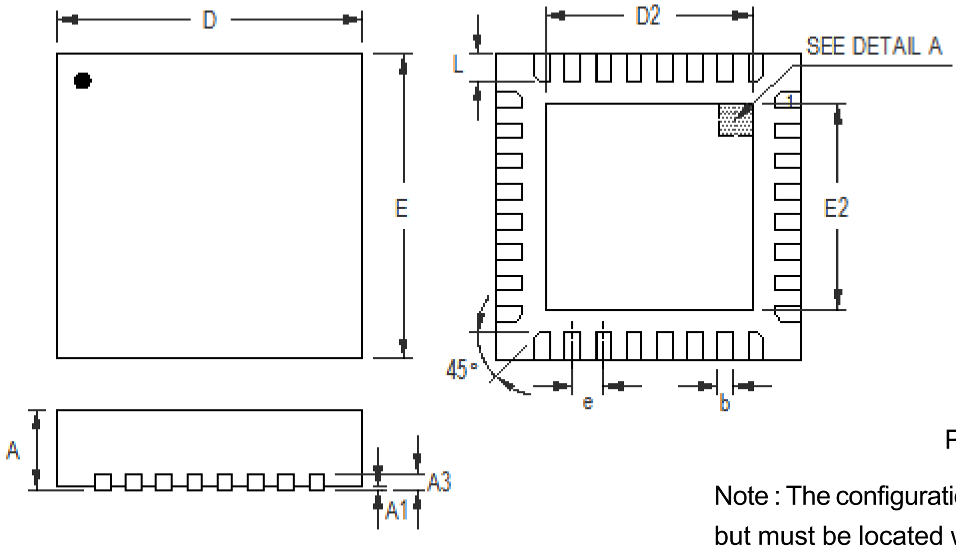
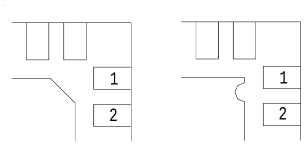



Figure 12. Power Up/Off Sequence and Sleep Off/Wake Up Sequence

## Outline Dimension




**DETAIL A**

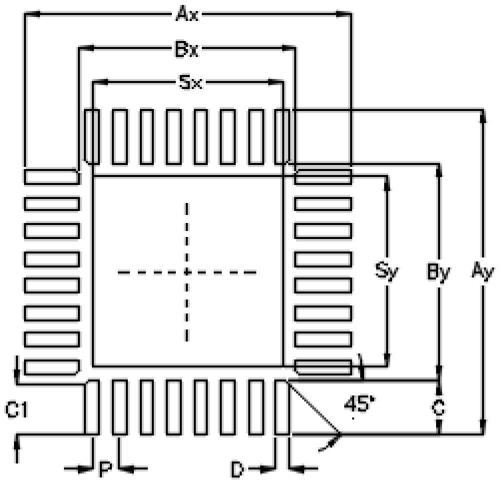
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| D | 3.900 | 4.100 | 0.154 | 0.161 |
| D2 | 2.650 | 2.750 | 0.104 | 0.108 |
| E | 3.900 | 4.100 | 0.154 | 0.161 |
| E2 | 2.650 | 2.750 | 0.104 | 0.108 |
| e | 0.400 | | 0.016 | |
| L | 0.300 | 0.400 | 0.012 | 0.016 |

**W-Type 32L QFN 4x4 Package**

## Footprint Information




| Package | Number of Pin | Footprint Dimension (mm) | | | | | | | | | | Tolerance |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | P | Ax | Ay | Bx | By | C*32 | C1*8 | D | Sx | Sy | |
| V/W/U/XQFN4*4-32 | 32 | 0.40 | 4.80 | 4.80 | 3.20 | 3.20 | 0.80 | 0.75 | 0.20 | 2.80 | 2.80 | ±0.05 |

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