RICHTEK®

RT4823Q

Wide Input and Ultra-Low Quiescent Current Boost Converter with High Efficiency

1 General Description

The RT4823Q is a boost converter designed to provide a minimum output voltage from a single-cell Li-Ion battery, even when the battery voltage is below the system minimum. The RT4823Q allows systems to take advantage of new battery chemistries that can supply significant energy even when the battery voltage is lower than the required voltage for system power ICs. By combining built-in power transistors, synchronous rectification, and low supply current, this IC provides a compact solution for systems using advanced Li-Ion battery chemistries.

In boost mode, output voltage regulation is guaranteed up to a maximum load current of 1500mA. Quiescent current in shutdown mode is less than 1μA, which maximizes battery life. The regulator transitions smoothly between bypass and normal boost mode. The device can be forced into bypass mode to reduce quiescent current.

The RT4823Q is available in the WL-CSP-9B 1.3x1.2 (BSC) package. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

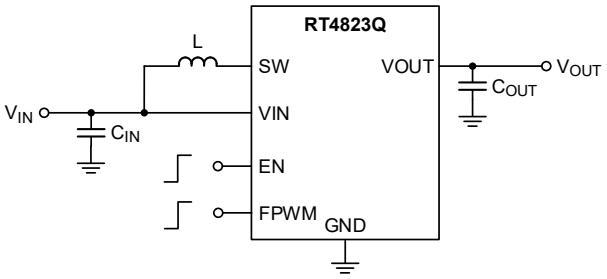
2 Applications

- NFC Device Power Supply
- USB Charging Ports
- PC Accessory Applications
- TWS (True Wireless Stereo) Hall Sensors
- Gaming Device Sensors

3 Features

- **Ultra-Low Operating Quiescent Current**
- **Quick Start-Up Time (< 430μsec)**
- **Few External Components Needed: A 1μH Inductor, A 0402 Case Size Input Capacitor, and A 0603 Case Size Output Capacitor**
- **Input Voltage Range: 1.8V to 5.5V**
- **Support V_{IN} > V_{OUT} Operation**
- **Default Boost Output Voltage Setting: V_{OUT} = 5V**
- **Maximum Continuous Load Current: 1.5A at V_{IN} > 3V Boosting V_{OUT} to 5V**
- **Up to 93% Efficiency**
- **EN(H), FPWM(H): Forced PWM Mode**
- **EN(H): Boost Mode**
- **EN(L): Shutdown Mode**
- **Internal Synchronous Rectifier**
- **Overcurrent Protection**
- **Cycle-by-Cycle Current Limit**
- **Overvoltage Protection**
- **Short-Circuit Protection**
- **Over-Temperature Protection**
- **Small WL-CSP-9B 1.3x1.2 (BSC) Package**

4 Simplified Application Circuit



5 Ordering Information

RT4823Q □

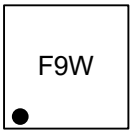
└Package Type (1)

WSC : WL-CSP-9B 1.3x1.2 (BSC)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information



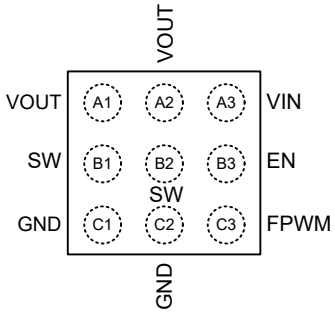
F9: Product Code

W: Date Code

Table of Contents

7 Pin Configuration

(TOP VIEW)

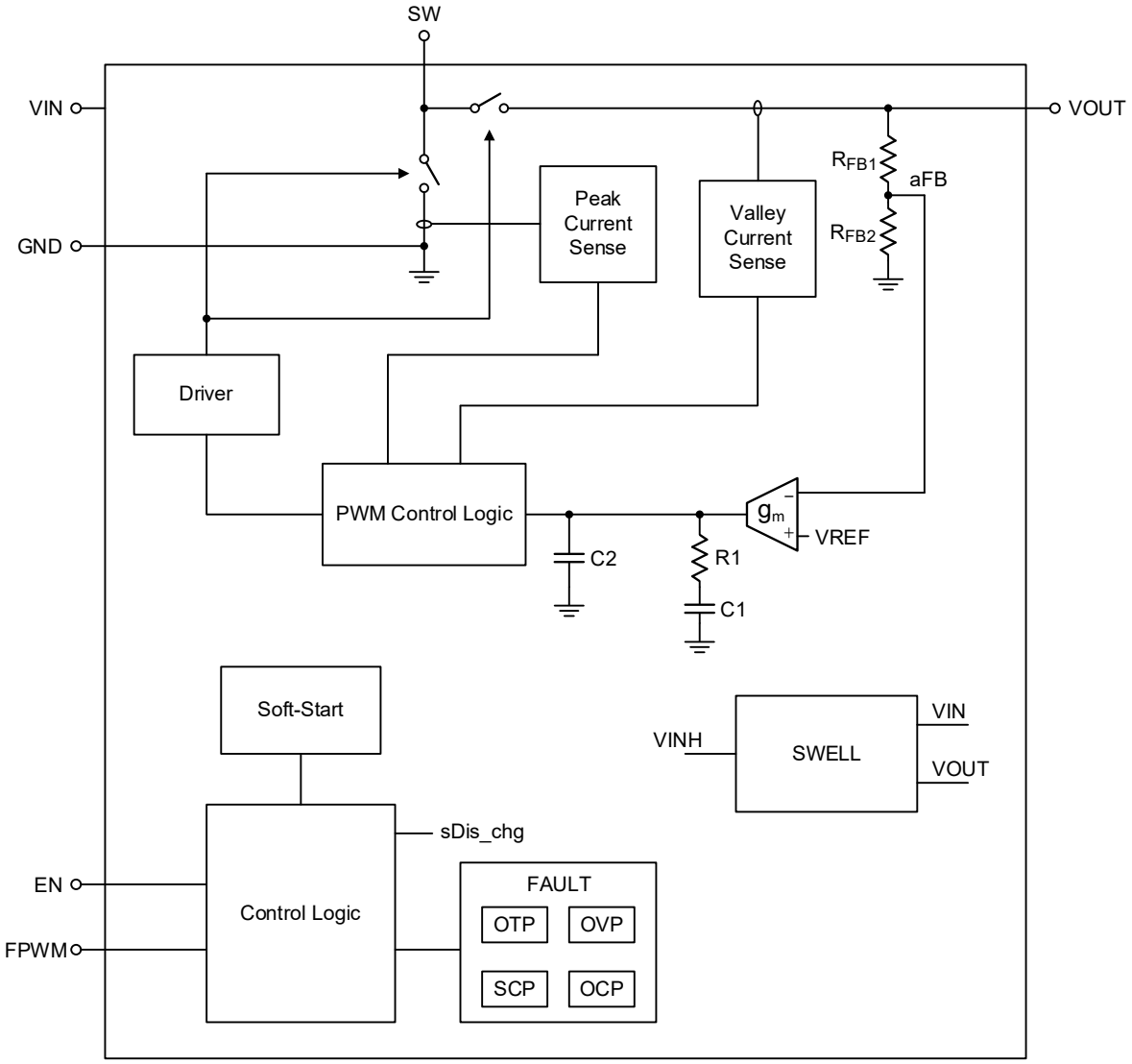


WL-CSP-9B 1.3x1.2 (BSC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
A1, A2	VOUT	Output voltage. Place C_{OUT} as close as possible to the device.
A3	VIN	Input voltage. This pin must be connected to the input power supply. It is used to provide internal power to the chip.
B1, B2	SW	Switching node. The power inductor should be connected between the SW and the power input.
B3	EN	Enable. When this pin is set to HIGH, the circuit is enabled. Do not leave this pin floating.
C1, C2	GND	Ground. This is the power and signal ground reference for the chip. The C_{OUT} bypass capacitor should be connected to these pins with the shortest path possible.
C3	FPWM	Force PWM mode. This pin is used to control the converter into forced PWM mode. When this pin is set to HIGH, the circuit enters FPWM mode. Do not leave this pin floating.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN, VOUT, SW, EN, FPWM ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
- WL-CSP-9B 1.3x1.2 (BSC) ---------- 1.54W
- Package Thermal Resistance (Note 3)
- WL-CSP-9B 1.3x1.2 (BSC) ---------- 64.9°C/W
- Lead Temperature (Soldering, 10 sec.)---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-9 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Input Voltage Range (Boost Mode) ---------- 1.8V to 5.5V
- Output Voltage Range ---------- 5V
- Input Capacitor, CIN ---------- 4.7µF
- Output Capacitor, COUT ---------- 3.5µF to 50µF
- Inductance, L ---------- 0.7µH to 2.2µH
- Input Current (Average current into SW) ---------- 1.8A
- Input Current (Peak current into SW)---------- 4A
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{IN} = 3.6V, C_{IN} = 4.7µF, C_{OUT} = 10µF, L1 = 1µH. All typical (Typ) limits apply for T_A = 25°C, unless otherwise specified. All minimum (Min) and maximum (Max) apply over the full operating ambient temperature range (–40°C ≤ T_A ≤ 85°C).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply						
VIN Operation Range	V_{IN}		1.8	--	5.5	V
Into VIN Operating Quiescent Current	I_{Q_NSW}	I_{OUT} = 0mA, V_{IN} = 3.6V, EN = FPWM = GND	--	0.1	0.5	µA
Into VOUT Standby Mode Quiescent Current	I_{Q_NSW}		--	2	3	µA
VIN Quiescent Current (Device Normal Switching)	I_{Q_SW}	V_{IN} = 3.6V, V_{OUT} = 5V, FPWM = EN = GND	--	--	1	µA
		V_{IN} = 3.6V, V_{OUT} = 5V, FPWM = GND, EN = VIN	--	4	6	
		V_{IN} = 3.6V, V_{OUT} = 5V, FPWM = EN = VIN	--	10	--	mA
Power-On Reset	V_{POR}		1.2	1.5	1.75	V
Enable, FPWM						
Low-Level Input Voltage	V_{IL}		--	--	0.4	V
High-Level Input Voltage	V_{IH}		1.2	--	--	V
Input Leakage Current	I_{LK}	Input connected to GND or VIN	--	--	0.5	µA
Output						
Regulated DC Output Voltage	V_{OUT}	1.8V ≤ V_{IN} ≤ 4.8V, I_{OUT} = 0mA, PFM operation	5.04	5.06	5.08	V
		V_{IN} = 3.6V, I_{OUT} = 1A, PWM operation	4.95	5	5.05	V
Power Switch						
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	80	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	80	--	mΩ
Minimum On-Time	t_{ON_MIN}	V_{IN} = 1.8V to 4.8V, V_{OUT} = 5V	20	--	60	ns
Maximum Duty Cycle	D_{MAX}	V_{IN} = 1.8V, V_{OUT} = 5V, I_L = 400mA	68.8	--	--	%
Switch Peak Current Limit (V_{IN} or V_{OUT} > 2.2V)	I_{LIM_PEAK}	V_{IN} = 3.6V, V_{OUT} = 5V	--	4000	--	mA
Switch Valley Current Limit (V_{IN} or V_{OUT} > 2.2V)	I_{LIM_VALLEY}	V_{IN} = 3.6V, V_{OUT} = 5V	--	3700	--	mA
Negative OCP	I_{LIM_NEG}		–3	–2	–1	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator						
Oscillator Frequency	f_{OSC}	V_{IN} = 3.6V	3	3.5	4	MHz
		V_{IN} < 2.5V → start to reduce frequency	2	--	--	
Soft-Start						
Start-Up Time	t_{START_BST}	V_{IN} = 3.6V, BP = GND, I_{OUT} = 0mA. Time from active EN to VOUT	130	430	550	μs
Pre-Charge Current Limit	I_{LIM_PRE}	V_{IN} = 3.6V, EN = 0 → 1.8V	250	300	350	mA
Protection						
Short-Circuit Protection	V_{SCP}		0.5	0.7	0.9	V
Over-Temperature Protection	T_{OTP}		140	150	160	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
Overcurrent Protection	I_{OCP}	V_{IN} = 5V	4	5	5.5	A
Efficiency						
Efficiency	η	V_{OUT} = 5V, V_{IN} = 3.6V, Load = 10μA	--	72	--	%
		V_{OUT} = 5V, V_{IN} = 3.6V, Load = 10mA	--	90	--	
		V_{OUT} = 5V, V_{IN} = 3.6V, Load = 600mA	--	93	--	
		V_{OUT} = 5V, V_{IN} = 3.6V, Load = 1000mA	--	91	--	

13 Typical Application Circuit

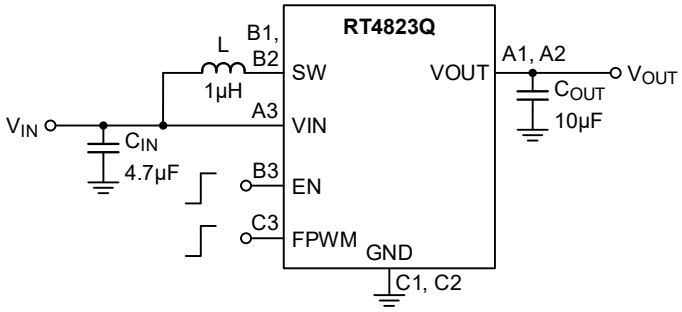
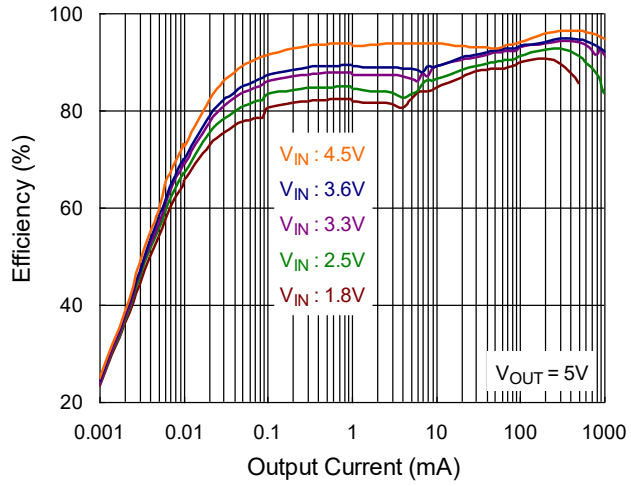


Table 1. Recommended Components Information

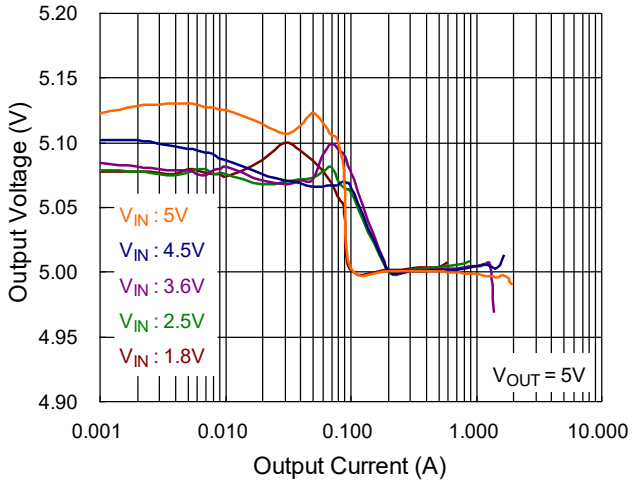
Reference	Part Number	Description	Package	Manufacturer
C_{IN}	GRM155R60J475ME47D	4.7µF/6.3V/X5R	0402	Murata
C_{OUT}	GRM188R60J106ME47D	10µF/6.3V/X5R	0603	Murata
L	DFE252012F-1R0M=P2	1.0µH/3.3A	2.5x2.0x1.2mm	Murata

14 Typical Operating Characteristics

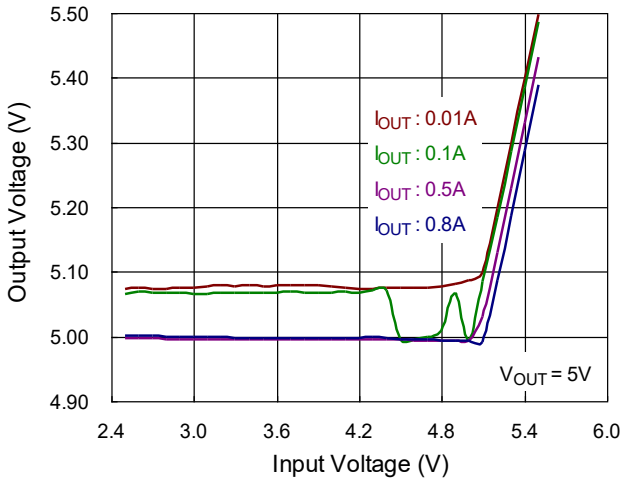
Efficiency vs. Output Current



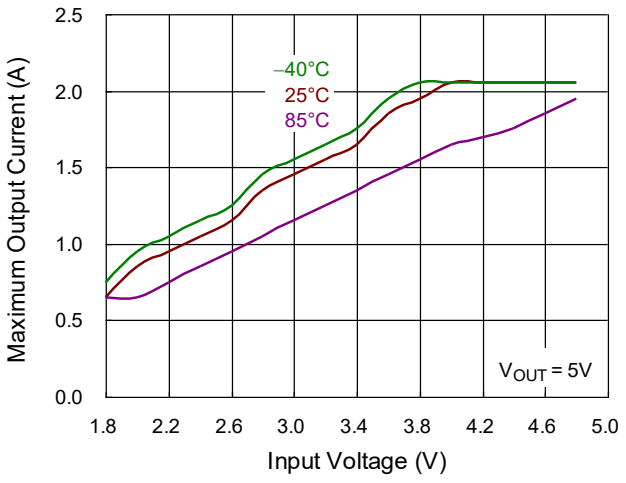
Boost Load Regulation



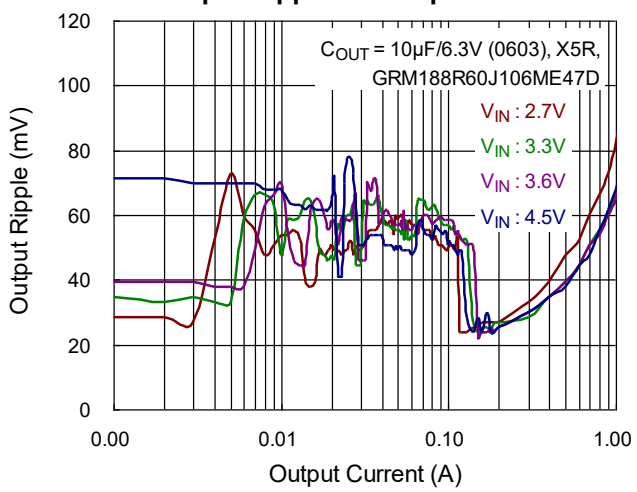
Boost Line Regulation



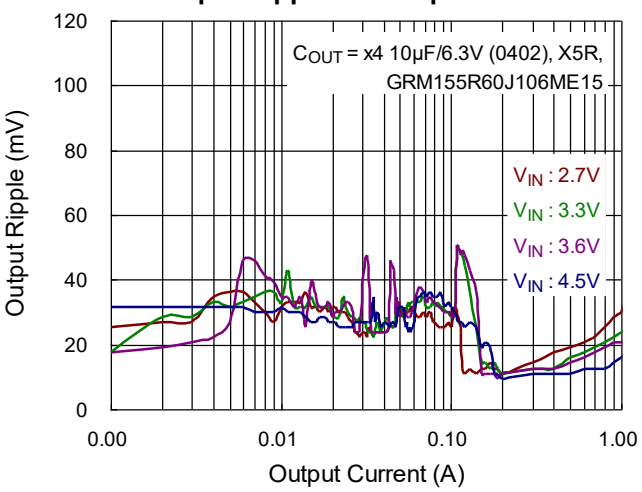
Maximum Output Current vs. Input Voltage



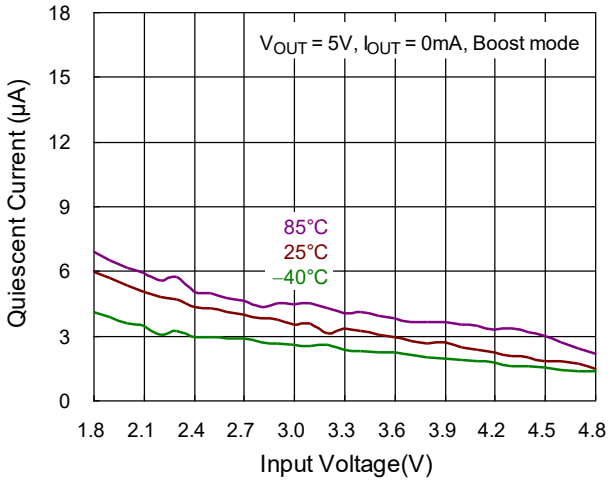
Output Ripple vs. Output Current



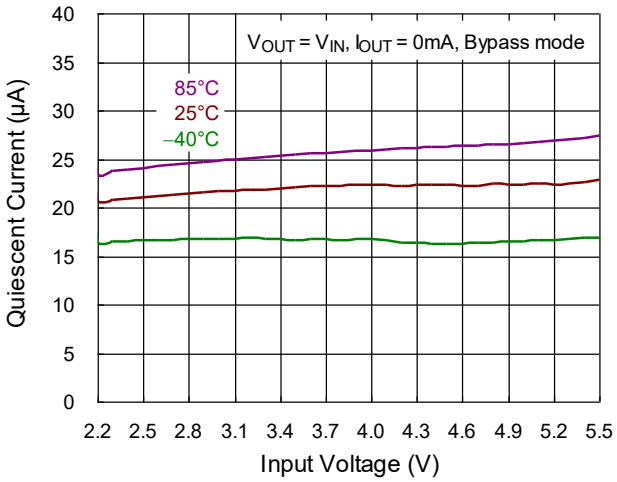
Output Ripple vs. Output Current



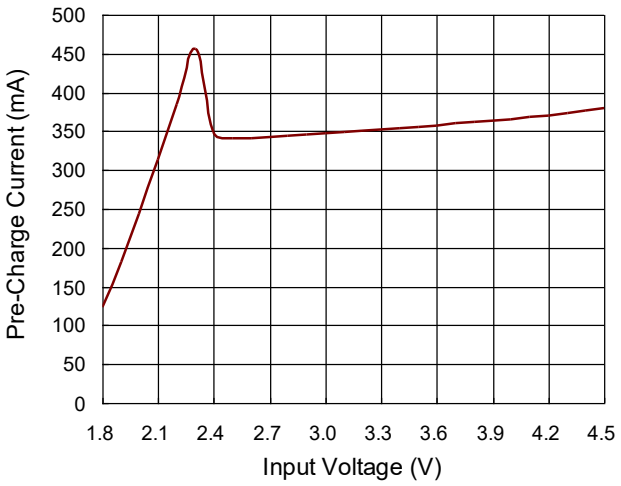
Quiescent Current vs. Input Voltage



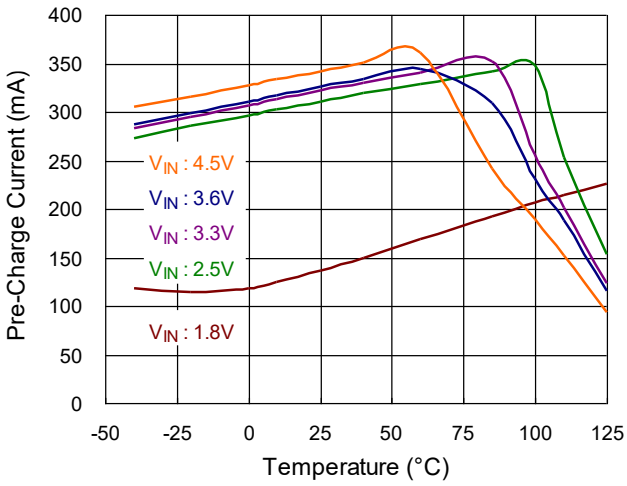
Quiescent Current vs. Input Voltage



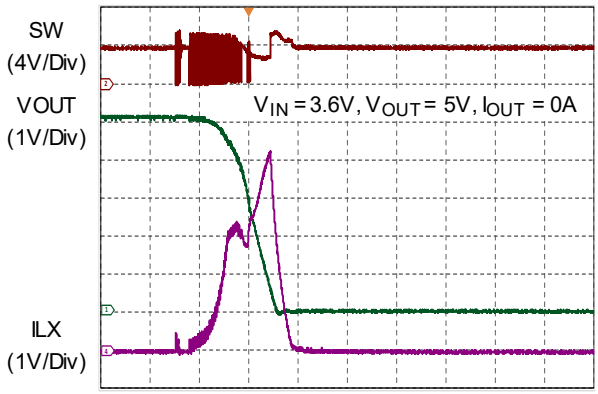
Pre-Charge Current vs. Input Voltage



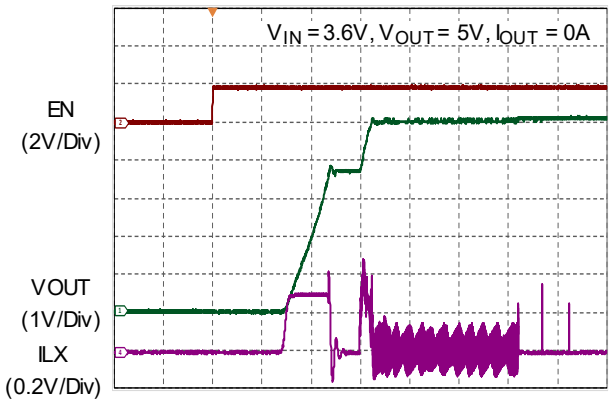
Pre-Charge Current vs. Temperature



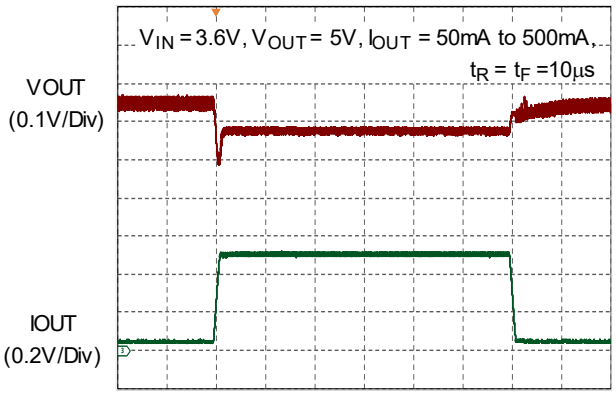
Boost Short Circuit



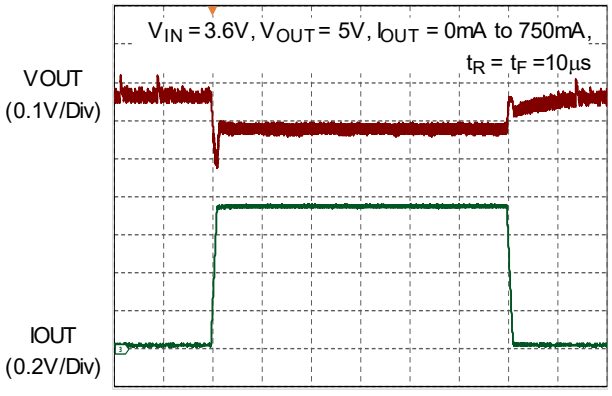
Power-On



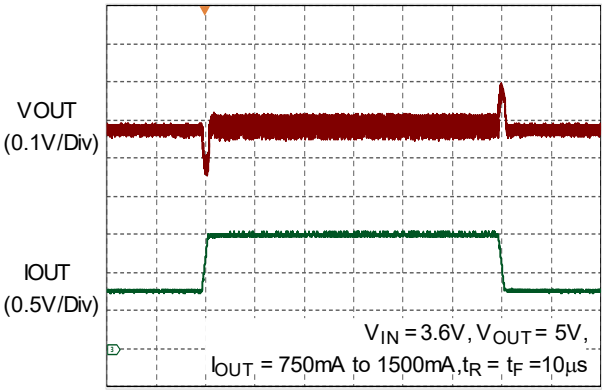
Load Transient



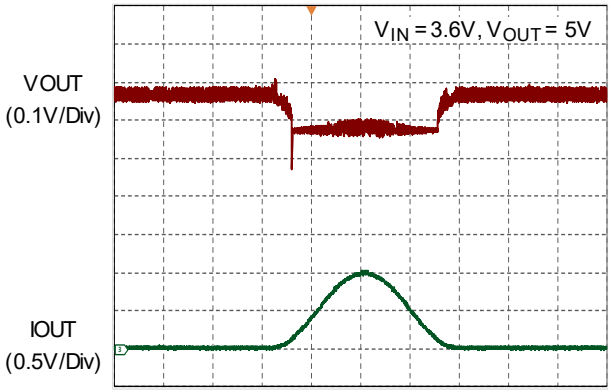
Load Transient



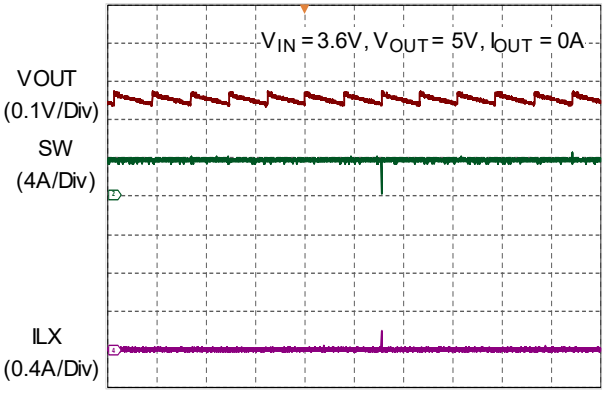
Load Transient



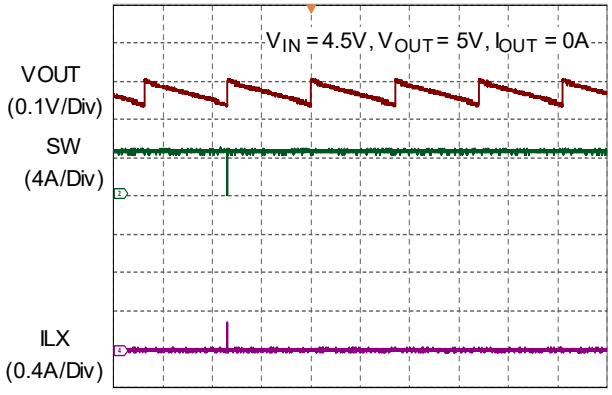
Sine Waveform Stability



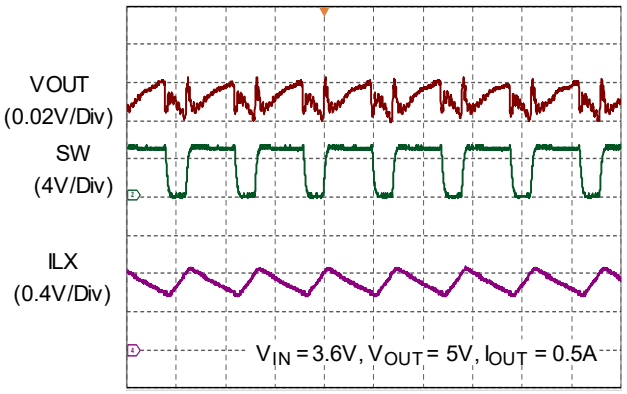
PFM Output Ripple



PFM Output Ripple

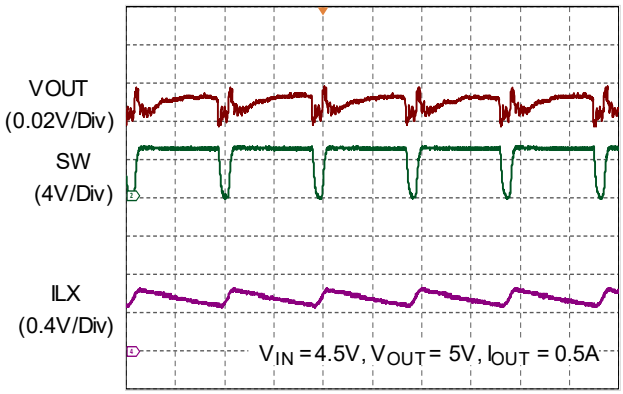


PWM Output Ripple



Time (0.0002ms/Div)

PWM Output Ripple



Time (0.0002ms/Div)

15 Operation

The RT4823Q combines built-in power transistors, synchronous rectification, and low supply current, providing a compact solution for systems using advanced Li-Ion battery chemistries.

In boost mode, output voltage regulation is guaranteed up to a maximum load current of 1.5A. Quiescent current in shutdown mode is less than 1μA, which maximizes battery life.

15.1 Power-On Reset

If the input voltage is lower than the POR threshold, the internal digital and analog circuits are disabled. If the input voltage is higher than the POR threshold, the boost converter behaves as follows:

1. The IC digital circuit is activated.
2. After the EN pin is turned on, internal registers start to load the default value via eFuse.
3. The boost converter enters free-running mode (details in the free-running mode section).
4. If VOUT > 2.2V (or VIN > 2.2V), the boost converter will enter closed-loop control.

Figure 1 and Figure 2 show the eFuse download diagram and flow chart. When the input voltage is higher than the POR threshold and EN goes high, eFuse starts to load in the digital circuit. The deglitch time is 3μs to 15μs (maximum), and the eFuse download time is 16μs to 24μs (maximum). When eFuse data starts to download, the RT4823Q internal circuit ensure the download progress is completed unless VIN < POR threshold.

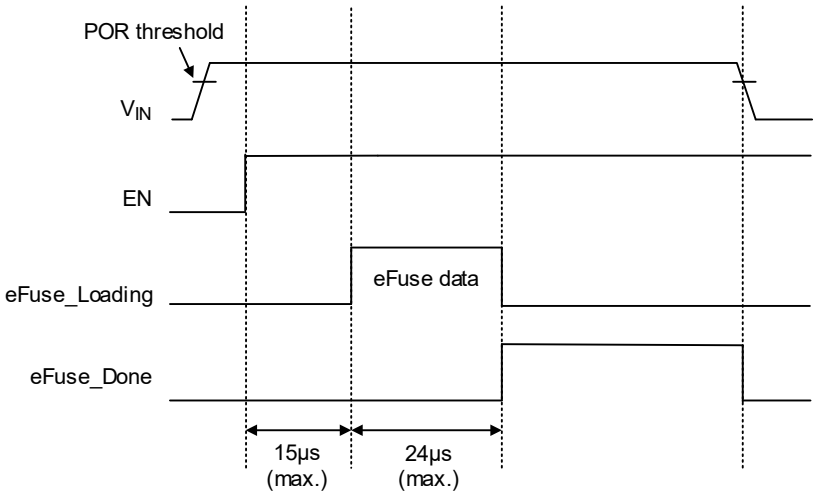


Figure 1. eFuse Download Timing Diagram

15.2 Free-Running Mode

If both VIN and VOUT are lower than 2.2V, the boost converter will enter free-running mode. In this mode, the switching frequency is 1.5MHz and the duty cycle of the boost converter is 25%. This is the power-on stage, and a current limit function is implemented for converter soft-start. The current limit level should be lower than 900mA.

15.3 EN and FPWM

As shown in Table 2, there are three device states in the RT4823Q. When both EN and FPWM are pulled low, the device enters shutdown mode and the quiescent current is less than 1μA. If EN is pulled high, the RT4823Q enters boost mode with low quiescent operation. When the RT4823Q is in boost mode and FPWM is pulled high, the RT4823Q enters FPWM mode. There should be a delay time (< 250μs) from when EN is pulled high to when power is ready to guarantee normal operation.

Table 2. Pin Configuration for Converter

EN Input	FPWM Input	Mode Define	Device State
0	0	Shutdown mode	The device is shut down. The device shutdown current is approximately about 1μA (maximum).
1	0	Boost PFM	The device is active in Boost PFM low quiescent mode. The supply current is approximately 4μA (typical).
1	1	Boost PWM	The device is in force PWM mode.

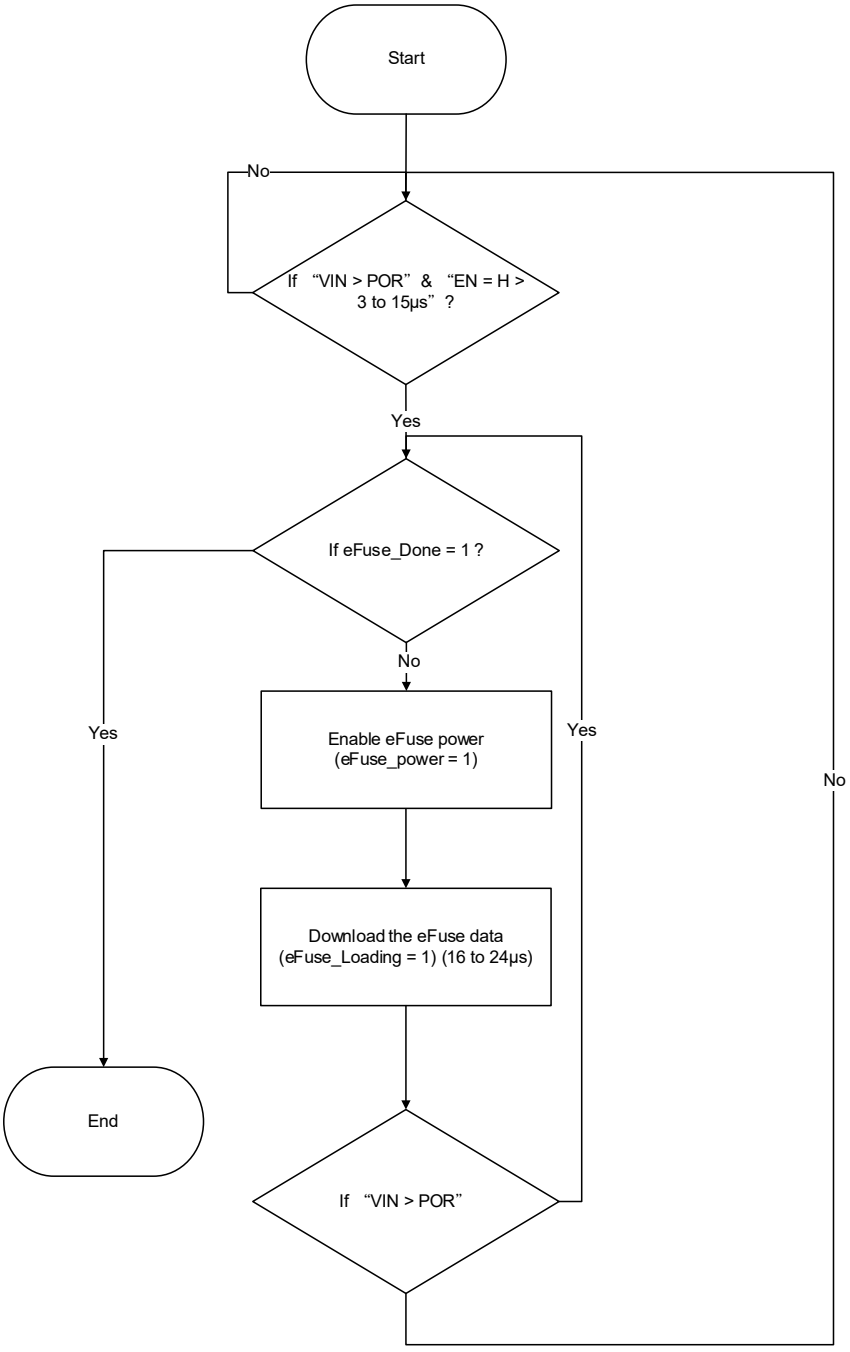


Figure 2. eFuse Download Flow Chart

15.4 Enable

The boost converter can be enabled or disabled using the EN pin. When the EN pin voltage is higher than the logic-high threshold, the device starts operating according to the operation diagram shown in Figure 2. In shutdown mode, the converter stops switching, and the internal control circuit is turned off. The output voltage discharges through component consumption (e.g., capacitor ESR), as there is no dedicated discharge function in this state.

15.5 Soft-Start State

During the soft-start state, if VOUT reaches 99% of V_{OUT_Target}. The RT4823Q will enter boost operation. When the system powers on with heavy loading (higher than pre-charge current), the RT4823Q remains in the pre-charge state until the load is released.

15.6 Boost/Auto Bypass Mode

There are two normal operation modes: boost mode and auto bypass mode. In boost mode (V_{IN} – 0.3V < V_{OUT_Target}), the converter boosts the output voltage to V_{OUT_Target}, delivering power to the load through internal synchronous switches after the soft-start state. In auto bypass mode (V_{IN} – 0.3V ≥ V_{OUT_Target}), the input voltage is delivered directly to the output terminal, providing maximum current capacity with the RT4823Q. Detailed information is shown below.

15.7 Boost Mode (Auto PFM/PWM Control Method)

To save power and improve efficiency at low loads, the boost converter operates in PFM (Pulse Frequency Modulation) as the inductor drops into DCM (Discontinuous Current Mode). The switching frequency is proportional to the load to maintain output voltage regulation. When the load increases and the inductor current enters continuous current mode, the boost converter automatically switches to PWM mode.

Table 3. The RT4823Q Start-Up Description

Mode	Description	Condition
LIN	Linear startup	V_{IN} - 200mV ≥ V_{OUT}
Soft-Start	Boost soft-start	0.99 x V_{OUT_Target} > V_{OUT} ≥ V_{IN} - 200mV
Boost	Boost mode	V_{OUT_Target} ≥ 0.99 x V_{OUT_Target}
If V_{IN} increases higher than V_{OUT}		
Auto Bypass	Auto bypass mode	V_{IN} ≥ V_{OUT} Control loop auto transfer between auto bypass mode and boost mode.

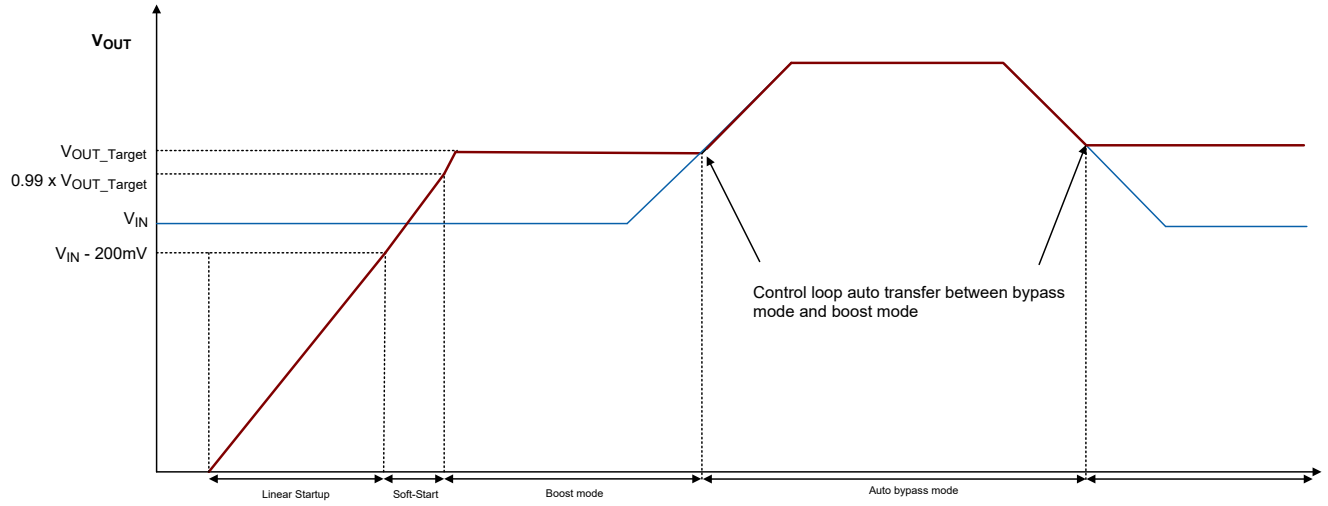


Figure 3. V_{OUT} Mode Transition Diagram with EN L to H and V_{IN} Variation (I_{OUT} = 0A)

15.8 Protection

The RT4823Q features several protections, which are listed in the table below. The table describes the protection behaviors.

Protection Type	Fault Event Trigger	Fault Deglitch Time	Protection Method	Fault Protection Latch Time	Reset Method
OCP_IL5A	I_{L_peak} > I_{OCP}	No delay	Turn off UG, LG	20ms, Auto-recovery	I_{L_peak} < I_{OCP}
OCP	I_{L_valley} > I_{LIM_VALLEY}	No delay	Stop LG switching	N/A	I_{L_valley} < I_{LIM_VALLEY}
OVP	V_{OUT} > 6V	100ns	Turn off UG, LG	N/A	V_{OUT} < 6V
SCP	V_{OUT} < V_{SCP}	No delay	Turn off UG, LG	20ms, Auto-recovery	V_{OUT} > V_{SCP}
OTP	TEMP > T_{OTP}	170μs	Turn off UG, LG	Turn off UG, LG	TEMP < T_{OTP} - T_{OTP_HYS}
SCP_SS	V_{IN} - V_{OUT} > 0.2V	2ms	UG OCP = 0.3A	N/A	V_{IN} - V_{OUT} < 0.2V

16 Application Information

(Note 6)

16.1 Start-Up

The RT4823Q can be powered via the EN pin. The following steps must be followed for startup.

1. Configure the input voltage (VIN) within the recommended operating range.
2. Set the MODE pin for PFM or PWM mode selection.
3. Enable the boost converter using the EN pin.

16.2 Power-Off

When the RT4823Q is turned off, the device enters a shutdown state. In this mode, the converter stops its switching operation, the internal control circuitry is deactivated, and the load is disconnected from the input. As a result, the output voltage may decrease below the input voltage while in shutdown.

16.3 Power Frequency Modulation (PFM)

PFM is used to improve efficiency at light load. When the output voltage is lower than a set threshold voltage, the converter will operate in PFM. It raises the output voltage with several pulses until the loop exits PFM.

16.4 Over-Temperature Protection (OTP)

The device has a built-in temperature sensor which monitors the internal junction temperature. If the temperature exceeds the threshold, the device stops operating. As soon as the IC temperature decreases below the threshold with a hysteresis, it starts operating again. The built-in hysteresis is designed to avoid unstable operation at IC temperatures near the over-temperature threshold.

16.5 Inductor Selection

The primary concern in inductor selection is the maximum load of the application. An example is given by the application conditions and equations below.

Application conditions:

V_{IN} = 3V, V_{OUT} = 5V, I_{OUT} = 1.5A, converter efficiency = 81%, Frequency = 3.5MHz, L = 1μH.

Step 1: To calculate the input current (I_{IN}).

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times Eff} = 3.086A$$

Step 2: To calculate the duty cycle of the boost converter.

$$D = 1 - \frac{V_{IN}}{V_{OUT}} = 0.4$$

Step 3: To calculate the peak current of the inductor.

$$I_{L(Peak)} = I_{IN} + 0.5 \times \frac{V_{IN} \times D}{L \times Freq} = 3.258A$$

The recommended nominal inductance value is 1μH. It is recommended to use an inductor with a DC saturation current of at least 3300mA.

16.6 Input Capacitor Selection

It is recommended to use an input capacitor with a minimum capacitance of 4.7μF and a rate voltage of 6.3V for DC bias. This helps to improve the transient response of the regulator and the EMI performance of the entire power supply circuit for the switch (SW). Additionally, the input capacitor should be placed as close as possible to the VIN and GND pins of the IC.

16.7 Output Capacitor Selection

It is recommended to use at least a 10μF capacitor to reduce V_{OUT} ripple. The output voltage ripple is inversely proportional to the output capacitance (C_{OUT}). The output capacitor should be selected based on the desired output ripple, which can be calculated using the following formula:

$$V_{RIPPLE(P-P)} = t_{ON} \times \frac{I_{LOAD}}{C_{OUT}}$$

and

$$t_{ON} = t_{SW} \times D = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

therefore :

$$C_{OUT} = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \frac{I_{LOAD}}{V_{RIPPLE(P-P)}}$$

and

$$t_{SW} = \frac{1}{f_{SW}}$$

The maximum V_{RIPPLE} occurs at minimum input voltage and maximum output load.

16.8 Boost Converter Sleeping Mode Operation

The RT4823Q implements both PFM (Pulse Frequency Modulation) mode and PWM (Pulse Width Modulation) mode. The PFM mode is designed for power-saving operation when the system operates under light load conditions.

There is a mode transition between PFM and PWM modes. When the system load increases, the operating mode transitions from PFM to PWM. Please note that within this small load current range, the mode change can cause an increase in output ripple.

16.9 Current Limit

The RT4823Q employs a valley-current limit detection scheme to sense the inductor current during the off-time. When the load current increases such that it exceeds the valley current-limit threshold, the off-time is extended until the current decreases to the valley-current threshold. The next on-time begins after the current decreases to the valley-current threshold. The on-time is determined by the ratio of (V_{OUT} – V_{IN}) / V_{OUT}. The output voltage decreases when the load current further increases. The current limit function is implemented using this scheme. Refer to Figure 4 for more details.

16.10 Overcurrent Protection (OCP)

The RT4823Q implements an OCP function. When the converter operates in boost mode, the peak current limit and valley current limit functions cannot protect the IC from short circuits or extremely high loads. Therefore, the RT4823Q includes a truth disconnection function. When the peak current exceeds 5A (typical), the boost converter will turn off both the high-side MOSFET (UG) and the low-side MOSFET (LG).

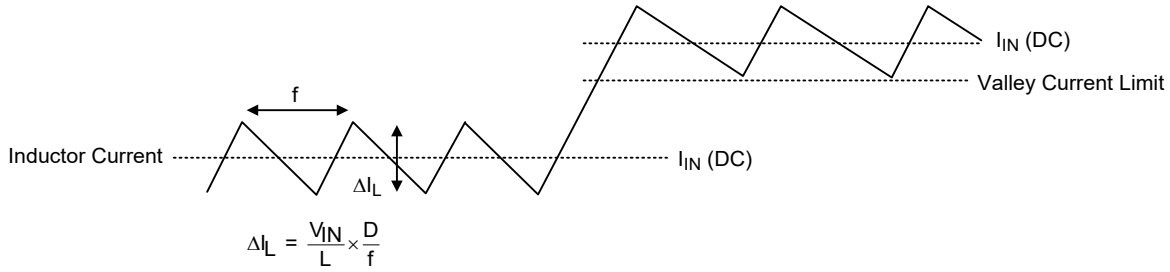


Figure 4. Inductor Currents in Current Limit Operation

16.11 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-9B 1.3x1.2 (BSC) package, the thermal resistance, θ_{JA}, is 64.9°C/W on a standard JEDEC 51-9 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (64.9°C/W) = 1.54W for a WL-CSP-9B 1.3x1.2 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

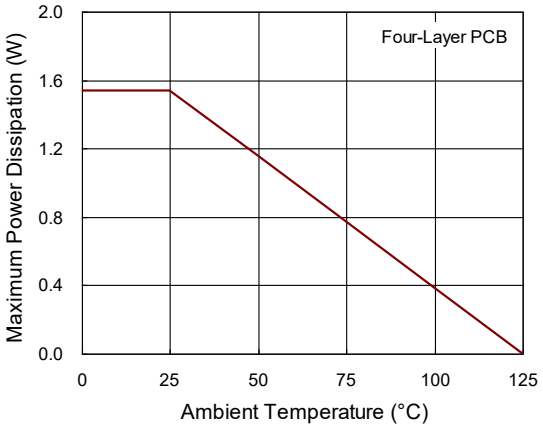


Figure 5. Derating Curve of Maximum Power Dissipation

16.12 Layout Considerations

The PCB layout is an important step to maintain the high performance of the RT4823Q.

Both the high current and the fast switching nodes demand full attention in the PCB layout to save the robustness of the RT4823Q. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RT4823Q, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins, respectively, for effective filtering.
- For thermal considerations, it is necessary to maximize the copper area for the power stage area, especially around the SW pin.

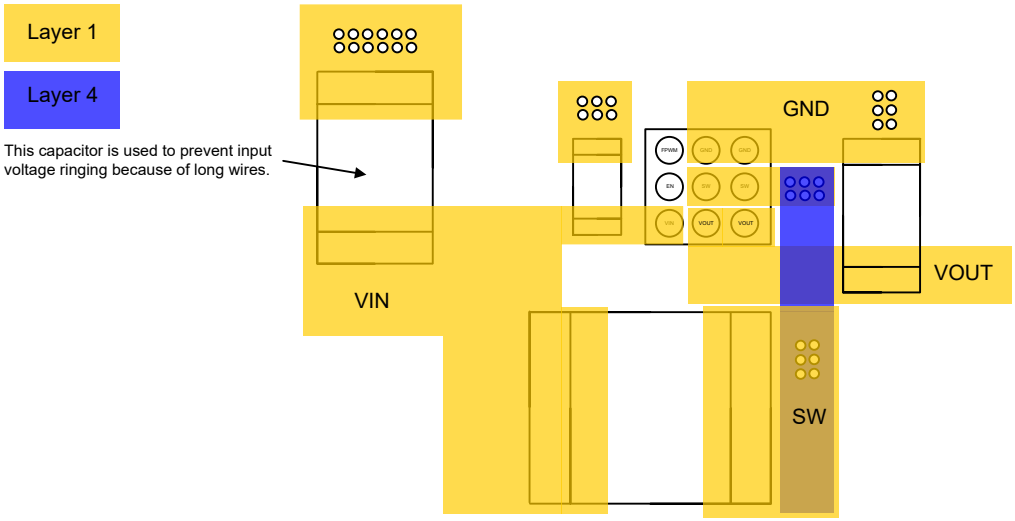
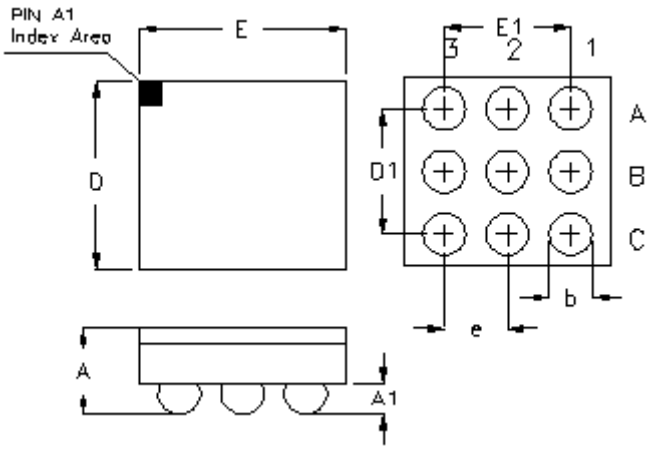


Figure 6. PCB Layout Guide

Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

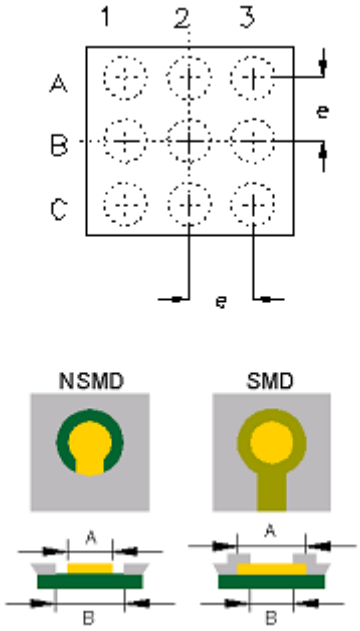
17 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.160	1.240	0.046	0.049
D1	0.800		0.031	
E	1.260	1.340	0.050	0.053
E1	0.800		0.031	
e	0.400		0.016	

9B WL-CSP 1.3x1.2 Package (BSC)

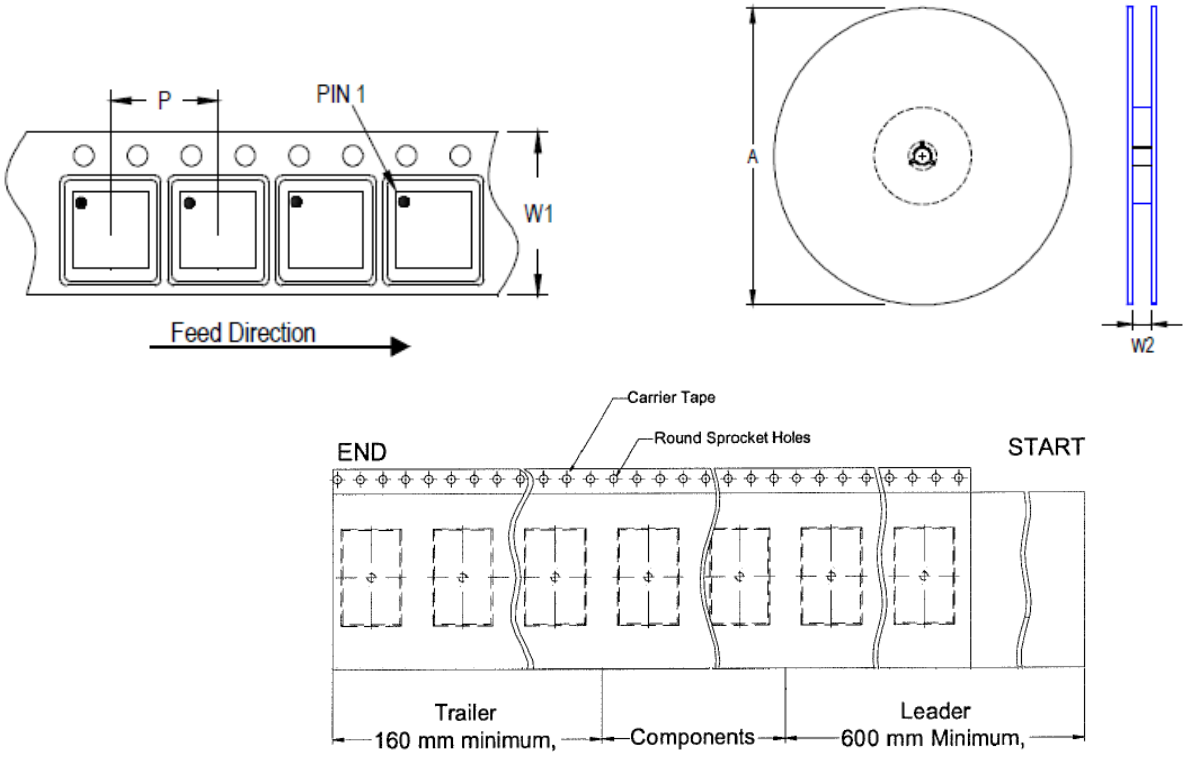
18 Footprint Information



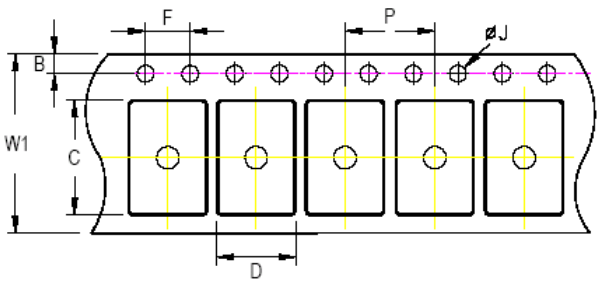
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.3x1.2-9(BSC)	9	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

19 Packing Information

19.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
WL-CSP 1.3x1.2	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.7mm	0.8mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 1.3x1.2	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description
00	2025/9/29	First Edition