Dual-Phase PWM Controller with Dual Integrated Drivers

General Description

The RT8692 is a 2/1 phase synchronous Buck PWM controller optimized for high performance graphic microprocessor. The IC integrates a Constant-On-Time (COT) PWM controller, two MOSFET drivers with internal bootstrap diodes, as well as channel current balance and protection functions including overvoltage protection (OVP), undervoltage protection (UVP), current limit, and thermal shutdown into the WQFN-20L 3x3 package.

The RT8692 adopts $R_{DS(ON)}$ current sensing technique. Current limit is accomplished through continuous inductor current sensing, while $R_{DS(ON)}$ current sensing is used for accurate channel current balance. Using the method of current sampling utilizes the best advantages of each technique.

The RT8692 features external reference input control, of which the feedback voltage is regulated and tracks external input reference voltage. Other features include adjustable switching frequency, dynamic phase number control, internal soft-start, power good indicator, and enable functions.

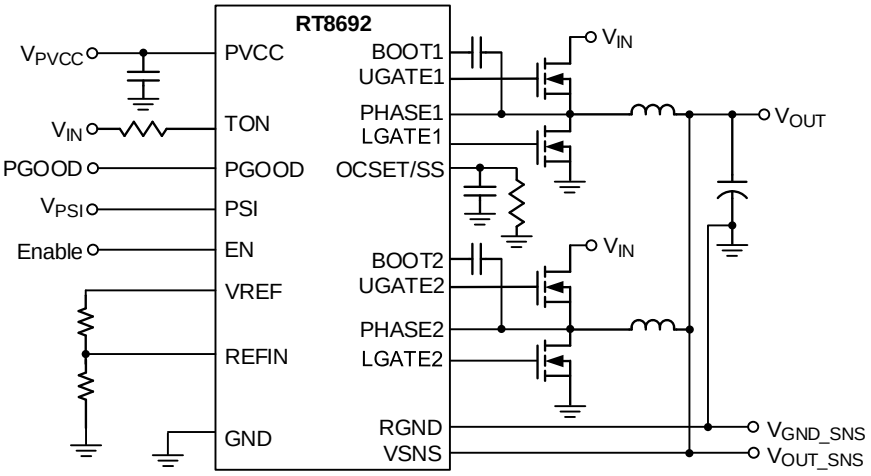
Features

- **Dual-Phase PWM Controller**
- **VOUT Operating Range: 0.3V to 2V**
- **1% High Accuracy 2V Reference**
- **Differential Remote Voltage Sensing**
- **Power State Indicator**
  - **1P-CCM/2P-CCM/1P-DEM/2P-DEM**
- **Two Embedded MOSFET Drivers and Embedded Switching Boot Diode**
- **External Reference Input Control**
- **Dynamic Phase Number Control**
- **Lossless $R_{DS(ON)}$ Current Sensing for Current Balance**
- **Internal/External Soft-Start**
- **Adjustable Current-Limit Threshold**
- **Adjustable Switching Frequency**
- **UVP/OVP Protection**
- **Shoot Through Protection and Short Pulse Free Technology**
- **Thermal Shutdown**
- **Power Good Indicator (EN to PG high = 500μs)**

Applications

- Desktop PC Memory, VTT Power
- Chipset/RAM Power Supply
- Generic DC-DC Power Regulator

Simplified Application Circuit



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Ordering Information

RT8692 □-□

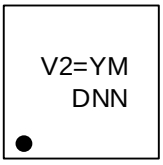
Packing
A: Standard

Package Type
N: WQFN-20L 3x3 (W-Type)

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

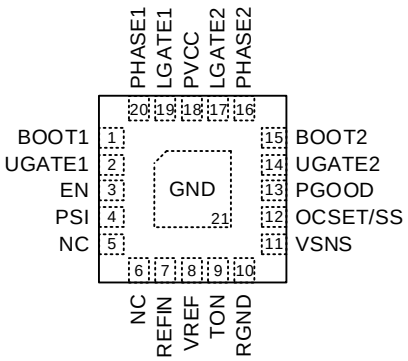
Marking Information



V2= : Product Code
YMDNN : Date Code

Pin Configuration

(TOP VIEW)



WQFN-20L 3x3

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Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT1	Bootstrap supply for PWM1. This pin powers the high-side MOSFET driver.
2	UGATE1	High-side gate driver of PWM1. This pin provides the gate drive for the converter's high-side MOSFET. Connect this pin to the gate of high-side MOSFET.
3	EN	Enable control input. Active high input. When PVCC POR, the input voltage must not exceed PVCC.
4	PSI	Power saving interface. When the voltage is pulled below 0.4V, the device operates into 1 phase DEM. When the voltage is between 0.7V to 0.88V, the device operates into 1 phase forced CCM. When the voltage is between 1.08V to 1.35V, the device operates into 2 phase DEM. When the voltage is between 1.6V to 5.5V, the device operates into 2 phase forced CCM.
5	NC	No connect.
6	NC	No connect.
7	REFIN	External reference input.
8	VREF	Reference voltage output. This is a high precision voltage reference (2V) from the VREF pin to RGND pin.
9	TON	On-time/switching frequency adjustment input. Connecting a 100pF ceramic capacitor between C_{TON} and ground is optional for noise immunity enhancement.
10	RGND	Negative remote sense input. Connect this pin to the ground of output load.
11	VSNS	Positive remote sense input. Connect this pin to the positive terminal of output load.
12	OCSET/SS	Current limit setting. Connect a resistor from OCSET/SS to GND to set the current-limit threshold. The external soft-start time can also be set through by connecting a capacitor from OCSET/SS pin to GND.
13	PGOOD	Power good indicator output. Active high open-drain output.
14	UGATE2	High-side gate driver of PWM2. This pin provides the gate drive for the converter's high-side MOSFET. Connect this pin to the gate of high-side MOSFET.
15	BOOT2	Bootstrap supply for PWM2. This pin powers the high-side MOSFET driver.
16	PHASE2	Switch node for PWM2. This pin is return node of the high-side driver of PWM 2. Connect this pin to the source of high-side MOSFET together with the drain of low-side MOSFET and the inductor.
17	LGATE2	Low-side gate driver of PWM2. This pin provides the gate drive for the converter's low-side MOSFET. Connect this pin to the gate of low-side MOSFET.
18	PVCC	Supply voltage input. Connect this pin to a 5V bias supply. Place a high- quality bypass capacitor from this pin to GND.
19	LGATE1	Low-side gate driver of PWM1. This pin provides the gate drive for the converter's low-side MOSFET. Connect this pin to the gate of low-side MOSFET.
20	PHASE1	Switch node for PWM1. This pin is return node of the high-side driver of PWM 1. Connect this pin to the source of high-side MOSFET together with the drain of low-side MOSFET and the inductor.
21 (Exposed Pad)	GND	Ground. The Exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation.

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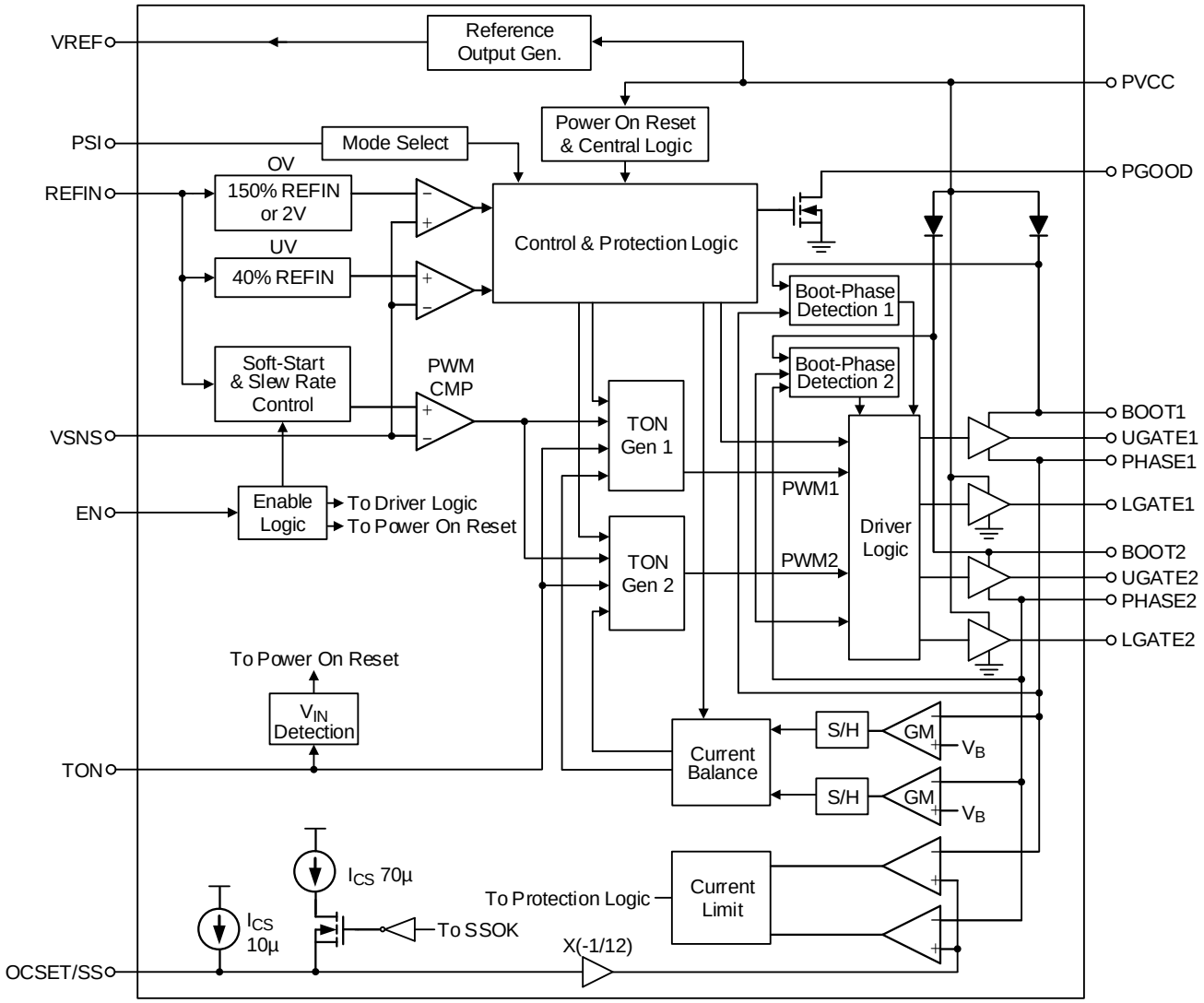
Functional Block Diagram



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Absolute Maximum Ratings (Note 1)

- TON to GND ---------- –0.3V to 30V
- RGND to GND ---------- –0.7V to 0.7V
- BOOTx to PHASEx
  - DC ---------- –0.3V to 6V
  - <100ns ---------- –5V to 7.5V
- BOOTx to GND
  - DC ---------- –0.3V to 36V
  - <100ns ---------- –5V to 42V
- PHASEx to GND
  - DC ---------- –5V to 30V
  - <100ns ---------- –10V to 42V
- UGATEx to GND
  - DC ---------- –5V to 36V
  - <100ns ---------- –10V to 42V
- UGATEx to PHASEx
  - DC ---------- –0.3V to 6V
  - <100ns ---------- –5V to 7.5V
- LGATEx to GND
  - DC ---------- –0.3V to 6V
  - <100ns ---------- –5V to 7.5V
- Other Pins ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-20L 3x3 ---------- 2.67W
- Package Thermal Resistance (Note 2)
  - WQFN-20L 3x3, θ_{JA} ---------- 30°C/W
  - WQFN-20L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage, VIN ---------- 2.5V to 26V
- Supply Voltage, PVCC ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –10°C to 105°C

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Electrical Characteristics

(V_{PVCC} = 5V, typical values are referenced to $T_A = T_J$ = 25°C, Min and Max values are referenced to $T_A = T_J$ from −10°C to 105°C, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller							
PVCC Supply Voltage		V_{PVCC}		4.5	--	5.5	V
PVCC Supply Current		I_{SUPPLY}	V_{EN} = 3.3V, 1phase DEM mode, not switching, VREF external R = 40k	--	0.4	--	mA
PVCC Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	--	10	μA
PVCC POR Threshold				3.8	4.1	4.4	V
POR Hysteresis				--	0.3	--	V
Switching Frequency		f_{SW}	R_{TON} = 500kΩ (Note 5)	270	300	330	kHz
Minimum On-Time		$t_{ON(MIN)}$		--	70	--	ns
Minimum Off-Time		$t_{OFF(MIN)}$		--	300	--	ns
EN Input Voltage							
EN Input Voltage	Logic-High	V_{EN_H}		1.2	--	5.5	V
	Logic-Low	V_{EN_L}		--	--	0.55	
Mode Decision							
2 Phase CCM		V_{PSI}		1.6	1.8	5.5	V
2 Phase DEM		V_{PSI}		1.08	1.2	1.35	V
1 Phase CCM		V_{PSI}		0.7	0.8	0.88	V
1 Phase DEM		V_{PSI}		--	0	0.4	V
Protection Function							
Zero Current Crossing Threshold				–8	--	8	mV
Current Limit Setting Current		I_{OCSET}	$T_A = T_J$ = 25°C	9	10	11	μA
Current Limit Setting Current Temperature Coefficient		I_{OCSET_TC}		--	4700	--	ppm/°C
Current-Limit Threshold			R_{OCSET} = 120k	--	100	--	mV
Current-Limit Comparator Error			V_{OCSET} = 20mV	–5	--	5	mV
Absolute Overvoltage Protection Threshold		$V_{OVP, Absolute}$	$V_{REFIN} \leq$ 1.33V	1.9	2	2.1	V
Relative Overvoltage Protection Threshold		$V_{OVP, Relative}$	V_{REFIN} > 1.33V	145	150	155	%
OV Fault Delay			FB forced above OV threshold	--	5	--	μs
Relative Undervoltage Protection Threshold		V_{UVP}	UVP	35	40	45	%
UV Fault Delay			FB forced above UV threshold	--	3	--	μs
Thermal Shutdown Threshold		T_{SD}		--	150	--	°C

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VOUT Soft-Start (PGOOD Blanking Time)		From V_{EN} = high to VOUT regulation point, V_{REFIN} = 1V	--	0.5	--	ms
Error Amplifier						
VSNS Error Comparator Threshold (Valley)		V_{REFIN} = 1V	–11	–6	–1	mV
Reference						
Reference Voltage	V_{VREF}	Sourcing current = 1mA	1.98	2	2.02	V
Driver On-Resistance						
UGATE Driver Source	$R_{UGATEsr}$	BOOTx – PHASEx forced to 5V	--	2	4	Ω
UGATE Driver Sink	$R_{UGATEsk}$	BOOTx – PHASEx forced to 5V	--	1	2	Ω
LGATE Driver Source	$R_{LGATEsr}$	LGATEx, high state	--	1.5	3	Ω
LGATE Driver Sink	$R_{LGATEsk}$	LGATEx, low state	--	0.7	1.5	Ω
Dead-Time		From LGATE falling to UGATE rising	--	30	--	ns
		From UGATE falling to LGATE rising	--	20	--	
Internal Boost Diode Resistance	R_{BOOT}	PVCC to BOOTx, I_{BOOT} = 10mA	--	80	--	Ω

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Not production tested. Test condition is V_{IN} = 8V, V_{OUT} = 1V, I_{OUT} = 20A using application circuit.

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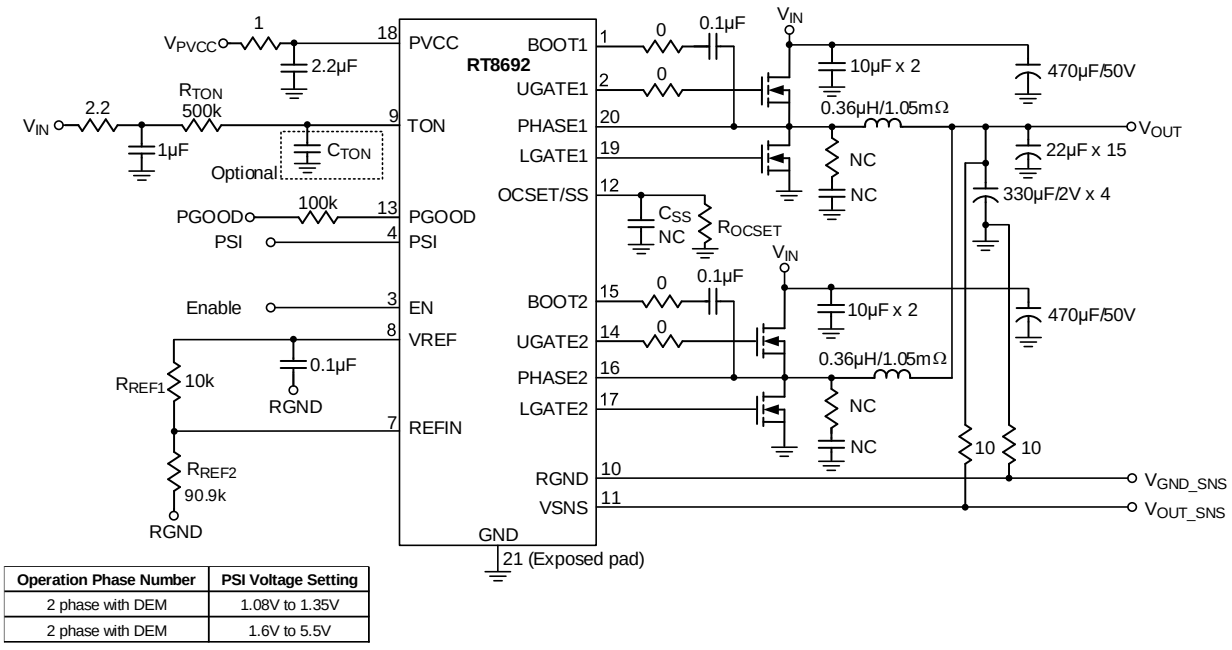
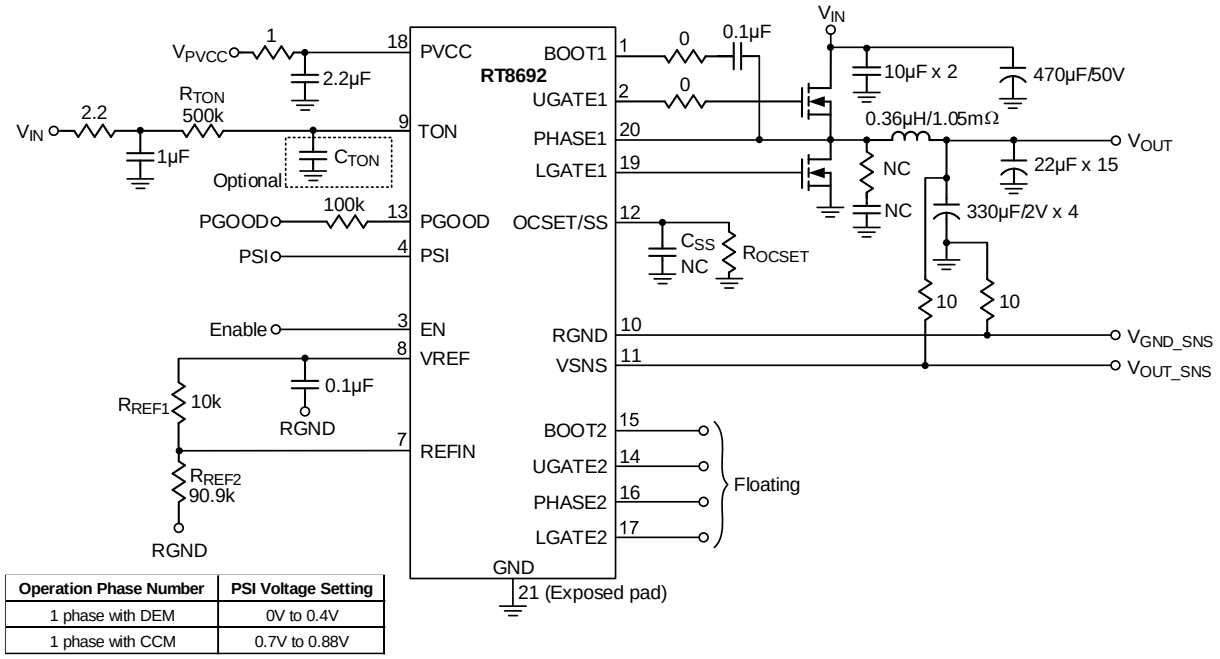
Typical Application Circuit



Operation Phase Number	PSI Voltage Setting
2 phase with DEM	1.08V to 1.35V
2 phase with DEM	1.6V to 5.5V

Figure 1. 2 Active Phase Configuration



Operation Phase Number	PSI Voltage Setting
1 phase with DEM	0V to 0.4V
1 phase with CCM	0.7V to 0.88V

Figure 2. 1 Active Phase Configuration

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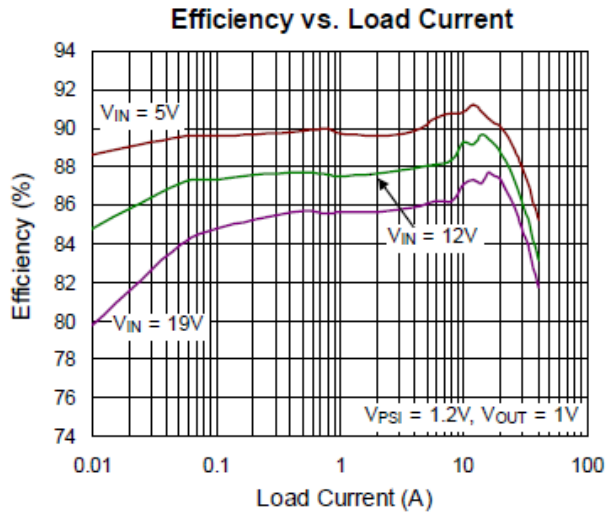
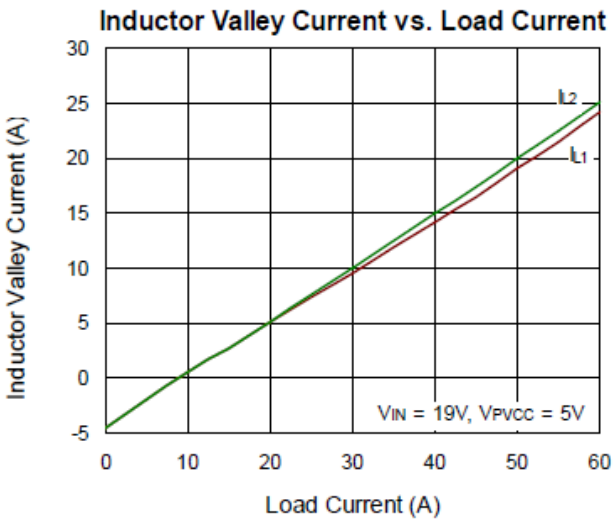
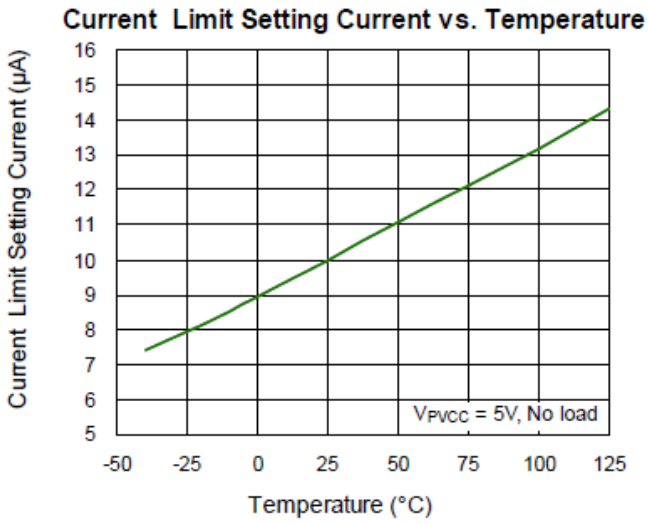
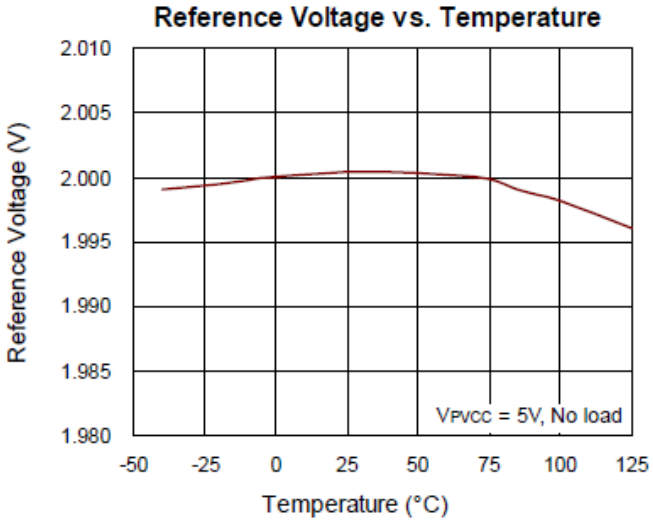
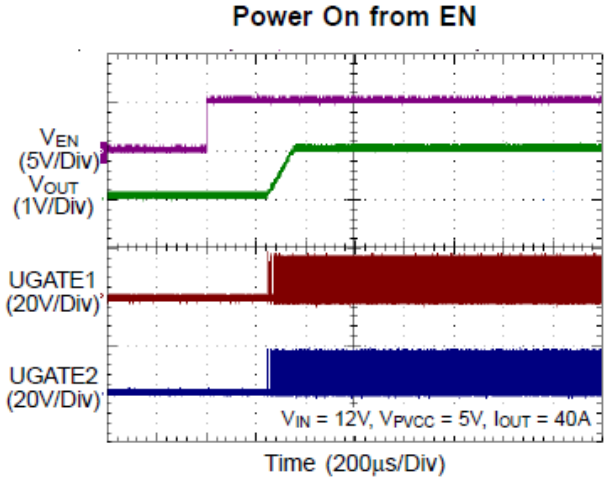
Typical Operating Characteristics

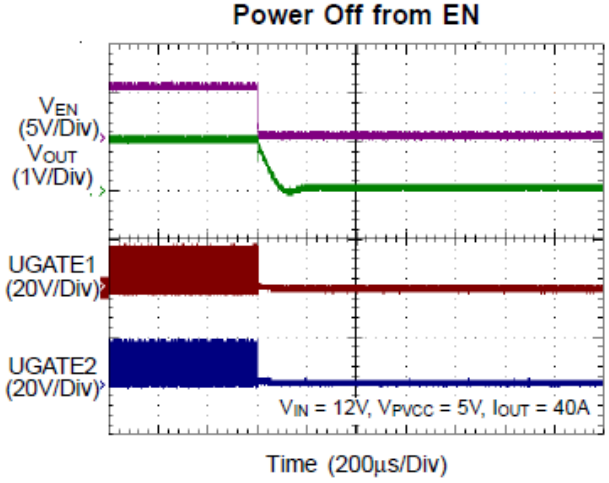












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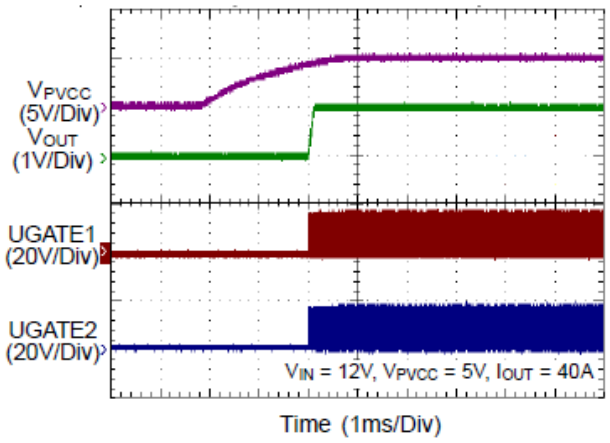
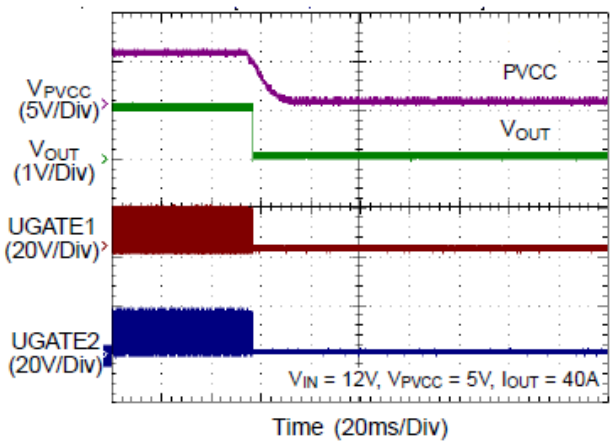
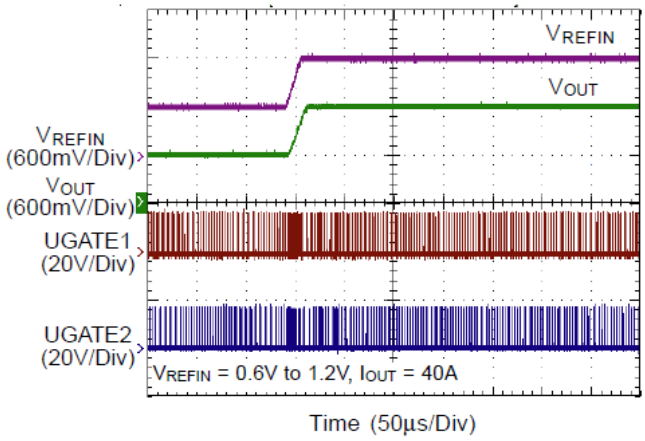
Power On from PVCC



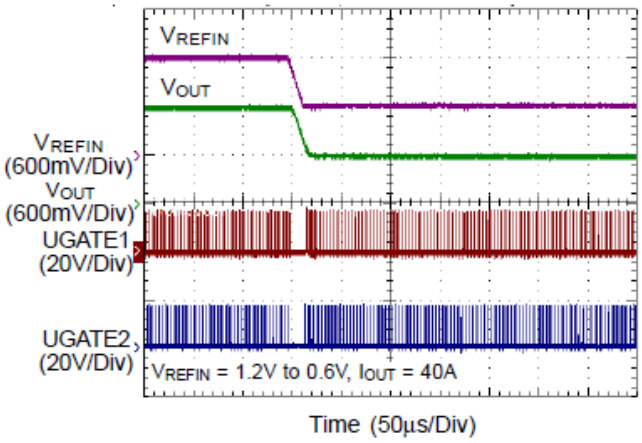
Power Off from VCC



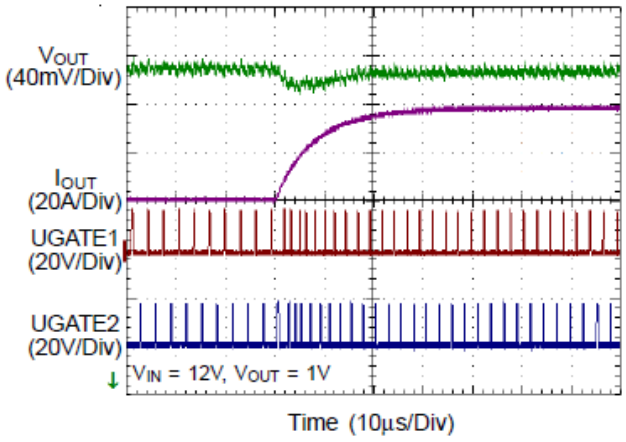
Dynamic Output Voltage Control



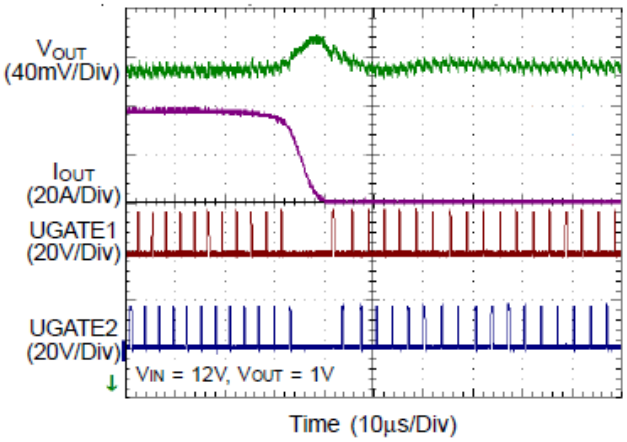
Dynamic Output Voltage Control



Load Transient Response



Load Transient Response



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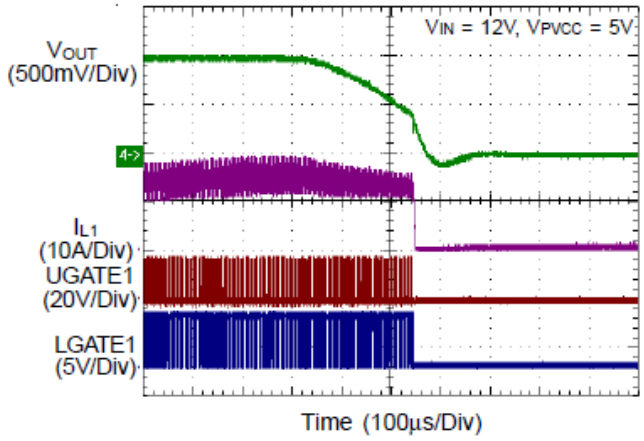
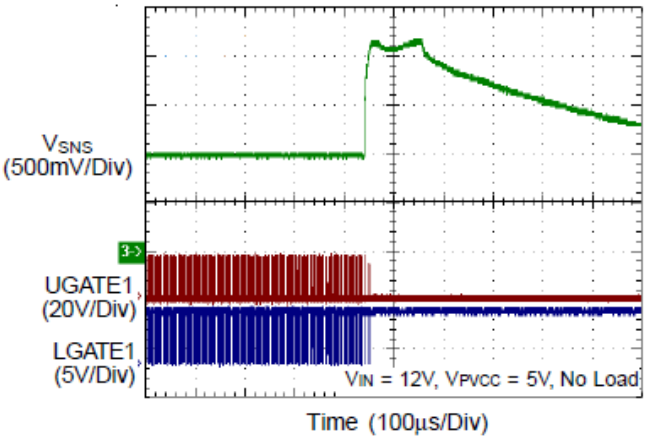
Current Limit and UVP



OVP



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Operation

The RT8692 is a dual-phase synchronous Buck PWM controller with integrated drivers optimized for high performance graphic microprocessor and computer applications. The IC integrates a COT (Constant-On-Time) PWM controller with two MOSFET drivers, as well as output current monitoring and protection functions. Referring to the function block diagram of TON Genx, the synchronous UGATE driver is turned on at the beginning of each cycle. After the internal one-shot timer expires, the UGATE driver is turned off. The pulse width of this one-shot is determined by the converter's input voltage and the output voltage to keep the frequency fairly constant over the input voltage range and output voltage. Another one-shot sets a minimum off-time.

Soft-Start (SS)

For soft-start function, an internal current source charges an internal capacitor to build the soft-start ramp voltage. The output voltage will track the internal ramp voltage during soft-start interval.

PGOOD

The power good output is an open-drain architecture.

When the soft-start is finished, the PGOOD open-drain output is high impedance.

Current Balance

The RT8692 implements internal current balance mechanism in the current loop. The RT8692 senses per phase current and compares it with the average current. If the sensed current of any particular phase is higher than average current, the on-time of this phase is adjusted to be shorter.

Current Limit

The current limit circuit employs a unique “valley” current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. Thus, the current to the load exceeds average output inductor current, the output voltage falls and eventually crosses the undervoltage protection threshold, inducing IC shutdown.

Overvoltage Protection (OVP) & Undervoltage Protection (UVP)

The output voltage is continuously monitored for over-voltage and undervoltage protection. When the output voltage exceeds its set voltage threshold (If $V_{REFIN} \leq$ 1.33V, OV = 2V, or $V_{REFIN} >$ 1.33V, OV = 1.5 x V_{REFIN}), UGATE goes low and LGATE is forced high. When it is less than 40% of its set voltage, undervoltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. The controller is latched until PVCC is re-supplied and exceeds the POR rising threshold voltage or EN is

reset.

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Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The RT8692 is a dual-phase synchronous Buck PWM controller with integrated drivers optimized for high performance graphic microprocessor and computer applications. A COT (Constant-On-Time) PWM controller and two MOSFET drivers with internal bootstrap diodes are integrated so that the external circuit can be easily designed and the number of component is reduced.

The topology solves the poor load transient response timing problems of fixed-frequency mode PWM and avoids the problems caused by widely varying switching frequencies in conventional constant on-time and constant off-time PWM schemes. The IC supports dynamic mode transition function with various operating states, which include single phase with CCM, dual-phase with CCM, single phase with diode emulation mode and dual-phase with diode emulation mode operation. These different operating states make the system efficiency as high as possible.

The RT8692 provides external reference input control, which the feedback voltage is regulated and tracks external input reference voltage. It also features complete fault protection functions including overvoltage, undervoltage and current limit.

Remote Sense

The RT8692 uses the remote sense path (VSNS and RGND) to overcome voltage drops in the power lines by sensing the voltage directly at the end of GPU. Normally, to protect remote sense path disconnecting, there are two resistors (R_{Local}) connecting between local sense path and remote sense path. That is, in application with remote sense, the R_{Local} is recommended to be 10Ω to 100Ω. If no need of remote sense, the R_{Local} is recommended to be 0Ω.

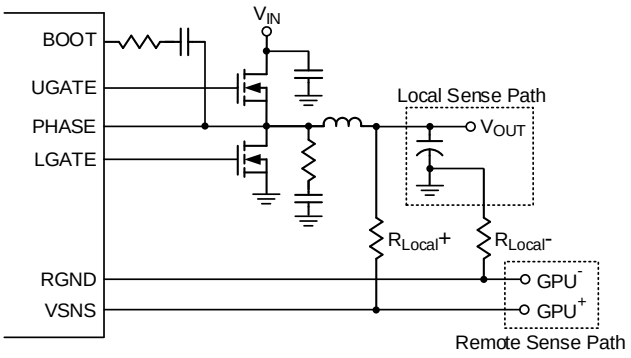

Figure 3. Output Voltage Sensing

PWM Operation

The RT8692 integrates a Constant-On-Time (COT) PWM controller, and the controller provides the PWM signal which relies on the output ripple voltage comparing with internal reference voltage as shown in Figure 4. Referring to the function block diagram of TON Genx, the synchronous UGATE driver is turned on at the beginning of each cycle. After the internal one-shot timer expires, the UGATE driver is turned off. The pulse width of this one-shot is determined by the converter input voltage and the output voltage to keep the frequency fairly constant over the input voltage and output voltage range. Another one-shot sets a minimum off-time.

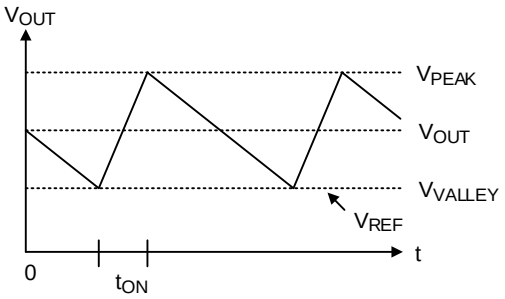

Figure 4. Constant On-Time PWM Control

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On-Time Control

The on-time one-shot comparator has two inputs. One input monitors the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to V_{OUT}, thereby making the on-time of the high- side switch directly proportional to output voltage and inversely proportional to input voltage. The implementation results in a nearly constant switching frequency without the need for a clock generator.

$$T_{ON} = \frac{2 \times V_{OUT} \times 3.2p}{V_{IN} - 0.5} \times R_{TON}$$

and then the switching frequency F_S is:

$F_S = V_{OUT}/(V_{IN} \times T_{ON})$

R_{TON} is a resistor connected from the V_{IN} to TON pin.

The recommended operation frequency range is from 250kHz to 750kHz.

Active Phase Circuit Setting

The RT8692 can be set for 2 phase or 1 phase operation by hardware circuit. When set to 1 phase operation, UGATE2, BOOT2, PHASE2, LGATE2 pins are floating, and the voltage of PSI pin must be set to the 1 phase operation threshold. Refer to Table 1 for detail.

Mode Selection

The RT8692 can operate into 2 phases with forced CCM, 1 phase with forced CCM, 1 phase with DEM and 2 phases with DEM according to PSI voltage setting. If PSI voltage is pulled below 0.4V, the controller operates into 1 phase with DEM. In DEM operation, the RT8692 automatically reduces the operation frequency at light load condition for saving power loss. If PSI voltage is pulled between 0.7V to 0.88V, the controller switches operation into 1 phase with forced CCM. If PSI voltage is pulled between 1.08V to 1.35V, the controller switches operation into 2 phase with DEM. If PSI voltage is pulled between 1.6V to 5.5V, the controller switches operation into 2 phase with forced CCM. The operation mode is summarized in Table 1. Moreover, the PSI pin is valid after POR of VR.

Table 1

Operation Phase Number	PSI Voltage Setting
1 phase with DEM	0V to 0.4V
1 phase with CCM	0.7V to 0.88V
2 phase with DEM	1.08V to 1.35V
2 phase with DEM	1.6V to 5.5V

Diode-Emulation Mode

In diode-emulation mode, the RT8692 automatically reduces switching frequency at light-load condition to maintain high efficiency. As the output current decreases from heavy-load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low-side MOSFET allows only partial of negative current when the inductor freewheeling current reaches negative value. As the load current is further decreased, it takes a longer time to discharge the output capacitor to the level that requires the next “ON” cycle. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction condition. The transition load point to the light load operation is shown in Figure 5 and can be calculated as follows:

$$I_{LOAD(SKIP)} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is on-time.

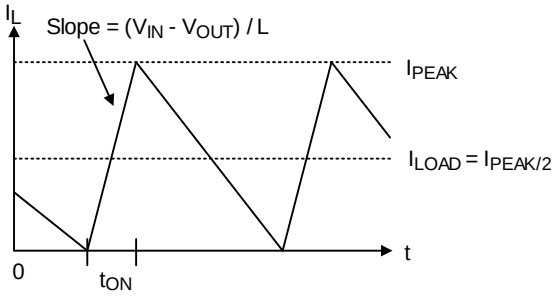

Figure 5. Boundary Condition of CCM/DEM

The switching waveforms may be noisy and asynchronous in light loading diode-emulation operation condition, but this is a normal operating

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condition that results in high light-load efficiency. Trade-off in DEM noise vs. light-load efficiency is made by varying the inductor value. Generally, low inductor values produce a broad high efficiency range vs. load curve, while higher values result in higher full load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. The disadvantages for using higher inductor values include larger physical size and degraded load-transient response (especially at low input voltage levels).

Forced-CCM Mode

The low noise, forced-CCM mode disables the zero-crossing comparator, which controls the low-side switch on-time. This causes the low-side gate drive waveform to be the complement of the high-side gate drive waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop to maintain a duty ratio V_{OUT}/V_{IN}. The benefit of forced-CCM mode is to keep the switching frequency fairly constant.

Enable and Disable

The EN pin is a high impedance input that allows power sequencing between the controller bias voltage and another voltage rail. The RT8692 remains in shutdown if the EN pin is lower than 550mV. When the EN voltage rises above the 1.2V high level threshold, the RT8692 begins a new initialization and soft-start cycle.

Power On Reset (POR), UVLO

Power On Reset (POR) occurs when VPVCC rises above approximately 4.1V (typical), the RT8692 resets the fault latch circuit and prepares for PWM operation. When the VPVCC is lower than 3.8V (typical), the undervoltage lockout (UVLO) circuitry inhibits switching by keeping UGATE and LGATE low.

Soft-Start

The RT8692 provides internal soft-start function and external soft-start function. The soft-start function is used to prevent large inrush current and output voltage overshoot while the converter is being powered up. The soft-start function automatically begins once the chip is enabled. There is a delay time around 200μs from EN goes high to VOUT begins to ramp-up.

If external capacitor from OCSET/SS pin to GND is removed, the internal soft-start function is chosen. An internal current source charges the internal soft-start capacitor so that the internal soft-start voltage ramps up linearly. The output voltage will track the internal soft-start voltage during the soft-start interval. After the internal soft- start voltage exceeds the REFIN voltage, the output voltage no longer tracks the internal soft-start voltage but follows the REFIN voltage. Therefore, the duty cycle of the UGATE signal as well as the input current at power up are limited.

The soft-start process is finished when the internal SSOK goes high and protection is not triggered. Figure 6 shows the internal soft-start sequence.

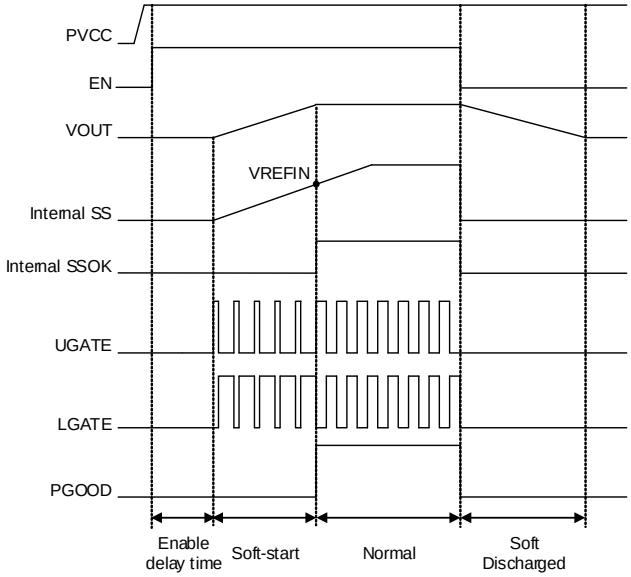

Figure 6. Internal Soft-Start Sequence

The RT8692 also provides external soft-start function, and the external soft-start sequence is shown in Figure 7, connecting an additional capacitor from OCSET/SS pin to GND. The external capacitor is charged by internal current source to build soft-start voltage ramp. If external soft-start function is chosen, the external soft-start time should be set longer than internal soft-start time to avoid output voltage tracking the internal soft-start ramp. The external soft-start time setting is shown in Figure 8 and the recommended external soft-start slew rate is from 0.1V/ms to 0.4V/ms.

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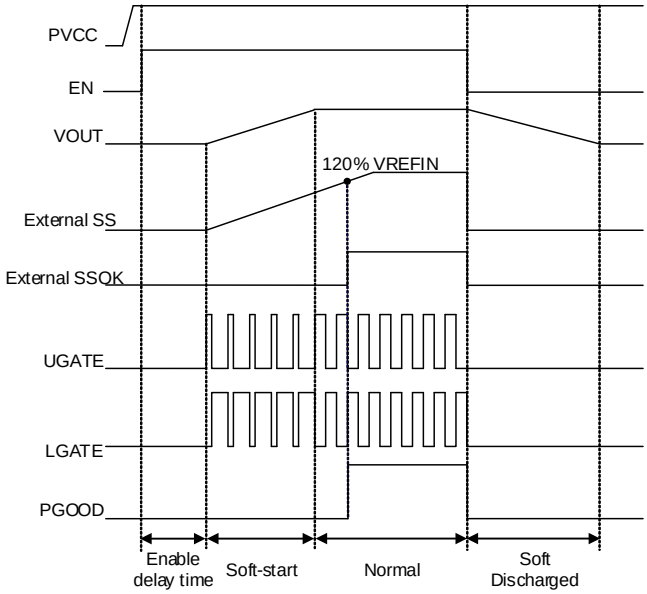

Figure 7. External Soft-Start Sequence

The soft-start time can be calculated as:

$$t_{SS} = -(C_{SS} \times R_{OCSET}) \times \ln\left[1-\left(\frac{V_{REFIN}}{I_{SS} \times R_{OCSET}}\right)\right]$$

where I_{SS} = 80μA (typ.), V_{REFIN} is the voltage of REFIN pin, R_{OCSET} is the current limit setting resistor, and C_{SS} is the external capacitor placed from OCSET/SS pin to GND.

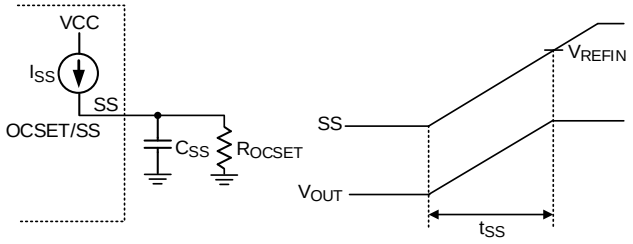

Figure 8. External Soft-Start Setting

For ensuring the soft-start function work normally, below setting limitation must be followed:

R_{OCSET} x 60μA > 1.2 x V_{REFIN}

Power Good Output (PGOOD)

The PGOOD pin is an open-drain output, and it requires a pull-up resistor. During soft-start, the PGOOD is held low and is allowed to be pulled high after V_{OUT} exceeds UVP threshold, under OVP threshold and satisfy soft-start setting limitation. In addition, if any protection is triggered during operation, the PGOOD is pulled low immediately.

Output Voltage Setting

The RT8692 supports external reference input to provide more flexible applications. The VREF pin and REFIN pin are implemented to be external reference input function. It will try to maintain the VOUT at REFIN pin input voltage.

$$V_{REFIN} = \left(\frac{R_{REF2}}{R_{REF1} + R_{REF2}}\right) \times V_{REF}$$

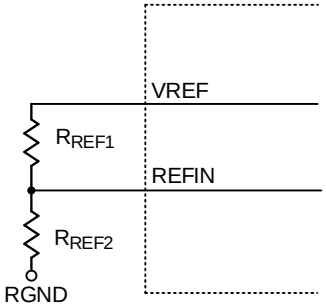

Figure 9. REFIN Voltage Setting

Current Limit

The RT8692 provides cycle-by-cycle current limit control by detecting the PHASE voltage drop across the low-side MOSFET when it is turned on. The current limit circuit employs a unique "valley" current sensing algorithm as shown in Figure 10. If the magnitude of the current sense signal at PHASE is above the current-limit threshold, the PWM is not allowed to initiate a new cycle.

In order to provide both good accuracy and a cost effective solution, the RT8692 supports temperature compensated MOSFET $R_{DS(ON)}$ sensing.

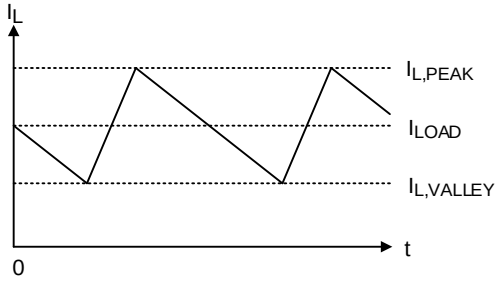

Figure 10. "Valley"Current Limit

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In an overcurrent condition, the current to the load exceeds the average output inductor current. Thus, the output voltage falls and eventually crosses the undervoltage protection threshold, inducing IC shutdown.

Current Limit Setting

The RT8692 adopts per-phase current-limit protection. The current-limit threshold can be set by a resistor (R_{OCSET}) between OCSET/SS pin and GND. Once PVCC exceeds the POR threshold and chip is enabled, an internal current source I_{OCSET} flows through R_{OCSET}. After soft-start end, I_{OCSET} is 10μA. The voltage across R_{OCSET} is stored as the current-limit protection threshold V_{OCSET}. The threshold range of V_{OCSET} is 20mV to 200mV. It can be calculated according to the following equation:

$$V_{OCSET} = \frac{I_{OCSET} \times R_{OCSET}}{12}$$

R_{OCSET} can be determined using the following equation:

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{DS\_ON} \times 12}{I_{OCSET}}$$

where I_{VALLEY} represents the desired per-phase inductor limit current (valley inductor current) and I_{OCSET} is current limit setting current which has a temperature coefficient to compensate the temperature dependency of the $R_{DS(ON)}$.

If R_{OCSET} is not present, there is no current path for I_{OCSET} to build the current-limit threshold. In this situation, the current-limit threshold is internally preset to 200mV.

Negative Current Limit

The RT8692 supports cycle-by-cycle negative current limit. The absolute value of negative current-limit threshold is the same as the positive current-limit threshold. If negative inductor current is rising to trigger negative current limit, the low-side MOSFET is turned off and the current flows to input side through the body diode of the high-side MOSFET. At this time, output voltage tends to rise because this protection limits current to discharge the output capacitor. In order to prevent shutdown because of overvoltage protection, the low-side MOSFET is turned on again 400ns after it is turned off. If the device hits the negative current-limit threshold again before output voltage is discharged to the target level, the low-side MOSFET is turned off and process repeats. It ensures maximum allowable discharge capability when output voltage continues to rise. On the other hand, if the output is discharged to the target level before negative current-limit threshold is reached, the low-side MOSFET is turned off, the high-side MOSFET is then turned on, and the device keeps normal operation.

Current Balance

The RT8692 implements current balance mechanism in the current loop. The RT8692 senses per phase current signal and compares it with the average current. If the sensed current of any particular phase is higher than the average current, the on-time of this phase is decreased.

The current balance accuracy is mainly related with on-resistance of low-side MOSFET ($R_{LG,DS(ON)}$). That is, in practical application, using lower $R_{LG,DS(ON)}$ will reduce the current balance accuracy.

Output Overvoltage Protection (OVP)

The output voltage can be continuously monitored for overvoltage protection. If REFIN voltage is lower than 1.33V, the overvoltage threshold follows absolute overvoltage 2V. If R_{EFIN} voltage is higher than 1.33V, the overvoltage threshold follows relative overvoltage 1.5 x V_{REFIN}. When OVP is triggered, UGATE goes low and LGATE is forced high. The RT8692 is latched once OVP is triggered and can only be released by PVCC or EN power on reset. A 5μs delay is used in OVP detection circuit to prevent false trigger.

Output Undervoltage Protection (UVP)

The output voltage can be continuously monitored for under- voltage protection. When the output voltage is less than 40% of its set voltage, undervoltage protection is triggered and then all UGATE and LGATE gate drivers are forced low. There is a 3μs delay built in the UVP circuit to prevent false transitions. During soft-start, the UVP blanking time is equal to PGOOD blanking time.

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MOSFET Gate Driver

The RT8692 integrates high current gate drivers for the MOSFETs to obtain high efficiency power conversion in synchronous Buck topology. A dead-time is used to prevent the cross conduction for high-side and low-side MOSFETs. Because both the two gate signals are off during the dead- time, the inductor current freewheels through the body diode of the low-side MOSFET. The freewheeling current and the forward voltage of the body diode contribute power losses to the converter. The RT8692 employs adaptive dead time control scheme to ensure safe operation without sacrificing efficiency. Furthermore, elaborate logic circuit is implemented to prevent cross conduction. For high output current applications, two power MOSFETs are usually paralleled to reduce $R_{DS(ON)}$. The gate driver needs to provide more current to switch on/off these paralleled MOSFETs. Gate driver with lower source/sink current capability results in longer rising/falling time in gate signals and higher switching loss. The RT8692 embeds high current gate drivers to obtain high efficiency power conversion.

MOSFET Selection

The majority of power loss in the step-down power conversion is due to the loss in the power MOSFETs. For low voltage high current applications, the duty cycle of the high-side MOSFET is small. Therefore, the switching loss of the high-side MOSFET is of concern. Power MOSFETs with lower total gate charge are preferred in such kind of application.

However, the small duty cycle means the low-side MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter. To improve the overall efficiency, the MOSFETs with low $R_{DS(ON)}$ are preferred in the circuit design. In some cases, more than one MOSFET are connected in parallel to further decrease the on-state resistance. However, this depends on the low-side MOSFET driver capability and the budget.

Inductor Selection

Inductor plays an important role in step-down converters because the energy from the input power rail is stored in it and then released to the load. From the viewpoint of efficiency, the DC Resistance (DCR) of inductor should be as small as possible to minimize the copper loss. In addition, the inductor occupies most of the board space so the size of it is important. Low profile inductors can save board space especially when the height is limited. However, low DCR and low profile inductors are usually not cost effective.

Additionally, higher inductance results in lower ripple current, which means the lower power loss. However, the inductor current rising time increases with inductance value. This means the transient response will be slower. Therefore, the inductor design is a trade-off between performance, size and cost.

In general, inductance is designed to let the ripple current ranges between 20% to 40% of full load current. The inductance can be calculated using the following equation:

$$L_{min} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times k \times I_{OUT\_rated}} \times \frac{V_{OUT}}{V_{IN}}$$

where k is the ratio between inductor ripple current and rated output current.

Input Capacitor Selection

Voltage rating and current rating are the key parameters in selecting input capacitor. Generally, input capacitor voltage rating should be 1.5 times greater than the maximum input voltage for a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation:

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is to select proper capacitor for RMS current rating. Using more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank is a good design. Besides, placing ceramic capacitor close to the drain of the high-side MOSFET is helpful in reducing the input voltage ripple at heavy load.

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Output Capacitor Selection

The output filter capacitor must have ESR low enough to meet output ripple and load transient requirement, yet have high enough ESR to satisfy stability requirements. Also, the capacitance must be high enough to absorb the inductor energy going from a full load to no load condition without tripping the OVP circuit. Organic semiconductor capacitor(s) or special polymer capacitor(s) are recommended.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 105°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-20L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board.

The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (105°C – 25°C)/(30°C/W) = 2.67W for a WQFN-20L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 11 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

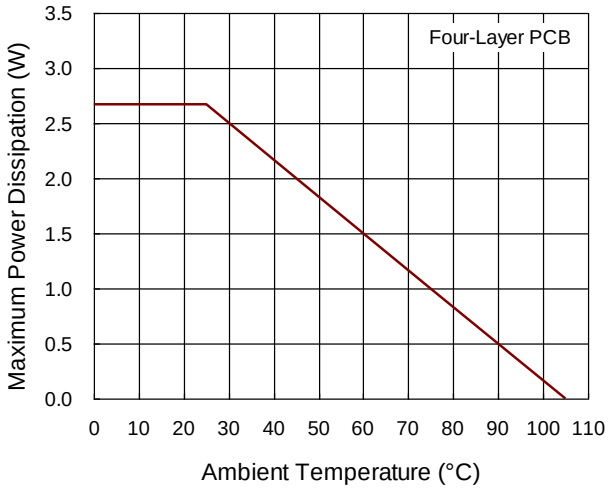

Figure 11. Derating Curve of Maximum Power Dissipation

Layout Considerations

Layout is very important in high frequency switching converter design. If designed improperly, the PCB can radiate excessive noise and contribute to the converter instability. Following layout guidelines must be considered before starting a layout for the RT8692.

- Place the RC filter as close as possible to the PVCC pin.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as VSNS, RGND, EN, PSI, PGOOD, VREF, TON and REFIN should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.

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- Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.

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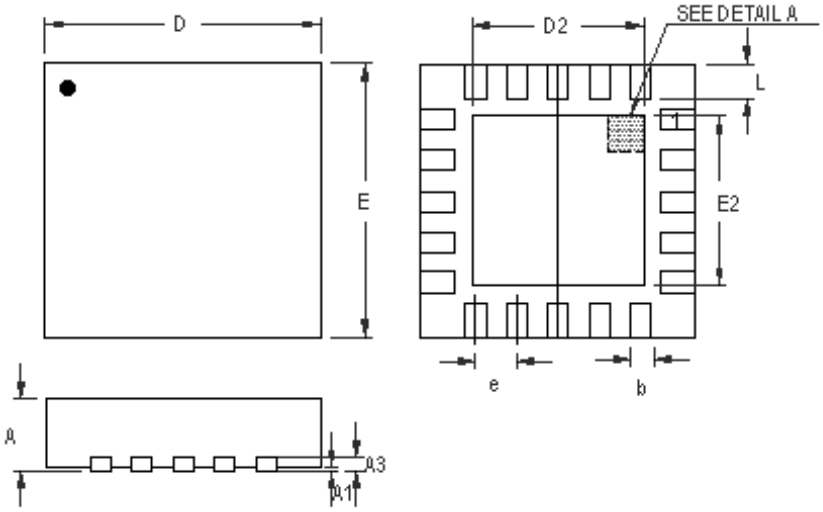
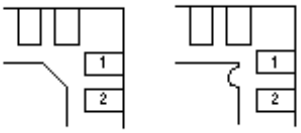
Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D2	1.650	1.750	0.065	0.069
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 20L QFN 3x3 Package

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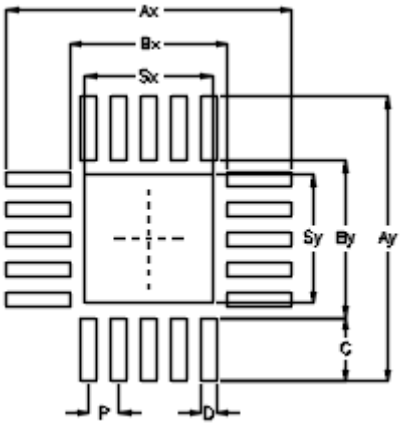
Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3*3-20	20	0.40	3.80	3.80	2.10	2.10	0.85	0.20	1.70	1.70	±0.05

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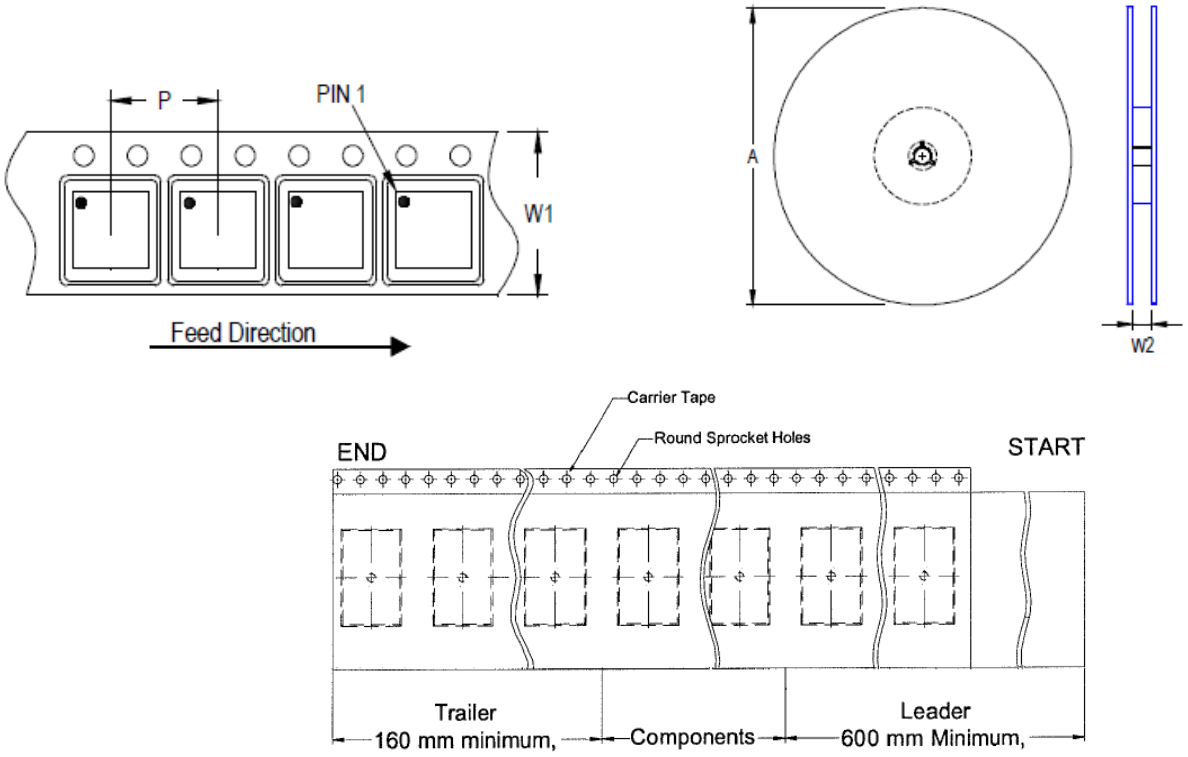
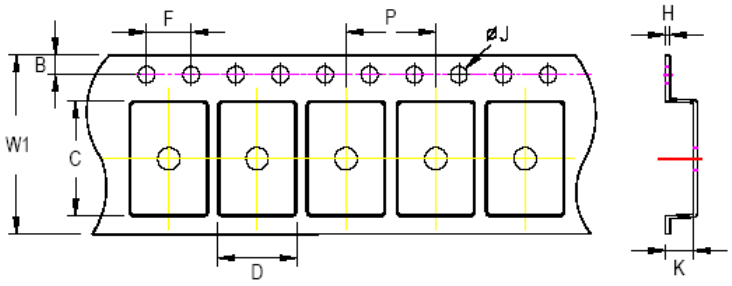
Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

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Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN & DFN 3x3	7”	1,500	Box A	18.3*18.3*8.0	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	1	1,500	For Combined or Partial Reel.			

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Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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RICHTEK

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Datasheet Revision History

Version	Date	Description	Item
00	2023/8/17	Final	

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