RICHTEK®

RT8843A/RT8843B/RT8843D

Multi-Phase PWM Controller with PWM-VID Reference

1 General Description

The RT8843A/RT8843B/RT8843D is a 3/2/1 multi-phase synchronous buck controller optimized for high-performance graphic microprocessors and supports the nVidia OVR3i+ specification with a PWM-VID interface. It can support both DrMOS with current output and DCR current sensing. The RT8843A/RT8843B/RT8843D adopts AC G-NAVP™ (Green Native AVP), which is Richtek's proprietary topology derived from the finite DC gain of the internal GM amplifier with current mode control. By utilizing the AC G-NAVP™ topology, the operating frequency of the RT8843A/RT8843B/RT8843D varies with VID, load, and input voltage to further enhance efficiency, even in CCM (Continuous Conduction Mode). Moreover, the AC G-NAVP™ with CCRCOT (Constant Current Ripple COT) technology provides superior output voltage ripple over the entire input/output range.

The RT8843A/RT8843B/RT8843D features an external reference input and PWM-VID dynamic output voltage control, where the output voltage is regulated and tracks the external input reference voltage. The RT8843A/RT8843B/RT8843D can set the internal RAMP amplitude through the PINSETx pin, optimizing stability and load transient performance. The RT8843A/RT8843B/RT8843D also provides complete fault protection functions, including Overvoltage Protection (OVP), Undervoltage Protection (UVP), Per-phase Current Limit, and Over-Temperature Protection (OTP). The recommended junction temperature range is from –40°C to 125°C.

2 Features

- **Multi-Phase PWM Controller**
- **PWM Tri-State Voltage, Pre-Short UVP**
  - **RT8843A: 1.95V, without Pre-Short UVP**
  - **RT8843B: 1.65V, without Pre-Short UVP**
  - **RT8843D: 1.65V, with Pre-Short UVP**
- **PWM-VID Dynamic Output Voltage Control**
- **Support 1.8V PWM-VID Interface**
- **Power State Indicator**
  - **1-Phase-DEM, Full-Phase DEM, Full-Phase CCM**
- **External Reference Input Control**
- **3/2/1-Phase Hardware Setting**
- **Adjustable Soft-Start Time**
- **Adjustable Per-Phase Current-Limit Threshold**
- **Adjustable Switching Frequency**
- **UVP, OVP, OTP Protection**
- **Pre-Short UVP Protection for RT8843D**
- **Power-Good Indicator**

3 Applications

- GPU Core Power for OVR3i+ Specification

4 Ordering Information

RT8843□□□

Package Type[1]
QW: WQFN-20L 3x3 (W-Type)

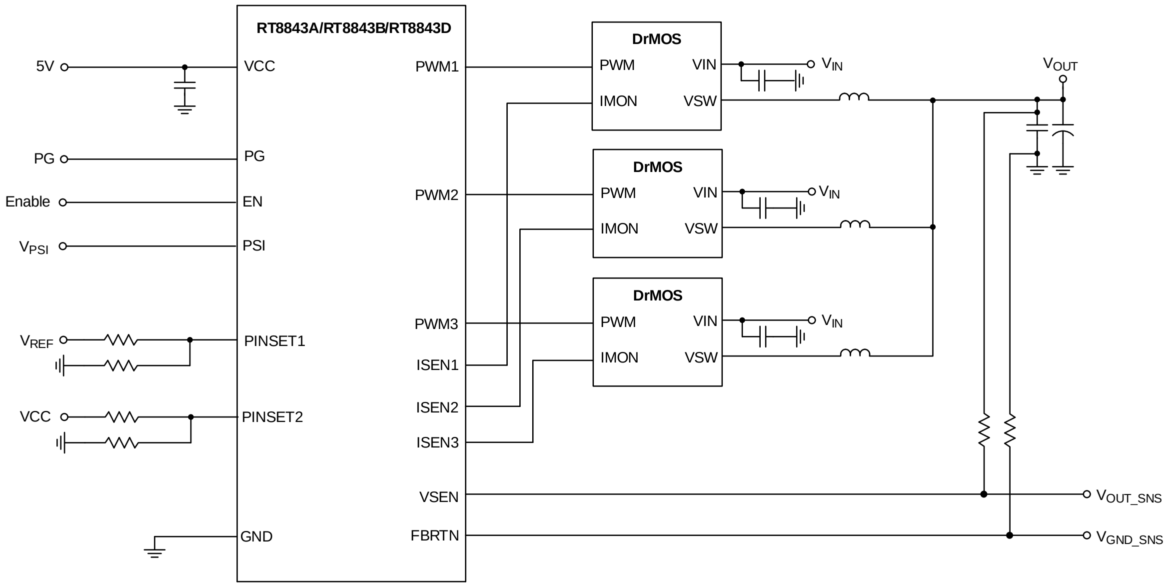
Lead Plating System
G: Richtek Green Policy Compliant[2]

PWM Tri-State Voltage, Pre-Short UVP
A: 1.95V, without Pre-Short UVP
B: 1.65V, without Pre-Short UVP
D: 1.65V, with Pre-Short UVP

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

5 Simplified Application Circuit



6 Marking Information

RT8843A

PJ=YM
DNN

PJ=: Product Code
YMDNN: Date Code

RT8843D

XW=YM
DAN

XW=: Product Code
YMDAN: Date Code

RT8843B

T0=YM
DNN

T0=: Product Code
YMDNN: Date Code

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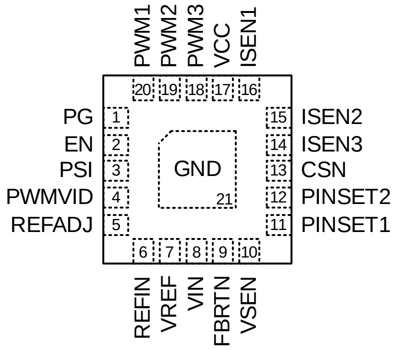
7 Pin Configuration



WQFN-20L 3x3

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PG	Power-Good indicator output. Active high open-drain output. A 10k pull high resistor is needed.
2	EN	Enable control input. Active high input.
3	PSI	Controller power state setting input. H: full-phase CCM. MID: full-phase DEM. L:1-phase DEM.
4	PWMVID	Programming output voltage control input. Refer to PWM-VID Dynamic Output Voltage Control.
5	REFADJ	Reference adjustment output. Refer to PWM-VID Dynamic Output Voltage Control.
6	REFIN	External reference input.
7	VREF	Reference voltage output. This is a high-precision reference voltage (2V) from the VREF pin to the FBRTN pin. A ceramic capacitor connected between this pin and FBRTN should be 0.1μF.
8	VIN	Connect an R_{TON} resistor from this pin to the input voltage to set the frequency. Do not place a decoupling capacitor on this pin.
9	FBRTN	Return ground. This pin is the negative input of the output voltage differential remote sense.
10	VSEN	Voltage sense input. This pin is connected to the output voltage terminal.
11	PINSET1	Soft-start, internal ramp, and OCSET setting input. Do not place a decoupling capacitor on this pin
12	PINSET2	DrMOS IMON function, Auto-ZCD function, and Internal compensation setting input. Do not place a decoupling capacitor on this pin.
13	CSN	Output 1.36V when the DrMOS IMON function is enabled.
14, 15, 16	ISEN[3:1]	Current sense inputs of phases 1, 2, and 3. These pins can also be used for hardware setting of the multi-phase number. When an ISENx pin is pulled up to VCC with a 100kΩ resistor, the PHASEx is disabled and the maximum phase number reduces to x-1. For example, if the ISEN2 pin is pulled up to VCC, the maximum phase number is 1. Both PHASE2 and PHASE3 are disabled.
17	VCC	Supply voltage input. Connect this pin to a 5V bias supply. Place a high-quality bypass capacitor from this pin to GND.
18, 19, 20	PWM[3:1]	PWM outputs.
21 (Exposed Pad)	GND	Ground. The exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation.

9 Functional Block Diagram

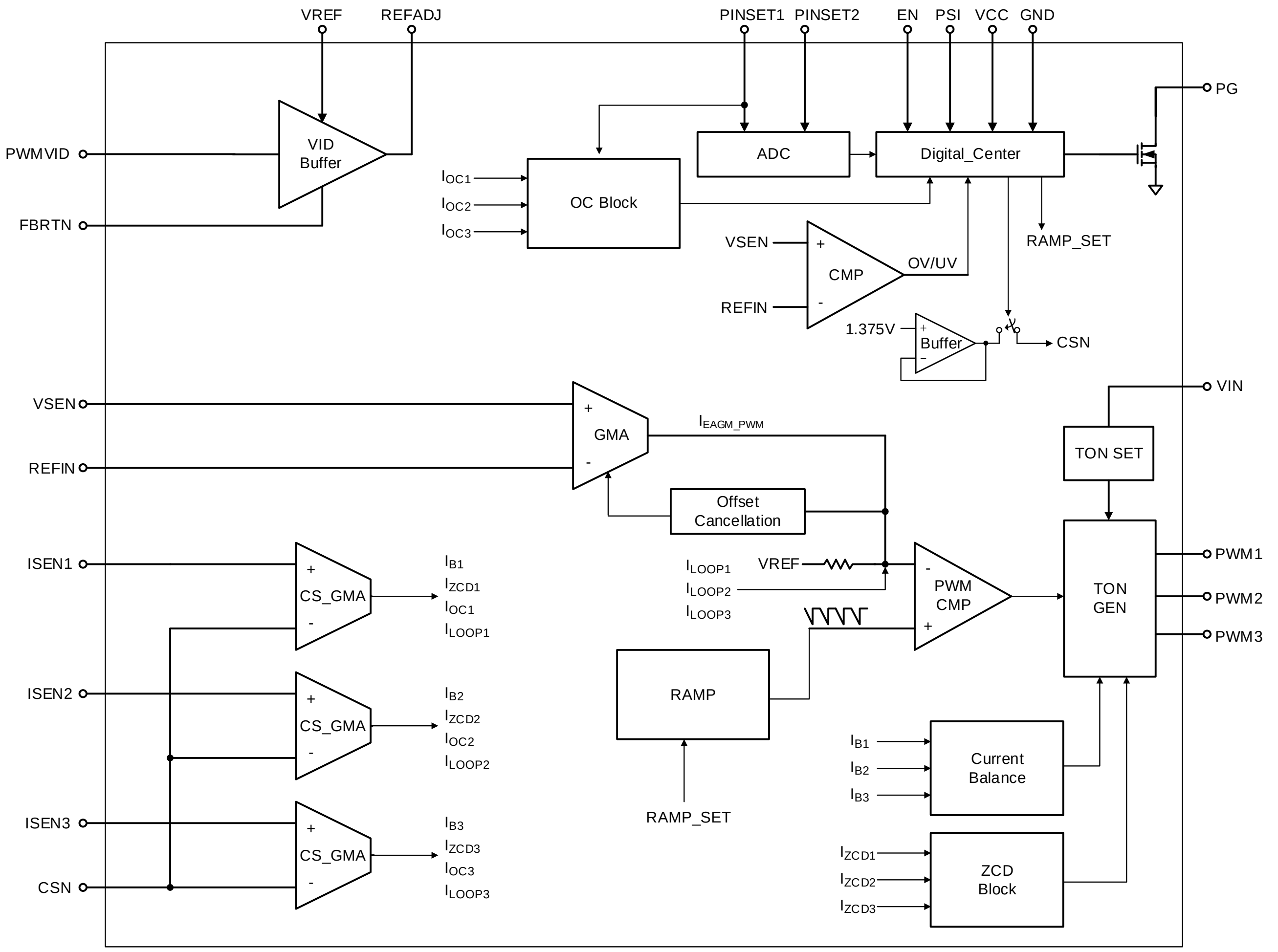


Figure 1. Functional Block Diagram for RT8843A/RT8843B

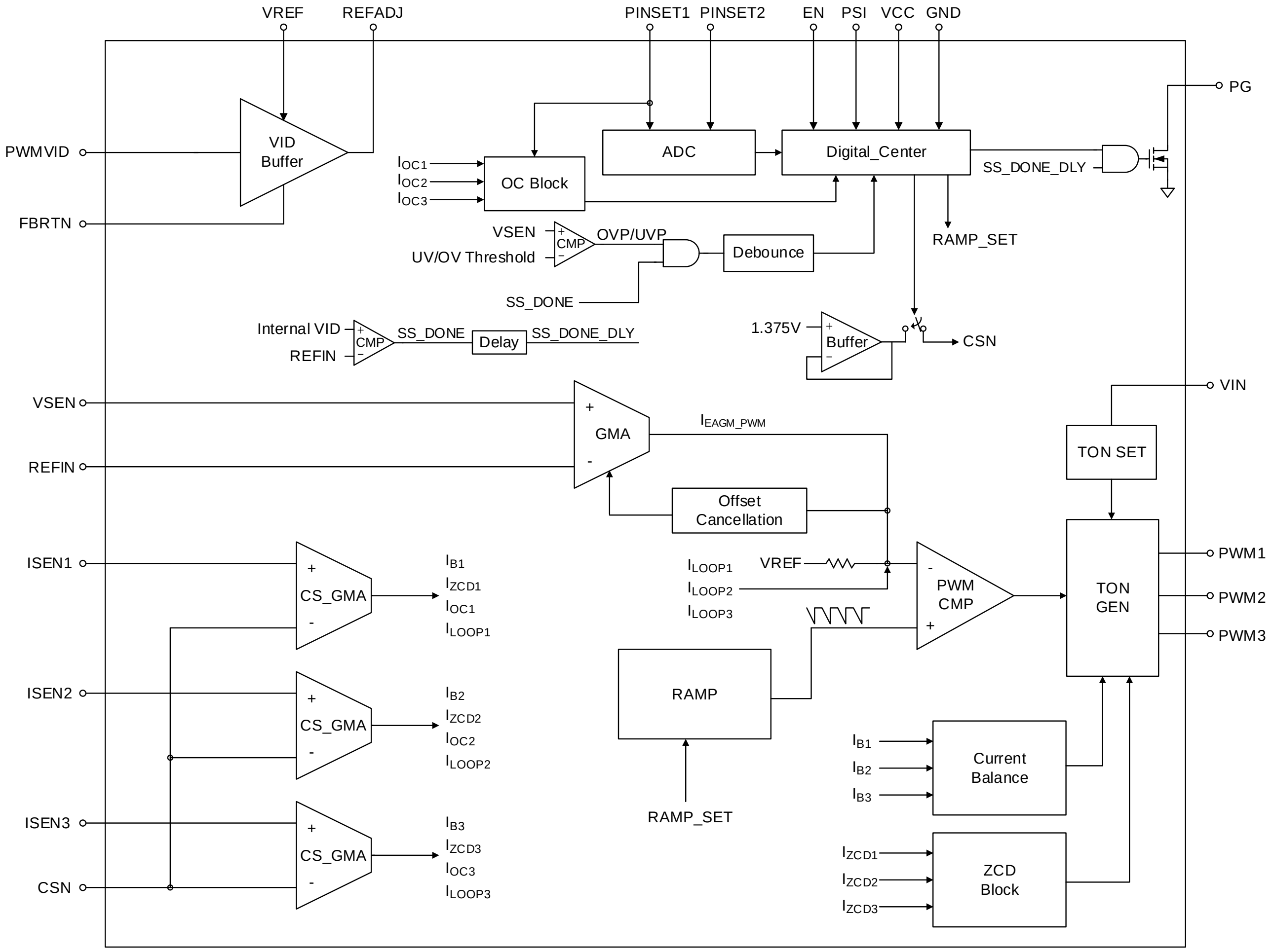


Figure 2. Functional Block Diagram for RT8843D

10 Absolute Maximum Ratings

(Note 2)

- VIN to GND ---------- –0.3 to 28V
- VCC to GND ---------- –0.3 to 6V
- FBRTN to GND ---------- –0.3 to 0.3V
- Other Pins ---------- –0.3 to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-20L 3x3 ---------- 3.33W
- Package Thermal Resistance (Note 3)
  WQFN-20L 3x3, θ_{JA} ---------- 30°C/W
  WQFN-20L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM ---------- 2kV

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Input Voltage, V_{IN} ---------- 2.7 to 25V
- Supply Voltage, V_{VCC} ---------- 4.5 to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{VCC} = 5V, typical values are referenced to T_A = T_J = 25°C, Min and Max values are referenced to T_A = T_J from –10°C to 105°C, unless other noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
VCC Supply Voltage	V_{CC}		4.5	5	5.5	V
VCC Supply Current	I_{VCC}	EN = high, not switching	--	6	--	mA
VCC Shutdown Current	I_{SHDN}	EN = 0V	--	--	10	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC POR Threshold	$V_{CC\_UVLO\_R}$	VCC rising voltage	--	4.3	--	V
VCC UVLO Threshold	$V_{CC\_UVLO\_F}$	VCC falling voltage	--	4.1	--	V
POR Hysteresis	$V_{CC\_UVLO\_HYS}$		--	200	--	mV
Reference Voltage						
Reference Voltage	V_{REF}		1.98	2	2.02	V
CSN Output Voltage	V_{CSN_OUT}		1.3	1.375	1.45	V
PWMVID Input Voltage						
PWMVID Input Voltage Logic-High	V_{PWMVID_H}		1.2	--	--	V
PWMVID Input Voltage Logic-Low	V_{PWMVID_L}		--	--	0.6	V
Soft-Start						
Soft-Start Ramp Up Slew Rate	SR_{SS}	Slew rate set to 1mV/μs	0.9	1	1.1	mVμs
PG Blanking Time	t_{PG}	From EN go high to PG go high	--	--	2	ms
EN and Logic Input						
EN Threshold	V_{EN_H}	Logic high level	0.7	--	--	V
	V_{EN_L}	Logic low level	--	--	0.3	
Leakage Current of EN	I_{EN_ILK}		–1	--	1	μA
Leakage Current of PG	I_{PG_ILK}		–1	--	1	μA
Leakage Current of PSI	I_{PSI_ILK}		–1	--	1	μA
PSI Input Voltage						
PSI Logic High Threshold	V_{PSI_IH}		1.6	--	--	V
PSI Logic Tri-State Threshold	V_{PSI_HIZ}		0.8	--	1.2	V
PSI Logic Low Threshold	V_{PSI_IL}		--	--	0.4	V
TON Setting						
ON-Time Setting	t_{ON}	I_{TON} = 40μA, V_{REFIN} = 1V	190	210	230	ns
I_{PINSET}						
PIN SET Current	I_{PINSET}	V_{PINSET} = 1V	79.2	80	80.8	μA
EA/GM Amplifier						
Input Offset	V_{EAOFS}		–3	--	3	mV
CS Amplifier						
Input Offset	V_{EAOFS}		–0.6	--	0.6	mV
Protection Function						

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Relative Overvoltage Protection Threshold	V_{ROVP}	$V_{REFIN} \geq 1.33V$	142.5	150	157.5	%
Absolute Overvoltage Protection Threshold	V_{ABOVP}	$V_{REFIN} < 1.33V$,	1.9	2	2.1	V
OV Fault Delay	t_{DLY_OVP}	FB forced above OV threshold	--	5	--	μs
Relative Undervoltage Protection Threshold	V_{RUVP}		35	40	45	%
UV Fault Delay	t_{DLY_UVP}	FB forced above UV threshold	--	3	--	μs
Over-Temperature Protection Threshold	T_{OTP}		--	150	--	°C
Voltage between ISENx and CSN Pins	$V_{ISENx-CSN}$	V_{OCSET} = 800mV, ISNEx – CSN, for DCR DrMOS Application	21	25	29	mV
		V_{OCSET} = 800mV, ISENx – CSN, for SPS DrMOS Application	70	77	84	mV
PWM Driving Capability						
PWM Source Resistance	R_{PWM_SRC}		--	30	--	Ω
PWM Sink Resistance	R_{PWM_SNK}		--	10	--	Ω
PWM Tri-State Voltage (Note 6)	V_{PWM_Tri}	RT8843A	1.65	1.95	2.2	V
		RT8843B/RT8843D	1.4	1.65	1.9	V

Note 6. Pull the PWM to the HIZ voltage for 200ns when the PWM enters HIZ.

13 Typical Application Circuit

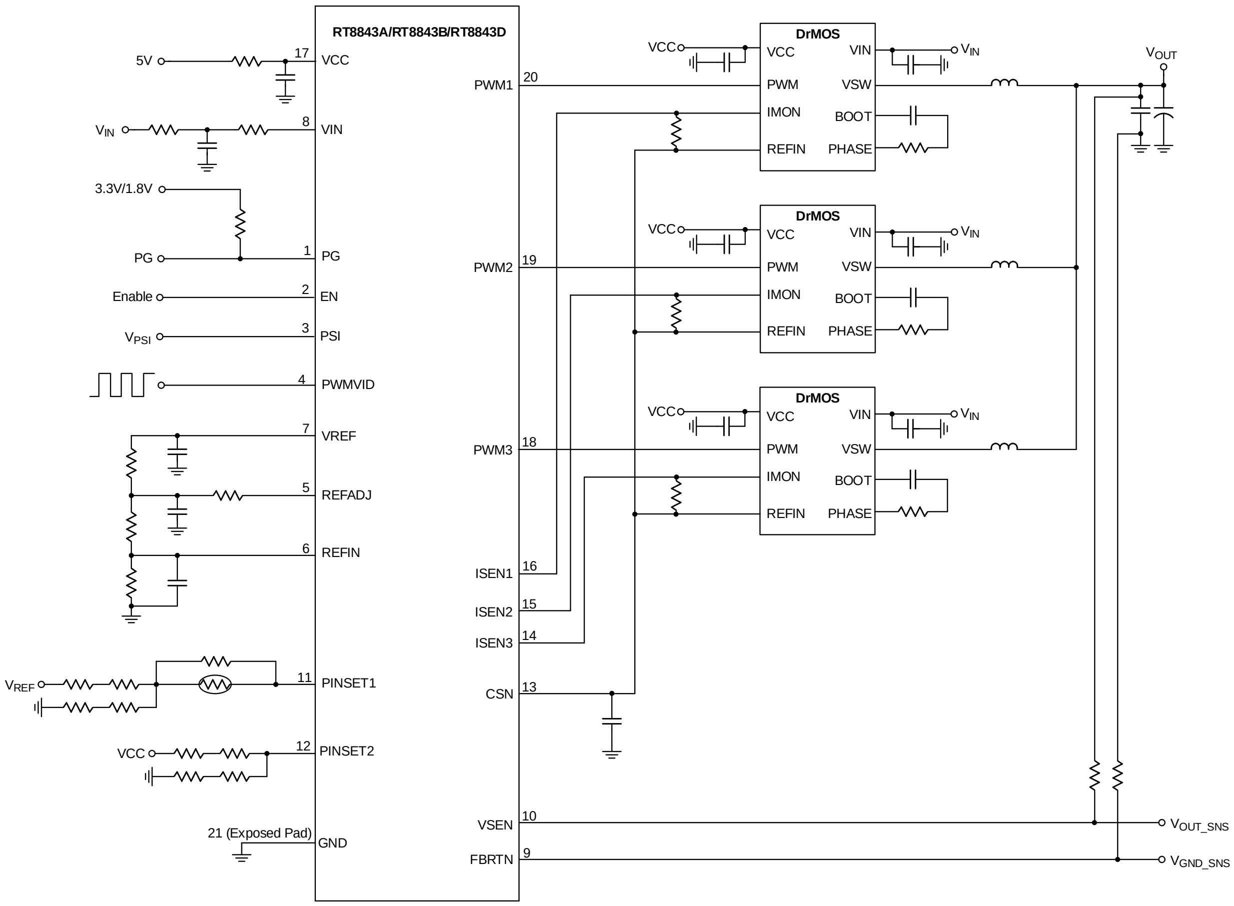


Figure 3. 3-Active Phase IMON Configuration

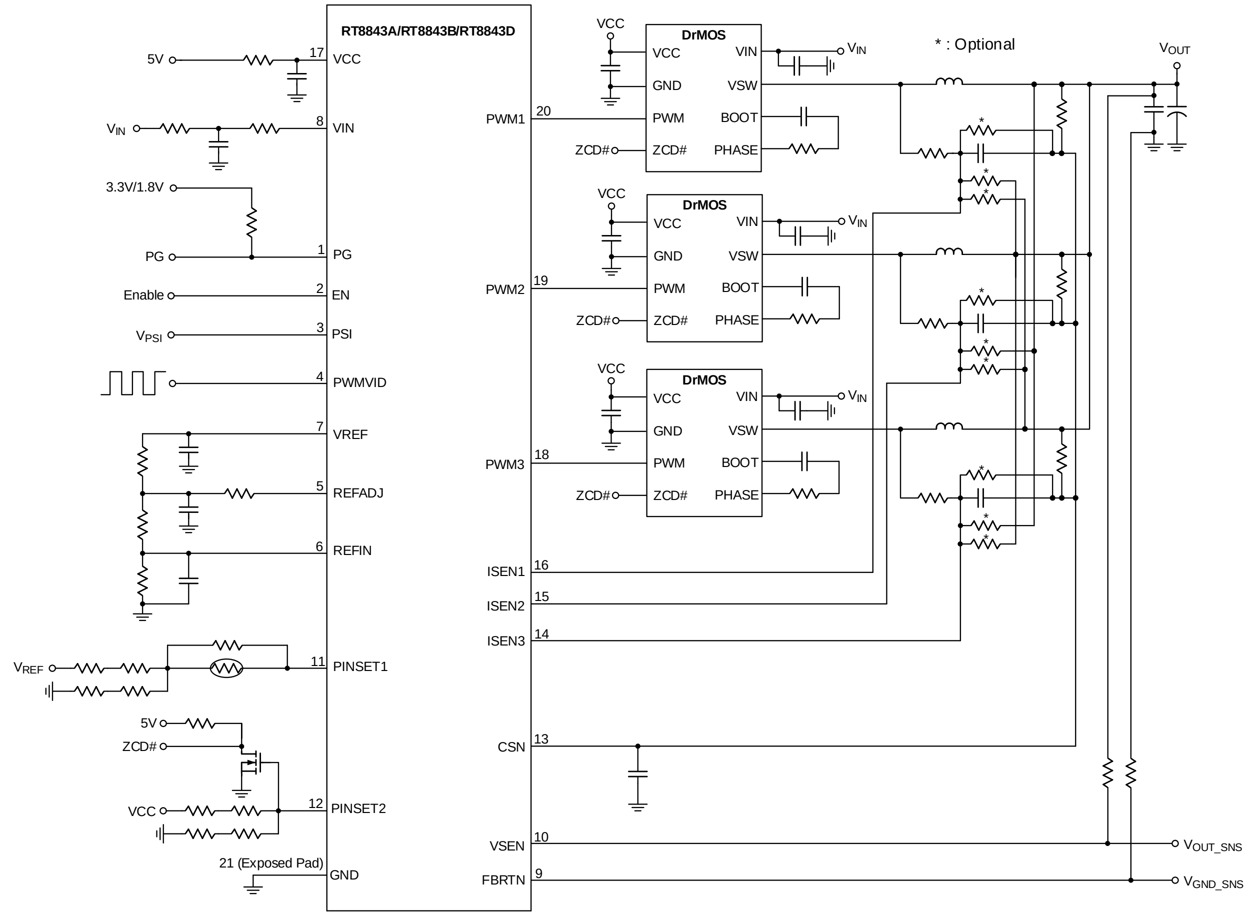
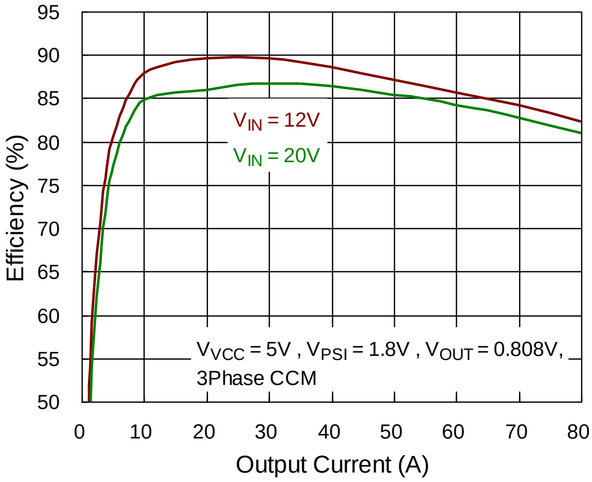


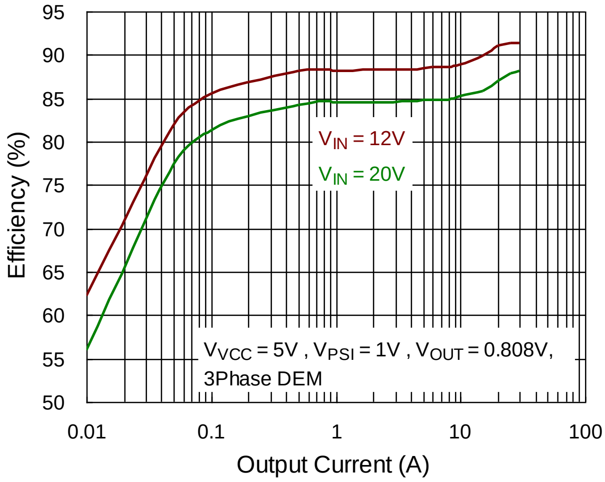
Figure 4. 3-Active Phase DCR Configuration

14 Typical Operating Characteristics

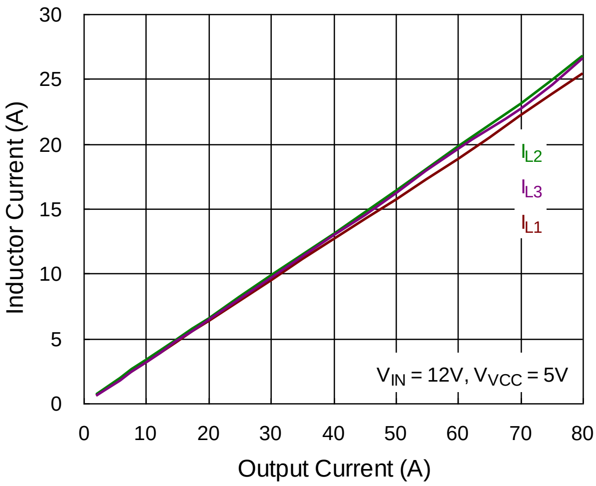
Efficiency vs. Output Current



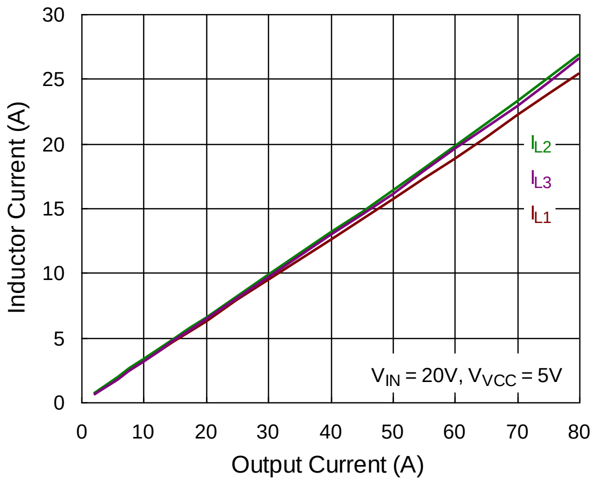
Efficiency vs. Output Current



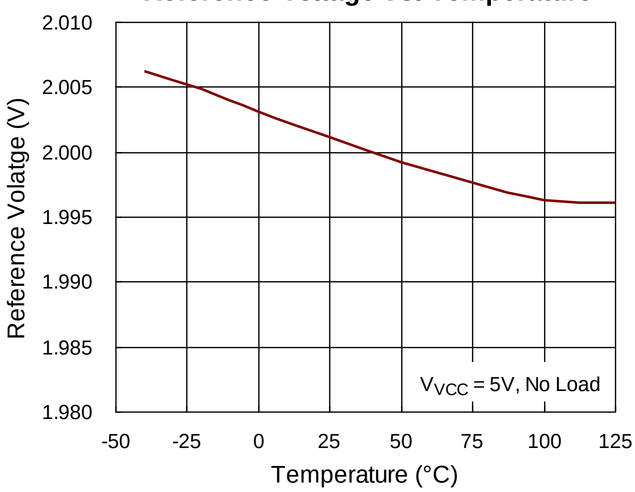
Inductor Current vs. Output Current



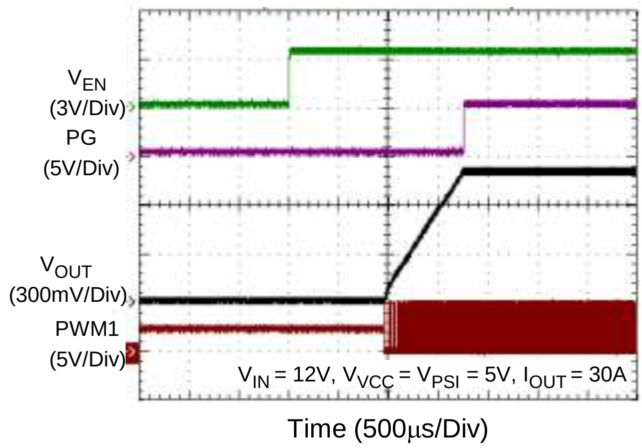
Inductor Current vs. Output Current



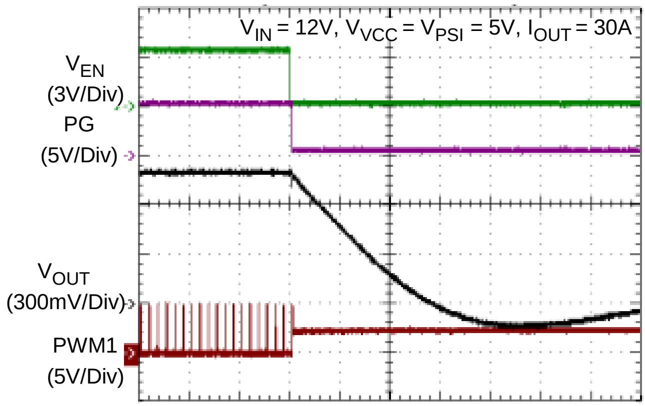
Reference Voltage vs. Temperature



Power On from EN

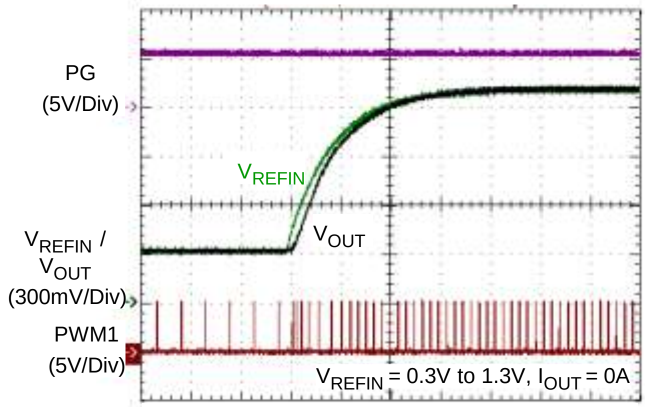


Power Off from EN



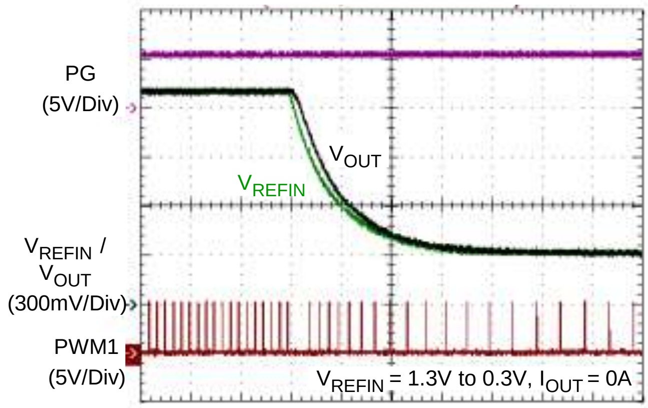
Time (20μs/Div)

Dynamic Output Voltage Control



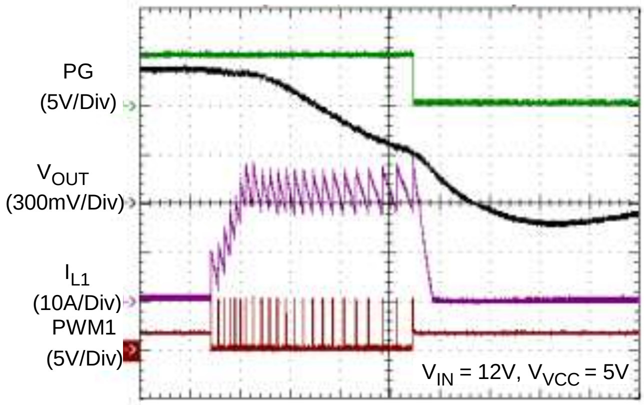
Time (20μs/Div)

Dynamic Output Voltage Control



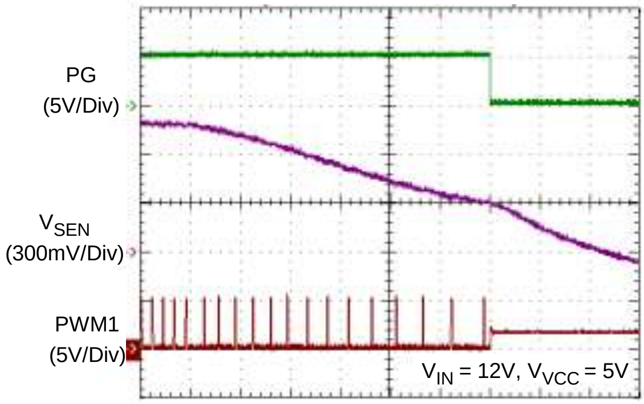
Time (20μs/Div)

Per Phase Current Limit



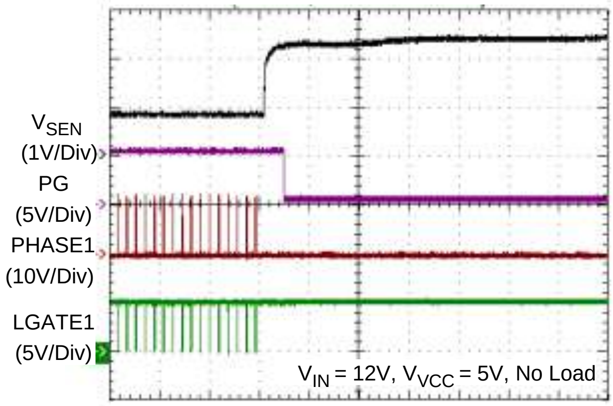
Time (20μs/Div)

UVP



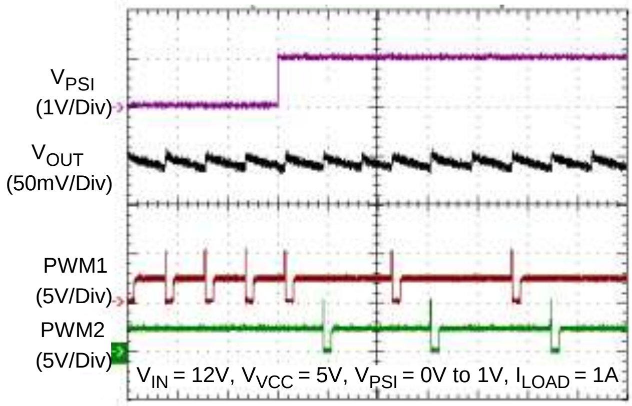
Time (10μs/Div)

OVP



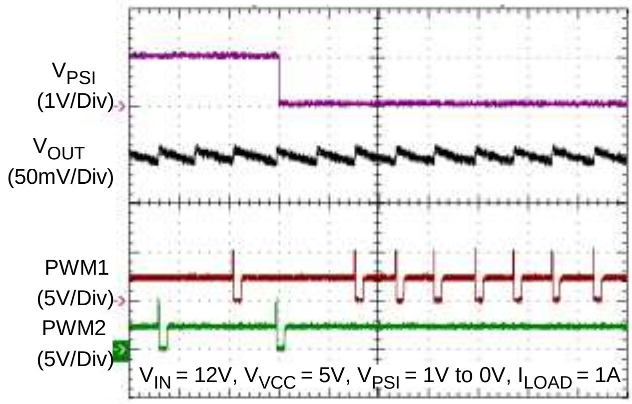
Time (20μs/Div)

Mode Transition



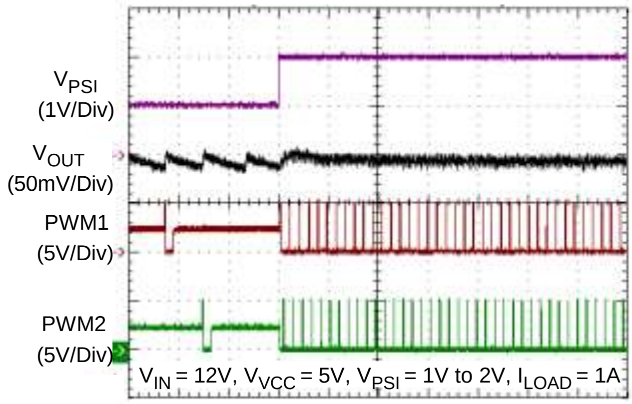
Time (20μs/Div)

Mode Transition



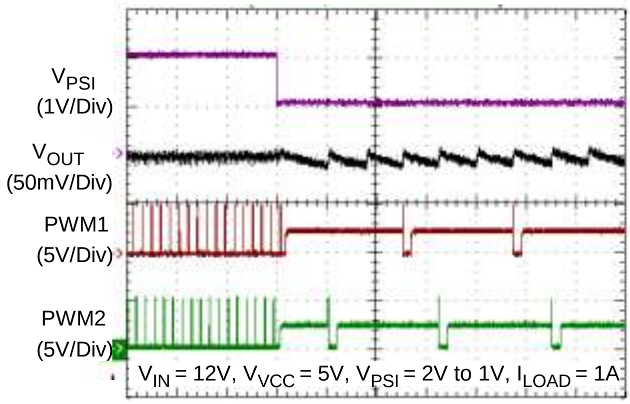
Time (20μs/Div)

Mode Transition



Time (20μs/Div)

Mode Transition



Time (20μs/Div)

15 Application Information

(Note 8)

The RT8843A/RT8843B/RT8843D is a multi-phase synchronous buck controller optimized for high-performance graphic microprocessors and computer applications.

The RT8843A/RT8843B/RT8843D adopts AC G-NAVP^{TM} (Green Native Adaptive Voltage Positioning), which is Richtek's proprietary topology derived from the finite DC gain of the internal GM amplifier with current mode control. By utilizing the AC G-NAVP^{TM} topology, the operating frequency of the RT8843A/RT8843B/RT8843D varies with VID, load, and input voltage to further enhance the efficiency, even in CCM. Moreover, the AC G-NAVP^{TM} with CCRCOT (Constant Current Ripple COT) technology provides superior output voltage ripple over the entire input/output range.

The RT8843A/RT8843B/RT8843D features an external reference input and PWM-VID dynamic output voltage control, where the output voltage is regulated and tracks the external input reference voltage. In addition, the RT8843A/RT8843B/RT8843D integrates multiple functions, including Internal-Ramp-Setting, AI Gain Selection, Soft-Start Time Setting, SPS Current Sensing, Auto-Zero-Current Detection, and Per-phase Current Limit. These functions can be achieved through the PINSET voltage settings. The RT8843A/RT8843B/RT8843D also provides comprehensive protection including Overvoltage Protection (OVP), Undervoltage Protection (UVP), and Over-Temperature Protection (OTP).

15.1 Power-On Reset (POR), UVLO

Power-On Reset (POR) occurs when V_{VCC} rises to approximately 4.3V (typical), and the RT8843A/RT8843B/RT8843D resets the fault latch circuit and prepares for PWM operation.

When the V_{VCC} is lower than 4.1V (typical), the PWMx signal is kept low to inhibit any switching through Undervoltage-Lockout (UVLO).

15.2 Enable and Disable

The EN pin is a high-impedance input that allows power sequencing between the controller bias voltage and another voltage rail. The RT8843A/RT8843B/RT8843D remains in shutdown mode if the EN pin voltage is lower than 300mV. When the EN voltage rises above the 700mV high-level threshold, the RT8843A/RT8843B/RT8843D begins a new initialization and soft-start cycle. The EN timing must occur after VCC POR to ensure that the PINSET function can be set normally.

15.3 Power-Good Indicator (PG)

The PG pin is an open-drain output and requires a pull-up resistor. During the soft-start time period, PG remains low. When the output voltage reaches the REFIN voltage, PG is pulled high and latched. If OVP/UVP is triggered or EN goes low during operation, PG will be pulled low immediately.

15.4 Operation Mode Setting

The RT8843A/RT8843B/RT8843D provides three operation modes: 1-phase with DEM, multi-phase with DEM, and multi-phase with CCM. In DEM operation, the RT8843A/RT8843B/RT8843D automatically reduces the operation frequency under light-load conditions for saving power loss. The operating mode can be set by the voltage of the PSI pin, as listed in Table 1. Moreover, the PSI pin is valid after POR of VR.

Table 1

Operation Mode	PSI Voltage Setting
1-Phase with DEM	0V to 0.4V
Multi-Phase with DEM (Note 7)	0.8V to 1.2V
Multi-Phase with CCM (Note 7)	1.6V to 5.5V

Note 7. Multi-phase number by hardware setting

15.5 PWM-VID Dynamic Output Voltage Control

The RT8843A/RT8843B/RT8843D features a PWM-VID input for dynamic output voltage control, as shown in Figure 5. This design reduces the number of device pins and enables a wide dynamic voltage range. The output voltage is determined by the applied voltage on the REFIN pin and the duty cycle of PWMVID.

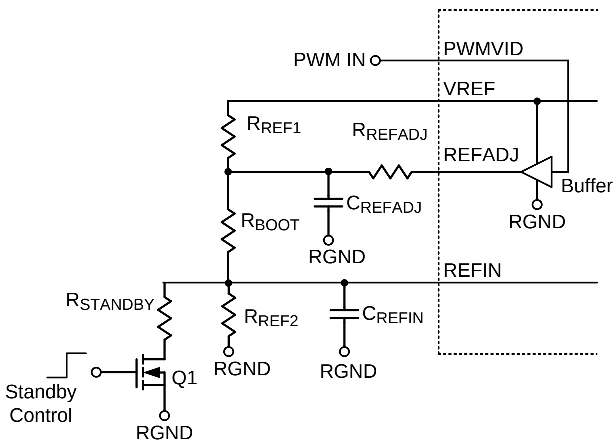


Figure 5. PWM-VID Analog Circuit Diagram

Through utilizing the external circuit and the VID control signal, the controller provides three operation modes, as shown in Figure 6.

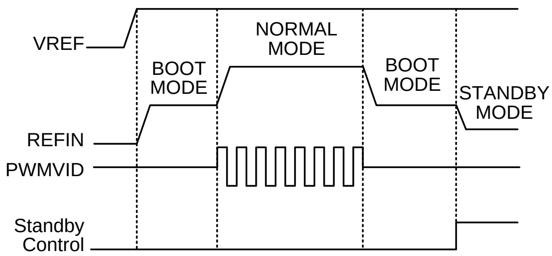


Figure 6. PWM-VID Time Diagram

15.6 BOOT Mode

When the PWMVID is not driven, the buffer output is in a tri-state condition. At this time, the PWM-VID circuit is working in BOOT mode, and Q1 is turned off. Furthermore, REFIN is connected to a resistor divider, as shown in Figure 5. The following equation expresses the V_{BOOT} equation from REFIN and the divider resistors.

$$V_{BOOT} = V_{VREF} \times \left(\frac{R_{REF2}}{R_{REF1} + R_{REF2} + R_{BOOT}} \right)$$

where V_{VREF} = 2V (typical)

Choose R_{REF2} to be approximately 10kΩ, and the R_{REF1} and R_{BOOT} can be calculated using the following equations:

$$R_{REF1} + R_{BOOT} = \frac{R_{REF2} \times (V_{VREF} - V_{BOOT})}{V_{BOOT}}$$

$$R_{REF1} = \frac{R_{REF2} \times (V_{VREF} - V_{BOOT})}{V_{BOOT}} - R_{BOOT}$$

$$R_{BOOT} = \frac{R_{REF2} \times (V_{VERF} - V_{BOOT})}{V_{BOOT}} - R_{REF1}$$

15.7 Standby Mode

When the PWMVID control enters the standby mode, the standby voltage can be set via $R_{STANDBY}$ and Q1, as shown in Figure 5. The standby voltage is set to a voltage that is lower than the PWMVID operating range. Assuming the PWMVID operating range is 0.3V to 1.3V, then the standby voltage will be set below 0.3V. However, if the REFIN voltage is lower than 0.2V, the controller will pull the PWM signal into a tri-state. Therefore, the standby voltage setting range is recommended from 0.2V to the lowest voltage of the PWMVID operation voltage.

The following conditions must be met when entering standby mode:

- The PWMVID pin is floating.
- Q1 is enabled.

Furthermore, the desired value can be set using the following equation:

$$V_{STANDBY} = V_{VREF} \times \frac{R_{REF2} // R_{STANDBY}}{R_{REF1} + R_{BOOT} + (R_{REF2} // R_{STANDBY})}$$

By choosing R_{REF1}, R_{REF2}, and R_{BOOT}, the $R_{STANDBY}$ can be calculated using the following equation:

$$R_{STANDBY} = \frac{V_{STANDBY} \times R_{REF2} \times (R_{REF1} + R_{BOOT})}{V_{VREF} \times R_{REF2} - V_{STANDBY} \times (R_{REF1} + R_{REF2} + R_{BOOT})}$$

15.8 Normal Mode

If the PWMVID pin is driven by a PWM signal and switch Q1 is disabled, as shown in Figure 5. The V_{REFIN} can be adjusted from V_{min} to V_{max}, where V_{min} is the voltage at zero percent PWM duty cycle, and V_{max} is the voltage at one hundred percent PWM duty cycle. V_{min} and V_{max} can be set using the following equations:

$$V_{min} = V_{VREF} \times \frac{R_{REF2}}{R_{REF2} + R_{BOOT}} \times \frac{R_{REFADJ} // (R_{BOOT} + R_{REF2})}{R_{REF1} + \left[(R_{REFADJ} // (R_{BOOT} + R_{REF2})) \right]}$$

$$V_{max} = V_{VREF} \times \frac{R_{REF2}}{(R_{REF1} // R_{REFADJ}) + R_{BOOT} + R_{REF2}}$$

By choosing R_{REF1}, R_{REF2}, and R_{BOOT}, the R_{REFADJ} can be calculated using the following equation:

$$R_{REFADJ} = \frac{R_{REF1} \times V_{min}}{V_{max} - V_{min}}$$

The relationship between PWMVID duty and V_{REFIN} is shown in Figure 7, and V_{OUT} can be set according to the following equation:

$$V_{OUT} = V_{min} + N \times V_{STEP}$$

where V_{STEP} is the resolution of each voltage step:

$$V_{STEP} = \frac{V_{max} - V_{min}}{N_{max}}$$

where N_{max} is the total number of available voltage steps, and N is the number of steps at a specific V_{OUT}. The dynamic voltage VID period ($T_{vid} = T_u \times N_{max}$) is determined by the unit pulse width (T_u), and the available step number (N_{max}). The recommended T_u is 27ns.

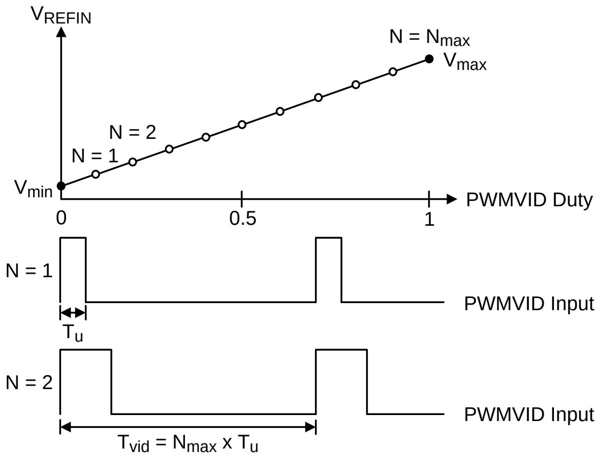


Figure 7. PWM-VID Analog Output

15.9 VID Slew Rate Control

In the RT8843A/RT8843B/RT8843D, the V_{REFIN} slew rate is proportional to the PWM-VID duty, and the rising time and falling time are the same. In normal mode, the V_{REFIN} slew rate SR can be estimated by C_{REFADJ} using the following equation:

$$SR = \frac{\left(V_{REFIN\_Final} - V_{REFIN\_Initial}\right) \times 80\%}{2.2 \times R_{SR} \times C_{REFADJ}}$$

$$R_{SR} = \left[\left(R_{REF1} // R_{REFADJ}\right)\right] // \left(R_{BOOT} + R_{REF2}\right)$$

15.10 Remote Sense Setting

To accurately detect the load voltage and avoid the voltage drop from the output to the load, the RT8843A/RT8843B/RT8843D uses a high-accuracy differential amplifier to directly detect the voltage at the end of the GPU through the VSEN and FBRTN pins. The V_{OUT} sensing network from the controller to the load and output needs to be specially designed according to different load conditions. The output voltage detection circuit has two loops: the remote sense path (from the controller to the load end of the GPU) and the local sense path (from the controller to the output capacitor), as shown in Figure 8. When the load is the GPU, in order to make the GPU voltage consistent with R_{EFIN}, the R_{Remote} must be set to 0Ω. At this time, the purpose of the local sense path is to avoid the output overvoltage caused by an open GPU. Therefore, R_{Local} must be placed with a 10Ω to 100Ω resistor. If the GPU is not used and the load is from the end of V_{OUT}, the R_{Local} must be set to 0Ω to avoid PWM jitter caused by a delayed output voltage signal. Considering the component placement, it is recommended to place all the detecting resistors on the controller side. This setting minimizes the local sense path and makes system debugging easier as any noise coupling occurring on the sensing path.

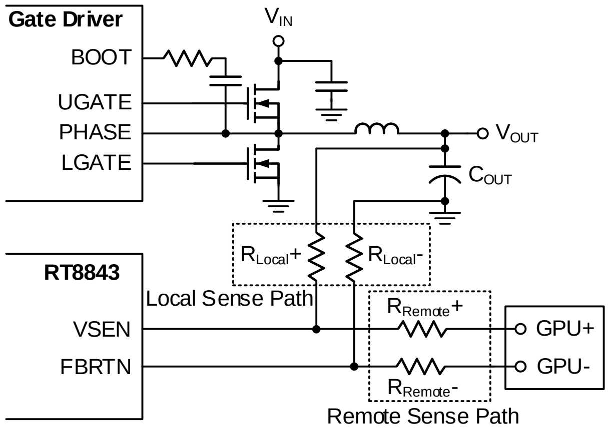


Figure 8. Output Voltage Sensing

15.11 Multi-Function Pin Setting

To reduce the total number of pins required for the package, the RT8843A/RT8843B/RT8843D utilizes a multi-function pin setting mechanism through PINSET1 and PINSET2 pins. Table 2 summarizes the overall pin setting functions. Figure 9 shows the Pin Setting Circuit. The voltage divider for each PINSET pin is used to set the desired function. The setting voltage of each PINSET pin can be represented as follows:

$$V_{PINSET1} = V_{REF}(2V) \times \frac{R3 + R4}{R1 + R2 + R3 + R4}$$

$$V_{PINSET2\_V} = V_{VCC}(5V) \times \frac{R3 + R4}{R1 + R2 + R3 + R4}$$

$$V_{PINSET2\_I} = 80\mu \times \frac{(R1 + R2) \times (R3 + R4)}{R1 + R2 + R3 + R4}$$

Table 3, Table 4, and Table 5 show the pin setting functions. Table 6 shows an example of the ramp configuration for a typical 300kHz application.

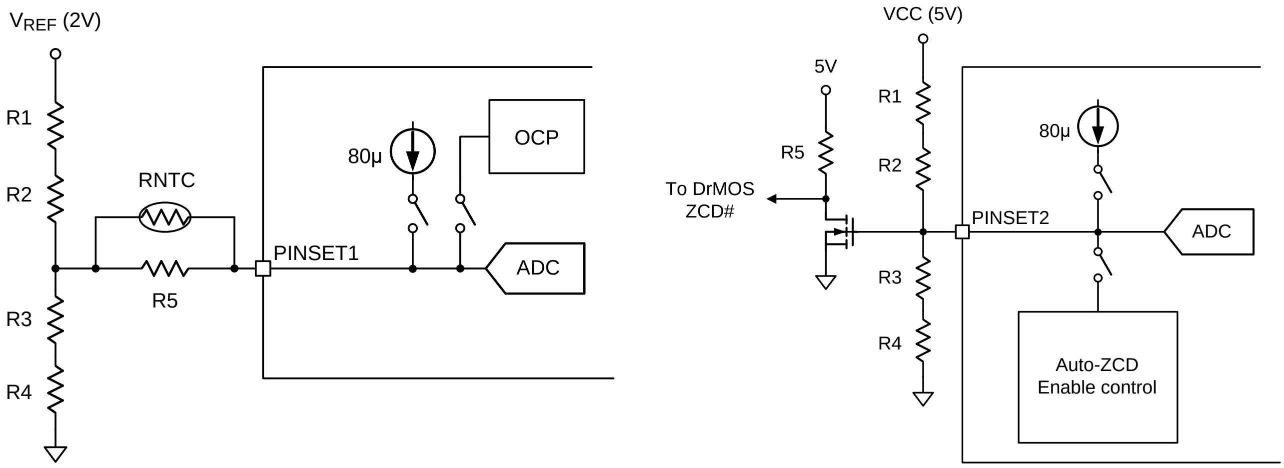


Figure 9. Multi-Function Pin Setting Circuit

Table 2. Pin Set Table

	Function 1	Function 2	Function 2	Function 3	Function 4
PINSET1	Soft-Start Slew Rate	Ramp Amplitude <2:0>	N/A	N/A	N/A
PINSET2	Ramp Valley	Ramp Amplitude <3>	Dr.IMON Enable/Disable	Auto-ZCD Enable/Disable	AI Gain

Table 3. PINSET1 Pin Setting for Soft-Start Slew Rate and Ramp Amplitude

SS Slew Rate (mV/μs)	RAMP Amplitude <2:0> (mV) $V_{RAMP\_AMP} = \frac{30000 \times (16 - RAMP <3:0>)}{f_S}$			$V_{PINSET1} = V_{REF}(2V) \times \frac{R3 + R4}{R1 + R2 + R3 + R4}$			
				Min	**Typ**	**Max**	**Unit**
1	0	0	0	0	15.625	18.125	mV
	0	0	1	44.375	46.875	49.375	mV
	0	1	0	75.625	78.125	80.625	mV
	0	1	1	106.875	109.375	111.875	mV
	1	0	0	138.125	140.625	143.125	mV
	1	0	1	169.375	171.875	174.375	mV
	1	1	0	200.625	203.125	205.625	mV
	1	1	1	231.875	234.375	236.875	mV
2	0	0	0	263.125	265.625	268.125	mV
	0	0	1	294.375	296.875	299.375	mV
	0	1	0	325.625	328.125	330.625	mV
	0	1	1	356.875	359.375	361.875	mV
	1	0	0	388.125	390.625	393.125	mV
	1	0	1	419.375	421.875	424.375	mV
	1	1	0	450.625	453.125	455.625	mV
	1	1	1	481.875	484.375	486.875	mV
6	0	0	0	513.125	515.625	518.125	mV
	0	0	1	544.375	546.875	549.375	mV
	0	1	0	575.625	578.125	580.625	mV
	0	1	1	606.875	609.375	611.875	mV
	1	0	0	638.125	640.625	643.125	mV
	1	0	1	669.375	671.875	674.375	mV
	1	1	0	700.625	703.125	705.625	mV
	1	1	1	731.875	734.375	736.875	mV

Table 4. PINSET2_V Pin Setting for Ramp Amplitude and Ramp Valley

RAMP Valley (mV)	RAMP Amplitude <3> (mV) $V_{RAMP\_AMP} = \frac{30000 \times (16 - RAMP<3:0>)}{f_S}$	$V_{PINSET2\_V} = V_{VCC}(5V) \times \frac{R3 + R4}{R1 + R2 + R3 + R4}$			
		Min	Typ	Max	Unit
100	0	0	25	27.5	mV
100	1	72.5	75	77.5	mV
150	0	122.5	125	127.5	mV
150	1	172.5	175	177.5	mV
200	0	222.5	225	227.5	mV
200	1	272.5	275	277.5	mV
250	0	322.5	325	327.5	mV
250	1	372.5	375	377.5	mV
300	0	422.5	425	427.5	mV
300	1	472.5	475	477.5	mV
350	0	522.5	525	527.5	mV
350	1	572.5	575	577.5	mV
400	0	622.5	625	627.5	mV
400	1	672.5	675	677.5	mV
450	0	722.5	725	727.5	mV
450	1	772.5	775	777.5	mV
500	0	822.5	825	827.5	mV
500	1	872.5	875	877.5	mV
550	0	922.5	925	927.5	mV
550	1	972.5	975	977.5	mV
600	0	1022.5	1025	1027.5	mV
600	1	1072.5	1075	1077.5	mV
650	0	1122.5	1125	1127.5	mV
650	1	1172.5	1175	1177.5	mV
700	0	1222.5	1225	1227.5	mV
700	1	1272.5	1275	1277.5	mV
750	0	1322.5	1325	1327.5	mV
750	1	1372.5	1375	1377.5	mV
800	0	1422.5	1425	1427.5	mV
800	1	1472.5	1475	1477.5	mV
850	0	1522.5	1525	1527.5	mV
850	1	1572.5	1575	1577.5	mV

Table 5. PINSET2_I Pin Setting for Enable Dr.IMON, Enable Auto-ZCD, and AI Gain Selection

Dr.IMON	Auto_ZCD#	AI Gain	$V_{PINSET2\_I} = 80\mu \times \frac{(R1 + R2) \times (R3 + R4)}{R1 + R2 + R3 + R4}$			
			Min	Typ	Max	Unit
Disable	Disable	Disable	0	50	55	mV
		1X	145	150	155	mV
		2X	245	250	255	mV
		4X	345	350	355	mV
Disable	Enable	Disable	445	450	455	mV
		1X	545	550	555	mV
		2X	645	650	655	mV
		4X	745	750	755	mV
Enable	Disable	Disable	845	850	855	mV
		1X	945	950	955	mV
		2X	1045	1050	1055	mV
		4X	1145	1150	1155	mV
Enable	Enable	Disable	1245	1250	1255	mV
		1X	1345	1350	1355	mV
		2X	1445	1450	1455	mV
		4X	1545	1550	1555	mV

Table 6. Ramp Amplitude Example for 300kHz Frequency

Code <3:0>					Ramp Amplitude (mV)
3 (PINSET2)	2	1	0	DEC	
0	0	0	0	0	1600
0	0	0	1	1	1500
0	0	1	0	2	1400
0	0	1	1	3	1300
0	1	0	0	4	1200
0	1	0	1	5	1100
0	1	1	0	6	1000
0	1	1	1	7	900
1	0	0	0	8	800
1	0	0	1	9	700
1	0	1	0	10	600
1	0	1	1	11	500
1	1	0	0	12	400
1	1	0	1	13	300
1	1	1	0	14	200
1	1	1	1	15	100

15.12 Soft-Start

The RT8843A/RT8843B/RT8843D provides the soft-start function that is used to prevent large inrush currents and output voltage overshoot while the converter is being powered up. The soft-start sequence is shown in Figure 10. When EN goes high, the RT8843A/RT8843B/RT8843D enters the internal circuit initialization and pinset function setting. The soft-start circuit starts after the IC initialization is completed. During the soft-start period, the output voltage follows the internal soft-start ramp up. The soft-start slew rate has 3 stages that can be adjusted through the PINSET1 pin, as shown in the Table 3. And the soft-start time can be calculated as follows:

$$T_{SS} = 900\mu s + \frac{V_{OUT}}{SR}$$

where V_{OUT} is the target output voltage and SR is the soft-start slew rate.

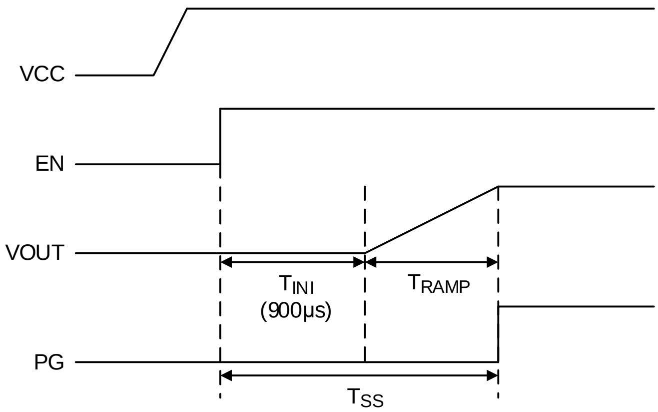


Figure 10. Soft-Start Sequence

15.13 Switching Frequency Setting

Connecting a resistor R_{TON} between the input terminal and the VIN pin to set the on-time width. The R_{TON} can be calculated using the following formula:

$$R_{TON} = \frac{V_{IN}\text{-}0.9}{8.8 \times 10^{-12} \times V_{IN} \times fs} \quad (V_{OUT} > 0.9V)$$

$$R_{TON} = \frac{V_{OUT}}{V_{IN}} \times \frac{V_{IN}\text{-}V_{OUT}}{7.9 \times 10^{-12} \times fs} \quad (0.9V < V_{OUT} < 0.5V)$$

$$R_{TON} = \frac{V_{OUT}}{V_{IN}} \times \frac{V_{IN}\text{-}0.5}{7.9 \times 10^{-12} \times fs} \quad (V_{OUT} < 0.5V)$$

When the load increases, the on-time keeps constant. The off-time width will be reduced, allowing the input terminal to provide more power to the output to regulate the output voltage. Hence, higher load current will result in a higher switching frequency.

The higher switching frequency operation can reduce the size of power components and PCB space, but the high switching frequency will increase the switching loss. Therefore, the frequency setting must be traded-off between the component size and overall efficiency.

The recommended frequency setting range is 150kHz to 1.5MHz. And the minimum T_{ON} cannot be less than 70ns; otherwise the frequency will be lower than the desired value.

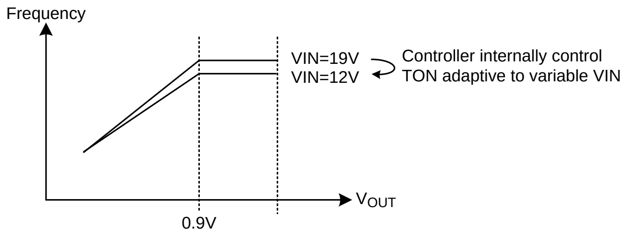


Figure 11. Switching Frequency with Different V_{OUT}

15.14 Ramp Setting

The RT8843A/RT8843B/RT8843D provides an internal ramp that effectively suppresses PWM signal jitter in small output ripple applications. The ramp amplitude and valley can be set through the PINSET1 and PINSET2 pins, as shown in Table 3 and Table 4. The ramp amplitude can be set in a total of 16 steps. Furthermore, the value according to the different switching frequency can be calculated using the following formula:

$$V_{RAMP\_AMP} = \frac{30000 \times \left(16\text{-}RAMP\langle 3:0 \rangle\right)}{fs}$$

Table 6 is a calculation example of a ramp amplitude with a switching frequency of 300kHz. A higher amplitude has better suppression of jitter, but it will reflect poor load transient performance. Therefore, the design of the ramp amplitude need to be traded-off between stability and transient performance. To ensure that the PWM jitter rate is below 15% and the load transient response can meet V_{OUT} −10%/ +20% of system specifications, the default setting of ramp amplitude is recommended to choose approximately 300mV. In addition, in order to ensure the stability at DEM (the multi-pulse phenomenon does not occur), the ramp valley is recommended to be chosen 50mV larger than ramp amplitude.

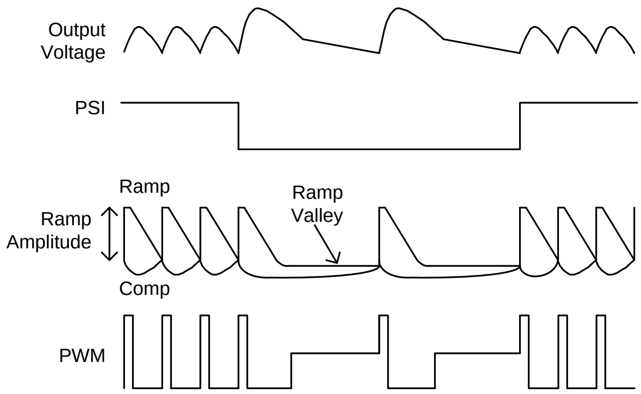


Figure 12. Mode Transition Behavior

15.15 Current Sensing

The RT8843A/RT8843B/RT8843D provides a per-phase current sensing amplifier for different current sensing topologies, including DCR current sensing and SPS current sensing. This current signal is used for loop control, zero current detection, current balance, and per-phase current limit.

15.16 DCR Current Sensing

The RT8843A/RT8843B/RT8843D can support inductor DCR current sensing to get each phase current signal, as illustrated in Figure 13. An external low-pass filter R_{X1} and C_X reconstruct the current signal. The low-pass filter time constant R_{X1} x C_X should match time constant L/DCR of the inductance and DCR. The R_X and C_X can be fine-tuned for transient performance. If the RC network time constant is smaller than the inductor time constant L/DCR, the V_{CS} current signal leads the inductor current signal, triggering early per-phase current limits during load transients. If the RC network time constant is larger than the inductor time constant L/DCR, the V_{CS} current signal has a sluggish rise and delays triggering per-phase current limits during load transients. If the RC network time constant matches the inductor time constant L/DCR, the trigger level of the per-phase current limit will meet the desired value. R_{X1} is highly recommended as two 0603 size resistors in series to enhance the current signal accuracy. An X7R type capacitor is suggested for C_X in the application. R_{X2} is optional for preventing V_{CS} from exceeding the current sense amplifier input range (–10mV to 90mV). The time constant of (R_{X1} // R_{X2}) x C_X should match L/DCR. The current sense lines must be routed as a differential pair from the inductor to the controller on the same layer. When the DCR current sensing circuit is selected, the DrIMON enable/disable of the PINSET2 function must be set to Disable.

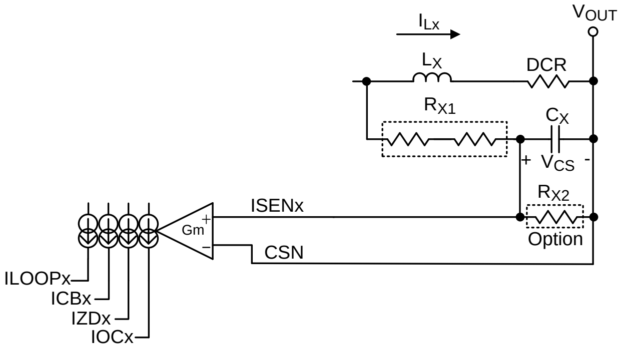


Figure 13. Inductor DCR Current Sensing Method

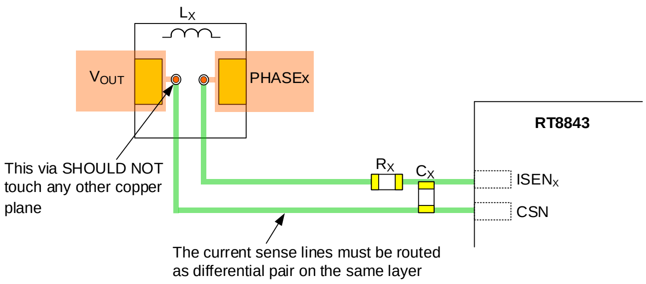


Figure 14. PCB Layout of DCR Current Sensing

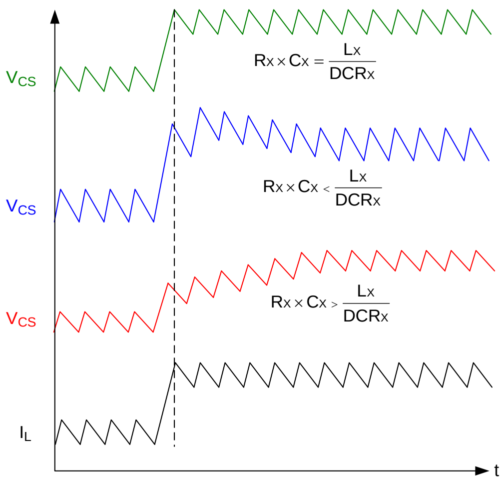


Figure 15. All Kinds of RC Network Time Constant

Table 7. Pin Setting of DrIMON

DrIMON [0]	Enable/Disable
0	Disable
1	Enable

15.17 SPS Current Sensing

The RT8843A/RT8843B/RT8843D current sensing circuit can also support SPS current sensing. SPS (Smart Power Stage) can accurately detect the internal MOSFET current for a reference of the PWM controller. The SPS current sensing circuit simplifies the quantity of components in the external circuit and provides a more accurate current signal unlike the DCR detection circuit. SPS has two kinds of current signals: current output and voltage output. Figure 16 shows the current reporting circuit of the different current signals. When the SPS current sensing is used, the DrIMON enable/disable of the PINSET2 function must be set to enable. After the DrIMON enable is set, the inverting input of the current-sense amplifier generates a 1.375V reference voltage for the SPS current sensing circuit. The current is reported to the controller as a differential voltage between the ISENx and CSN pins with a conversion gain to represent the inductor current I_L, as shown in equations below:

$$V_{ISENx\text{-}CSN} = gain(A/A) \times I_L \times R_{IMON}$$

…(Current Type Signal)

$$V_{ISENx\text{-}CSN} = gain(V/A) \times I_L \times \frac{R_{IMON2}}{R_{IMON1}+R_{IMON2}}$$

…(Voltage Type Signal)

For a larger current sense gain as a voltage type, it is recommended to place a voltage divider resistor between the IOUT and REFIN pins to avoid the controller's current-sense amplifier input voltage range from exceeding –10mV to 90mV.

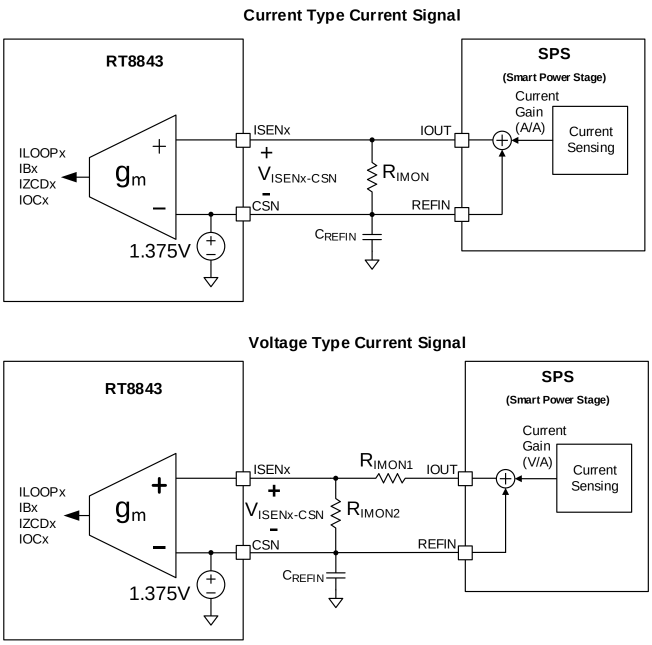


Figure 16. SPS Current Sensing

15.18 Auto-Zero Crossing Detection (Auto-ZCD)

The RT8843A/RT8843B/RT8843D can support the system to use the ZCD threshold of DrMOS under light-load conditions. The ZCD function of DrMOS can be enabled by pulling down the ZCD# pin of DrMOS. When using the Auto-ZCD function, the Auto-ZCD# function of PINSET2 must be set to enable. Once the Auto-ZCD function is enabled, PINSET2 turns on the external NMOS and pulls the ZCD# voltage of DrMOS low, as shown in Figure 9. The Auto-ZCD function only works at the status of ZCD# = L, PWM = L, and GH = L. At this status, if the inductor current I_L > 0A, then GL = H. Conversely, if the inductor current I_L < 0A, then GL = L. In addition, once Auto-ZCD is enabled, the controller only operates in FCCM regardless of the PSI setting voltage.

15.19 Current Balance

The per-phase current sense signal of the RT8843A/RT8843B/RT8843D is compared with the sensed average current. The comparison result adjusts each phase PWM width to optimize current and thermal balance. When the PCB layout makes the parasitic impedance inconsistent from the inductor to the output, that will affect the performance of the current balance. Figure 17 shows a method to eliminate the parasitic impedance. Place two R_{CB} resistors in each phase of the DCR sensing circuit to cancel the R_{PCB} effect and improve current balance. The value of R_{CBx} can be calculated using the following equation:

$$R_{CBx} = R_{Xx} = N \times \frac{L}{DCR \times C_{Xx}}$$

where N is the phase number.

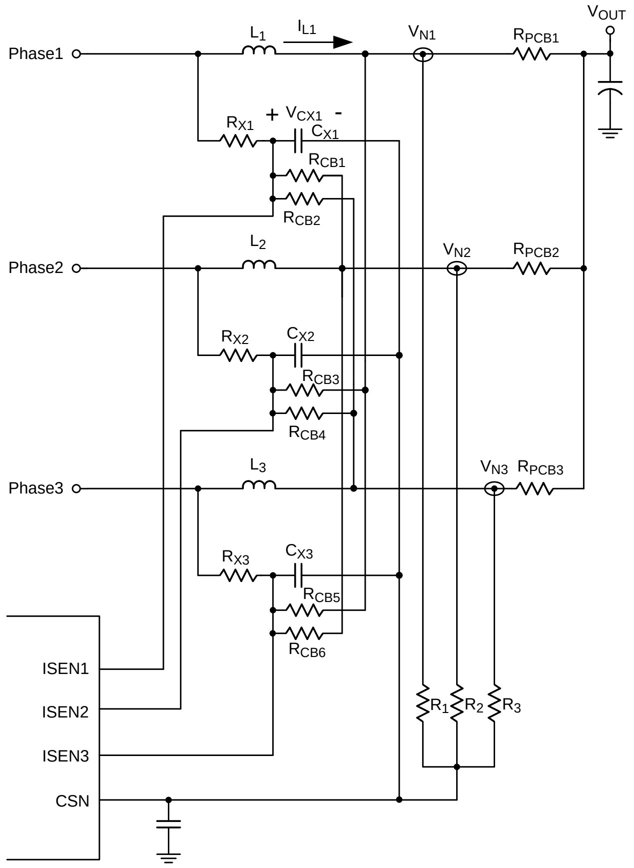


Figure 17. Current Balance Improving

15.20 Per-Phase Current Limit

The RT8843A/RT8843B/RT8843D incorporates a per-phase current limit mechanism to prevent overcurrent event. The per-phase current-limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The per-phase current-limit threshold can be set by the PINSET1 pin. When the DCR sensing circuit is selected, in order to ensure the accuracy of the current signal over a wide temperature range, it is recommended to use the NTC compensation circuit, as shown in Figure 9. The current-limit threshold can be calculated according to the following equation:

$$V_{OCSET} = V_{REF} - \left(\begin{array}{l} V_{REF} \times \dfrac{R3 + R4}{R1 + R2 + R3 + R4} + 80\mu \\ \times \left[(R5 // R_{NTC}) + (R1 + R2) // (R3 + R4) \right] \end{array} \right)$$

$$= V_{ISENx-CSN} \times 32 = DCR \times I_{LIM} \times 32$$

where the I_{LIM} is the desired pre-phase current limit threshold.

On the other hand, when the SPS current sensing is selected, as shown in Figure 18, and the current-limit threshold can be calculated using the following equation:

$$V_{OCSET} = V_{REF} - \left(\begin{array}{l} V_{REF} \times \dfrac{R3 + R4}{R1 + R2 + R3 + R4} + 80\mu \\ \times \left[(R1 + R2) // (R3 + R4) \right] \end{array} \right)$$

$$= V_{ISENx-CSN} \times 32/3.08$$

$$= I_{MON\_SLOPE} \text{ x } R_{IMON} \times (I_{L\_OC} + \Delta I_L \times t_{CSA\_delay} \times f_{SW}) \times 32/3.08 \text{ (Current Type DRMOS)}$$

$$= V_{MON\_SLOPE} \text{ x } R_{IMON2} / (R_{IMON1} + R_{IMON2}) \times (I_{L\_OC} + \Delta I_L \times t_{CSA\_delay} \times f_{SW}) \times 32/3.08 \text{ (Voltage Type DRMOS)}$$

where ΔI_L is the peak-to-peak inductor ripple current, t_{CSA_delay} is the delay time of the current-sense amplifier, which is shown in Figure 16, and f_{SW} is the switching frequency.

Richtek provides a Microsoft Excel-based design tool to help design desired per-phase current-limit threshold.

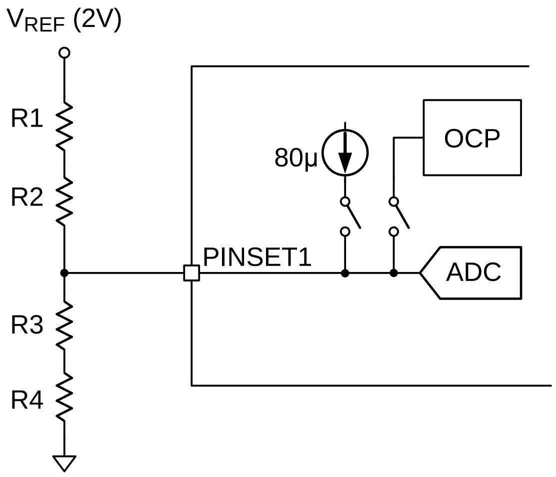


Figure 18. PINSET1 without NTC Network

15.21 AC Droop

The RT8843A/RT8843B/RT8843D adopts a new feature, AC-droop, to effectively suppress load transient ring-back and control overshoot for zero load line application. Figure 19 shows the condition without AC-droop control. The output voltage without AC-droop control has extra ring back ΔV2 due to C area charge.

Figure 20 shows the condition with AC-droop control. While loading occurs, the controller temporarily changes the VID target to the short-term voltage target. The short-term voltage target is related to the transient loading current ΔI_{CC} and can be represented as follows:

Short_Term_Voltage_Target = V_{CS} x 9 x AI

Where the V_{CS} is the current sensing signal from DCR sensing or SPS current sensing. For DCR sensing, V_{CS} = I_{CC_MAX} x DCR. The current gain (AI) can be set by the Pin Setting of AI Gain. Users can select AI gain according to Table 8 to set the desired short-term voltage target. The short-term voltage target reverts to the VID target slowly after approximately 100μs. The short-term voltage target can help the inductor current not to exceed the loading current too much, and then the ring back can be suppressed. As shown in Figure 20, the overshoot amplitude is reduced to only ΔV3.

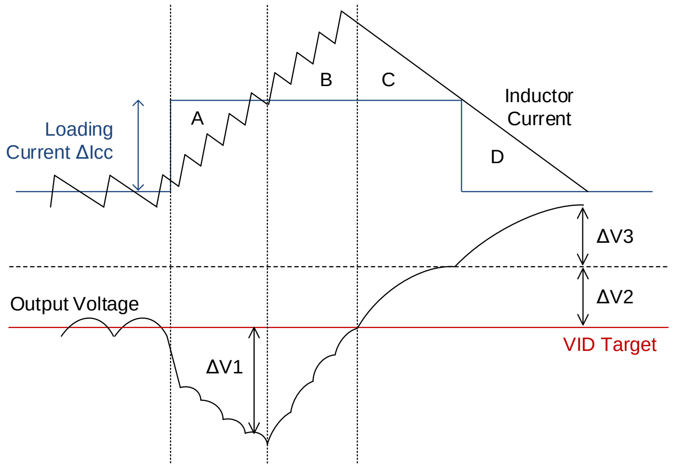


Figure 19. Zero Load Line without AC-Droop Control

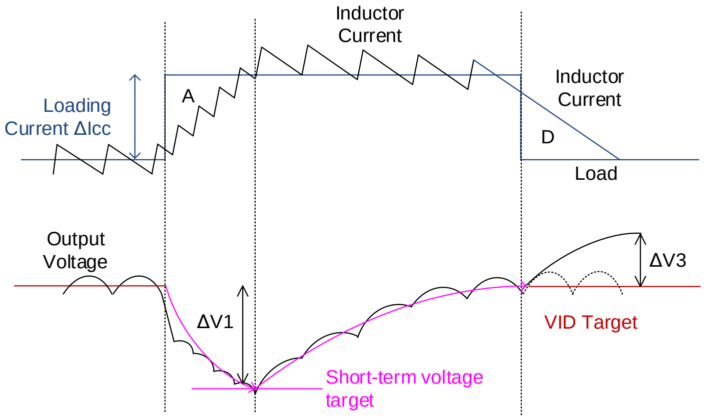


Figure 20. Zero Load Line with AC-Droop Control

Table 8. Pin Setting of AI Gain

AI Gain [1:0]	Gain Value
00	Disable
01	1/16
10	2/16
11	4/16

15.22 Overvoltage Protection

The output voltage can be continuously monitored through the VSEN pin for overvoltage protection. If the REFIN voltage is lower than 1.33V, the overvoltage threshold follows the absolute overvoltage 2V. If the REFIN voltage is higher than 1.33V, the overvoltage threshold follows the relative overvoltage 1.5 x V_{REFIN}. The overvoltage protection mechanism is illustrated in Figure 21. When OVP is triggered with 5μs filter time, the controller de-asserts PG and starts the NVP function. After NVP is enabled, the controller controls the PWM as low when VSEN is higher than VID. When VSEN is lower than VID, the PWM is controlled in tri-state to prevent large negative inductor current that may damage MOSFETs or drivers. After 45μs from the OVP trigger, VID starts to ramp down to 0V with a slow slew rate. During this period, PWMx is not allowed to turn on. The controller controls PWMx to be low or tri-state to pull down the output voltage with VID. The OVP is in latch mode protection, and it can be released by VCC or EN power-on reset.

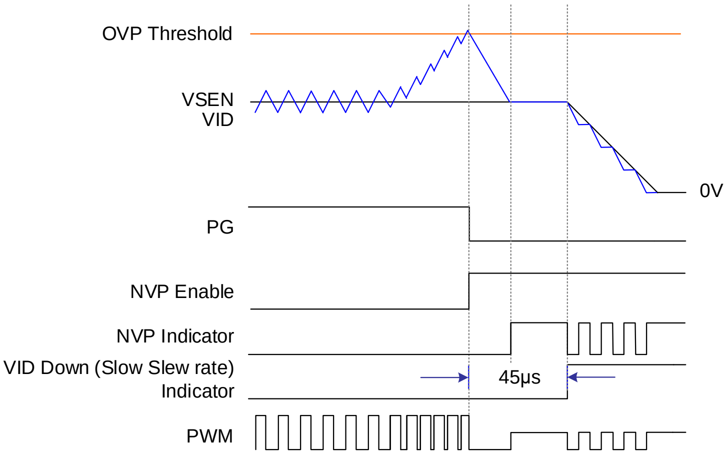


Figure 21. Overvoltage Protection Mechanism

The RT8843A/RT8843B/RT8843D reduces the on-time by pulling the PWM low when VSEN is higher than REFIN + 28mV to prevent overcharging of the output capacitor. Therefore, output voltage overshoot is reduced. When zero current (ZC) is detected, the on-time reduction threshold increases to REFIN + 36mV.

15.23 Undervoltage Protection

The output voltage can be continuously monitored through the VSEN pin for undervoltage protection. When the output voltage is less than the UVP threshold with 3μs filter time, the controller de-asserts PG and controls all PWMs to tri-state to turn off the high-side and low-side power MOSFETs. During soft-start, the UVP blanking time is equal to the PG blanking time.

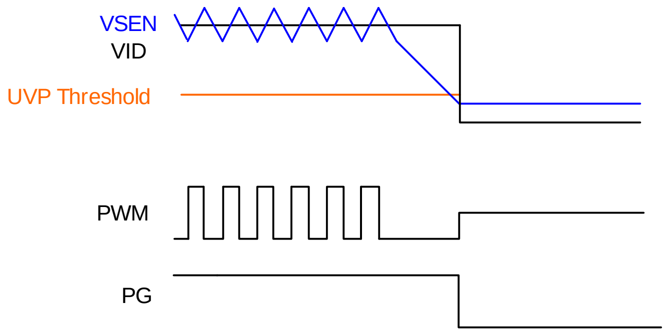


Figure 22. Undervoltage Protection Mechanism

15.24 Inductor Selection

The switching frequency and ripple current determine the inductor value as follows:

$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{I_{RIPPLE(MAX)}} \times T_{ON}$$

where T_{ON} is the UGATE turn-on period.

Higher inductance results in lower ripple current, which means lower power loss. However, the inductor current rising time increases with inductance value. This means the transient response will be slower. Therefore, the inductor design is a trade-off between performance, size and cost.

The RT8843A/RT8843B/RT8843D supports inductor DCR sensing for loop control, zero-current-detection, current balance, and per-phase current limiting. To ensure the accuracy of the DCR sensing signal, the minimum DC resistance of the inductor must be greater than 0.2mΩ. The core must be large enough to prevent inductor saturation under heavy load conditions.

15.25 Output Capacitor Selection

The selection of C_{OUT} is determined by considering the voltage ripple and transient loads, and ensuring that the control loop is stable. Loop stability can be checked by viewing the load transient response. The peak-to-peak output ripple, ΔV_{OUT}, is characterized by two components: ESR ripple ΔV_{P-P_ESR} and capacitive ripple ΔV_{P-P_C}, which can be expressed as follows:

$$\Delta V_{OUT} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C}$$

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

where R_{ESR} is the equivalent series resistance of C_{OUT}. The output ripple reaches at the maximum input voltage since the ΔI_L increases with the input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding transient loads, the V_{SAG} and V_{SOAR} requirements should be taken into consideration for choosing the output capacitance value. The amount of the output sag is a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The worst-case output sag voltage can be determined by using the following equation:

$$\Delta V_{OUT\_SAG} = \frac{L \times (I_{L\_PEAK})^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

When the load is removed, the amount of overshoot due to stored inductor energy can be calculated as follows:

$$\Delta V_{OUT\_SOAR} = \frac{L \times (I_{L\_PEAK})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. Choose X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

15.26 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 105°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-20L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (105°C – 25°C) / (30°C/W) = 3.33W for a WQFN-20L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 23 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

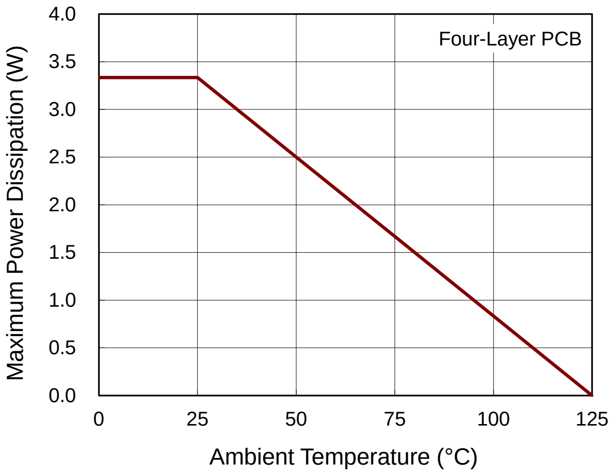


Figure 23. Derating Curve of Maximum Power Dissipation

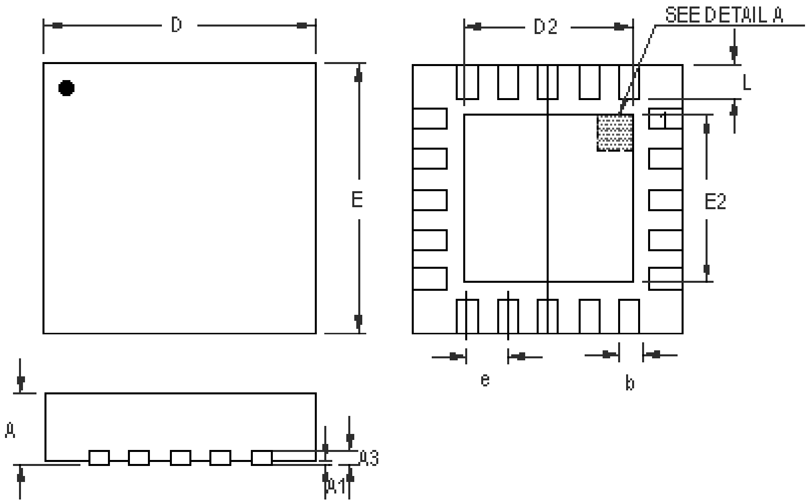
15.27 Layout Considerations

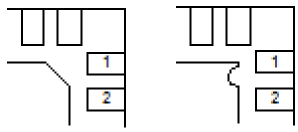
Careful PCB layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all of the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for optimum PCB layout:

- Keep the high-current paths short, especially at the ground terminals.
- Keep the power traces and load connections short. This is essential for high efficiency.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be longer than the discharging path.
- Place the current sense components close to the controller. ISENx and CSN connections for current limit and voltage positioning must be made using Kelvin sense connections to guarantee the current sense accuracy. The PCB trace from the sense nodes should be paralleled back to the controller.
- Route high-speed switching nodes away from sensitive analog areas such as PINSETx, ISENx, CSN, VSEN, FBRTN, and among others.

Note 8. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

16 Outline Dimension





DETAIL A

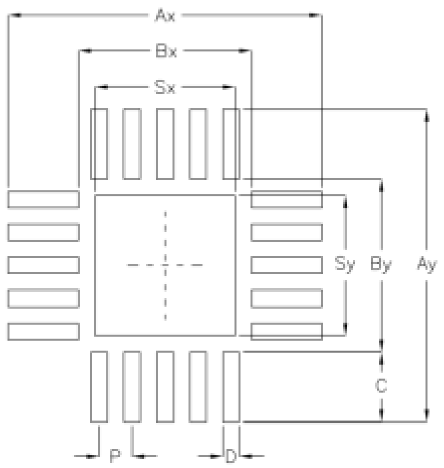
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D2	1.650	1.750	0.065	0.069
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 20L QFN 3x3 Package

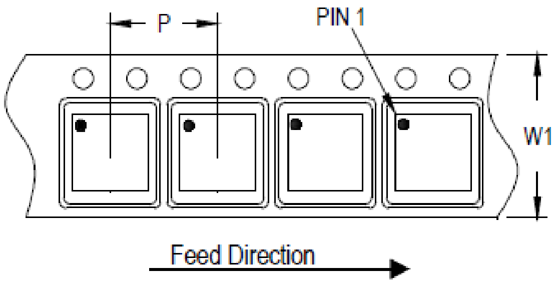
17 Footprint Information

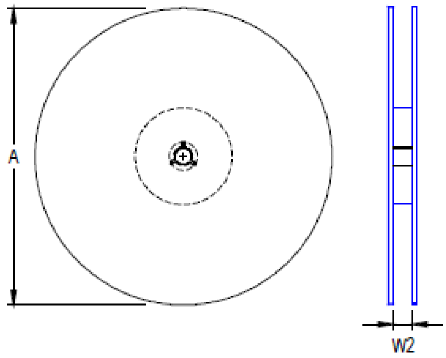


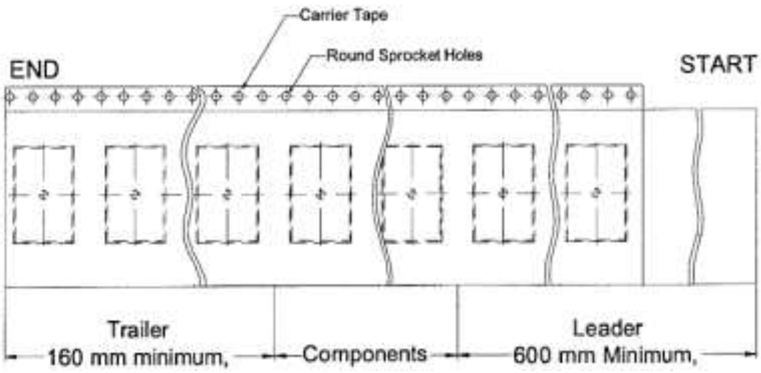
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3*3-20	20	0.40	3.80	3.80	2.10	2.10	0.85	0.20	1.70	1.70	±0.05

18 Packing Information

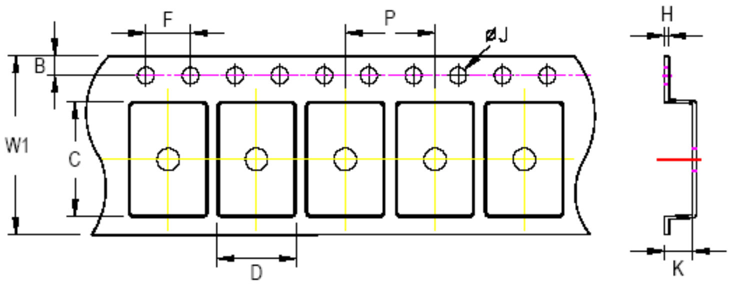
18.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

18.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 3x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

18.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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19 Datasheet Revision History

Version	Date	Description	Item
04	2024/10/14	Modify	Merge RT8843A/B/D
05	2025/7/8	Modify	*Features on page 1* *Ordering Information on page 1* *Packing Information on page 38* - Added Tape Size “K”