SA24481/SA24483/SA24483E

High Efficiency, 36V Input, 1A/3A Synchronous Step Down Regulator

General Description

The SA2448x is a high efficiency synchronous step-down DC-DC converter capable of delivering a load current of 1A/3A. It operates over a wide input voltage range of 4.5V to 36V and integrates main and synchronous MOSFET switches with very low $R_{DS(ON)}$ to minimize conduction loss.

The SA2448x uses a peak current control scheme. The switching frequency is adjustable from 300kHz to 2.2MHz using an external resistor. The SA24483E works at Force Continuous Conduction Mode (FCCM) under light load for small output voltage ripple. The SA24481/SA24483 feature frequency reduction and ultralow quiescent operating to achieve high efficiency under light load. Additionally, the internal soft-start function limits inrush current during power-up.

The SA2448x is available in a QFN2×2-12 Package.

Part Number	Output Current	Light Load Mode
SA24481TLQ	1A	PFM
SA24483TLQ	3A	PFM
SA24483ETLQ	3A	FCCM

Key Features

- Input Voltage Range: 4.5-36V
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 130/75mΩ
- Low quiescent current: I_Q = 18 μA (Typ.)
- Internal Compensation
- Internal 1ms Soft-start Limits the Inrush Current
- Adjustable Switching Frequency Range: 300kHz to 2.2MHz
- Light Load Operating Mode
  - SA24481/SA24483: PFM
  - SA24483E: FCCM
- Output Current Capability
  - SA24481: 1A
  - SA24483/SA4483E: 3A
- ±1% 0.6V Reference Over -40°C~125°C
- Cycle-by-cycle Peak Current Limitation
- Short Circuit Protection
- Spread Spectrum Function
- Thermal Shutdown and Auto Recovery
- Compact Package: QFN2×2-12
- Automotive AEC-Q100 Grade 1 Qualified
- MSL Rating: MSL1

Applications

- Automotive
- Industrial
- High-Voltage DC/DC Converters

Typical Application

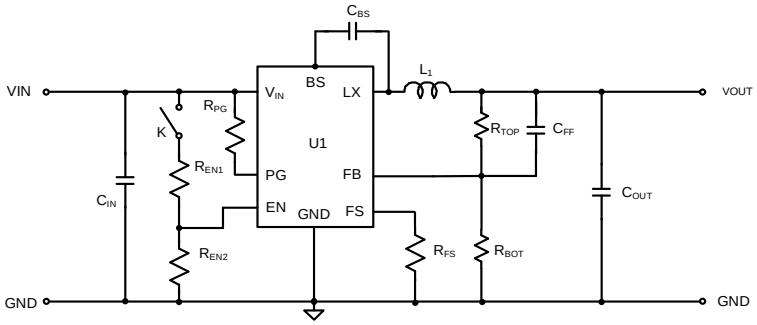


Figure 1. Typical Application Circuit

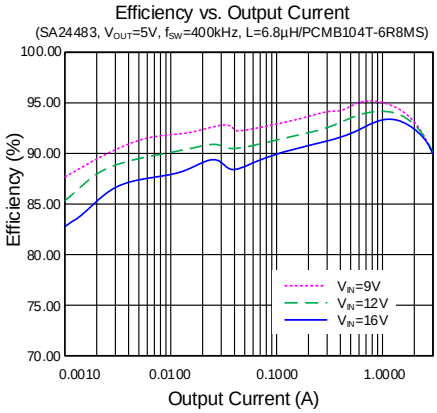


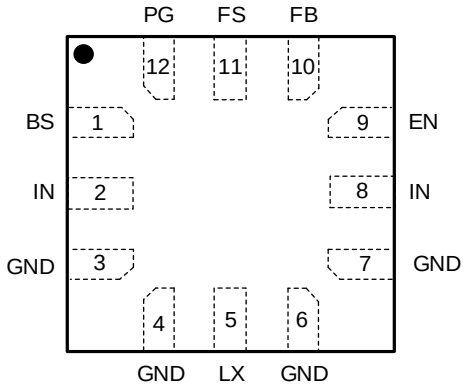
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SA24481TLQ	QFN2×2-12 RoHS-Compliant and Halogen-Free	**LCR*xyz***
SA24483TLQ		**GNG*xyz***
SA24483ETLQ		**KFF*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



(QFN2×2-12)

Pin Description

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin.
IN	2, 8	Input pin. Decouple this pin to GND pin with at least 4.7μF ceramic cap.
LX	5	Inductor pin. Connect this pin to the switching node of inductor.
GND	3, 4, 6, 7	Ground.
EN	9	Enable control. Pull high to turn on. Do not leave it floating.
FB	10	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6*(1+R_1/R_2)$.
FS	11	Frequency setting pin. Connect a resistor from this pin to GND to program the switching frequency. The switching frequency equals to: $fsw(kHz) =10^6/(9.3\times R_{FS}(k\Omega)+30)$.
PG	12	Power good indicator. Open drain output. High-impendence, externally pulled high when V_{OUT} is within the regulation range. Otherwise, internally pulled low.

Block Diagram

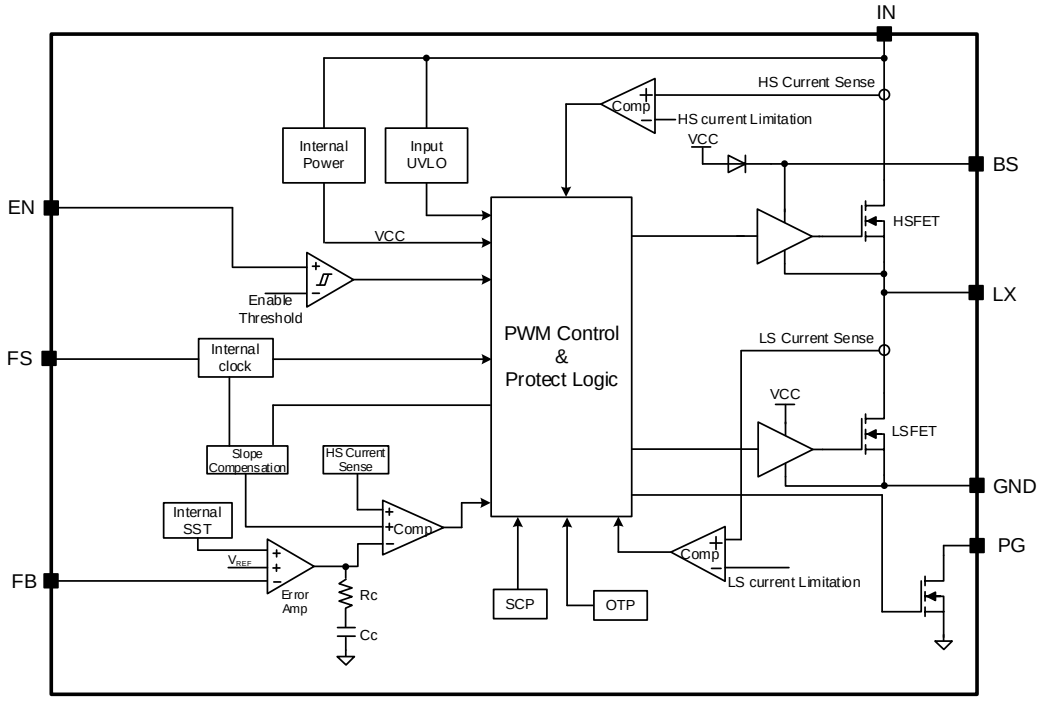


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	40	V
LX, FB, EN, FS, PG	-0.3	40	
BS-LX	-0.3	6	
Dynamic LX Voltage in 20ns Duration	GND - 5	IN + 5	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10s)		260	
Storage Temperature	-65	150	
ESD Susceptibility			
HBM (Human Body Model)		±2000	V
CDM (Charged Device Model)		±750	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	39.94	°C/W
$\theta_{JC(top)}$ Junction-to-Case (top) Thermal Resistance	15.53	
θ_{JB} Junction-to-Board Thermal Resistance	11	
Ψ_{JT} Junction-to-Top Characterization Parameter	0.6	
P_D Power Dissipation T_A= 25°C	3.1	W
Parameter (Note 3)	**Typ**	**Unit**
θ_{JA} Junction-to-Ambient Thermal Resistance	62.5	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	15.8	

Recommended Operating Conditions

Parameter (Note 4)	Min	Max	Unit
IN	4.5	36	V
Junction Temperature	-40	150	°C
Ambient Temperature	-40	125	

Electrical Characteristics

(V_{IN} = 12V, T_J = -40°C to +125°C. Typical values are at T_J=25°C, unless otherwise specified. (**Note 5**))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Input Voltage Range	V_{IN}		4.5		36	V
	Input UVLO Threshold	V_{UVLO}				4.5	V
	UVLO Hysteresis	V_{HYS}			0.3		V
	Quiescent Current	I_Q	SA24481/SA24483,I_{OUT}=0, V_{FB}=V_{REF}×105%		18	30	μA
	No Load Input Current	I_{NO_LOAD}	SA24483E, I_{OUT}=0,V_{OUT}=5V, f_{SW}=400kHz		10	20	mA
	Shutdown Current		EN=0		1	5	μA
Output	Feedback Reference Voltage	V_{REF}	T_J= -40°C~125°C, F_S=400kHz	0.594	0.6	0.606	V
			T_J= -40°C~125°C, F_S=2.2MHz	0.591	0.6	0.609	
	FB Input Current	I_{FB}	V_{FB}=0.65V	-50		50	nA
	Output Discharge Current	I_{DIS}			40		mA
	Soft-start Time	t_{SS}		0.5	1	2	ms
	Output Under Voltage Protection Threshold	V_{UVP}			33%		V_{REF}
	Hiccup Duty Cycle	D_{HICCUP}	(Note 6)		12.5		%
Power Good	Power Good Threshold	V_{PG}	V_{FB} falling, PG from high to low		87%		V_{REF}
			V_{FB} rising, PG from low to high		90%		V_{REF}
			V_{FB} rising, PG from high to low		115%		V_{REF}
			V_{FB} falling, PG from low to high		113%		V_{REF}
	Power Good Delay	T_{PG_F}	PG falling edge (Note 6)		20		μs
		T_{PG_R}	PG rising edge (Note 6)		150		μs
	Power Good Output Low Voltage	$V_{PG,LOW}$	I_{PG_LOW}=5mA			0.7	V
MOSFET	Top FET R_{ON}	$R_{DS(ON)1}$			130		mΩ
	Bottom FET R_{ON}	$R_{DS(ON)2}$			75		mΩ
	Top FET Current Limit	$I_{LIM,TOP81}$	SA24481	1.5	2	2.6	A
	Bottom FET Valley Current Limit	$I_{LIM,VAY81}$		1	1.5	2	A
	Top FET Current Limit	$I_{LIM,TOP83}$	SA24483	4	5	6	A
	Bottom FET Valley Current Limit	$I_{LIM,VAY83}$		2.8	3.5	4.5	A
	Top FET Current Limit	$I_{LIM,TOP83E}$	SA24483E	4	5	6	A
	Bottom FET Valley Current Limit	$I_{LIM,VAY83E}$		2.8	3.5	4.5	A
Enable (EN)	EN High Threshold	V_{ENH}		1.08	1.2	1.32	V
	EN Low Threshold	V_{ENL}		0.9	1.0	1.1	V
Frequency	Oscillator Frequency Program Range	$f_{OSC,RNG}$	R_{FS}=45.6k~360k	300		2200	kHz
	Oscillator Frequency Accuracy	$f_{OSC,ACC}$	F_{OSC}=2MHz, with R_{FS} resistor of 1% accuracy	-12%		12%	f_{OSC}
	Frequency Span Spread Spectrum Operation	f_{SS}	(Note 6)		±5		%

	Min ON Time	$t_{ON,MIN}$	(Note 6)		80		ns
	Min OFF Time	$t_{OFF,MIN}$	F_{OSC}=2MHz (Note 6)		90		ns
OTP	Thermal Shutdown Temperature	T_{SD}			165		°C
	Thermal Shutdown Hysteresis	$T_{SD,HYS}$			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy demo board.

Note 3: θ_{JA} is measured in the natural convection at T_A = 25°C on a 4-layer test board of JESD51-7 thermal measurement standard.

Note 4: The device is not guaranteed to function outside its operating conditions.

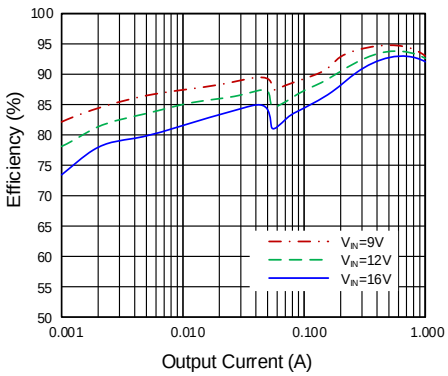
Note 5: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 6: Guaranteed by design or statistical correlation and not production tested.

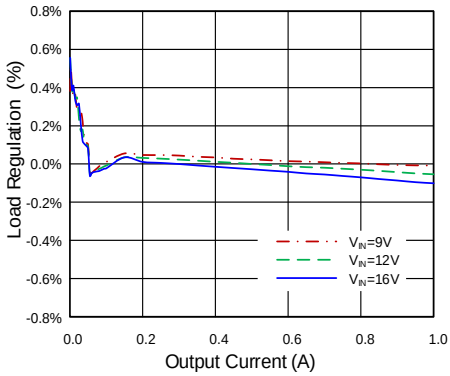
Typical Performance Characteristics

(V_{IN} = 12V, C_{OUT} = 44μF, f_{SW} = 400kHz, T_A = 25°C, unless otherwise specified)

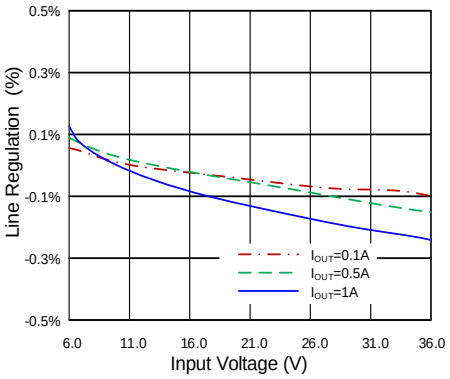
Efficiency vs. Output Current
(SA24481,V_{OUT}=5V,f_{SW}=400kHz,L=22uH(GCM31CC71C226ME36L)



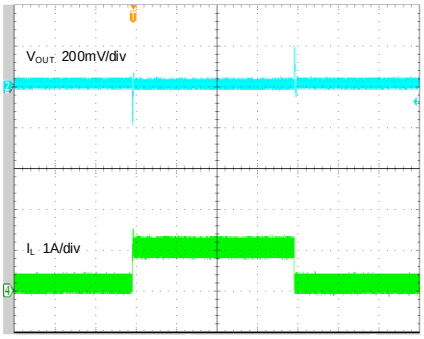
Load Regulation
(SA24481,V_{OUT}=5V,f_{SW}=400kHz,L=22uH(GCM31CC71C226ME36L)



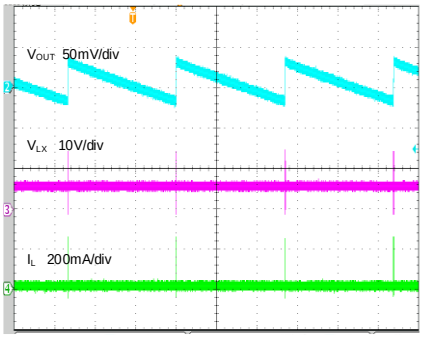
Line Regulation
(SA24481,V_{IN}=6-36V,V_{OUT}=5V,f_{SW}=400kHz)



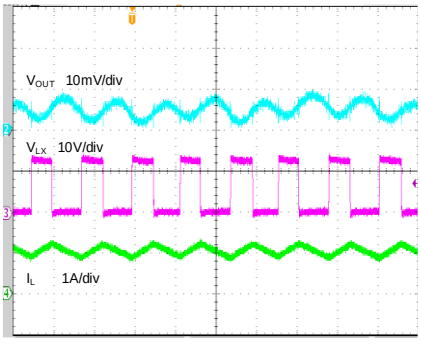
Load Transient
(SA24481, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.1-1A)



Output Ripple
(SA24481, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)

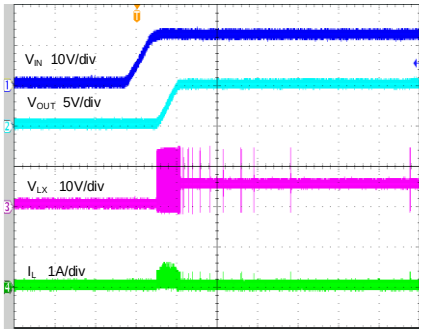


Output Ripple
(SA24481, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=1A)



VIN ON

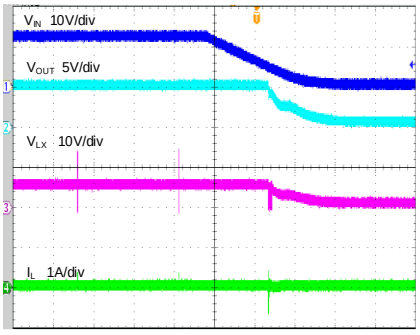
(SA24481, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (2ms/div)

VIN OFF

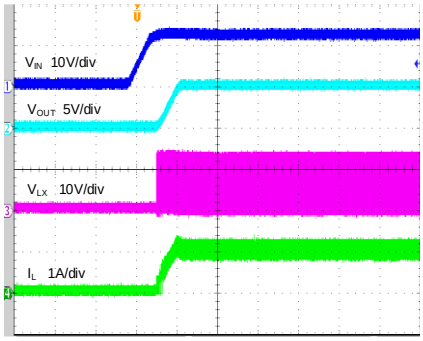
(SA24481, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (10ms/div)

VIN ON

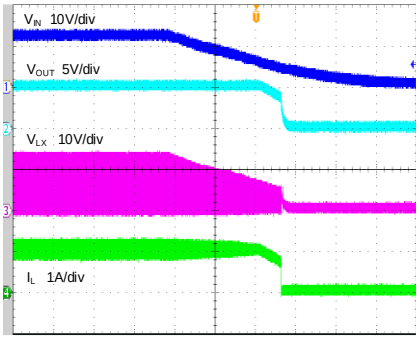
(SA24481, V_{IN}=12V,V_{OUT}=5V, I_{OUT}=1A)



Time (2ms/div)

VIN OFF

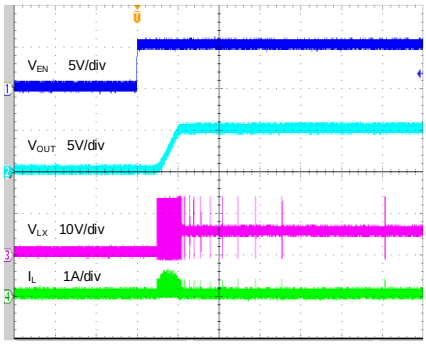
(SA24481, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1A)



Time (4ms/div)

EN ON

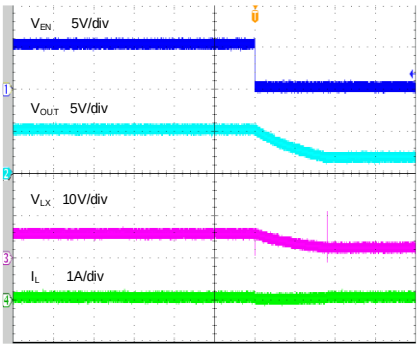
(SA24481, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (2ms/div)

EN OFF

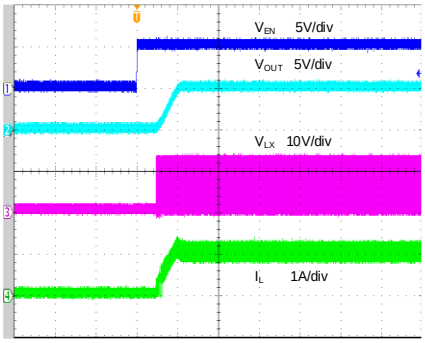
(SA24481, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (2ms/div)

EN ON

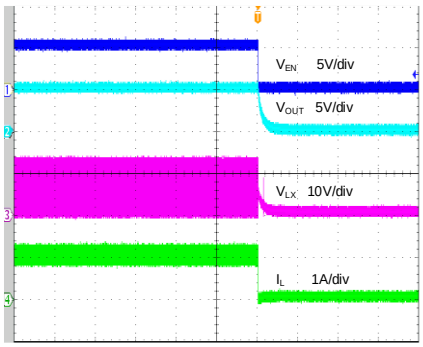
(SA24481, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=1A)



Time (2ms/div)

EN OFF

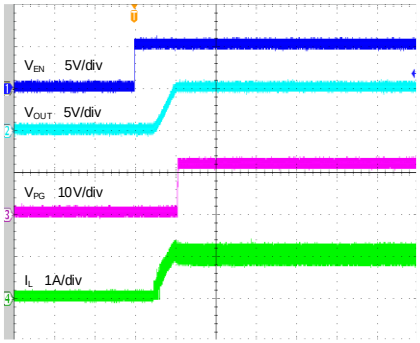
(SA24481, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=1A)



Time (2ms/div)

PG Rising By EN ON

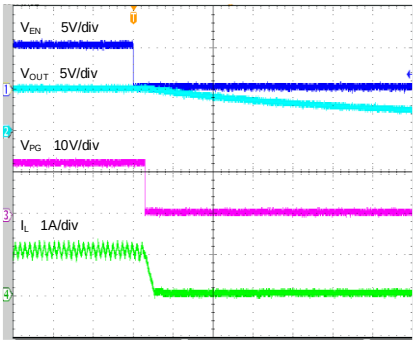
(SA24481, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1A)



Time (2ms/div)

PG Falling By EN OFF

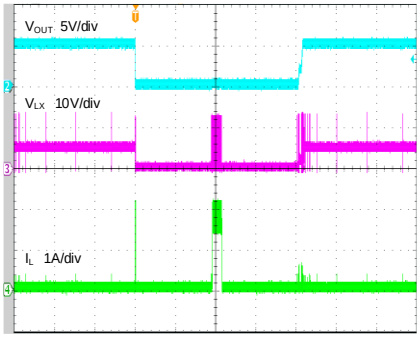
(SA24481, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1A)



Time (20µs/div)

Short Circuit Protection

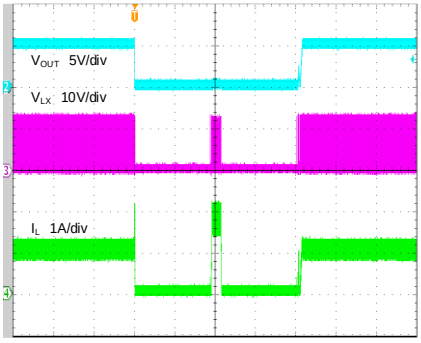
(SA24481, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (20ms/div)

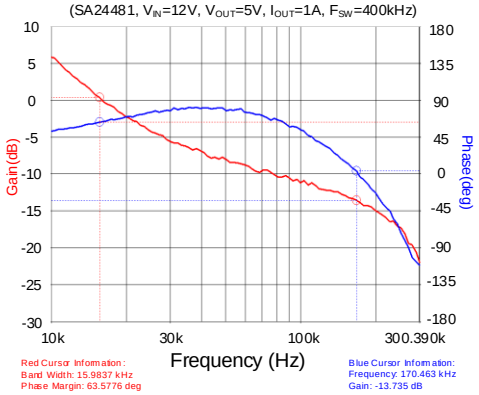
Short Circuit Protection

(SA24481, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=1A)

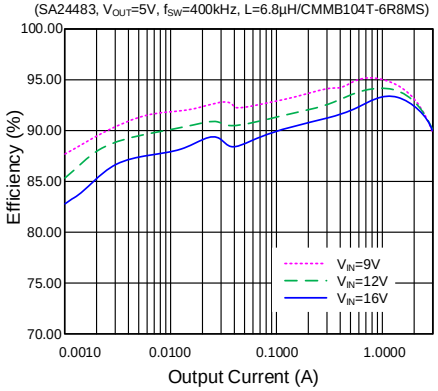


Time (20ms/div)

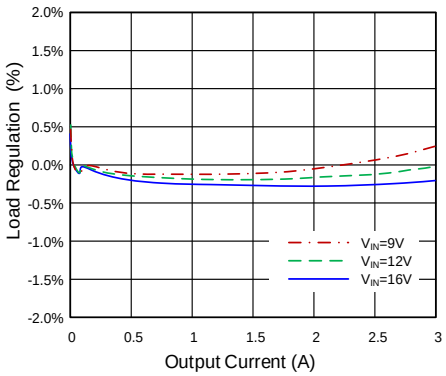
Bode Plot
(SA24481, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1A, F_{SW}=400kHz)



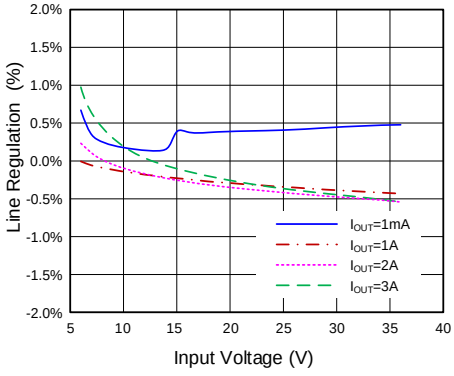
Efficiency vs. Output Current
(SA24483, V_{OUT}=5V, f_{SW}=400kHz, L=6.8µH/CMMB104T-6R8MS)



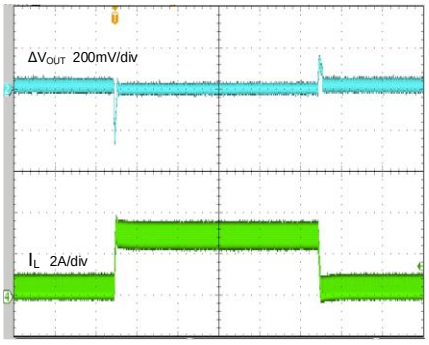
Load Regulation
(SA24483, V_{OUT}=5V, f_{SW}=400kHz, I_{OUT}=0-3A)



Line Regulation
(SA24483, V_{IN}=6-36V,V_{OUT}=5V, f_{SW}=400kHz)

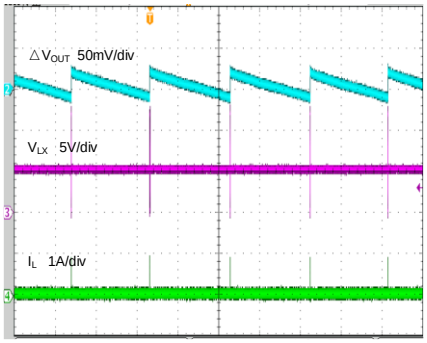


Load Transient
(SA24483, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0.3~3A)



Output Ripple

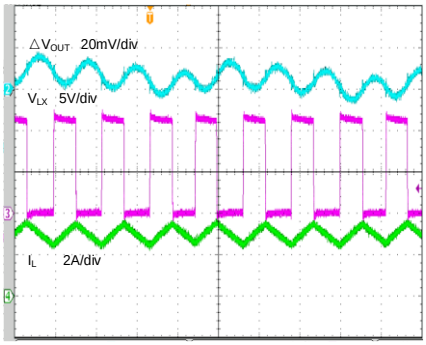
(SA24483, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (10ms/div)

Output Ripple

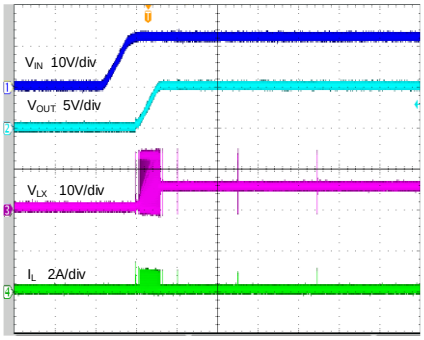
(SA24483, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=3A)



Time (2μs/div)

VIN ON

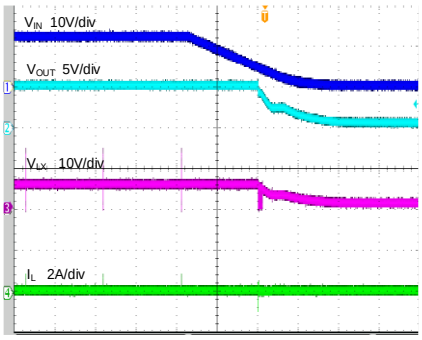
(SA24483, V_{IN}=12V,V_{OUT}=5V, I_{OUT}=0A, f_{SW}=400kHz)



Time (2ms/div)

VIN OFF

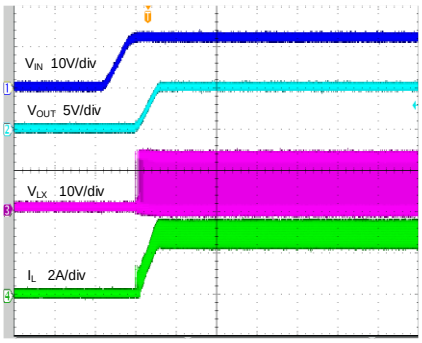
(SA24483, V_{IN}=12V,V_{OUT}=5V, I_{OUT}=0A, f_{SW}=400kHz)



Time (10ms/div)

VIN ON

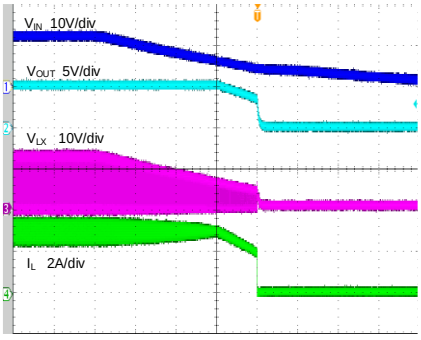
(SA24483, V_{IN}=12V,V_{OUT}=5V, I_{OUT}=3A, f_{SW}=400kHz)



Time (2ms/div)

VIN OFF

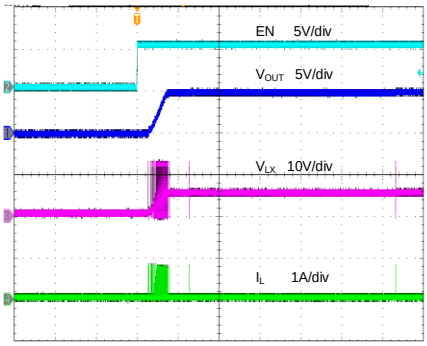
(SA24483, V_{IN}=12V,V_{OUT}=5V, I_{OUT}=3A, f_{SW}=400kHz)



Time (2ms/div)

EN ON

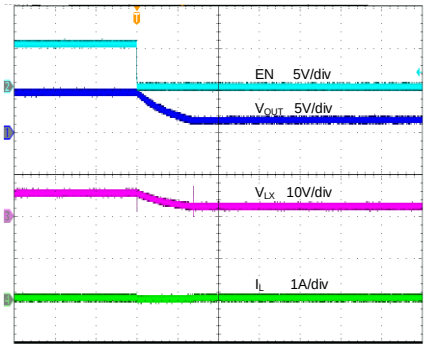
(SA24483, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (2ms/div)

EN OFF

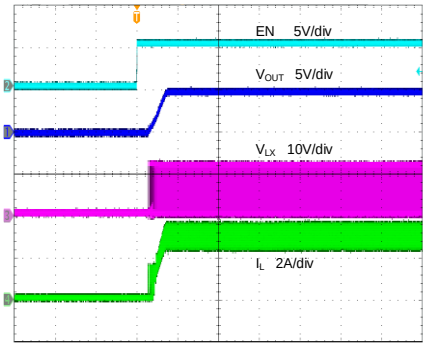
(SA24483, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (2ms/div)

EN ON

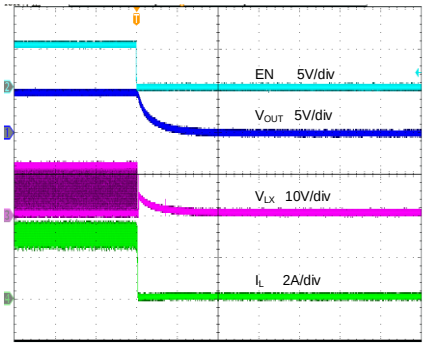
(SA24483, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=3A)



Time (2ms/div)

EN Off

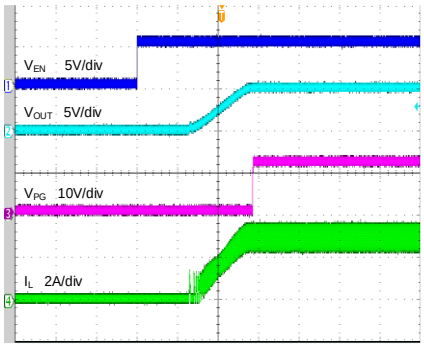
(SA24483, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=3A)



Time (200µs/div)

PG Rising By EN ON

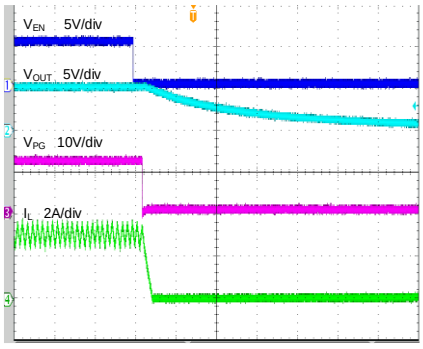
(SA24483, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, f_{SW}=400kHz)



Time (800µs/div)

PG Falling By EN OFF

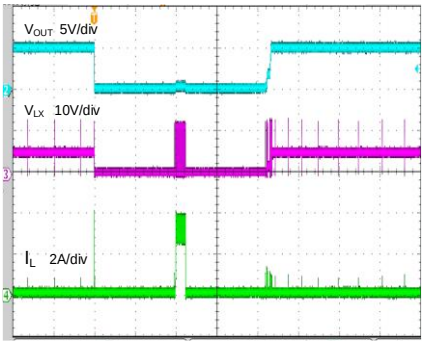
(SA24483, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, f_{SW}=400kHz)



Time (20µs/div)

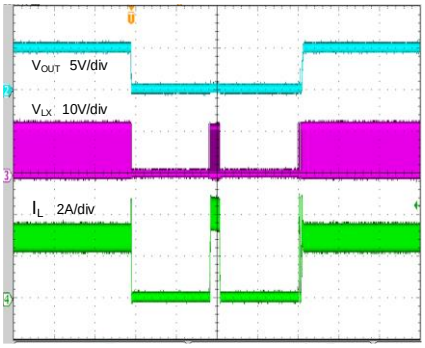
Short Circuit Protection

(V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



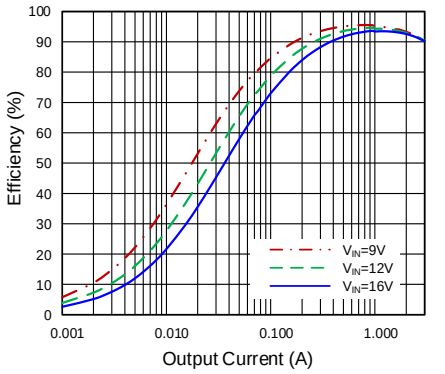
Short Circuit Protection

(V_{IN}=12V,V_{OUT}=5V,I_{OUT}=3A)



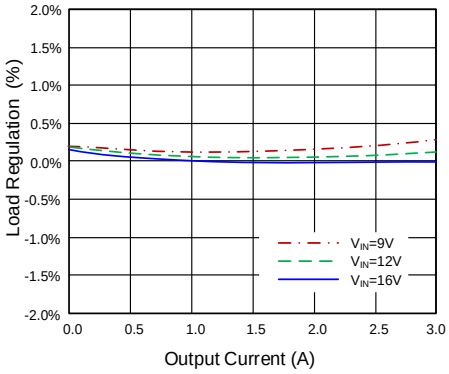
Efficiency vs. Output Current

(V_{OUT}=5V, f_{SW}=400kHz, L=6.8μH/CMMB104T-6R8MS)



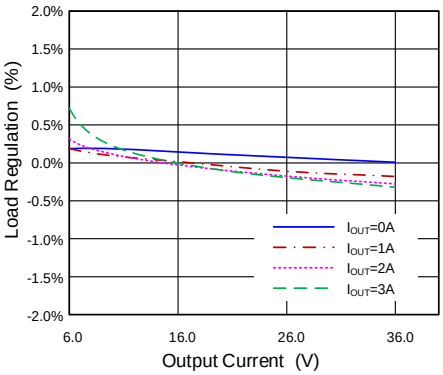
Load Regulation

(V_{OUT}=5V, f_{SW}=400kHz, I_{OUT}=0-3A)



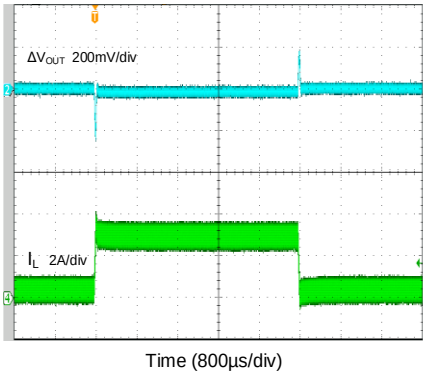
Line Regulation

(V_{IN}=6-36V,V_{OUT}=5V, f_{SW}=400kHz)



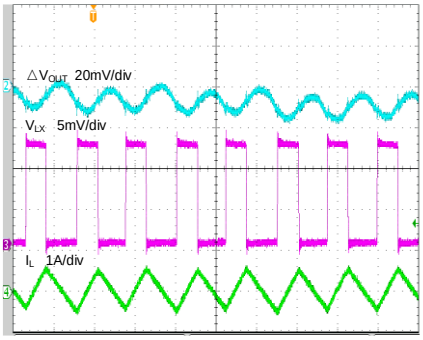
Load Transient

(V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0.3~3A)



Output Ripple

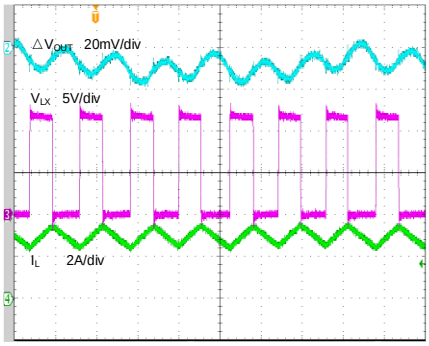
(SA24483E, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (10ms/div)

Output Ripple

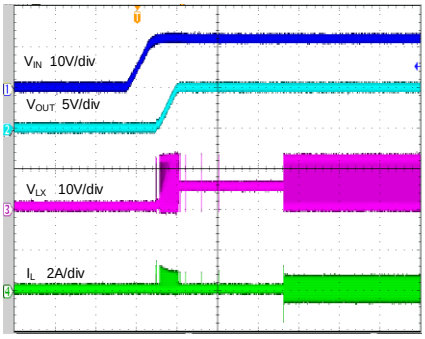
(SA24483E, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=3A)



Time (2μs/div)

VIN ON

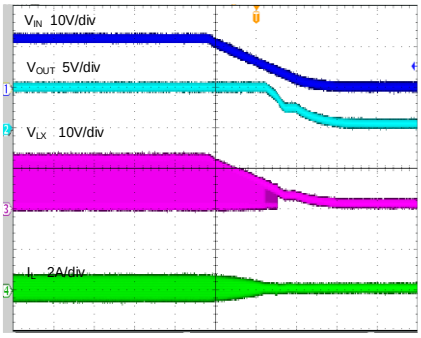
(SA24483E, V_{IN}=12V,V_{OUT}=5V, I_{OUT}=0A, f_{SW}=400kHz)



Time (2ms/div)

VIN OFF

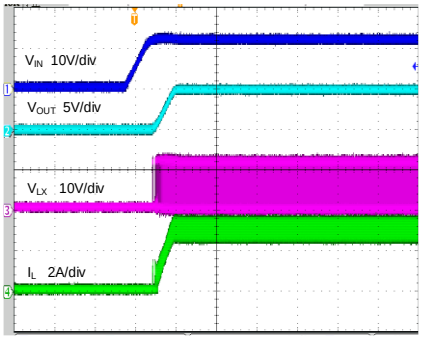
(SA24483E, V_{IN}=12V,V_{OUT}=5V, I_{OUT}=0A, f_{SW}=400kHz)



Time (10ms/div)

VIN ON

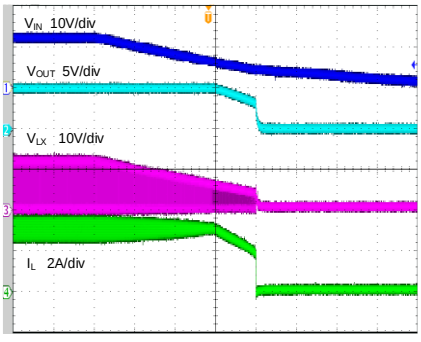
(SA24483E, V_{IN}=12V,V_{OUT}=5V, I_{OUT}=3A, f_{SW}=400kHz)



Time (2ms/div)

VIN OFF

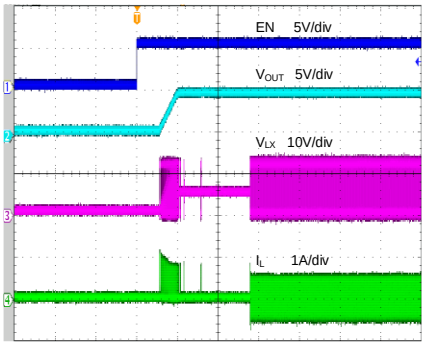
(SA24483E, V_{IN}=12V,V_{OUT}=5V, I_{OUT}=3A, f_{SW}=400kHz)



Time (2ms/div)

EN ON

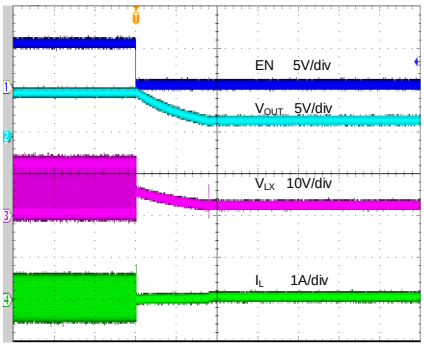
(SA24483E, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (2ms/div)

EN OFF

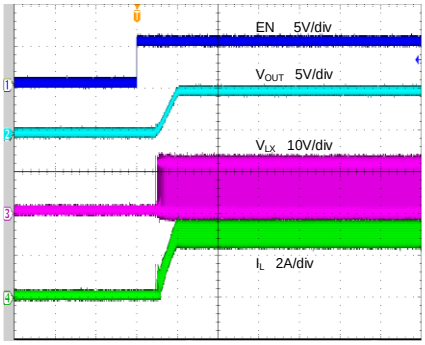
(SA24483E, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (2ms/div)

EN ON

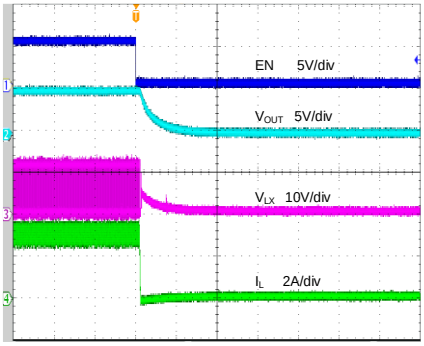
(SA24483E, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=3A)



Time (2ms/div)

EN Off

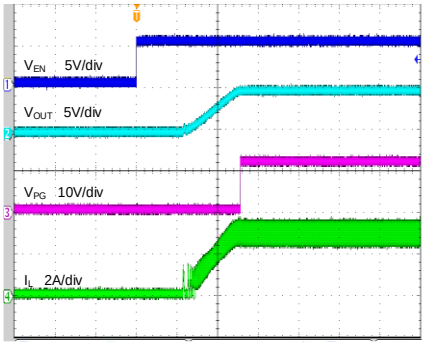
(SA24483E, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=3A)



Time (200µs/div)

PG Rising By EN ON

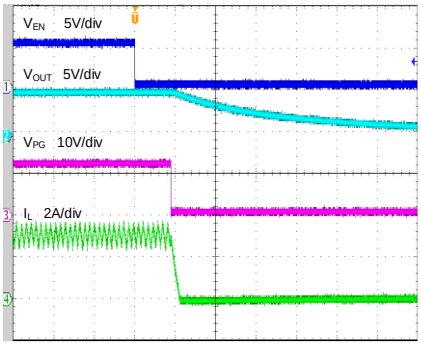
(SA24483E, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, f_{SW}=400kHz)



Time (800µs/div)

PG Falling By EN OFF

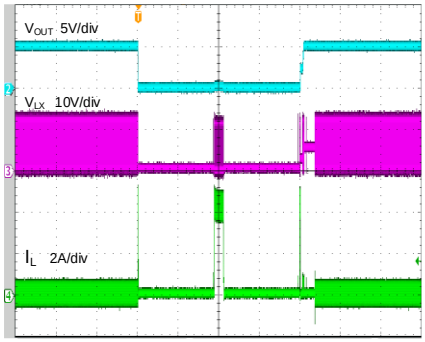
(SA24483E, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, f_{SW}=400kHz)



Time (20µs/div)

Short Circuit Protection

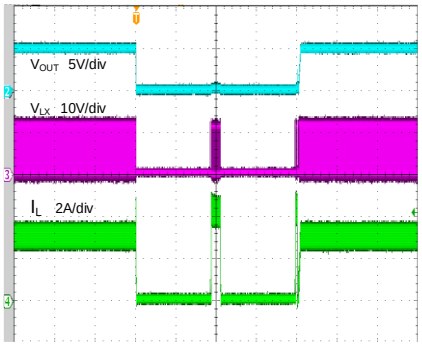
(SA24483E, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (20ms/div)

Short Circuit Protection

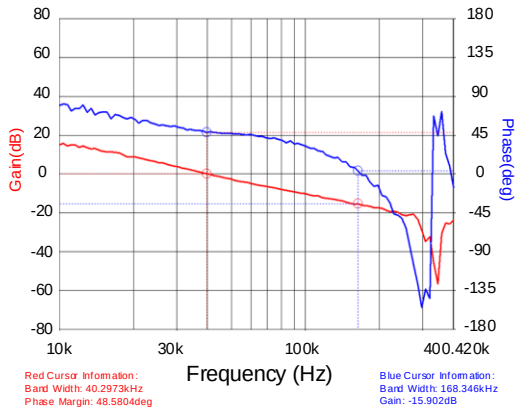
(SA24483E, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=3A)



Time (20ms/div)

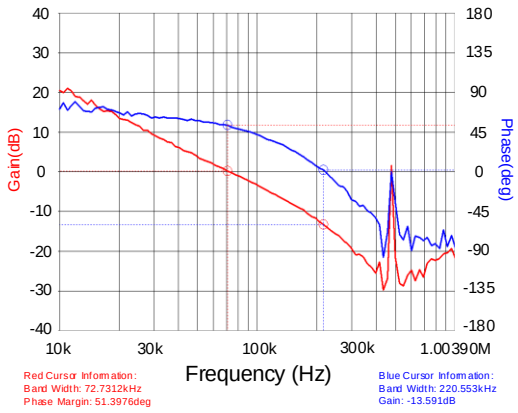
Bode Plot

(SA24483/E, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=2.4A, f_{SW}=400kHz)



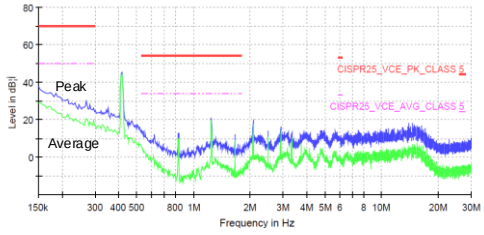
Bode Plot

(SA24483/E, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=2.4A, f_{SW}=2.2MHz)



CISPR 25 Class 5 Conducted Emission

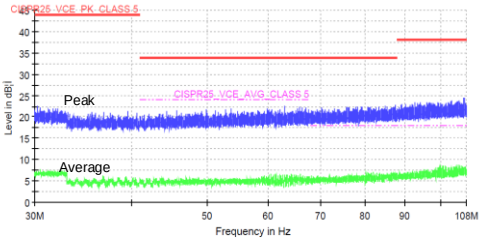
(SA24483, I_{OUT}=3A, F_{SCAN}=150kHz-30MHz)



Frequency In Hz

CISPR 25 Class 5 Conducted Emission

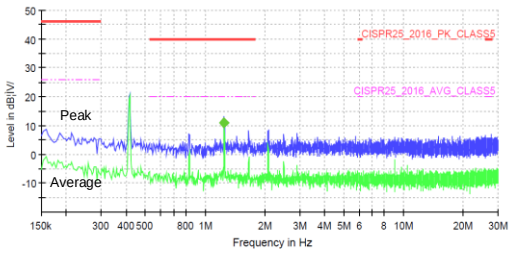
(SA24483, I_{OUT}=3A, F_{SCAN}=30MHz-108MHz)



Frequency In Hz

CISPR 25 Class 5 Radiated Emission

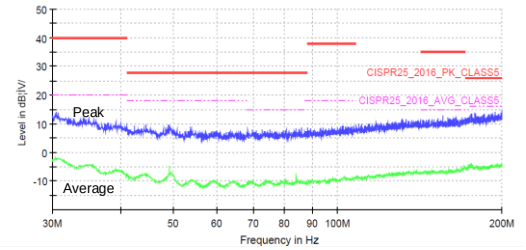
(SA24483, I_{OUT}=3A, F_{SCAN}=150kHz-30MHz)



Frequency In Hz

CISPR 25 Class 5 Radiated Emission

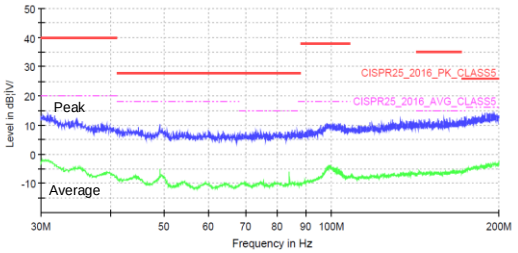
(SA24483, I_{OUT}=3A, F_{SCAN}=30MHz-200MHz, Horizontal)



Frequency In Hz

CISPR 25 Class 5 Radiated Emission

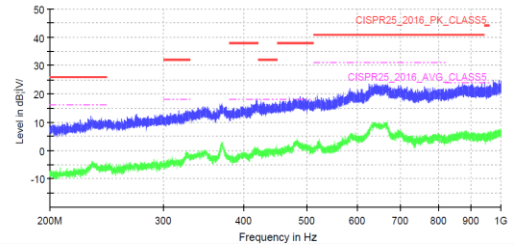
(SA24483, I_{OUT}=3A, F_{SCAN}=30MHz-200MHz, Vertical)



Frequency In Hz

CISPR 25 Class 5 Radiated Emission

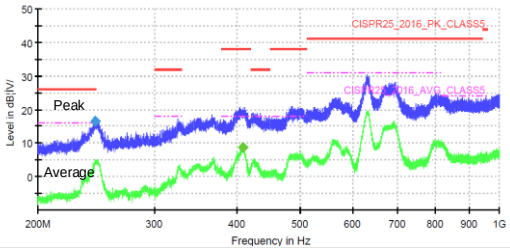
(SA24483, I_{OUT}=3A, F_{SCAN}=200MHz-1GHz, Horizontal)



Frequency In Hz

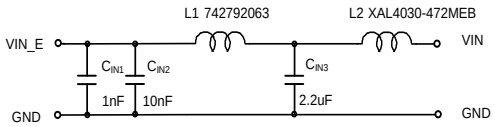
CISPR 25 Class 5 Radiated Emission

(SA24483, I_{OUT}=3A, F_{SCAN}=200MHz-1GHz, Vertical)



Frequency In Hz

EMI Filter



Functional Description

The SA2448x is a high-efficiency synchronous step-down DC-DC regulator featuring internal power and synchronous rectifier MOSFETs. It operates with fixed frequency and peak current control over a wide input voltage range of 4.5V to 36V and can deliver continuous output currents of 1A/3A.

The SA2448x is available in a QFN2x2 package. The switching frequency can be adjusted from 300kHz to 2.2MHz, allowing selection to meet application EMI limits and to minimize noise in critical frequency bands.

The SA2448x offers excellent efficiency over a wide range of applications by incorporating internal 130mΩ power and 75mΩ synchronous rectifier MOSFETs, along with frequency reduction at light load conditions to device with PFM mode. The 1μA shutdown supply current enables the device to be utilized in battery-powered applications. The SA2448x ensures safe operation under all conditions by providing cycle-by-cycle current limit, internal soft-start, short-circuit protection, and thermal shutdown.

General Features

Fixed Frequency PWM Control and Slope Compensation

The SA2448x uses fixed frequency and peak current mode control. The output voltage is fed back to the error amplifier through an external resistor divider connected to the FB pin and is compared with the internal reference voltage, V_{REF}. The output of the error amplifier (V_{COMP}) regulates both the peak current level and the output voltage.

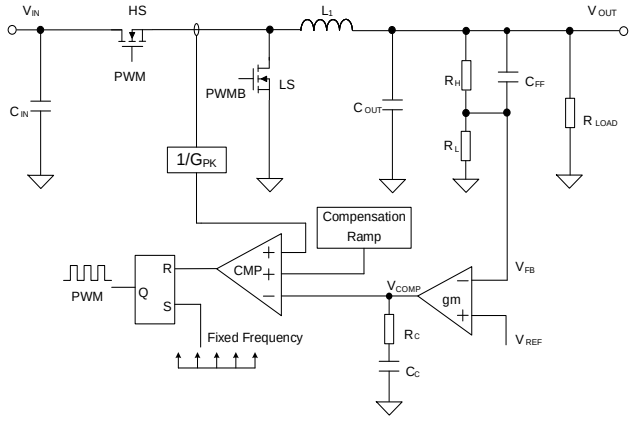


Figure 4. Fixed Frequency PWM Control and Slope Compensation Block Diagram

On the rising edge of the internally generated fixed-frequency clock, the internal high-side N-channel power MOSFET will turn on. The MOSFET current is converted into a ramp voltage signal using a $1/G_{PK}$ coefficient. When the sum of the ramp voltage and the compensation ramp reaches V_{COMP}, the high-side power MOSFET will turn off, and the synchronous rectifier MOSFET will turn on. Peak current mode control also provides an inherent cycle-by-cycle peak current limit.

ON-OFF Sequence

The normal startup of the chip is determined by two factors. First, the EN pin level must exceed the logic high level threshold. Second, the voltage present at VIN pin must exceed the UVLO rising threshold. After the EN pin level is set high, whether the chip is turned on is determined by the voltage of the VIN pin. When both conditions are met, the internal reference voltage starts ramping and the device starts operating. After a 1ms delay, the soft-start circuit is enabled and the SW node begins switching. After a fixed soft-start time t_{SS} (1ms typ.), the output reaches the target value.

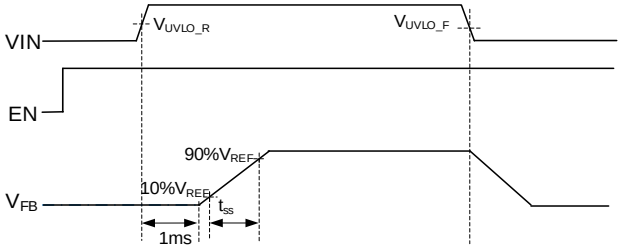


Figure 5. VIN ON/OFF Sequence

When the VIN pin voltage is higher than 4.5V, the EN pin voltage determines whether the chip begins operating. Once the EN pin voltage is above the logic high level, the internal reference voltage begins to build and the functional circuit begins operating. After a 1ms delay, the soft-start circuit begins operating and the SW node begins switching. After a fixed soft-start time, the output reaches the target value.

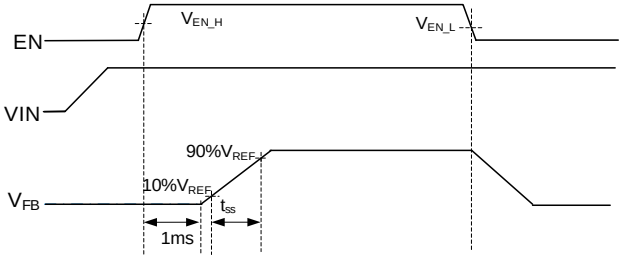


Figure 6. EN ON/OFF Sequence

Light Load Operation

The SA24481/SA24483 operate in pulse frequency modulation (PFM) mode under light load conditions. In PFM mode, the low-side synchronous rectifier is turned off when the current through the rectifier ramps down to zero, preventing recirculation current that can reduce efficiency during light loads. Additionally, the output of the error amplifier (V_{COMP}) naturally decreases, which in turn reduces the peak current under these conditions. When V_{COMP} decreases further with a reduced load and reaches the internal preset threshold, the device stops switching to minimize switching power loss and quiescent current,

thereby enhancing light load efficiency. Switching resumes when V_{COMP} rises above the threshold.

Power Good Indicator

The power good indicator (PG) is an open-drain output controlled by a window comparator connected to the feedback signal. This pin is pulled to ground if the output voltage is lower than 87% of the regulation voltage or higher than 115% of the regulation voltage. This pin enters a high-impedance state if the output voltage is between 90% and 113% of the regulation voltage.

PG should be connected to V_{IN} or another voltage source through a resistor (e.g., 10kΩ–100kΩ).

External Bootstrap Capacitor

The SA2448x integrates a floating power supply for the gate driver that operates the internal high-side N-channel power MOSFET. Connect a 0.1 µF low ESR ceramic capacitor between BS and LX for proper operation.

Adjustable Switching Frequency

The switching frequency can be adjusted from 300kHz to 2.2MHz by connecting a resistor between FS and GND. The switching frequency can be calculated using the following formula:

$$f_{SW}(kHz) = \frac{10^6}{9.3 \times R_{FS}(k\Omega) + 30}$$

Note that the device stability will be affected if the on-time is close to the minimum on-time, $t_{ON,MIN}$. Table 1 presents the switching frequency and R_{FS} resistor values for typical applications.

Table 1. Adjustable Switching Frequency

f_{SW}(kHz)	R_{FS}(kΩ)	V_{IN}(V), V_{OUT} = 3.3V	
		12	18
300	355	✓	✓
400	267	✓	✓
1000	104.3	✓	✓
2200	45.3	✓	×
400	OPEN*	✓	✓

** It's highly recommended to use a resistor to configure the switching frequency.*

Minimum Duty Cycle and Maximum Duty Cycle

The switching frequency is influenced not only by component tolerances but also by the minimum on-time and off-time limits. Consequently, the minimum duty cycle is approximately 3.2% at a 400kHz switching frequency, accounting for an approximate minimum on-time of 80ns. Due to the device's on-time stretch function, the maximum duty cycle can reach up to 95%.

For SA24483E (FCCM version), special attention should be paid whether minimum on time ($t_{ON,MIN}$) will be continuously trigged in the system application. This should be avoided for the sake of output voltage accuracy and ripple. Once the minimum on time is continuously triggered, the VOUT voltage will increase with the switching until the OVP (typ. 115%*V_{REF}) is triggered and the IC stops switching to prevent output voltage runaway. Then the output voltage drops and after the output voltage is less than the set point, the IC enters FCCM again. This switching behavior will be repeated unless the condition disappears.

Frequency Spread Spectrum

A ±5% variation in the internal oscillator frequency is used to generate sidebands of the switching frequency and its harmonics. This variation broadens the emission power spectrum and reduces the peak electromagnetic interference (EMI) switching noise.

Fault Protection Modes

Peak Current Limit Protection

Because the converter operates using peak current mode control, the SA2448x provides inherent cycle-by-cycle peak current limiting (top MOSFET current limit). During t_{ON}, if the high-side power MOSFET current exceeds the current limit threshold, it is turned off, and the low-side synchronous rectifier is turned on. A blanking time period is used at the beginning of the on-time, during which current sampling is disabled to avoid false triggers caused by switching noise. The priority of peak current limit protection is lower than that of the minimum on-time.

Valley Current Limit Protection

The SA2448x provides valley current limit for the bottom MOSFET. If the peak current limit is triggered, the high-side MOSFET is turned off. The high-side switch cannot be turned on again until the low-side synchronous rectifier current falls below the bottom MOSFET current limit and the inductor current returns to safe levels.

Short-Circuit Protection

The SA2448x integrates hiccup mode short-circuit protection. If V_{FB} is less than 33% of V_{REF} and the peak current limit is triggered, the short-circuit protection mode will be initiated.

The SA2448x will shut down for approximately 40ms and then restart with a complete soft-start cycle lasting approximately 5.6ms. If the fault condition is resolved, the device will resume normal operation. Refer to Figure 7.

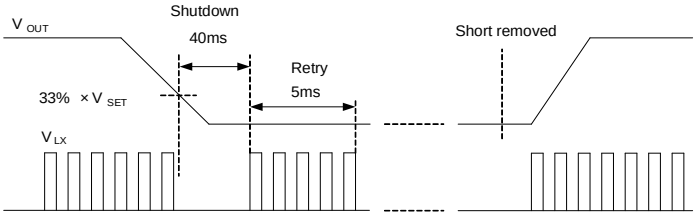


Figure 7. Short-Circuit Protection

Overtemperature Protection (OTP)

The SA2448x includes overtemperature protection (OTP) circuitry to prevent overheating caused by excessive power dissipation. This feature shuts down switching operations when the junction temperature exceeds 165°C. Once the junction temperature decreases by approximately 20°C, the IC will resume normal operation with a complete soft-start cycle. To ensure continuous operation, provide adequate cooling to prevent the junction temperature from exceeding the OTP threshold.

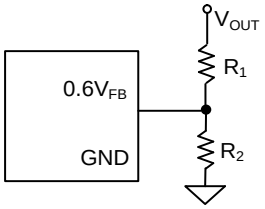
Application Information

The following paragraphs describe the selection process for the feedback resistors (R_1 and R_2), the input capacitor (C_{IN}), the output capacitor (C_{OUT}), and the output inductor (L).

Feedback Resistor-Divider R_1 and R_2

Choose R_1 and R_2 to program the proper output voltage. Select large resistance values between 10kΩ and 1MΩ for both R_1 and R_2 to minimize power consumption under light loads. Given V_{OUT} = 3.3V and R_1 = 100kΩ, then R_2 can be calculated as 22.2kΩ using the following equation:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} \times R_1$$



With a calculated value of 22.2kΩ for R_2, a standard 1% 22.1kΩ resistor is selected.

Input Capacitor Selection

Input filter capacitors are essential for reducing the ripple voltage on the input, filtering the switched current drawn from the input supply, and minimizing EMI. When selecting an input capacitor, choose a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating that exceeds the system requirements. The X7R series ceramic capacitors are often preferred due to their small size, low cost, surge current capability, and high RMS current ratings over wide temperature and voltage ranges. Systems powered by wall adapters or long, inductive wires may experience significant inductive ringing at the input of the device. In these cases, consider adding bulk capacitance, such as electrolytic, tantalum, or polymer capacitors. Utilizing a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet RMS current requirements) is beneficial in these scenarios.

Consider the RMS current rating of the input capacitor and, if necessary, parallel additional capacitors to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a requirement for input voltage ripple in the system, select an appropriate input capacitor that meets the specifications. Due to the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated as follows:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications, using two 10µF X7R capacitors connected in parallel is sufficient. Place the ceramic input capacitors as close to the IN and GND pins as possible.

Inductor Selection

The inductor is essential for supplying a constant current to the output load while being driven by the switched input voltage. Selecting a low inductor value can help reduce size and cost and enhance transient response; however, it will also increase peak inductor ripple current, which can reduce efficiency and increase output voltage ripple. The low DC resistance (DCR) of these low-value inductors may help minimize DC losses and improve efficiency. Conversely, higher inductor values generally exhibit higher DCR and slower transient response.

A reasonable compromise between size, efficiency, and transient response can be achieved by selecting a ripple current (ΔIL) that is approximately 20%–50% of the maximum output current. To calculate the approximate inductor value, begin by selecting the input and output

voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$) is a fixed value (SA24483/E is 3A,The SA24481 is 1A, and estimating ΔI_L as a percentage of that current.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and the required peak inductor current ($I_{L,PEAK}$) according to the following equations:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

$$I_{L,PEAK} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current in excess of $I_{L,PEAK}$.

For maximum efficiency, select an inductor with a low DCR that meets the requirements for inductance, size, and cost. Consider using low-loss ferrite materials.

Output Capacitor C_{OUT} Selection

Select the output capacitor C_{OUT} to meet the output ripple requirements, considering both steady-state ripple and transient conditions. Ceramic and POS types are typically chosen for their small size and low cost.

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors' equivalent series resistance (ESR) as well as the stored charge (capacitive ripple). When estimating the total ripple, both factors should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

It is recommended to use two X7R or better grade ceramic capacitors in parallel, each with a minimum capacitance of 22μF for typical applications.

Load Transient Considerations

The device integrates compensation components to achieve stability and fast transient responses. Adding a small ceramic capacitor, C_{FF}, in parallel with R_{TOP} may further enhance the load transient responses and is therefore highly recommended for applications with significant load transient step requirements.

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the IC package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated as follows:

$$P_{D,MAX} = (T_{J,MAX} - T_A) / \theta_{JA}$$

Where $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 150°C. The junction-to-ambient thermal resistance (θ_{JA}) is layout-dependent. For the QFN2×2-12 package, the thermal resistance (θ_{JA}) is 39.94°C/W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts feature a large area with long 2-oz. copper traces connected to each pin and substantial, unbroken 1-oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical board design requires the following:

- Wide copper traces that are well connected to the IC's backside pads leading to exposed copper areas on the component side of the board
- Good thermal vias from the exposed pad connecting to a wide middle-layer ground plane and to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A = 25°C may be calculated using the following formula:

$$P_{D,MAX} = (150℃ - 25℃)/(39.94℃/W) = 3.1W$$

Maximum power dissipation is dependent on the operating ambient temperature for a fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in Figure 8 to determine the impact of increasing ambient temperature on maximum power dissipation.

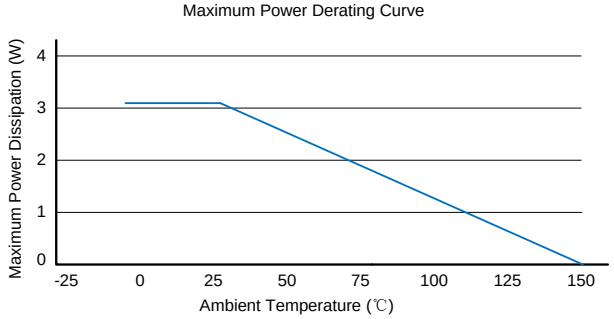
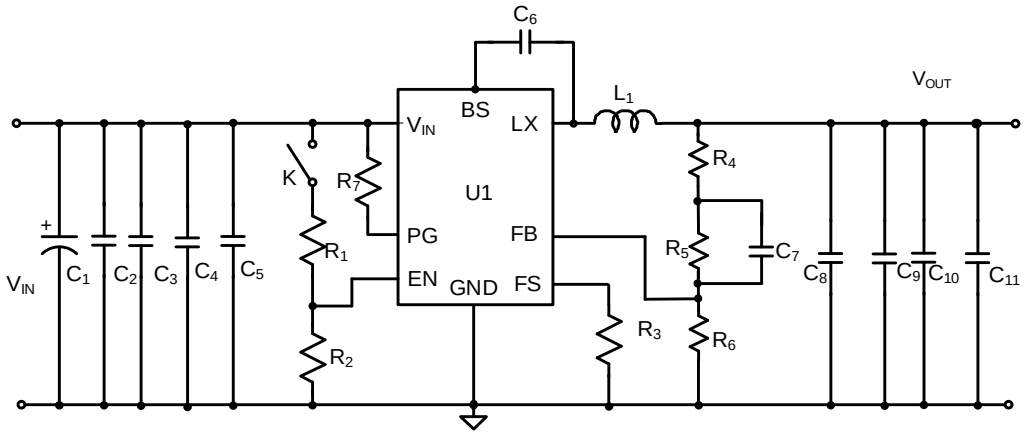


Figure 8. Derating Curve

Application Schematic



BOM List

Designator	Description	Part Number	Manufacturer
U_1	1A/3A, Buck	SA2448xTLQ	Silergy
C_1	47μF/100V Electrolytic Cap		
C_2, C_4	10μF/50V/X7T,1206	GCM31CD71H106KE36L	Murata
C_3, C_5, C_6	100nF/50V/0603 X7R	GCJ188R71H104KA12D	Murata
C_9, C_{11}	Null		
R_1	10k, 1%, 0603		YAGEO
R_2	1M, 1%, 0603		YAGEO
R_4	0Ω, 1%, 0603		YAGEO
R_7	100k, 1%, 0603		YAGEO

Recommend Component Values for Typical Applications

(SA24481TLQ)

V_{OUT}(V)	f_{SW}(kHz)	R_3(kΩ)	R_5(kΩ)	R_6(kΩ)	C_7(pF)	L_1/Part Number	C_{OUT}/Part Number
3.3	400	267	100	22.2	47	15μH VCMT063T-150MN5TM	22μF*2 GCM31CC71C226ME36L
5	400	267	100	13.7	47	22μH VCMT063T-220MN5TM	22μF*2 GCM31CC71C226ME36L
3.3	2200	45.3	100	22.2	33	3.3μH VCMT053T-3R3MN5TM	22μF*2 GCM31CC71C226ME36L
5	2200	45.3	100	13.7	33	4.7μH VCMT053T-4R7MN5TM	22μF*2 GCM31CC71C226ME36L

(SA24483TLQ, SA24483ETLQ)

V_{OUT}(V)	f_{SW}(kHz)	R_3(kΩ)	R_5(kΩ)	R_6(kΩ)	C_7(pF)	L_1/Part Number	C_{OUT}
1.2	400	267	100	100	68	2.2μH CMMB104T-2R2MS	22μF*2 GCM31CC71C226ME36L
3.3	400	267	100	22.2	68	4.7μH CMMB104T-4R7MS	22μF*2 GCM31CC71C226ME36L
5	400	267	100	13.7	68	6.8μH CMMB104T-6R8MS	22μF*2 GCM31CC71C226ME36L
12	400	267	100	5.23	68	10μH	22μF*2

						CMMB104T-100MS	GCM31CC71C226ME36L
3.3	2200	45.3	100	22.2	68	1.5μH CMMB104T-1R5MS	22μF*2 GCM31CC71C226ME36L
5	2200	45.3	100	13.7	68	2.2μH CMMB104T-2R2MS	22μF*2 GCM31CC71C226ME36L

Layout Design

Follow these PCB layout guidelines for optimal performance:

- Place C_{IN}, C_{BS}, R_{TOP}, R_{BOT}, and R_{FS} as close as possible to the converter.
- To achieve the best thermal and noise performance, maximize the PCB copper area connected to the GND pin. A ground plane is highly recommended if board space allows.
- Place CIN close to pins IN and GND. Minimize the loop area formed by CIN and GND.
- Separate the ground of the sensitive signal(RBOT, and RFS) from the ground of the power circuit as much as possible
- Minimize the PCB copper area associated with the LX pin.
- To reduce noise, ensure that R_{TOP}, R_{BOT} and the trace connecting to the FB pin are not adjacent to the LX net on the PCB layout.
- If the system chip driving the EN pin has a high impedance state during shutdown and the IN pin is connected directly to a power source such as a Li-Ion battery, add a 1MΩ pull-down resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator during shutdown.

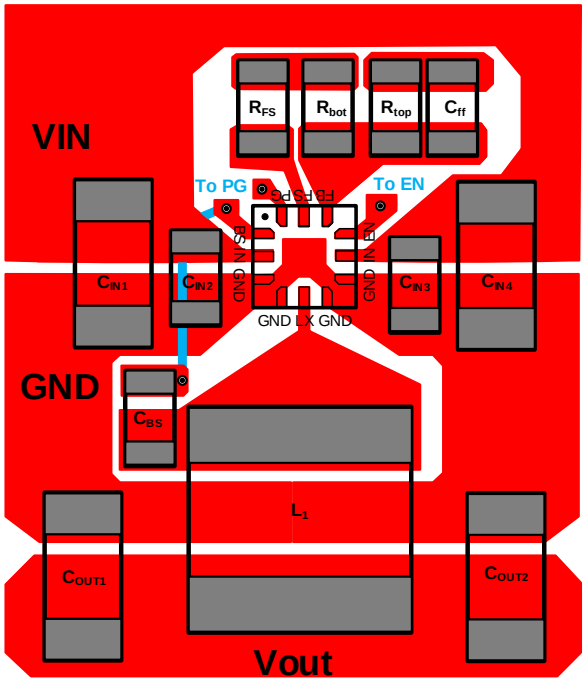
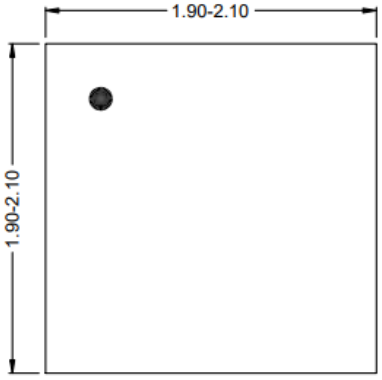
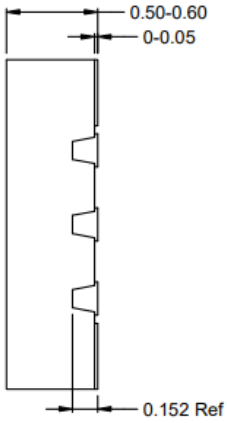


Figure 9. Suggested PCB Layout

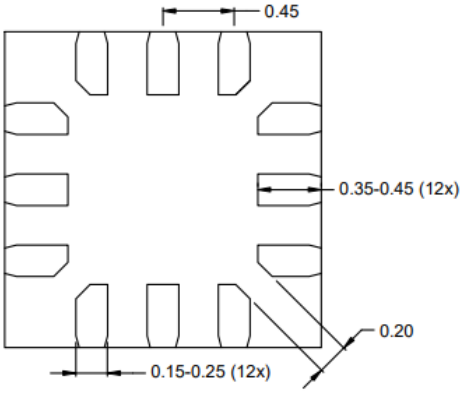
QFN2×2-12 Package Outline Drawing



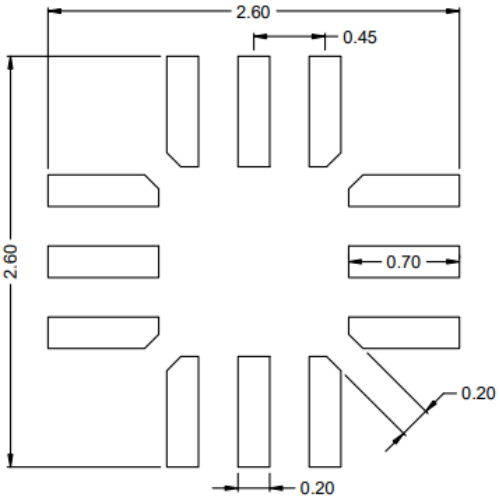
Top View



Side View



Bottom View



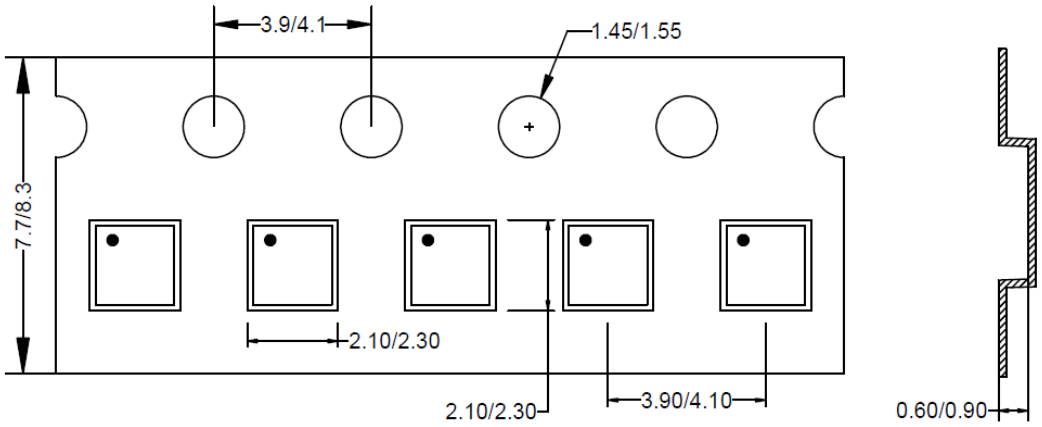
Recommended PCB Layout

Notes: *1. All dimensions in millimeter and exclude mold flash & metal burr.*

2. Recommended PCB layout only for reference.

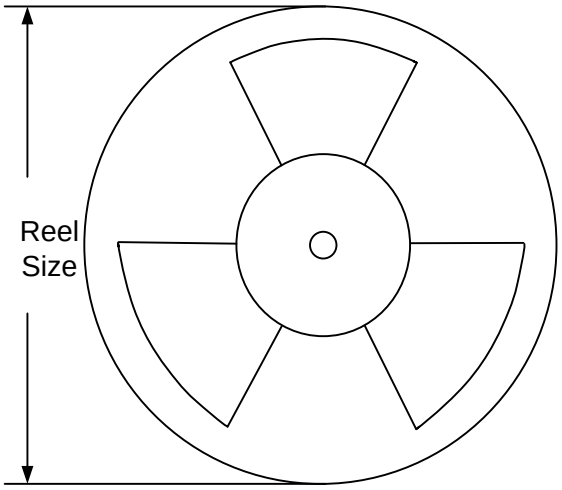
Tape and Reel Specification

Tape Dimensions and Pin 1 Orientation



Direction of feed ⟶

Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2×2	8	4	7"	400	160	3000

All Dimension are nominal

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Jun.10, 2025	Revision 1.0	SA24483TLQ initial release.	-
Sep.19, 2025	Revision 1.0A	1. OTP typical value change from 160°C to 165°C.	Page 5
		2. Add an annotation "R_{fs} open" Row in Table 1.	Page 18
Oct.15, 2025	Revision 1.0A1	Change SA24481TLQ recommend BOM list C7 from 47pF to 33pF on 2.2MHz application.	Page21
Oct.27, 2025	Revision 1.0A2	SA24483ETLQ initial release.	-
Nov.12, 2025	Revision 1.0A3	1. SA24481TLQ initial release. 2. Add “Typical Performance Characteristics” of SA24481TLQ.	P6-9

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