SA24506

High Efficiency, 36V Input, 6A Synchronous Step-Down Regulator

General Description

The SA24506 is a high-efficiency synchronous step-down DC-DC regulator featuring internal power and synchronous rectifier switches. It operates with fixed frequency and peak current control across a wide input voltage range of 3.5V to 36V, delivering up to 6A of continuous output current.

The SA24506 is specifically designed with a symmetric QFN package and adjustable LX rise time to achieve optimal EMI performance. The switching frequency can be adjusted from 300kHz to 2.3MHz, or synchronized to an external clock. The frequency selection allows for compliance with application EMI limits and helps to avoid noise in critical frequency bands.

The SA24506 offers excellent efficiency across a wide range of applications by providing internal 41mΩ power and 21mΩ synchronous rectifier switches, frequency reduction at light load conditions, and an external bias input. The 1μA shutdown supply current enables the device to be used in battery-powered applications. The SA24506 ensures safe operation under all conditions, offering cycle-by-cycle current limiting, input under-voltage lockout, internal soft-start, output under-voltage and over-voltage protection, and thermal shutdown.

The SA24506 is available in a QFN 3.5×4-14 package with wettable flanks.

Features

- 3.5V to 36V Input Voltage Range
- Support 42V Load Dump
- Support 3.0V Cold Crank
- 6A Output Current Capability
- Low $R_{DS(ON)}$ for Internal Switches: 41mΩ Top, 21mΩ Bottom
- Typical 11.5μA Quiescent Current and 1μA Shutdown Current.
- 300kHz to 2.3MHz Switching Frequency
- Synchronization to External Clock
- Spread Spectrum Function
- Hiccup Mode Output Short-Circuit Protection
- EN On/Off Control with Accurate Threshold
- Cycle-by-Cycle Peak Current Limit
- Power Good Indicator
- 1V ±1% Reference Voltage Over -40˚C to 150˚C Temperature Range
- QFN3.5×4-14 Package with Wettable Flanks
- Automotive AEC- Q100 Grade 1 Certified

Applications

- Automotive
- Industrial
- High Voltage DC/DC Converters

Typical Application

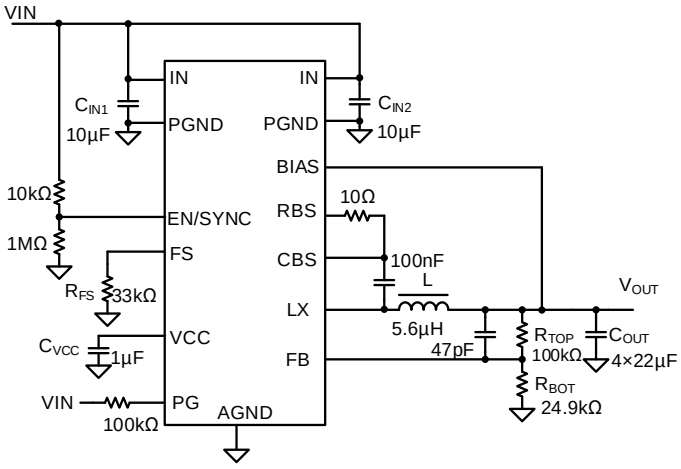

Figure 1. Schematic Diagram

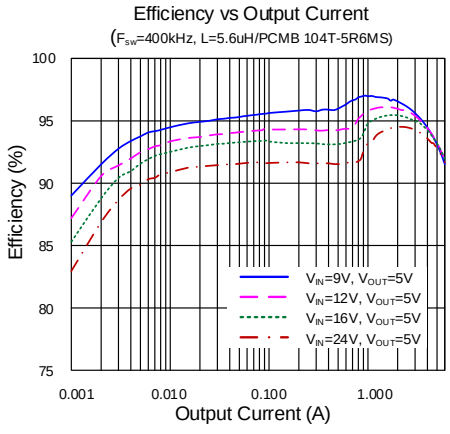

Figure 2. Efficiency vs. Output Current

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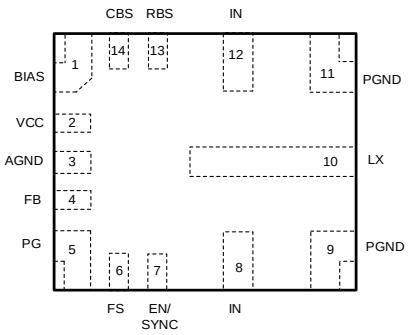
Ordering Information

Ordering Part Number	Package Type	Top Mark
SA24506XNQ	QFN3.5×4-14 RoHS-Compliant and Halogen-Free	**AATA*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



（QFN3.5×4-14）

Pin Description

Pin Name	Pin Number	Pin Description
BIAS	1	Input to internal LDO. Connect this pin to the output point for improved efficiency. Place a ceramic capacitor with value of 1μF or higher between BIAS and GND for improved noise immunity.
VCC	2	Decouple this pin to GND with at least a 1μF ceramic capacitor.
AGND	3	Analog ground pin.
FB	4	Output Feedback Pin. Connect this pin to the center point of the output resistor divider to program the output voltage: $V_{OUT} = 1\times(1 + R_{TOP}/R_{BOT})$.
PG	5	Power good indicator, open-drain output. PG is externally pulled high when the FB pin voltage is between 93.3% and 112% of the reference voltage. The PG pin is internally pulled low when the FB pin voltage is lower than 90% or greater than 115% of the reference voltage.
FS	6	Oscillator frequency programmable pin. Connect an external resistor to set the switching frequency F_{SW}. $F_{SW}(kHz) = 1.346 \times 10^4/(R_{FS}(k\Omega) + 0.444)$.
EN/SYNC	7	Enable control. Pull high to enable the device, pull low to disable the device. This pin can be used as an adjustable UVLO if it is connected to V_{IN} and GND through proper resistors. Do not leave floating. EN/SYNC also functions as a synchronization input. When it is connected to an external clock, the internal oscillator synchronizes to the external clock, and the device functions in forced PWM mode.
IN	8,12	Input pin. Decouple this pin to GND with at least a 22μF ceramic capacitor.
PGND	9,11	Power ground pin.
LX	10	Inductor pin. Connect this pin to the switching node of the inductor.
RBS	13	Connect to CBS through a resistor. This resistance can be used to determine LX node rise time.
CBS	14	Bootstrap pin. Supply high side gate driver. Connect a 0.1μF capacitor between this and the LX pins.

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Block Diagram

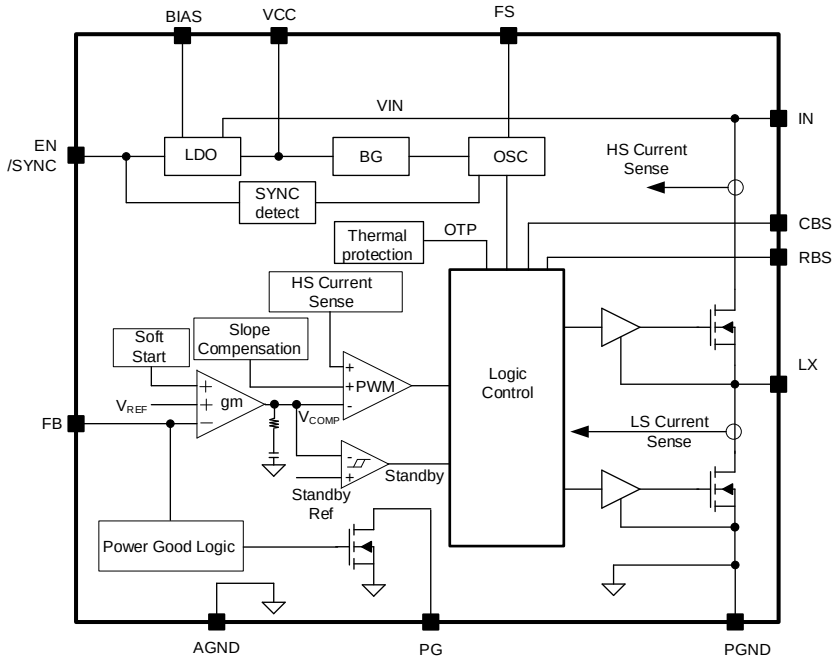

Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN, EN/SYNC, PG	-0.3	40	V
Dynamic IN, EN/SYNC Voltage for Load Dump	-0.3	42	
LX	-0.3	IN + 0.3	
Dynamic LX Voltage in 20ns Duration	GND - 5	IN + 5	
Dynamic LX Voltage in 1μs Duration	-1		
VCC, FB, FS	-0.3	6	
CBS -LX, RBS-LX	-0.3	6	
BIAS	-0.3	16	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10s)		260	
Storage Temperature	-65	150	
ESD Susceptibility			
HBM (Human Body Model)		±2000	V
CDM (Charged Device Model)		±750	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	34	°C/W
$\theta_{JC(top)}$ Junction-to-Case (Top) Thermal Resistance	22	
θ_{JB} Junction-to-Board Thermal Resistance	14	
P_D Power Dissipation T_A = 25°C	3.67	W
Parameter (Note 3)	**Typ**	**Unit**
θ_{JA} Junction-to-Ambient Thermal Resistance	62.3	°C/W

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Recommended Operating Conditions

Parameter (Note 4)	Min	Max	Unit
IN	3.5	36	V
OUT	1	0.95*V_{IN}	V
Junction Temperature	-40	150	°C
Ambient Temperature	-40	125	°C

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Electrical Characteristics

(V_{IN} = 12V, T_J = -40°C to +150°C. Typical values are at T_J = 25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation. (**Note 5**)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	UVLO Rising Threshold	$V_{IN,UVLO\_R}$		3.2	3.3	3.45	V
	UVLO Falling Threshold	$V_{IN,UVLO\_F}$		2.7	2.85	3.0	V
	Quiescent Current	I_{Q_VIN1}	V_{FB} = 105% × V_{REF}, no switching, V_{BIAS}=0V, measured on VIN pin		23		µA
		I_{Q_VIN2}	V_{FB} = 105% × V_{REF}, no switching, V_{BIAS}=5V, measured on VIN pin		3		µA
		I_{BIAS}	V_{FB} = 105% × V_{REF}, no switching, V_{BIAS}=5V, measured on BIAS pin		20		µA
		I_{Q_VIN3}	V_{FB} = 105% × V_{REF}, no switching, V_{BIAS}=Vout=5V, measured on VIN pin. **(Note 6)**		11.5		µA
	Shutdown Current	I_{SHDN}	V_{EN} = 0V, Typical value at T_J=25°C, Max value at T_J=150°C		1	7	µA
Output	Reference Voltage	V_{REF}		0.99	1	1.01	V
	Soft-Start Time	t_{SS}		0.6	1	1.5	ms
MOSFET	Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			41		mΩ
	Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			21		mΩ
	Top FET Current Limit	$I_{LMT,TOP}$		8	10	12.5	A
	Bottom FET Current Limit	$I_{LIM,BOT}$			7.5	9	A
	Bottom FET Negative Current Limit	$I_{LIM,NEG}$		-2	-3	-4	A
EN/SYNC	Input Voltage High	$V_{EN,H}$		1.1	1.2	1.3	V
	Input Voltage Low	$V_{EN,L}$		0.9	1.0	1.1	V
	Edge Height for SYNC	$V_{EN,SYNC}$	Rise/fall time < 30ns **(Note 7)**			3.6	V
Power-Good	Thresholds	$V_{PG,\ R}$	V_{FB} rising, PG from low to high	90.3	93.3	96.3	%
		$V_{PG,F}$	V_{FB} falling, PG from high to low	87	90	93	%
		$V_{PG,R}$	V_{FB} falling, PG from low to high	109	112	115	%
		$V_{PG,F}$	V_{FB} rising, PG from high to low	112	115	118	%
	PG Deglitch Time	T_{PG}			100		µs
	PG Output Low	$V_{PG,L}$	2mA sink current		0.1	0.3	V
	PG Leakage Current	$I_{PG,LK}$	PG high			1	µA
Switching Frequency	Switching Frequency Program Range	$F_{SW,RNG}$		300		2300	kHz
	Switching Frequency Setting Accuracy	F_{SW}	R_{FS} = 5.49k	2.00	2.27	2.54	MHz
			R_{FS} = 33k	352	400	448	kHz
	SYNC External Clock	f_{SYNC}	F_{SW}=400kHz	385	400		kHz
		f_{SYNC}	F_{SW}=2.1MHz	2.02	2.1		MHz
	Spread Spectrum	SSC	Percentage of F_{SW}		±6		%
	Minimum On Time	$t_{ON,MIN}$	**(Note 7)**		60		ns
	Minimum Off Time	$t_{OFF,MIN}$	**(Note 7)**		120		ns
	Maximum On Time	$T_{ON,MAX}$			100		µs
VCC	VCC Output Voltage	V_{CC}	V_{BIAS}>5.2V or V_{BIAS}<4V	4.8	5	5.2	V
BIAS	V_{BIAS} Rising Threshold	$V_{BIAS,R}$			4.5		V

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	V_{BIAS} Falling Threshold	$V_{BIAS,F}$			4.25		V
OVP	Output Over Voltage	V_{OVP}	V_{FB} rising	112	115	118	%
OTP	Temperature	T_{OTP}		150	165	180	°C
	Temperature Hysteresis	T_{HYS}			20		°C
SCP	Short Circuit Protection Threshold	V_{SCP}	V_{FB} as percent of V_{REF}	40	50	60	$\%V_{REF}$

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device under these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in natural convection at T_A = 25°C on a 2oz four-layer Silergy evaluation board. The case temperature θ_{JC} is measured at pin 10.

Note 3: θ_{JA} is measured in natural convection at T_A = 25°C on a four-layer test board of JESD51-7 thermal measurement standard.

Note 4: The device is not guaranteed to function outside its operating conditions.

Note 5: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \approx T_J$ = 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, testing, or statistical correlation.

Note 6: $I_{Q\_VIN3} = I_{Q\_VIN2} + I_{BIAS} \times (V_{OUT} / V_{IN})$.

Note 7: Guaranteed by design or statistical correlation and not production tested.

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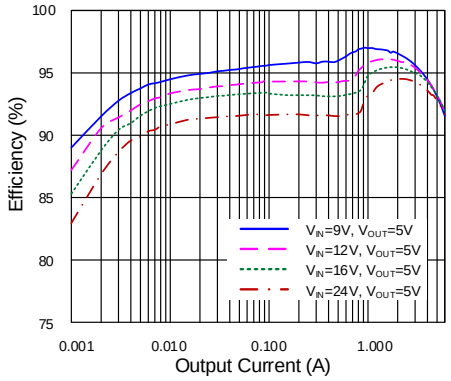
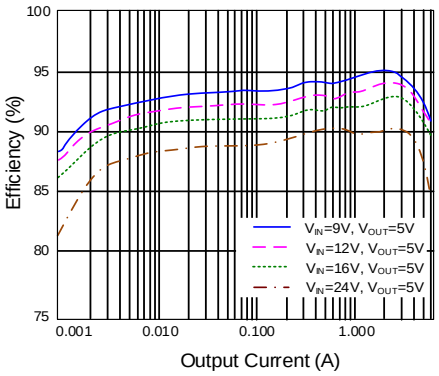
Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 12V, V_{OUT} = 5V, L = 5.6μH, C_{OUT} = 4 × 22μF/25V, F_{SW} = 400kHz, unless otherwise noted. The circuit is shown in the Application Schematic section.)

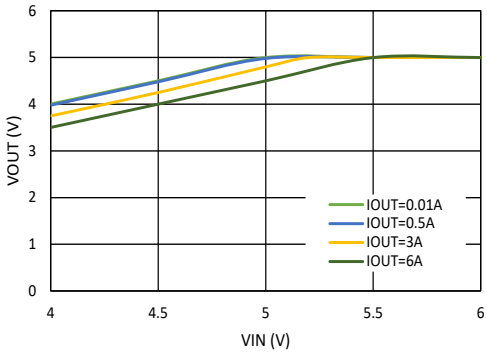
Efficiency vs Output Current
(F_{SW}=400kHz, L=5.6uH/PCMB 104T-5R6MS)



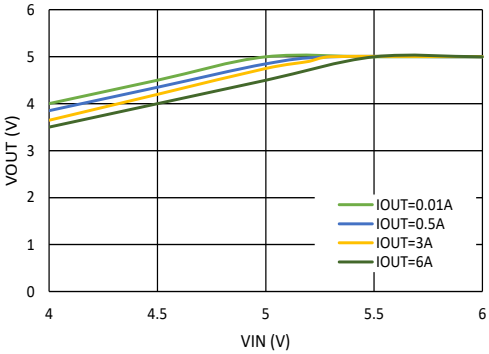
Efficiency vs Output Current
(Fsw=2.2MHz, L=1.0uH/PCMB 104T-1R0MS)



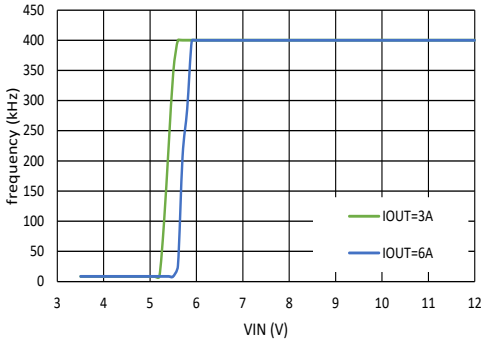
V_{OUT} Dropout Voltage vs V_{IN}
(F_{SW}=400kHz, V_{OUT}=5V)



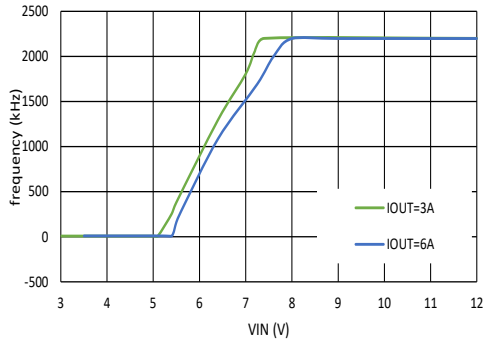
V_{OUT} Dropout Voltage vs V_{IN}
(F_{SW}=2.2MHz, V_{OUT}=5V)



Frequency Foldback vs V_{IN}
(F_{SW}=400kHz, V_{OUT}=5V)



Frequency Foldback vs V_{IN}
(F_{SW}=2.2MHz, V_{OUT}=5V)



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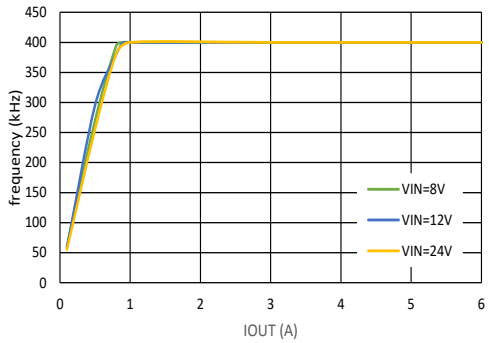
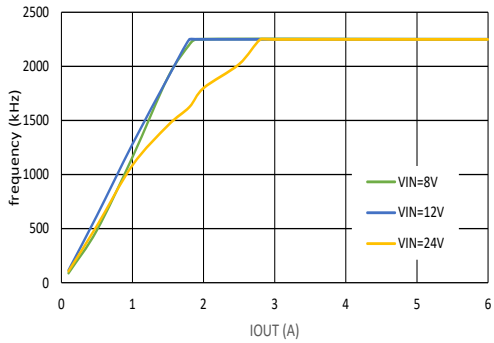
Frequency (PFM/CCM Switch Point) vs I_{OUT}

(F_{SW}=400kHz, V_{OUT}=5V)



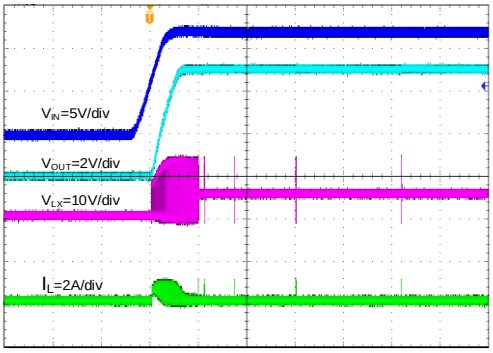
Frequency (PFM/CCM Switch Point) vs I_{OUT}

(F_{SW}=2.2MHz, V_{OUT}=5V)



Startup From V_{IN}

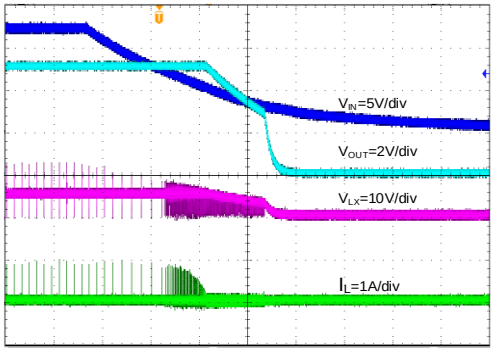
(V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (2ms/div)

Shutdown From V_{IN}

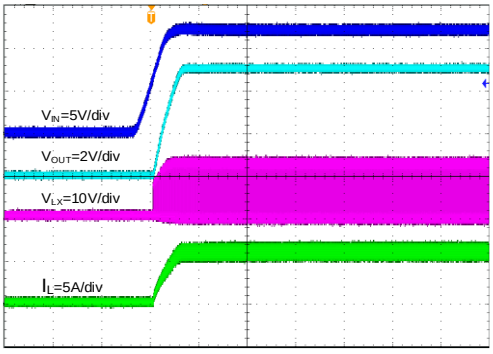
(V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (100ms/div)

Startup From V_{IN}

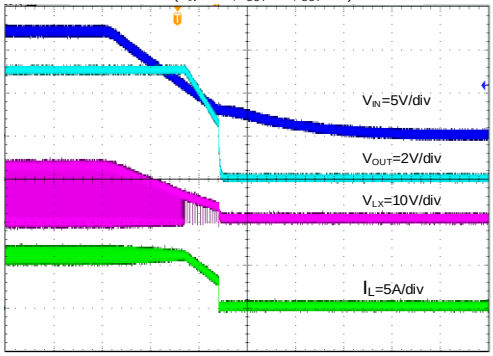
(V_{IN}=12V,V_{OUT}=5V,I_{OUT}=6A)



Time (2ms/div)

Shutdown From V_{IN}

(V_{IN}=12V,V_{OUT}=5V,I_{OUT}=6A)



Time (4ms/div)

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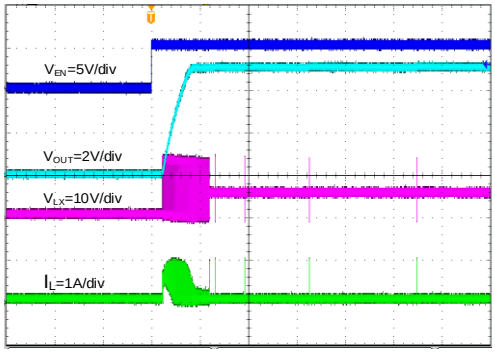
Startup From Enable

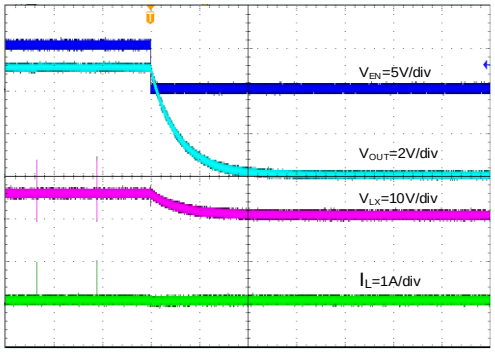
(V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (2ms/div)

Shutdown From Enable

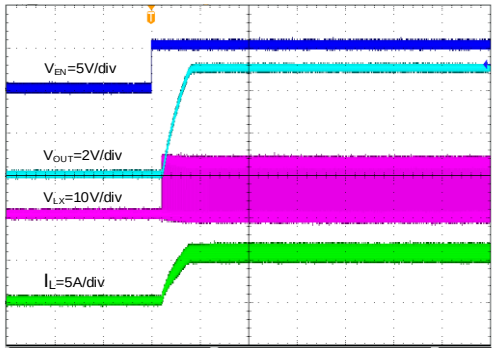
(V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (20ms/div)

Startup From Enable

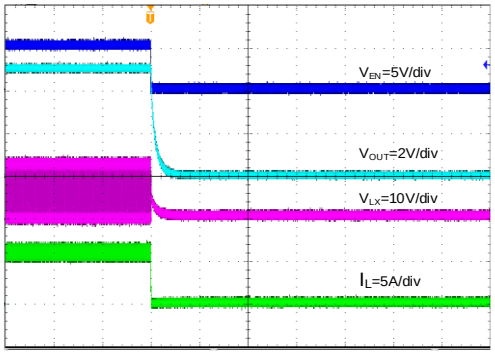
(V_{IN}=12V,V_{OUT}=5V,I_{OUT}=6A)



Time (2ms/div)

Shutdown From Enable

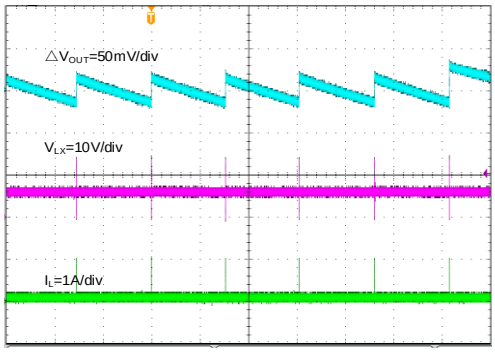
(V_{IN}=12V,V_{OUT}=5V,I_{OUT}=6A)



Time (800μs/div)

Output Ripple

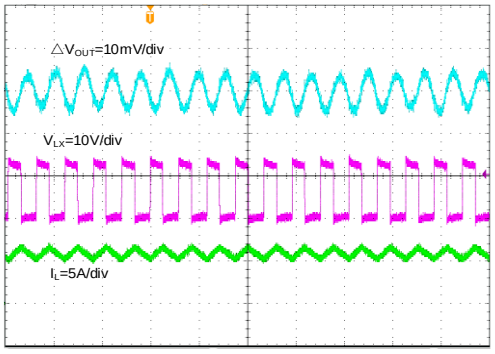
(V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (10ms/div)

Output Ripple

(V_{IN}=12V,V_{OUT}=5V,I_{OUT}=6A)



Time (4μs/div)

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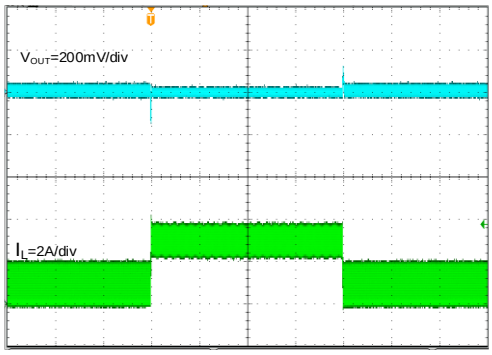
Load Transient

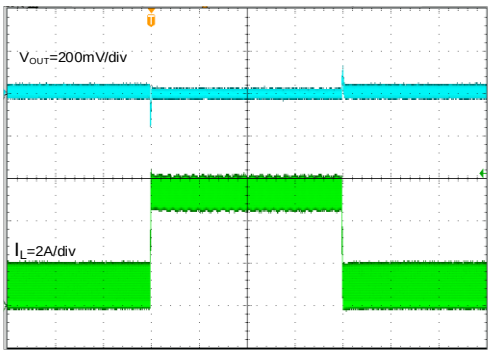
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.6 A ~ 3A)



Time (2ms/div)

Load Transient

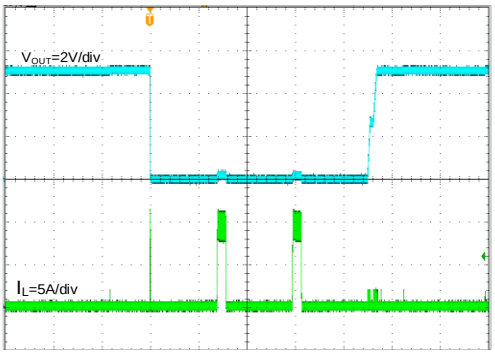
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.6 A ~ 5.4A)



Time (2ms/div)

Short Circuit Protection

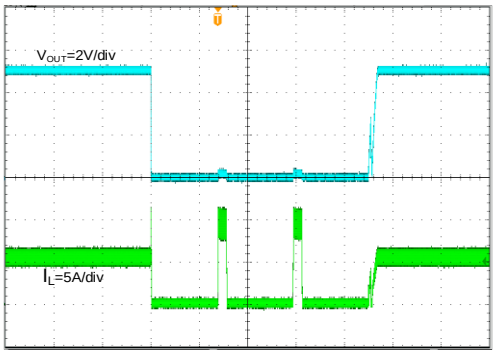
(V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (10ms/div)

Short Circuit Protection

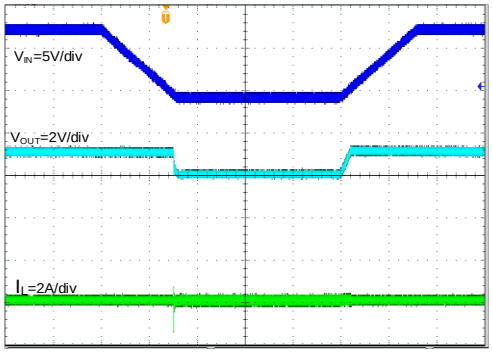
(V_{IN}=12V,V_{OUT}=5V,I_{OUT}=6A)



Time (10ms/div)

Recovery from Dropout

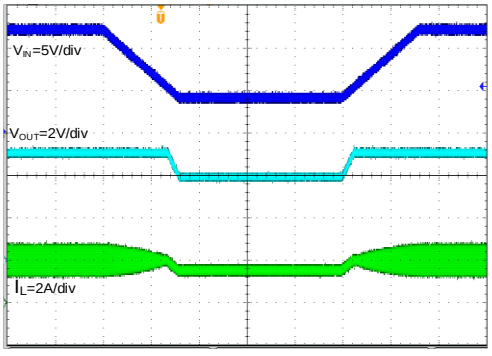
(V_{IN}=12V to 4V to 12V, V_{OUT}=5V, I_{OUT}=0A)



Time (10ms/div)

Recovery from Dropout

(V_{IN}=12V to 4V to 12V, V_{OUT}=5V, I_{OUT}=2A)



Time (10ms/div)

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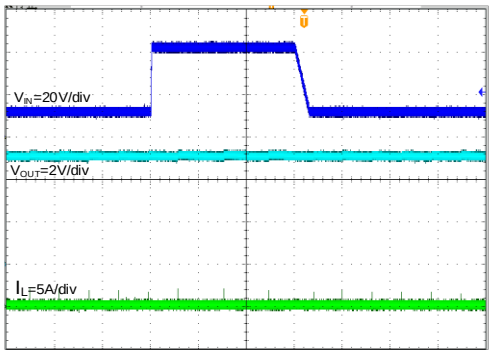
Load Dump

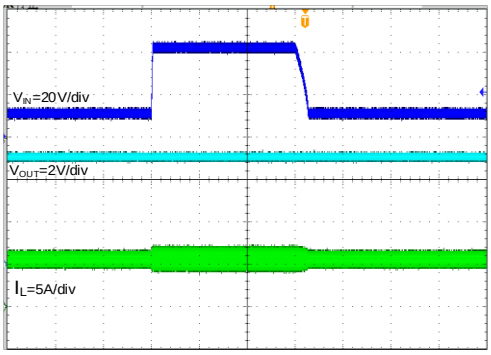
(V_{IN}=12V to 42V, V_{OUT}=5V, I_{OUT}=0A)



Time (100ms/div)

Load Dump

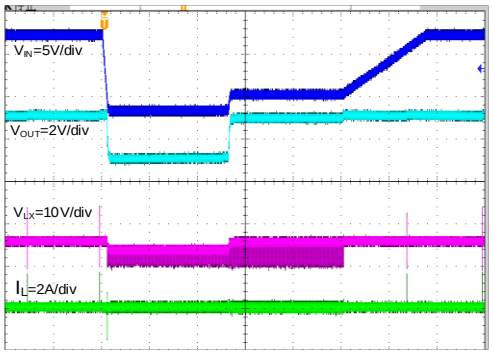
(V_{IN}=12V to 42V, V_{OUT}=5V, I_{OUT}=6A)



Time (100ms/div)

Cold Crank

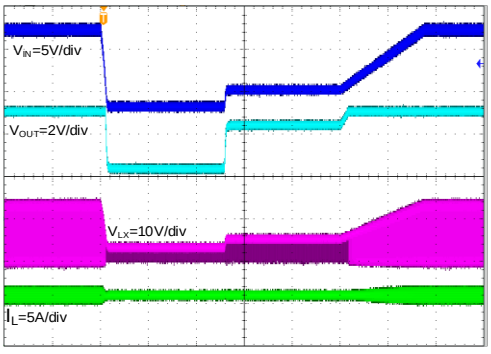
(V_{IN}=12V to 3V to 5V to 12V, V_{OUT}=5V, I_{OUT}=0A)



Time (40ms/div)

Cold Crank

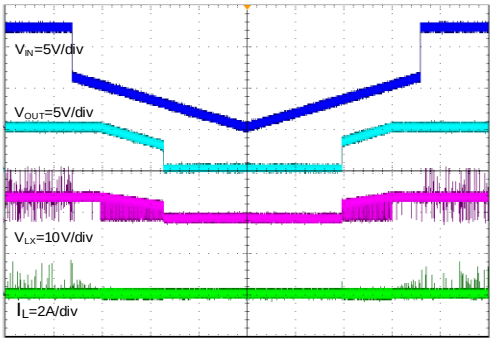
(V_{IN}=12V to 3V to 5V to 12V, V_{OUT}=5V, I_{OUT}=6A)



Time (40ms/div)

V_{IN} Ramps Down and Up Test

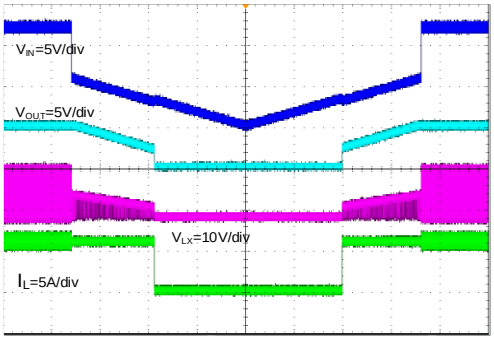
(V_{IN}=12V to 0V, V_{OUT}=5V, I_{OUT}=0A)



Time (200s/div)

V_{IN} Ramps Down and Up Test

(V_{IN}=12V to 0V, V_{OUT}=5V, I_{OUT}=6A)



Time (200s/div)

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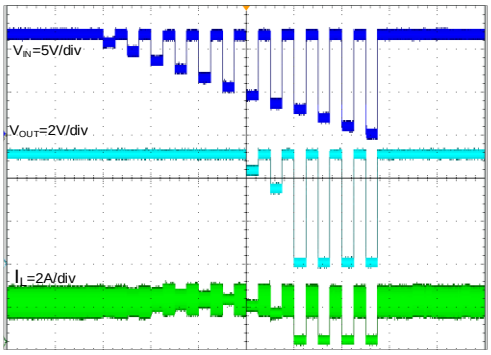
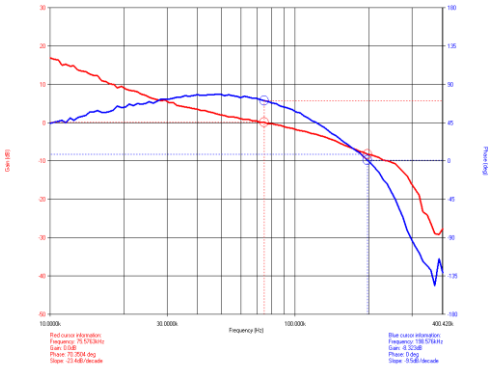
Reset Behavior at Voltage Drop

(V_{IN}=12V to 0V, V_{OUT}=5V, I_{OUT}=2A)



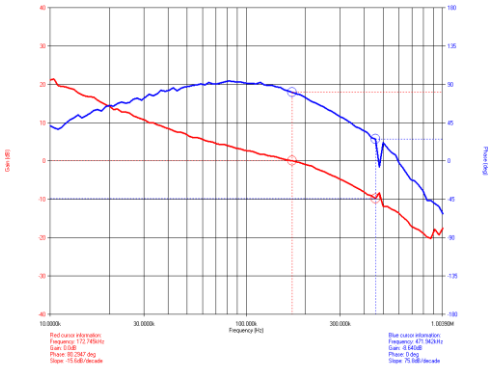
Bode Plot

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=400kHz)



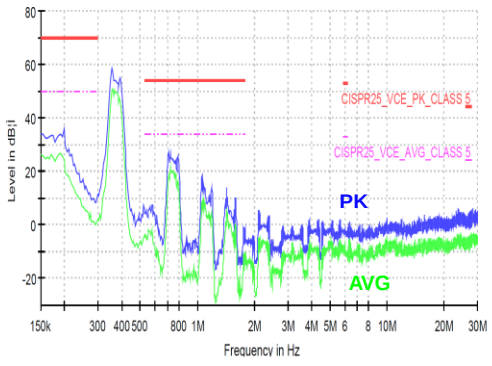
Bode Plot

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=2.2MHz)



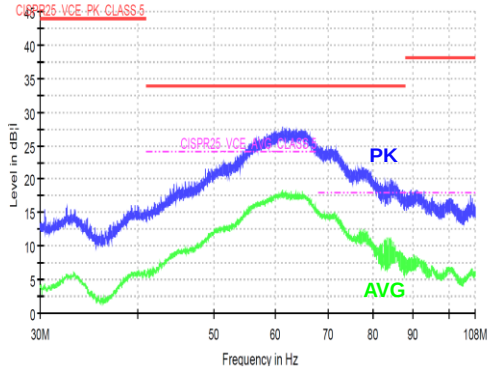
CISPR 25 Class 5 Conducted Emission

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=400kHz,
SubRange: 150kHz~30MHz)



CISPR 25 Class 5 Conducted Emission

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=400kHz,
SubRange: 30MHz~108MHz)



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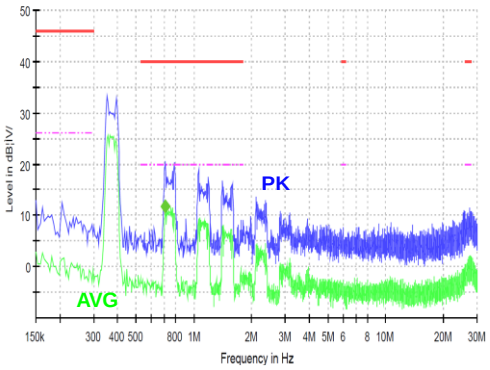
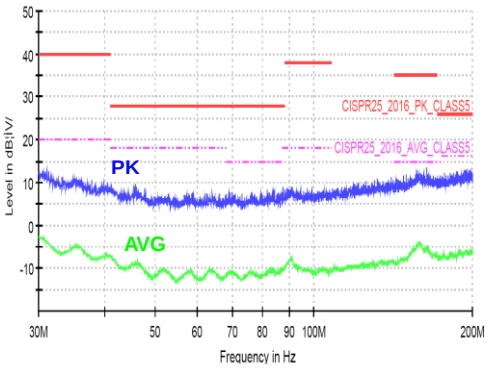
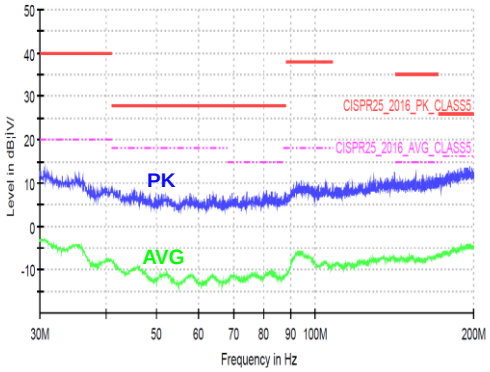
CISPR 25 Class 5 Radiated Emission
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=400kHz,
SubRange: 150kHz~30MHz)



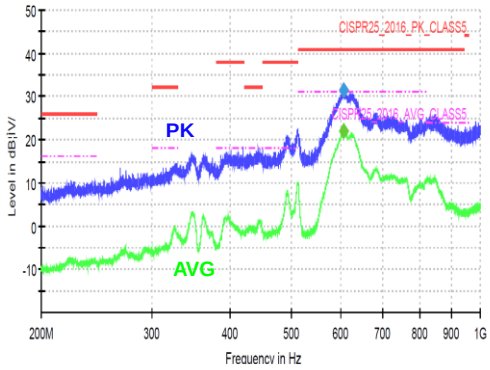
CISPR 25 Class 5 Radiated Emission
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=400kHz,
Horizontal SubRange: 30MHz~200MHz)



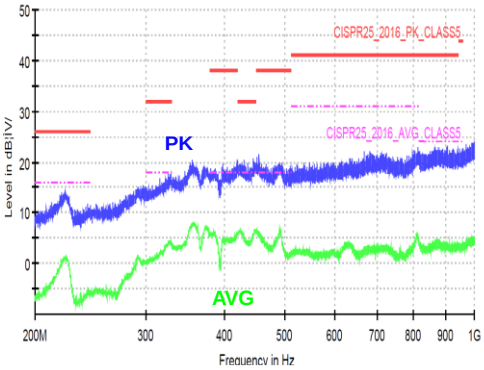
CISPR 25 Class 5 Radiated Emission
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=400kHz,
Vertical SubRange: 30MHz~200MHz)



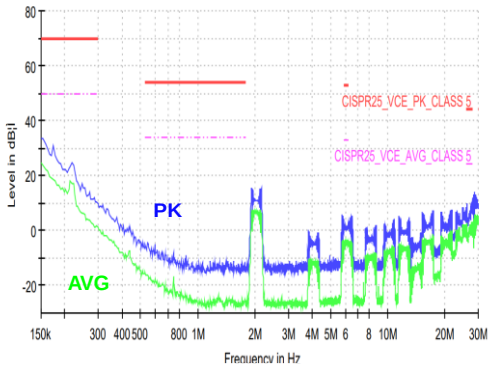
CISPR 25 Class 5 Radiated Emission
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=400kHz,
Horizontal SubRange: 200MHz~1GHz)



CISPR 25 Class 5 Radiated Emission
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=400kHz,
Vertical SubRange: 200MHz~1GHz)



CISPR 25 Class 5 Conducted Emission
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=2.2MHz,
SubRange: 150kHz~30MHz)



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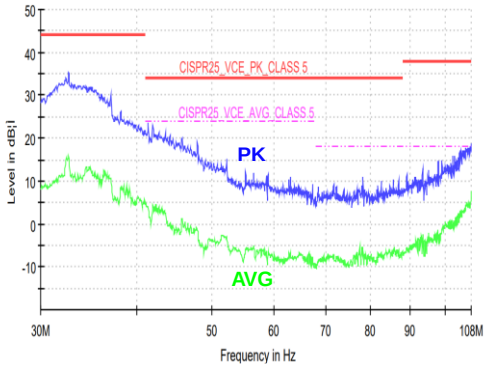
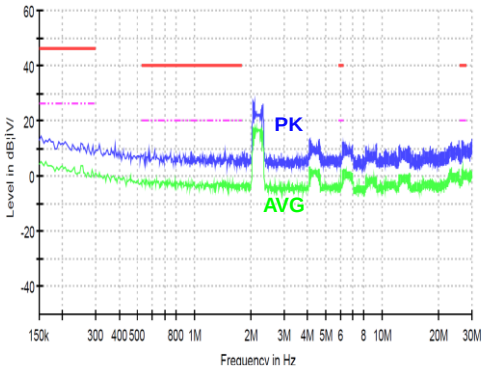
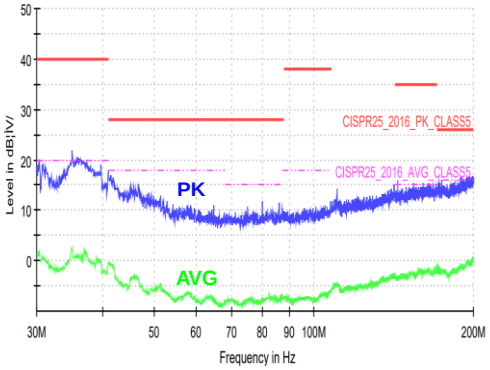
CISPR 25 Class 5 Conducted Emission
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=2.2MHz,
SubRange: 30MHz~108MHz)



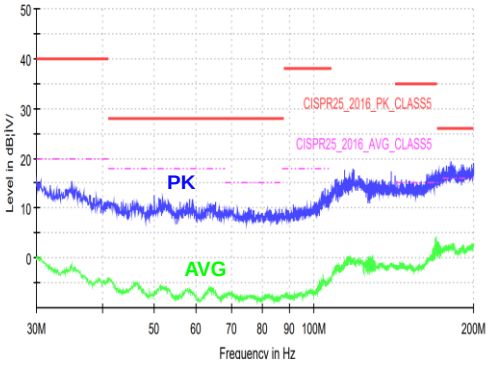
CISPR 25 Class 5 Radiated Emission
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=2.2MHz,
SubRange: 150kHz~30MHz)



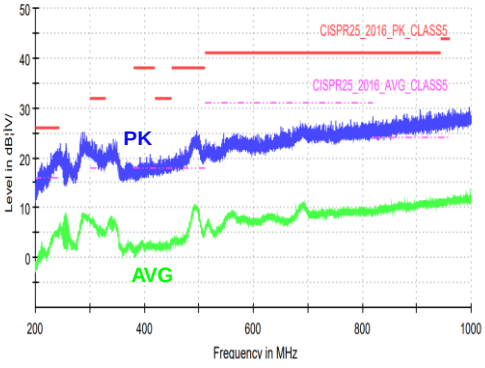
CISPR 25 Class 5 Radiated Emission
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=2.2MHz,
Horizontal SubRange: 30MHz~200MHz)



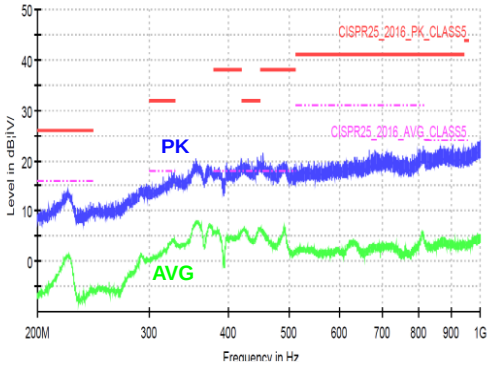
CISPR 25 Class 5 Radiated Emission
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=2.2MHz,
Vertical SubRange: 30MHz~200MHz)



CISPR 25 Class 5 Radiated Emission
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=2.2MHz,
Horizontal SubRange: 200MHz~1GHz)



CISPR 25 Class 5 Radiated Emission
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, F_{SW}=2.2MHz,
Vertical SubRange: 200MHz~1GHz)



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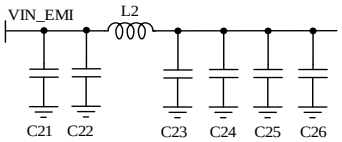
EMI Filter



C_{21}, C_{22}, C_{23}, C_{24}	2.2μF/50V/X7T/0805
C_{25}, C_{26}	0.47μF/50V/X7T/0603
L_2	1uH

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Functional Description

The SA24506 is a high-efficiency synchronous step-down DC-DC regulator featuring internal power and synchronous rectifier switches. It operates with fixed frequency and peak current control over a wide input voltage range of 3.5V to 36V, and can deliver up to 6A of continuous output current.

The SA24506 is specifically designed with a symmetric QFN package and an adjustable LX rise time to achieve optimal EMI performance. The switching frequency can be adjusted from 300 kHz to 2.3MHz, or synchronized to an external clock. The frequency can be selected to meet application EMI limits and to avoid noise in critical frequency bands.

The SA24506 offers excellent efficiency across a wide range of applications by providing internal 41mΩ power and 21mΩ synchronous rectifier switches, frequency reduction under light load conditions, and an external bias input. The 1μA shutdown supply current allows the device to be utilized in battery-powered applications. The SA24506 ensures safe operation under all operating conditions by providing cycle-by-cycle current limiting, input under voltage lockout, internal soft-start, output under voltage and overvoltage protection, and thermal shutdown.

General Features

Fixed Frequency PWM Control and Slope Compensation

The SA24506 employs a constant frequency peak current mode control strategy. The oscillator functions as a clock to ensure an accurate switching frequency. When the clock timer expires, the top FET is activated, and the inductor current ramps up. The top FET current is sensed and compared to the output of the error amplifier. When the current ramp reaches the internal V_{COMP}, the top FET will turn off, and the bottom FET will turn on until the next clock cycle.

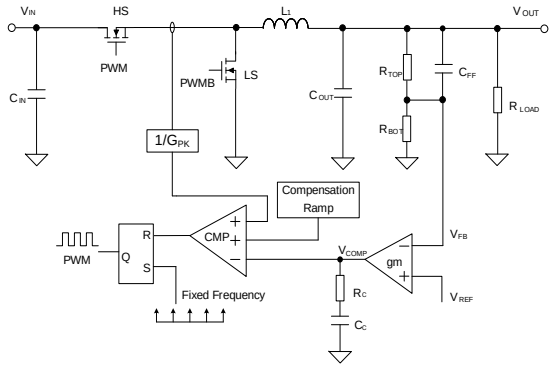

Figure 4. Fixed Frequency PWM Control and Slope Compensation

Light Load Operation

The SA24506 provides two light load operation modes: pulse frequency modulation (PFM) (default) and forced continuous current mode (FCCM). In PFM mode, the low-side synchronous rectifier is turned off when the current through the rectifier ramps to zero, preventing recirculation current that can reduce efficiency under light load conditions. Additionally, the output of the error amplifier (V_{COMP}) naturally decreases, which in turn reduces the peak current during light load conditions. When V_{COMP} decreases further with the decreasing load and reaches the preset low threshold, the device stops switching to minimize switching power loss and quiescent current, thereby improving light load efficiency. Switching resumes when V_{COMP} rises above the low threshold.

When EN/SYNC is used for synchronization and the internal oscillator is synchronized to an external clock, the SA24506 operates in FCCM mode across the entire output current range, including at low loads. The low-side synchronous rectifier remains on even when the inductor current crosses zero. Current flow continues until the high-side MOSFET switches on.

EN/SYNC and Adjustable Input Under voltage Lockout

The EN/SYNC input supports high voltage and logic-compatible thresholds. The input comparator design features a relatively accurate rising threshold. When the EN voltage rises to approximately 0.8V, VCC provides the EN comparator with the source supply. When the EN voltage is driven above $V_{EN,H}$, normal device operation is enabled, and the converter begins switching. When the EN voltage falls below $V_{EN,L}$, the device stops switching. When the EN voltage is driven lower than 0.4V, the device is shut down, reducing the input current to 1μA (typical).

If the default input UVLO threshold is too low for certain applications, a resistor divider can be added between VIN and GND, with the midpoint connected to EN, to adjust the input UVLO to a higher threshold. This pin does not have an internal pulldown resistor and should not be left floating.

The EN/SYNC pin can also serve as a synchronization input for the switching frequency. When an external clock, which is higher than the internal clock, is connected to EN/SYNC, the internal oscillator will synchronize to the external clock, spread spectrum will be disabled, and the IC will operate in FCCM mode under light load conditions. Note that the external clock detection is activated after the soft start is completed.

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VCC Linear Regulator and BIAS Input

The 5V internal linear regulator input (VCC) supplies power to the internal gate drivers, PWM logic, analog circuitry, and other blocks. Connect a low ESR ceramic capacitor with a minimum capacitance of 1μF from VCC to GND.

The BIAS pin is one of the inputs to the internal LDO. Connecting this pin to the output can reduce power loss caused by the internal LDO and improve efficiency. If the BIAS voltage is less than 4.25V (typical), the internal LDO will be powered directly by VIN.

When powering from V_{OUT}, place a ceramic capacitor with a value of 1μF or higher between BIAS and GND to reduce noise.

Power Good Indication

The power-good indicator is an open-drain output controlled by a window comparator connected to the feedback signal. If VFB is within the power-good range, PG will be in a high-impedance state. Otherwise, it will be pulled low. PG should be connected to VIN or another voltage source through a resistor (e.g., 10kΩ~100kΩ). Note that PG is pulled low before the soft start is completed.

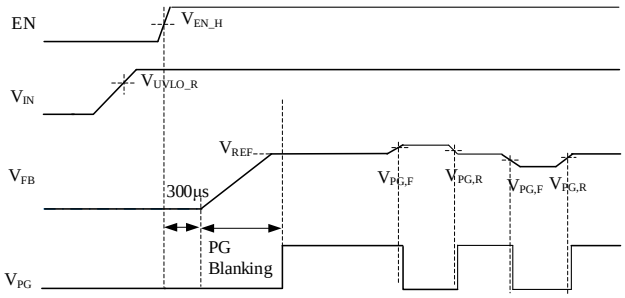

Figure 5. Power Good Logic

Adaptive Frequency Control at Dropout Operation and Low Duty Operation

In the dropout operation, the control circuit regulates the turn-off time of the top FET to ensure it is the minimum off time within each switching period, and it adjusts the on time once the maximum on time has expired. The maximum duty cycle can reach up to 99.8% over the -40°C to 125°C temperature range.

In low-duty operation, the control circuit regulates the turn-on time of the top FET to the minimum on-time in each switching period and adjusts the switching period to further reduce the duty cycle.

External Bootstrap Capacitor

The SA24506 integrates a floating power supply for the gate driver that operates the internal high-side N-channel power MOSFET. Connect a 0.1 μF low ESR ceramic capacitor between BS and LX for proper operation.

Adjustable LX Rising Time

The rising time (10%~90%) of LX node can be configured from 2.5ns to 12ns by a resistor between RBS and CBS. See Figure below.

The LX rising time can be adjusted for better efficiency when smaller RBS is used, or better EMI performance when larger RBS is used.

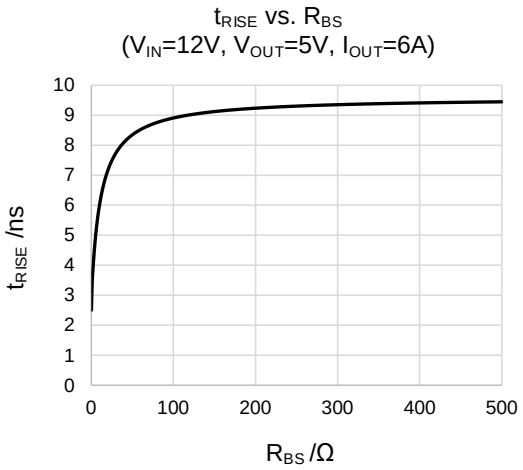

Figure 6. LX Rising Time

Adjustable Switching Frequency

The switching frequency can be adjusted from 300kHz to 2.3MHz by connecting a resistor between FS and GND. The switching frequency can be calculated using the following equation:

$$F_{SW}(kHz) = \frac{1.346 \times 10^4}{R_{FS}(k\Omega) + 0.444}$$

Note that the stability of the part will be affected if the on-time is close to the minimum on-time, $t_{ON,MIN}$. Table 1 presents the switching frequency and RFS values for typical applications.

Table 1. Adjustable Switching Frequency

F_{SW}(kHz)	R_{FS}(kΩ)	V_{IN}(V), V_{OUT}= 5V	
		12	36
300	44.2	✓	✓
400	33	✓	✓
1000	13.3	✓	✓
2200	5.49	✓	×

Frequency Spread Spectrum

The spread spectrum function is employed to optimize electromagnetic interference (EMI) performance. The

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operating frequency is varied ± 6% around the set switching frequency. The modulation signal is a triangular wave with a period of 330 µs. Consequently, Fsw ramps down by 6% and returns to the center frequency in 165 µs, then ramps up by 6% and returns to the center frequency in another 165 µs.

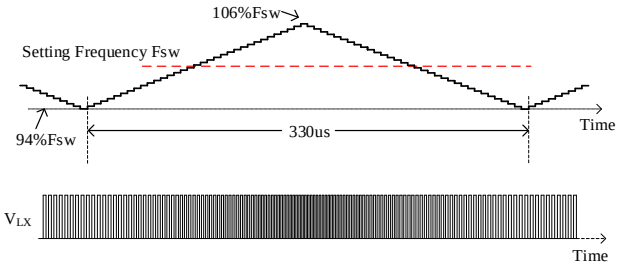

Figure 7. Spread Spectrum Clocking

Fault Protections

Cycle-by-Cycle Current Limit

As the load current increases, the top FET will turn off as soon as the current exceeds the peak current-limit threshold. The bottom FET will then turn on to ramp down the inductor current. The top FET will turn on again only if the inductor current decreases below the bottom FET current limit threshold.

If the load current continues to increase, the output voltage will drop.

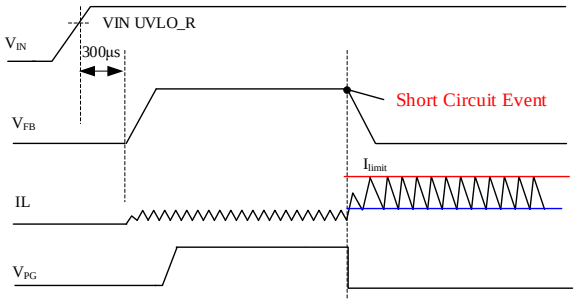

Figure 8. Cycle-by-Cycle Current Limit

Reverse Current Limit Protection

The SA24506 provides cycle-by-cycle reverse current limiting. When the current is below the reverse current limit (-3A, typical), the low-side synchronous rectifier is turned off, and the high-side power switch is turned on. A blanking off-time period is employed at the beginning of the on-time in the low-side synchronous rectifier, during which current sampling is disabled to prevent false triggers caused by switching noise.

Short-Circuit Protection

If VOUT is less than approximately 50% of the target output voltage for at least the SCP delay time (typically 100µs), the output short circuit protection (SCP) will be triggered, and the device will enter hiccup protection mode.

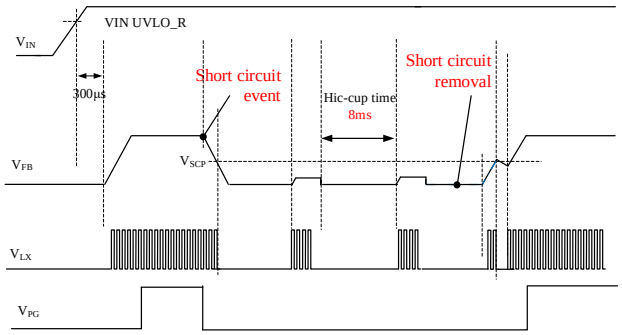

Figure 9. Short-Circuit Protection

When the output fault conditions are removed during the hiccup on-time, the internal soft-start circuit voltage VSS will be temporarily pulled low to avoid output overshoot if VFB exceeds the SCP threshold. Afterward, VSS will rise smoothly to ramp the output to the desired voltage during a new soft-start cycle.

Output Overvoltage Protection (OVP)

The SA24506 provides overvoltage protection. When the FB voltage exceeds VREF, VCOMP will decrease. If the SA24506 is operating in PFM mode, the high-side switch will not turn on when VCOMP is lower than the preset low threshold. However, if the frequency is synchronized to an external clock, switching will continue until the FB exceeds 115% of VREF, at which point overvoltage protection is triggered. The device will resume normal operation when the FB voltage falls below 112% of VREF.

Over temperature Protection (OTP)

The SA24506 includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This circuitry will shut down the device when the junction temperature exceeds 165°C (typ). Once the junction temperature cools by approximately 20°C (typ), the device will resume normal operation after a complete soft-start cycle. For continuous operation, ensure adequate cooling to prevent the junction temperature from exceeding the OTP threshold.

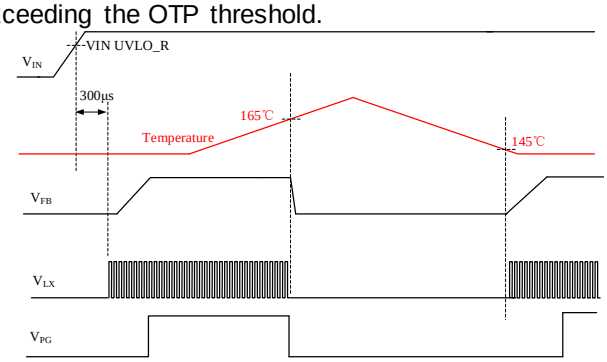

Figure 10. Over Temperature Protection

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Design Procedure

Feedback Resistor Selection

Choose R_{TOP} and R_{BOT} to set the appropriate output voltage. Select large resistance values for both R_{TOP} and R_{BOT} to minimize power consumption under light loads. A recommended value for R_{TOP} is between 10kΩ and 1MΩ. If V_{OUT} = 12V and R_{TOP} is selected to be 100kΩ, R_{BOT} can be calculated as 24.9 kΩ using the following equation:

$$R_{BOT} = \frac{1V}{V_{OUT} - 1V} \times R_{TOP}$$

Input Capacitor Selection

Input filter capacitors are necessary to reduce the ripple voltage at the input, filter the switched current drawn from the input supply, and mitigate electromagnetic interference (EMI). When selecting an input capacitor, choose a voltage rating that is at least 20% greater than the maximum voltage of the input supply and a temperature rating that exceeds the system requirements. X7R series ceramic capacitors are often selected due to their small size, low cost, surge current capability, and high RMS current ratings across a wide temperature and voltage range. Systems powered by wall adapters or other long, inductive wires may be susceptible to significant inductive ringing at the input of the device. In these cases, consider adding bulk capacitance, such as electrolytic, tantalum, or polymer-type capacitors. Utilizing a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is beneficial in these situations.

Consider the RMS current rating of the input capacitor, and parallel additional capacitors if necessary to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a requirement for input voltage ripple in the system, select an appropriate input capacitor that meets the specification. Given the very low equivalent series resistance (ESR) and equivalent series inductance (ESL) of ceramic capacitors, the input voltage ripple can be estimated as follows:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times F_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications, using three 10µF X7R capacitors connected in parallel is sufficient. Place the ceramic input capacitors as close to the IN and GND pins as possible.

Inductor Selection

The inductor is essential for supplying constant current to the output load while being driven by the switched input voltage. Selecting a low inductor value can help reduce size and cost and enhance transient response; however, it will increase peak inductor ripple current, thereby reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low-value inductors may help minimize DC losses and improve efficiency. In contrast, higher inductor values typically exhibit higher DCR and slower transient response.

A reasonable compromise between size, efficiency, and transient response can be achieved by selecting a ripple current (ΔI_L) of approximately 20%–50% of the desired full output load current. Begin calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (F_{SW}), the maximum output current ($I_{OUT,MAX}$), and estimating ΔI_L as a percentage of that current.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times F_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and the required peak inductor current $I_{L,PEAK}$ according to the following equations:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times F_{SW} \times L_1}$$

$$I_{L,PEAK} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current in excess of $I_{L,PEAK}$.

For maximum efficiency, select an inductor with a low DCR that meets the requirements for inductance, size, and cost. Low-loss ferrite materials should be considered.

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Output Capacitor C_{OUT} Selection

Select the output capacitor COUT to meet the output ripple requirements, considering both steady-state ripple and transient conditions. Ceramic and POS types are typically chosen due to their compact size and low cost.

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) affecting the output capacitors' equivalent series resistance (*ESR*) and the stored charge (capacitive ripple). When estimating the total ripple, both factors should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times F_{SW}}$$

It is recommended to use four X7R or better grade ceramic capacitors in parallel, each with a capacitance of at least 22μF for typical applications.

Load Transient Considerations

The device integrates compensation components to achieve good stability and fast transient response. Adding a small ceramic capacitor, CFF in parallel with RTOP may further enhance load transient response and is therefore highly recommended for applications with significant load transient step requirements.

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the IC package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated as follows:

$$P_{D,MAX} = (T_{J,MAX} - T_A) / \theta_{JA}$$

Where $T_{J,MAX}$ is the maximum junction temperature, TA is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 150°C. The junction-to-ambient thermal resistance, θ_{JA} is layout-dependent. For the QFN3.5×4-14 package, the thermal resistance θ_{JA} is 34°C/W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts feature a large area with long 2-oz. copper traces connected to each pin and extensive, unbroken 1-oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical board design requires the following:

- Wide copper traces that are well connected to the IC's backside pads leading to exposed copper areas on the component side of the board
- Good thermal vias from the exposed pad connecting to a wide middle-layer ground plane and to an exposed copper area on the board's solder side.
- The maximum power dissipation at TA = 25°C may be calculated using the following formula:

$$P_{D,MAX} = (150°C - 25°C) / (34°C/W) = 3.67W$$

- Maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in Figure 11 to calculate the effect of rising ambient temperature on the maximum power dissipation.

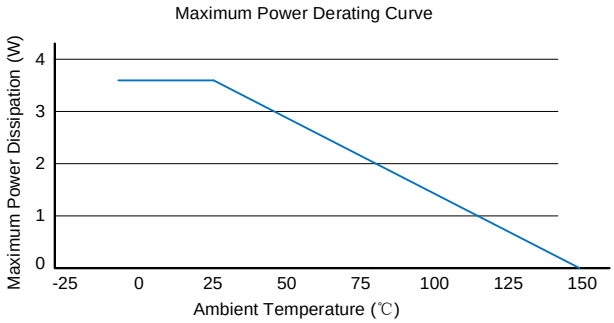

Figure 11. Derating Curve

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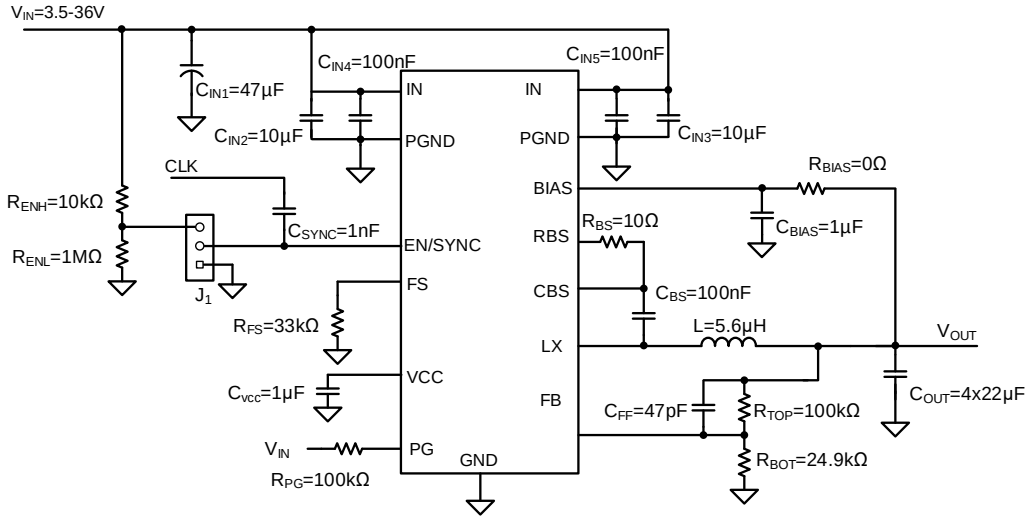
Application Schematic (V_{OUT} = 5V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
C_{IN1}	47µF/100V Electrolytic Cap		
C_{IN2}, C_{IN3}	10µF/50V/X7T/1206	GCM31CD71H106KE36K	mµRata
C_{IN4}, C_{IN5}	100nF/50V/X7R/0603	GCM188R71H104KA57D	mµRata
C_{OUT}	22µF/25V/X7S/1206	GCM31CC71E226ME36L	mµRata
C_{BS}	100nF/50V/X7R/0603	GCM188R71H104KA57D	mµRata
C_{FF}	47pF/50V/C0G/0603	GCM1885C1H470JA16D	mµRata
C_{VCC}	1µF/25V/X7R/0603	GCM188R71E105KA64D	mµRata
C_{BIAS}	1µF/25V/X7R/0603	GCM188R71E105KA64D	mµRata
C_{SYNC}	1nF/50V/X7R/0603	GCM188R71H102KA37D	mµRata
L	5.6µH	PCMB104T-5R6MS	Cyntec
R_{TOP}	100kΩ, 1%, 0603		
R_{BOT}	24.9kΩ, 1%, 0603		
R_{BS}	10Ω, 1%, 0603		
R_{BIAS}	0Ω, 1%, 0603		
R_{PG}	100kΩ, 1%, 0603		
R_{FS}	33kΩ, 1%, 0603		
R_{ENH}	10kΩ, 1%, 0603		
R_{ENL}	1MΩ, 1%, 0603		

Recommended Component Values for Typical Applications

V_{OUT} (V)	F_{SW} (kHz)	R_{FS} (kΩ)	R_{TOP} (kΩ)	R_{BOT} (kΩ)	C_{FF} (pF)	L	C_{OUT}
3.3	400	33	100	43	22	4.7µH/PCMB104T-4R7MS	4×22µF/GCM31CC71E226ME36L
3.3	2200	5.49	100	43	22	1µH/PCMB104T-1R0MS	3×22µF/GCM31CC71E226ME36L
5	400	33	100	24.9	47	5.6µH/PCMB104T-5R6MS	4×22µF/ GCM31CC71E226ME36L

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5	2200	5.49	100	24.9	22	1μH/PCMB104T-1R0MS	3×22μF/ GCM31CC71E226ME36L
12	400	33	100	9.1	10	10μH/PCMB104T-100MS	4×22μF/ GCM31CC71E226ME36L

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Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

Input Capacitors: Position the input capacitors as close as possible to the IN and GND pins to minimize the loop formed by these connections. The input capacitor should be connected to the IN and GND using a wide copper plane.

Output Capacitors: Connect the negative terminal of C_{OUT} to the GND pin using wide copper traces instead of vias to achieve better accuracy and stability of the output voltage.

Feedback Network: Place the feedback components (R_{TOP}, R_{BOT}, and C_{FF}) as close to the FB pin as possible. Avoid routing the feedback line near LX or other high-frequency signals, as it is sensitive to noise. Use a Kelvin connection to connect to C_{OUT} instead of the inductor output terminal.

LX Connection: Keep the LX area small to prevent excessive electromagnetic interference (EMI) while providing a wide copper trace to minimize parasitic resistance and inductance.

Control Signals: It is not recommended to connect control signals directly to V_{IN}. A resistor in the range of 1kΩ to 1MΩ should be used if the lines are pulled high to V_{IN}.

GND Vias: Place an adequate number of vias on the GND layer around the device for better thermal performance.

PCB Board: To achieve optimal thermal and noise performance, maximize the PCB copper area connected to the GND pin. A ground plane is highly recommended if board space permits. Connect the ground pad to a large copper area to enhance thermal performance.

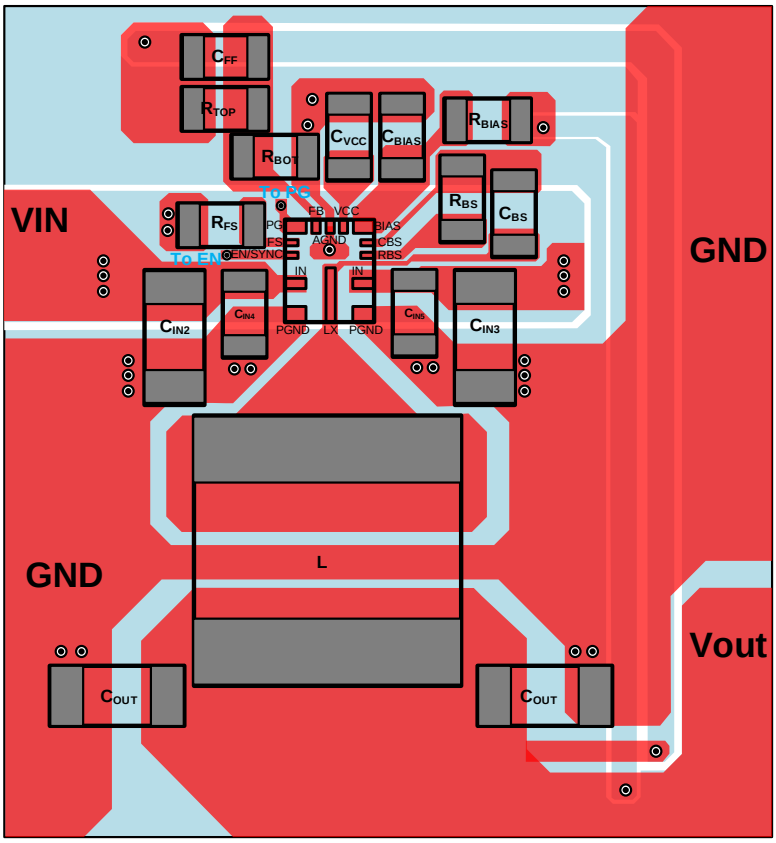

Figure 12. Suggested PCB Layout

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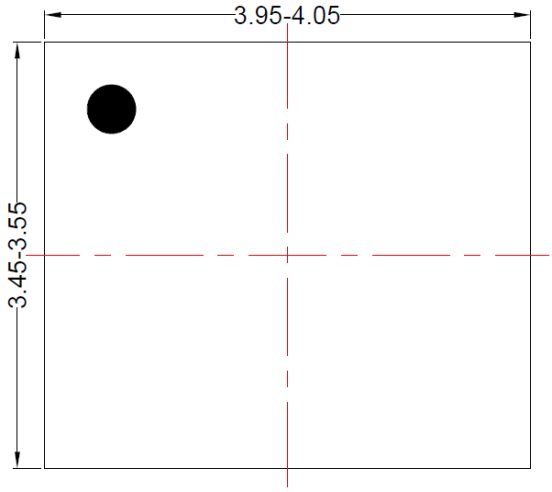
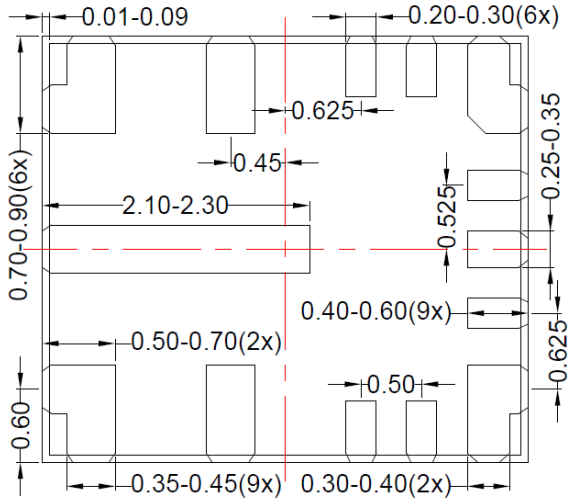
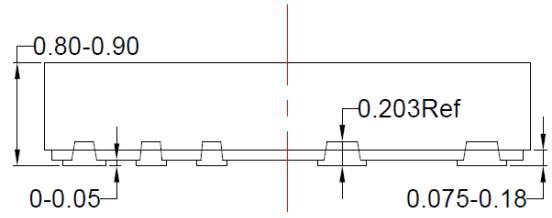
QFN3.5×4-14 Package Outline Drawing



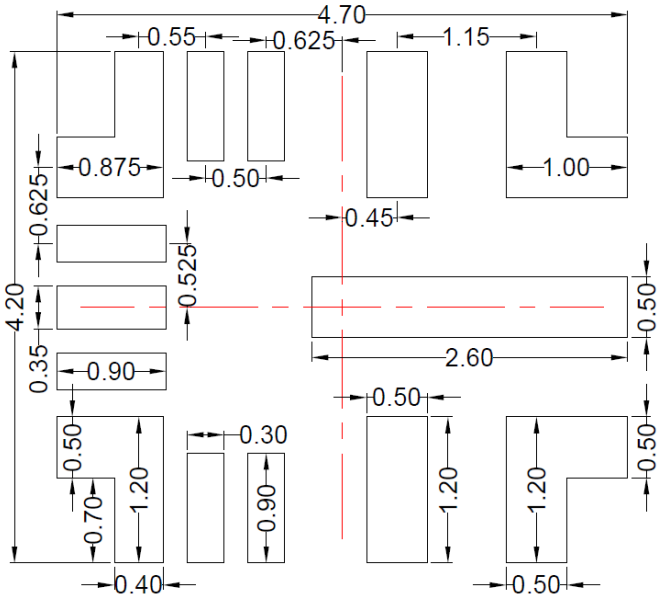
Top View



Bottom View



Side View



Recommended Pad Layout
(Reference Only)

Notes:

1. *All dimensions are in millimeters and exclude mold flash and metal burr.*
2. *Center line refers to the chip body center.*

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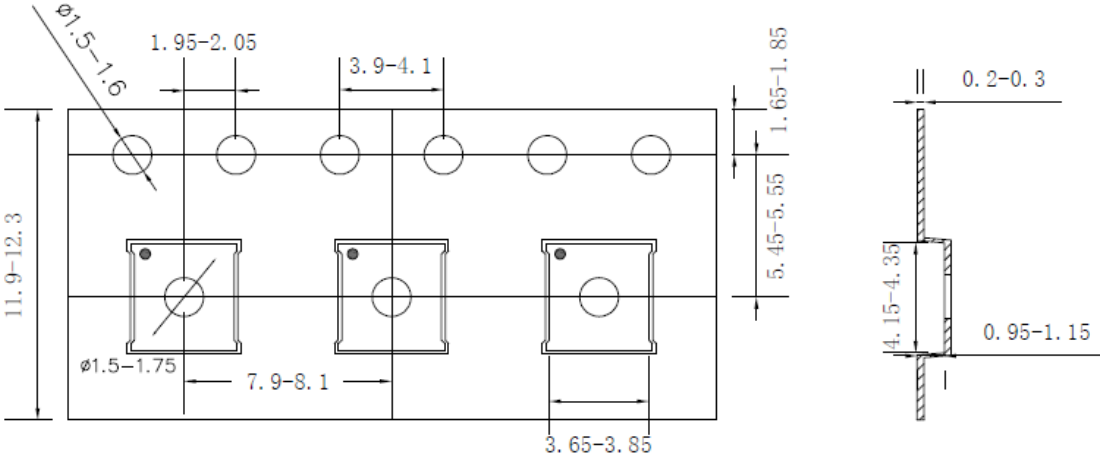
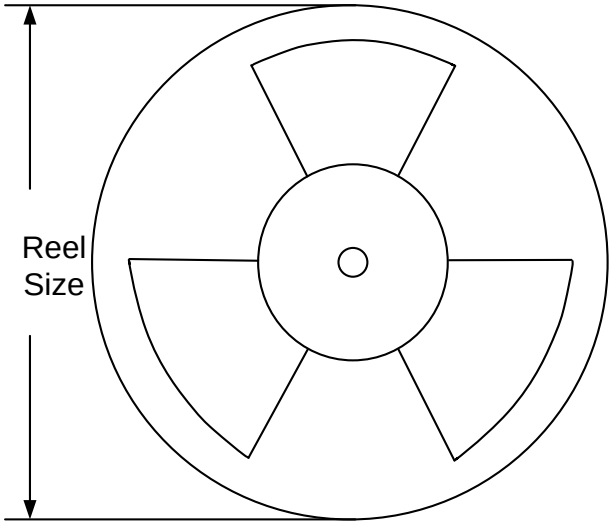
Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Direction of feed ⟶

Reel Dimensions



Package Types	Tape Width (mm)	Pocket Pitch (mm)	Reel Size (Inch)	Trailer * Length (mm)	Leader * Length (mm)	Qty per Reel (pcs)
QFN3.5×4	12	8	13"	400	400	5000

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