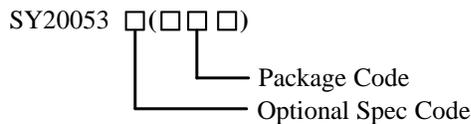


General Description

The SY20053 is a high efficiency 2.2MHz synchronous step down DC/DC regulator capable of delivering up to 3A output current. It can operate over a wide input voltage range from 2.4V to 5.5V and integrates main switch and synchronous switch with very low R_{DS(ON)} to minimize the conduction loss.

The SY20053 is in a space saving, low profile DFN1.5×1.5-6 package.

Ordering Information



Ordering Number	Package Type	Note
SY20053DQC	DFN1.5×1.5-6	3A

Features

- 2.4V to 5.5V Input Voltage Range
- Ultra-fast Load Transient Speed
- Low R_{DS(ON)} for Internal Switches (Top/Bottom):35mΩ /25mΩ
- High Switching Frequency 2.2MHz Minimizes the External Components
- ±1% Feedback or Output Voltage Accuracy (Full Temperature Range)
- PFM Mode for Light Load Efficiency
- 16μA Operating Quiescent Current
- Internal Soft-start Limits the Inrush Current
- 100% Dropout Operation
- Output Auto Discharge Function
- Power Good Indicator
- Auto Recovery for SCP/OVP/OTP Protection
- RoHS Compliant and Halogen Free
- Compact Package: DFN1.5×1.5-6

Applications

- Portable Electronics
- Industrial PC
- Smart Phone

Typical Applications

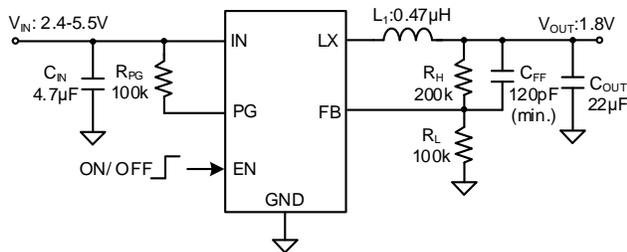


Figure1. Schematic Diagram

Inductor and C_{OUT} Selection Table

V _{OUT} (V)	L(μH)	C _{OUT} (μF)		
		10	22	44
1.2	0.33		☆	√
	0.47		√	√
1.8	0.33		√	√
	0.47		☆	√
2.5	0.47		☆	√
	0.68		√	√

Note: '☆' means recommended for most applications.

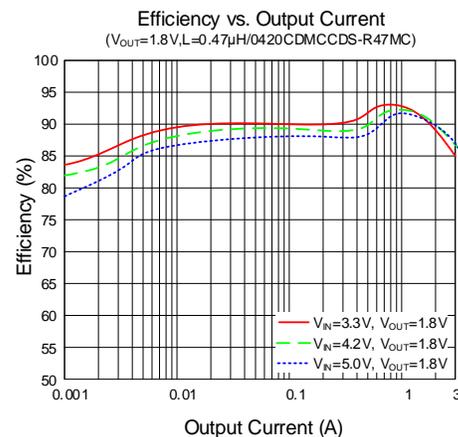
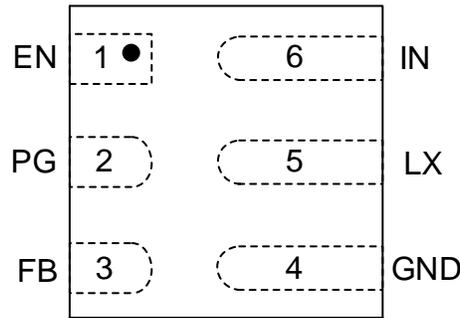


Figure2. Efficiency vs. Output Current

Pinout (top view)



(DFN1.5×1.5-6)

Top Mark: **d7xyz** (Device code: **d7**; *x*=year code, *y*=week code, *z*=lot number code)

Pin Name	Pin Number	Pin Description
EN	1	Enable control. Pull high to turn on. Do not leave it floating.
PG	2	Power good indicator (open drain output). Low if the $V_{FB} < 91.5\%$ or the $V_{FB} > 110\%$ of the V_{REF} ; high otherwise. Connect a pull-up resistor to the input.
FB	3	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT} = 0.6 \times (1 + R_H/R_L)$.
GND	4	Power ground pin.
LX	5	Inductor pin. Connect this pin to the switching node of inductor.
IN	6	Input pin. Decouple this pin to GND pin with at least a $4.7\mu F$ ceramic capacitor.

Block Diagram

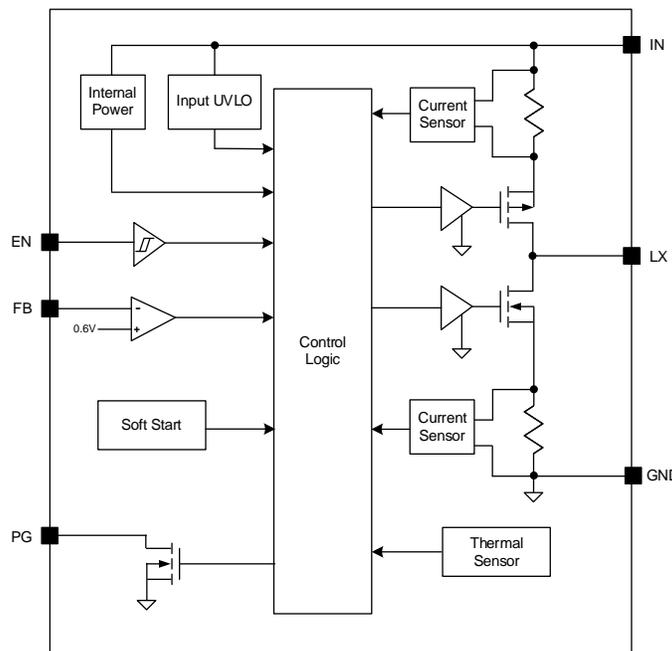


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage-----	-0.3V to 6.0V
FB, EN, PG Voltage-----	-0.3V to $V_{IN} + 0.6V$
LX Voltage-----	-0.3V ^(*1) to 6.0V ^(*2)
Power Dissipation, P_D @ $T_A = 25^\circ C$ -----	1.6W
Package Thermal Resistance (Note 2)	
θ_{JA} -----	62°C/W
θ_{JC} -----	8°C/W
Junction Temperature Range -----	-40°C to 150°C
Lead Temperature (Soldering, 10 sec.) -----	260°C
Storage Temperature Range -----	-65°C to 150°C
(*1) LX Voltage Tested Down to -3V <20ns	
(*2) LX Voltage Tested Up to +7V <20ns	

Recommended Operating Conditions (Note 3)

Supply Input Voltage -----	2.4V to 5.5V
Junction Temperature Range -----	-40°C to 125°C
Ambient Temperature Range -----	-40°C to 85°C

Electrical Characteristics

($T_J = -40^\circ C \sim 125^\circ C$, and $V_{IN} = 2.4V$ to 5.5V. Typical values are at $T_J = 25^\circ C$ and $V_{IN} = 5V$, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.4		5.5	V
Input UVLO Threshold	V_{UVLO}	V_{IN} falling, $T_J = 25^\circ C$	2.1	2.2	2.3	V
Input UVLO Hysteresis	V_{HYS}			160		mV
Quiescent Current	I_Q	$V_{FB} = 105\% V_{REF}$, $T_J = -40^\circ C \sim 85^\circ C$		16	26	μA
Shutdown Current	I_{SHDN}	$V_{EN} = 0V$, $T_J = 25^\circ C$		0.05	0.5	μA
Feedback Reference Voltage	V_{REF}	$I_{OUT} = 1A$, CCM	0.594	0.6	0.606	V
Output Voltage Load Regulation (Note 4)	ΔV_{LDR}	$I_{OUT} = 0.5A$ to 3A, $V_{OUT} = 1.8V$		0.1		%/A
Output Discharge FET R_{ON}	R_{DIS}	$V_{EN} = 0V$, $V_{LX} = 0.4V$		1		Ω
Top FET R_{ON}	$R_{DS(ON)1}$			35		m Ω
Bottom FET R_{ON}	$R_{DS(ON)2}$			25		m Ω
EN Input Voltage High	$V_{EN,H}$		1.0			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
EN Leakage Current	$I_{EN,LKG}$	EN=high		0.01	0.1	μA
Power Good Threshold	V_{PG}	V_{FB} falling, PG from high to low	89	91.5	94	%
		V_{FB} rising, PG from low to high	94	96	98	%
		V_{FB} rising, PG from high to low	107.5	110	112.5	%
		V_{FB} falling, PG from low to high	103	105	107	%
Power Good Delay (Note 4)	$t_{PG,R}$	PG from low to high		100		μs
	$t_{PG,F}$	PG from high to low		20		μs
Power Good Output Low	$V_{PG,L}$	$I_{PG} = 1mA$			0.4	V
PG Leakage Current	$I_{PG,LKG}$	$V_{PG} = 5V$		0.01		μA
Min ON Time	$t_{ON,MIN}$			50		ns
Maximum Duty Cycle (Note 4)	D_{MAX}		100			%
EN Turn On Delay	$t_{ON,DLY}$	from EN high to LX start switching		160		μs
Soft Start Time	t_{SS}	from EN high to 95% of V_{OUT} nominal, $T_J = 25^\circ C$	350	500	700	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Frequency	f_{SW}	$I_{OUT}=1A, V_{OUT}=1.8V$		2.2		MHz
Top FET Current Limit	$I_{LMT, TOP}$		3.7	4.3	5.0	A
Bottom FET Current Limit	$I_{LMT, BOT}$		3			A
Thermal Shutdown Temperature (Note 4)	T_{SD}			150		°C
Thermal Shutdown Hysteresis (Note 4)	T_{HYS}			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

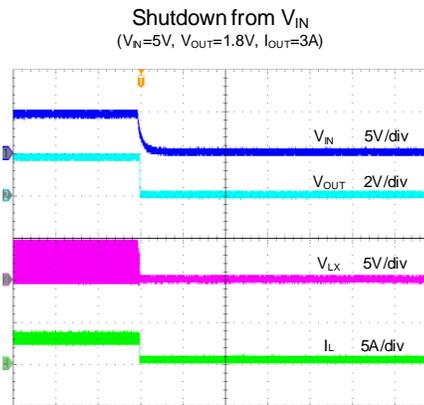
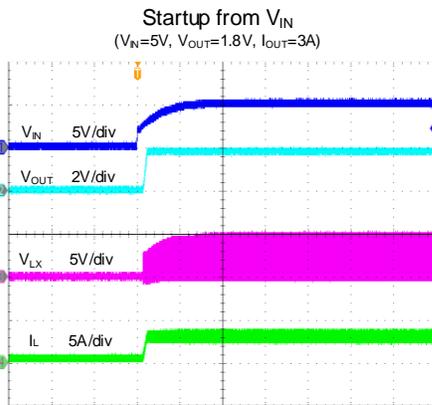
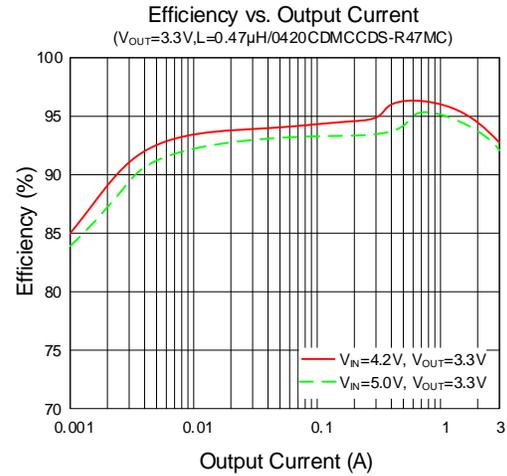
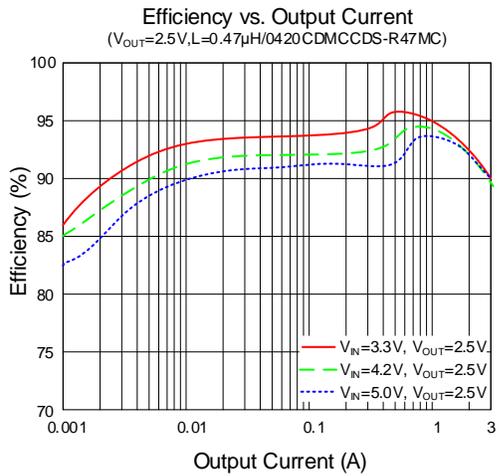
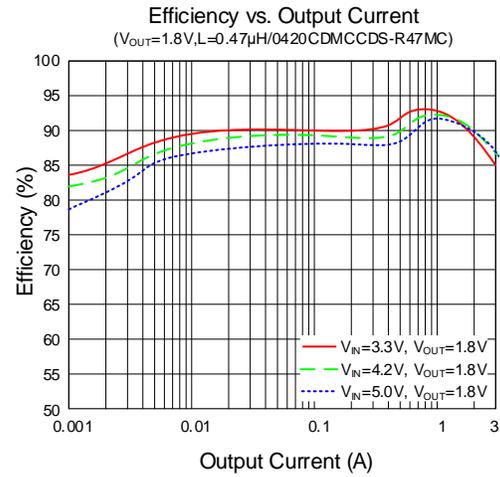
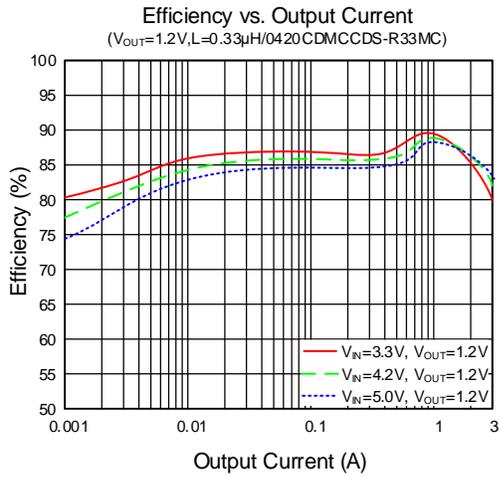
Note 2: Package thermal resistance is measured in the natural convection at $T_A=25^{\circ}C$ on a 6cm×6cm size 2-oz two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating condition.

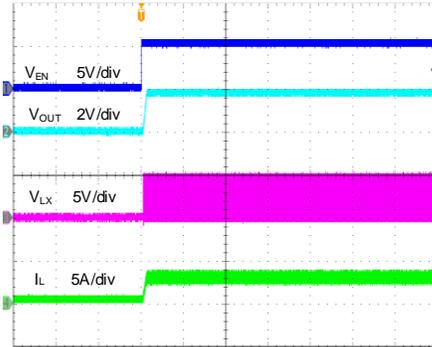
Note 4: Guaranteed by design.

Typical Performance Characteristics

($T_A=25^\circ\text{C}$, $V_{IN}=5\text{V}$, $L=0.47\mu\text{H}$, $C_{OUT}=2\times 10\mu\text{F}$, unless otherwise specified.)

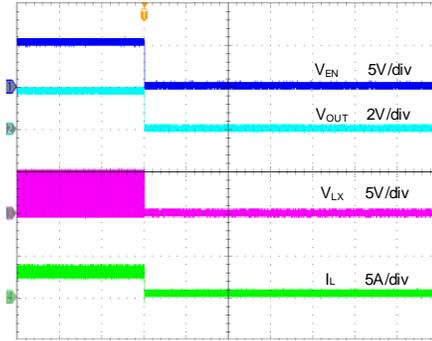


Startup from EN
($V_N=5V$, $V_{OUT}=1.8V$, $I_{OUT}=3A$)



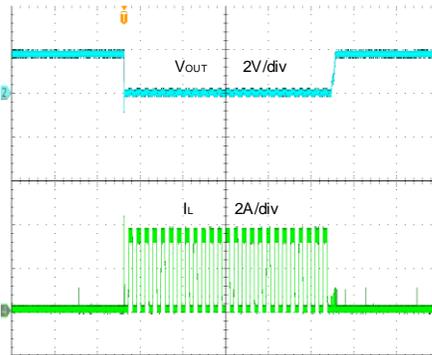
Time (4ms/div)

Shutdown from EN
($V_N=5V$, $V_{OUT}=1.8V$, $I_{OUT}=3A$)



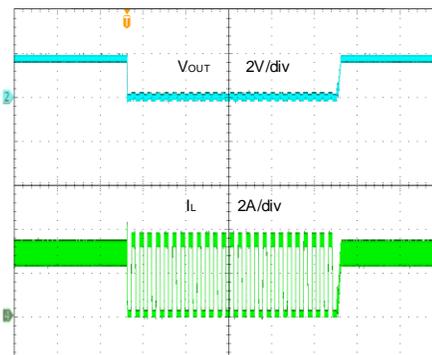
Time (4ms/div)

Short Circuit Protection
($V_N=5V$, $V_{OUT}=1.8V$, $I_{OUT}=0A$ -short)



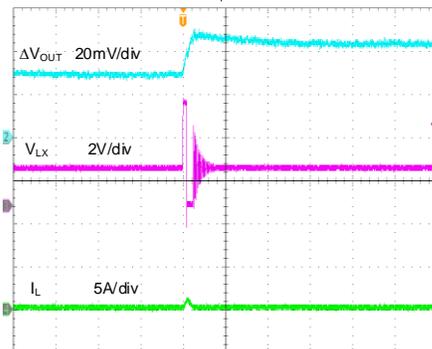
Time (4ms/div)

Short Circuit Protection
($V_N=5V$, $V_{OUT}=1.8V$, $I_{OUT}=3A$ -short)



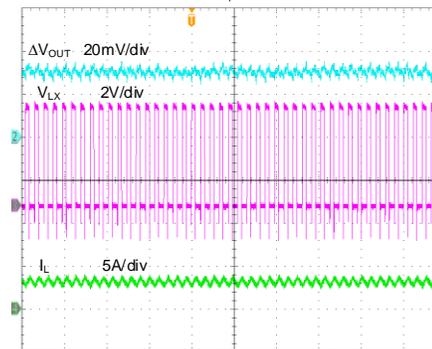
Time (4ms/div)

Output Ripple
($V_N=5V$, $V_{OUT}=1.8V$, $I_{OUT}=0A$)



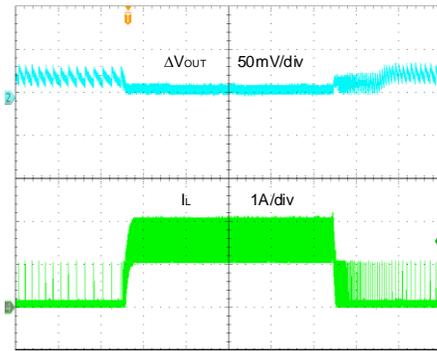
Time (2μs/div)

Output Ripple
($V_N=5V$, $V_{OUT}=1.8V$, $I_{OUT}=3A$)



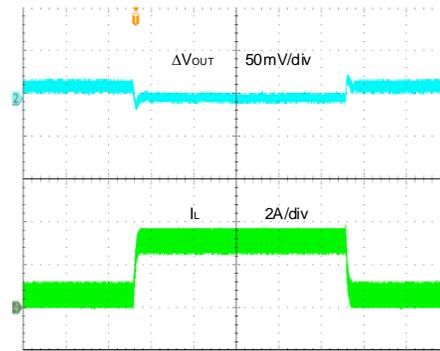
Time (2μs/div)

Load Transient
($V_N=5V$, $V_{OUT}=1.8V$, $I_{OUT}=0-1.5A$)



Time (100 μ s/div)

Load Transient
($V_N=5V$, $V_{OUT}=1.8V$, $I_{OUT}=0.3-3A$)



Time (100 μ s/div)

Operation

The SY20053 is a high efficiency 2.2MHz synchronous step-down DC/DC regulator capable of delivering up to 3A output current. It can operate over a wide input voltage range from 2.4V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY20053 adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads.

The SY20053 provides protection functions such as cycle by cycle current limiting and thermal shutdown protection.

Low output voltage ripple, small external inductor and capacitor sizes are achieved with 2.2MHz switching frequency.

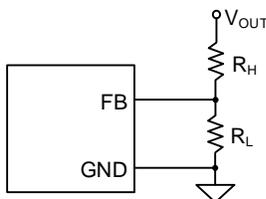
Applications Information

Because of the high integration in the SY20053, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN} , the output capacitor C_{OUT} , the output inductor L and the feedback resistors (R_H and R_L) need to be selected for the targeted application specifications.

Feedback Resistor Dividers R_H and R_L

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L . A value between 10k Ω and 1M Ω is highly recommended for both resistors. If V_{OUT} is 1.8V, $R_H = 100k\Omega$ is chosen, then using following equation, R_L can be calculated to be 49.9k Ω :

$$R_L = \frac{0.6V}{V_{OUT} - 0.6V} R_H$$



Input Capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

To minimize the potential noise problem, a typical X5R or better grade ceramic capacitor with 6.3V rating should be placed really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} , and IN/GND pins. In this case, a 4.7 μ F low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor with 6.3V rating and more than $2 \times 10\mu$ F capacitance.

Output Inductor L

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY20053 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT, MIN} > I_{OUT, MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with $DCR < 25m\Omega$ to achieve a good overall efficiency.

Inductor vs. Output Capacitor

The ripple base control strategy needs very little C_{OUT} to confirm stability. Too large inductor and C_{OUT} will

lead to instability. The recommended inductance and output capacitance is shown as below.

Inductance vs. Output Capacitance Selection Table
(Note 5)

L (μH)	C_{OUT} (μF)					
	22	44	88	120	180	220
0.33	Note6	√	√	√	√	√
0.47	√	√	√	√	√	√
0.68	√	√	√	√	×	×

Note 5: Tested with 120pF feedforward capacitor.

Note 6: Only suitable for $V_{\text{OUT}} < 2.0\text{V}$ application.

Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for small duty cycles, since even at very low duty cycles, the switching frequency can be reduced as needed once the on-time is close to the minimum on time, to always ensure a proper operation.

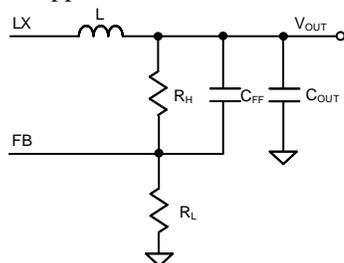
The device will enter 100% dropout mode if the output voltage is very close to the input voltage, while the top FET is constantly turned on, the bottom FET is turned off.

Power Good Indicator

The power good indicator is an open drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is greater than $V_{\text{PG,R}}$ and less than V_{OVP} for at least the power good delay time (low to high), PG will be high-impedance. Otherwise, it is pulled low. PG should be connected to V_{IN} or another voltage source through a resistor (e.g., 10k Ω ~100k Ω).

Load Transient Considerations

The SY20053 integrates the compensation components to achieve good stability and fast transient responses. Adding a small ceramic capacitor with more than 120pF capacitance in parallel with R_{H} may further speed up the load transient responses and is thus highly recommended, otherwise it may result in other application issues.



OCP and UVP Protection Method

The SY20053 adopts cycle by cycle current limitation for both HS FET and LS FET. If the high side power FET current gets higher than the peak current limit threshold, the high side power FET will turn off and the low side power FET will turn on. If the low side FET current gets higher than the valley current limit threshold, the low side FET will keep turning on until low side FET current decreases below the valley current limit threshold. So, both peak and valley current are limited. If the load current continues to increase in these conditions, the output voltage will drop. When the output voltage falls below 33% of the regulation level, UVP will be triggered and the IC will operate in hic-cup mode. The hic-cup on time and hic-cup off time ratio is 1:1. If the hard short is removed, the IC will return to normal operation.

Layout Design

The layout design of the SY20053 is relatively simple. For the best efficiency and minimum noise problem, the following components should be placed close to the IC: C_{IN} , L, R_{H} , R_{L} and C_{FF} .

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable. Place some vias in GND copper for heat sinking too.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.

4) The components R_{H} and R_{L} , and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) The feedback sampling point should be connected with C_{OUT} rather than the inductor output terminal.

6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1M Ω resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

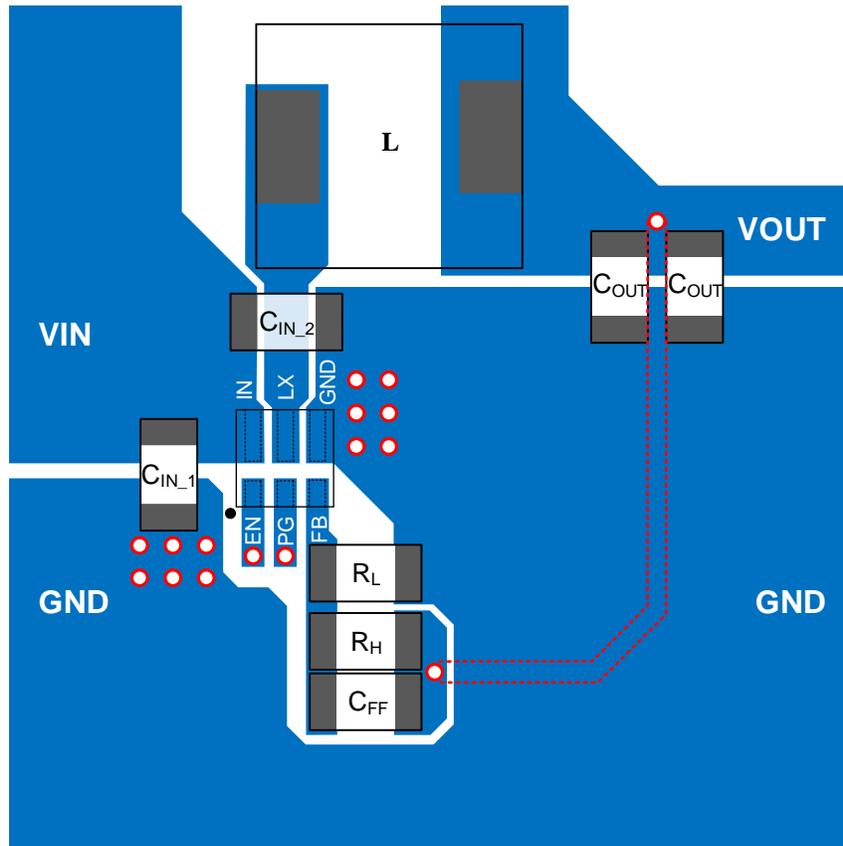
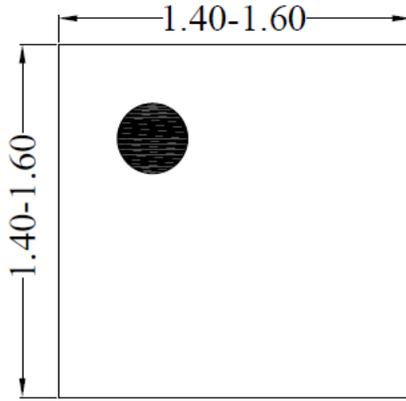
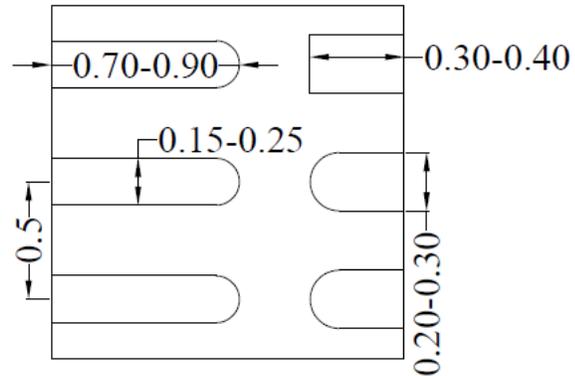


Figure4. PCB Layout Suggestion

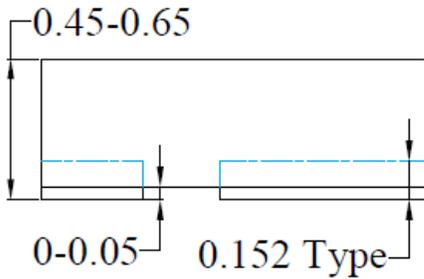
DFN1.5×1.5-6 Package Outline



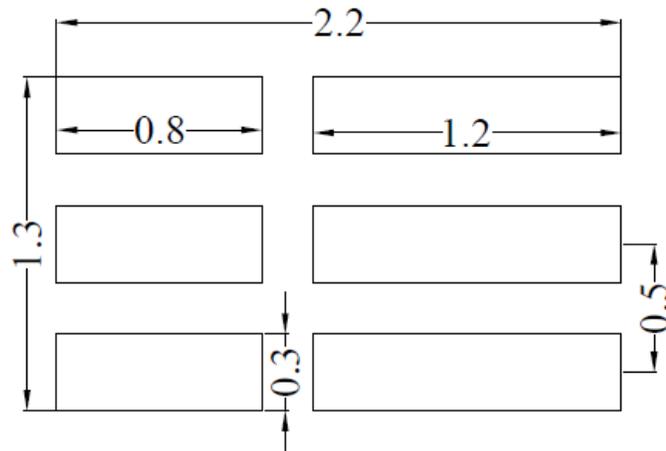
Top View



Bottom View



Front View



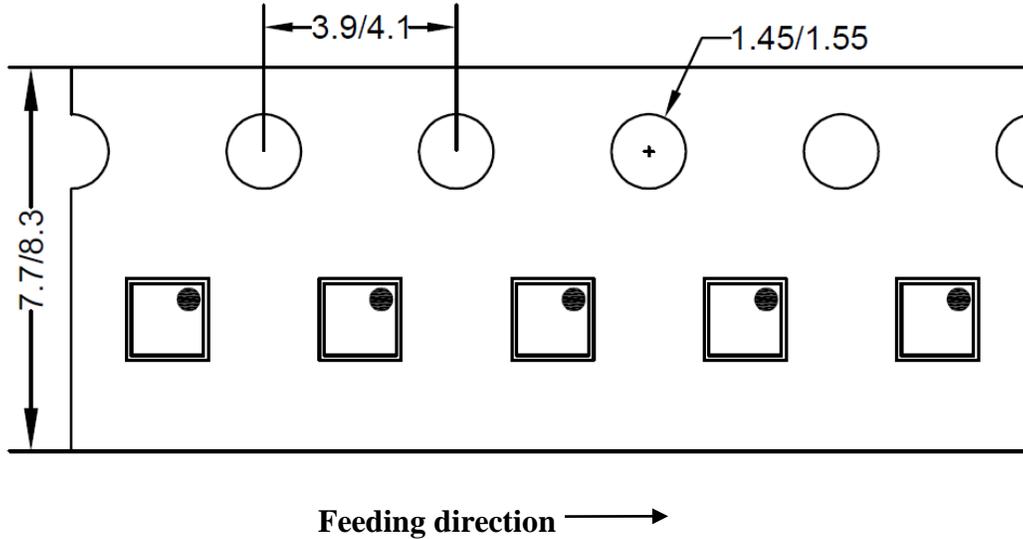
**Recommended PCB layout
(only for reference)**

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;

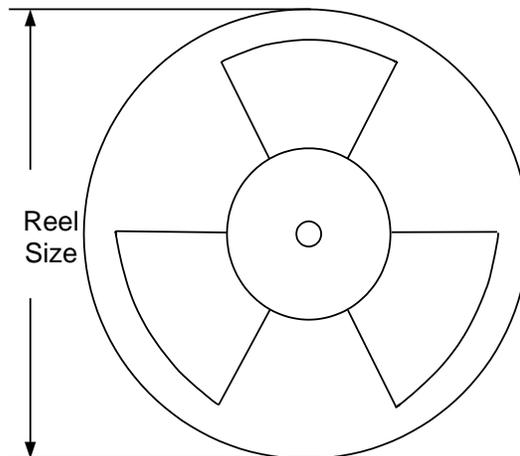
Taping & Reel Specification

1. Taping orientation

DFN1.5×1.5



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.5×1.5	8	4	7"	400	160	3000

3. Others: NA

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.
2. **Applications.** Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.
3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.
4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.
5. **Terms and conditions of commercial sale.** Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at <http://www.silergy.com/stdterms>, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.
6. **No offer to sell or license.** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com

© 2022 Silergy Corp.

All Rights Reserved.