SY20117E

High Efficiency, 1MHz, 3A Synchronous Step Down Regulator

General Description

The SY20117E is a high efficiency 1MHz synchronous step down DC/DC regulator, which is capable of delivering up to 3A output current. It can operate over a wide input voltage range from 2.5V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The low output voltage ripple, the small external inductor and the capacitor sizes are achieved with 1MHz switching frequency.

Ordering Information

SY20117 □(□□)□

- □ (last) — Temperature Code
- (□□) — Package Code
- □ (first) — Optional Spec Code

Ordering Number	Package type	Note
SY20117EDFC	DFN2×2-8	--

Features

- 2.5V to 5.5V Input Voltage Range
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 85mΩ /60mΩ
- High Switching Frequency 1MHz Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- 100% Dropout Operation
- Power Good Indicator
- Hic-cup for Short Circuit Protection
- Output Auto Discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: DFN2×2-8

Applications

- Set Top Box
- USB Dongle
- Media Player
- Smart Phone

Typical Application

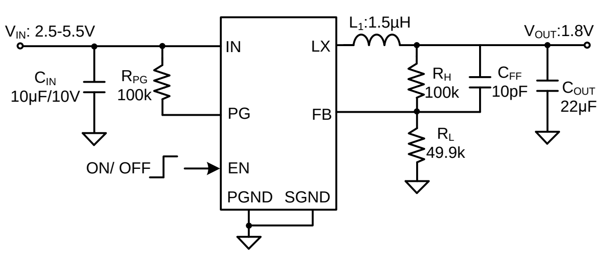


Figure1. Typical Application Circuit

Inductor and C_{OUT} Selection Table

V_{OUT} [V]	L [µH]	C_{OUT} [µF]			
		10	22	32	44
1.2	1.0		☆	√	√
	1.5		√	√	√
1.8	1.5		☆	√	√
	2.2			√	√
3.3	1.5		☆	√	√
	2.2		√	√	√

Note: '☆' means recommended for most applications.

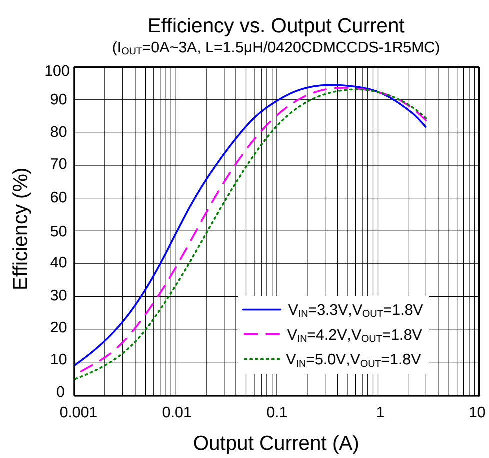
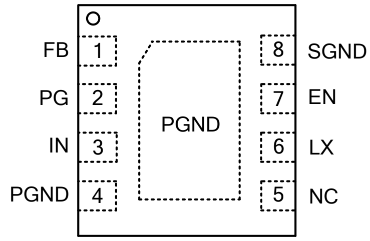


Figure2. Efficiency vs. Output Current

Pin out (Top View)



(DFN2×2-8)

Top Mark: 5Hxyz (device code: **5H**, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin No.	Pin Description
FB	1	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_H/R_L)$.
PG	2	Power good indicator (open drain output). Low if the output < 90% or the output >120% of regulation voltage; High otherwise. Connect a pull-up resistor to the input.
IN	3	Input pin. Decouple this pin to GND pin with at least a 10μF ceramic capacitor.
PGND	4/Exposed Paddle	Power ground pin.
NC	5	No connection.
LX	6	Inductor pin. Connect this pin to the switching node of inductor.
EN	7	Enable control. Pull high to turn on. Do not leave it floating.
SGND	8	Analog ground pin.

Block Diagram

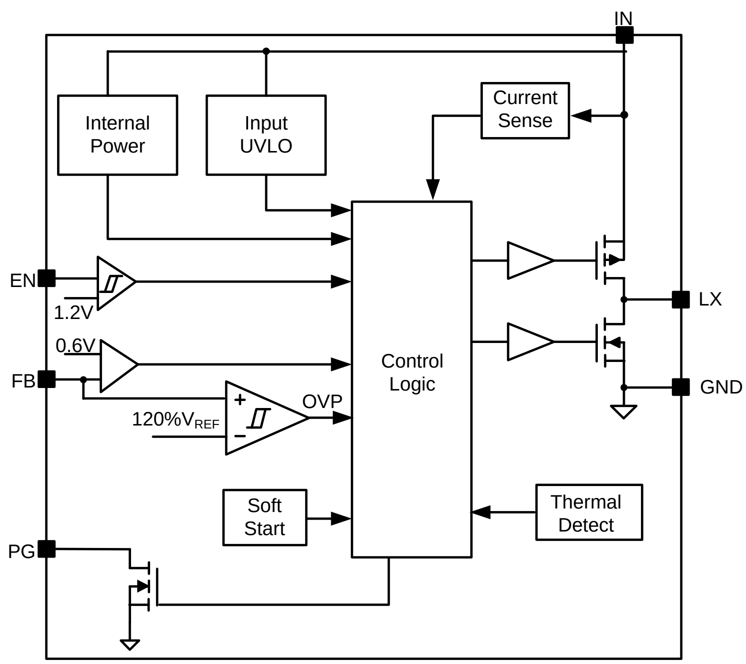


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage-- -0.3V to 6.0V
FB, EN, PG Voltage--- -0.3V to V_{IN} + 0.6V
LX Voltage--- -0.3V (*1) to 6.0V (*2)
Power Dissipation, P_D @ T_A = 25°C -- 1.4W
Package Thermal Resistance (Note 2)
θ_{JA} -- 70°C/W
θ_{JC} -- 25°C/W
Junction Temperature Range -- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range -- -65°C to 150°C

(*1) LX Voltage Tested Down to -3V <20ns
(*2) LX Voltage Tested Up to +7V <20ns

Recommended Operating Conditions (Note 3)

Supply Input Voltage --- 2.5V to 5.5V
Junction Temperature Range -- -40°C to 125°C
Ambient Temperature Range -- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.8V, L = 1.5μH, C_{OUT} = 22μF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Input UVLO Threshold	V_{UVLO}			2.45	2.5	V
Input UVLO Hysteresis	V_{YST}			150		mV
Shutdown Current	I_{SHDN}	V_{EN}=0V		0.1	1	μA
Feedback Reference Voltage	V_{REF}	I_{OUT}=0.5A, CCM	0.591	0.6	0.609	V
LX Node Discharge Resistance	R_{DIS}			50		Ω
Top FET R_{ON}	$R_{DS(ON)1}$			85		mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$			60		mΩ
EN Input Voltage High	$V_{EN,H}$		1.2			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
EN Input Current	I_{EN}				2	μA
PG Threshold for Under Voltage Detection	$V_{PG,UVP}$			90		%
PG Low Delay Time for Under Voltage Detection	$t_{UVP,DLY}$			10		us
PG Threshold for Over Voltage Detection	$V_{PG,OVP}$			120		%
PG Low Delay Time for Over Voltage Detection	$t_{OVP,DLY}$			20		us
Min ON Time	$t_{ON,MIN}$			50		ns
Maximum Duty Cycle	D_{MAX}		100			%
Turn on Delay Time	$t_{ON,DLY}$	from EN high to LX start switching		0.5		ms
Soft-start Time	t_{SS}	V_{OUT} from 0% to 100%		1		ms
Switching Frequency	f_{SW}	I_{OUT}=0.5A, CCM		1.0		MHz
Top FET Current Limit	$I_{LMT,TOP}$		3.7			A
Bottom FET Reverse Current Limit	$I_{LMT,RVS}$		0.47		0.9	A
Output Under Voltage Protection Threshold	V_{UVP}			50		$\%V_{REF}$
Output UVP Delay	$t_{UVP,DLY}$			10		μs
UVP Hic-cup ON Time	$t_{UVP,ON}$			3.5		ms
UVP Hic-cup OFF Time	$t_{UVP,OFF}$			3.5		ms
Thermal Shutdown Temperature	T_{SD}			160		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

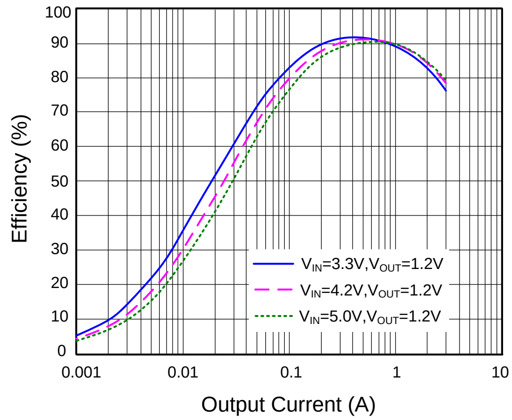
Note 2: θ_{JA} of SY20117EDFC is measured in the natural convection at T_A = 25°C on a 2-oz two-layer Silergy evaluation board. Paddle of DFN2×2-8 package is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

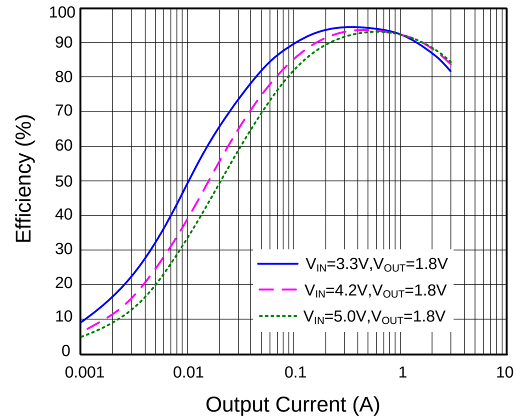
Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 5V, V_{OUT} = 1.8V, L = 1.5μH, C_{OUT} = 22μF, unless otherwise noted)

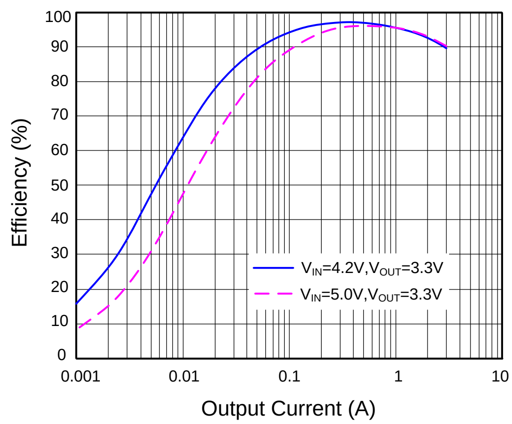
Efficiency vs. Output Current
(I_{OUT}=0A~3A, L=1.0μH/0420CDMCCDS-1R0MC)



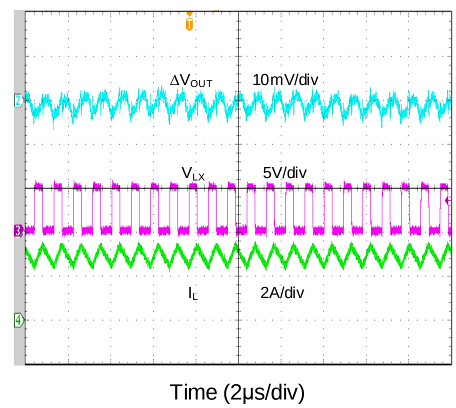
Efficiency vs. Output Current
(I_{OUT}=0A~3A, L=1.5μH/0420CDMCCDS-1R5MC)



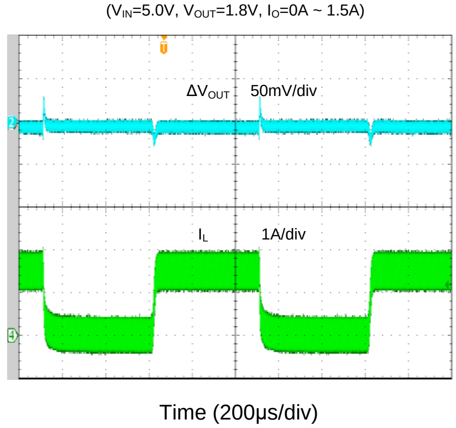
Efficiency vs. Output Current
(I_{OUT}=0A~3A, L=1.5μH/0420CDMCCDS-1R5MC)



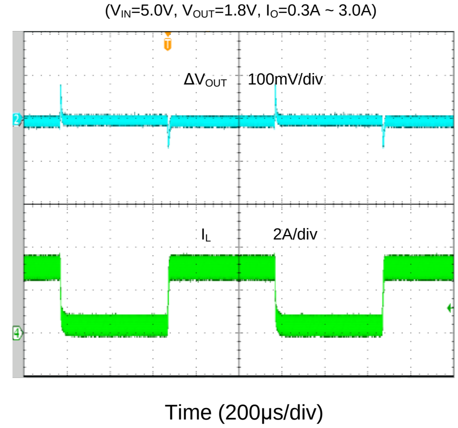
Output Ripple
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=3.0A)



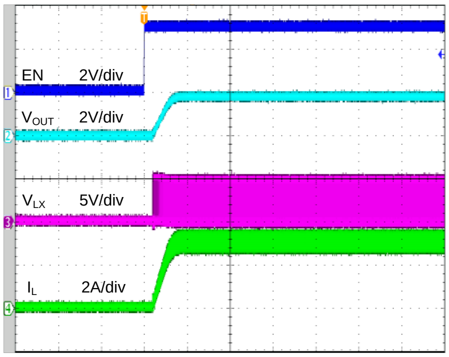
Load Transient
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A ~ 1.5A)



Load Transient
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0.3A ~ 3.0A)

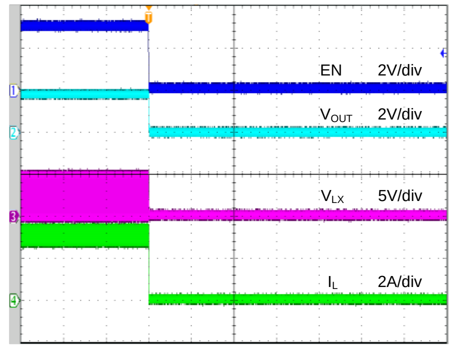


Startup from Enable
(V_{IN}=5.0V, V_{OUT}=1.8V, R_{LOAD}=0.6Ω)



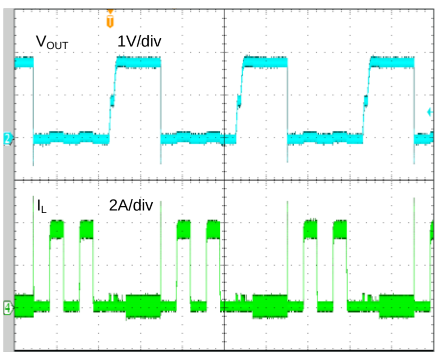
Time (2ms/div)

Shutdown from Enable
(V_{IN}=5.0V, V_{OUT}=1.8V,R_{LOAD}=0.6Ω)



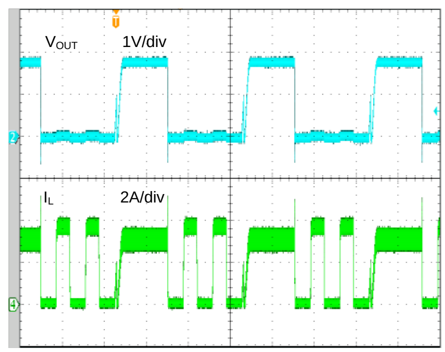
Time (2ms/div)

Short Circuit Protection
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A ~ Short)



Time (10ms/div)

Short Circuit Protection
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=3A ~ Short)



Time (10ms/div)

Operation

The SY20117E is a high efficiency 1MHz synchronous step down DC/DC regulator, which is capable of delivering up to 3A output current. It can operate over a wide input voltage range from 2.5V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The low output voltage ripple, the small external inductor and the capacitor sizes are achieved with 1MHz switching frequency.

Applications Information

Because of the high integration in the SY20117E, the application circuit based on this IC is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L and the feedback resistors (R_H and R_L) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_H and R_L

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value of between 1kΩ and 1MΩ is highly recommended for R_L. If R_L=100kΩ is chosen, then R_H can be calculated to be:

$$R_H = \frac{(V_{OUT} - 0.6V) \times R_L}{0.6V}$$

Input Capacitor C_{IN}

A typical X5R or better grade ceramic capacitor with 10V rating and greater than 10μF capacitance is recommended. This ceramic capacitor need to be placed really close to the IN and GND pins to minimize the potential noise problem. Care should be taken to minimize the loop area formed by C_{IN}, and the IN/GND pins.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor with 6.3V rating and greater than 22μF capacitance.

Output Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY20117E is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) For FCCM mode converter, in order to avoid the reverse current limit (0.47A min) being triggered at open load condition, when choosing the inductance, the 1/2 inductor ripple current (ΔI) should be smaller than the reverse current limit threshold. Otherwise the switching frequency will increase. The 1/2 inductor ripple current is calculated as:

$$\frac{1}{2}\Delta I = \frac{V_{OUT}(V_{IN} - V_{OUT})}{2 \times L \times f_{SW} \times V_{IN}} \leq 0.47$$

Where fsw is the switching frequency and 0.47 is the bottom FET reverse current limit. So the inductance can be calculated as:

$$L \geq \frac{V_{OUT}(V_{IN} - V_{OUT})}{0.94 \times V_{IN} \times f_{SW}}$$

3) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

4) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<60mΩ to achieve a good overall efficiency.

Load Transient Considerations

The SY20117E integrates the compensation components to achieve good stability and fast transient responses. In some application, adding a ceramic capacitor (feed-forward capacitor, C_{ff}) in parallel with R_H may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements. Typically, for 1.2V/1.8V/3.3V output, the R_H, R_L, C_{ff} is recommended as below:

Recommended Component Selection

V_{OUT}	R_H	R_L	C_{ff}
1.2V	49.9kΩ	49.9kΩ	22pF
1.8V	100kΩ	49.9kΩ	10pF
3.3V	100kΩ	22.1kΩ	10pF

OCP & SCP Method

With load current increasing, as soon as the high side FET current gets higher than peak current limit threshold, the high side FET will turn off. If the load current continues to increase, the output voltage will drop. When the output voltage falls below 50% of the regulation level, the output UVP will be detected and SY20117E will operate in hic-cup mode. The hic-cup frequency is 140Hz, the hip-cup duty cycle is 50%. If the hard short is removed, the IC will return to normal operation.

.

Layout Design

The layout design of the SY20117E regulator is relatively simple. For the best efficiency and minimum noise problems, the following components should be placed close to the IC: C_{IN}, L, R_H and R_L.

1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to the Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.

4) The components R_H, R_L and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

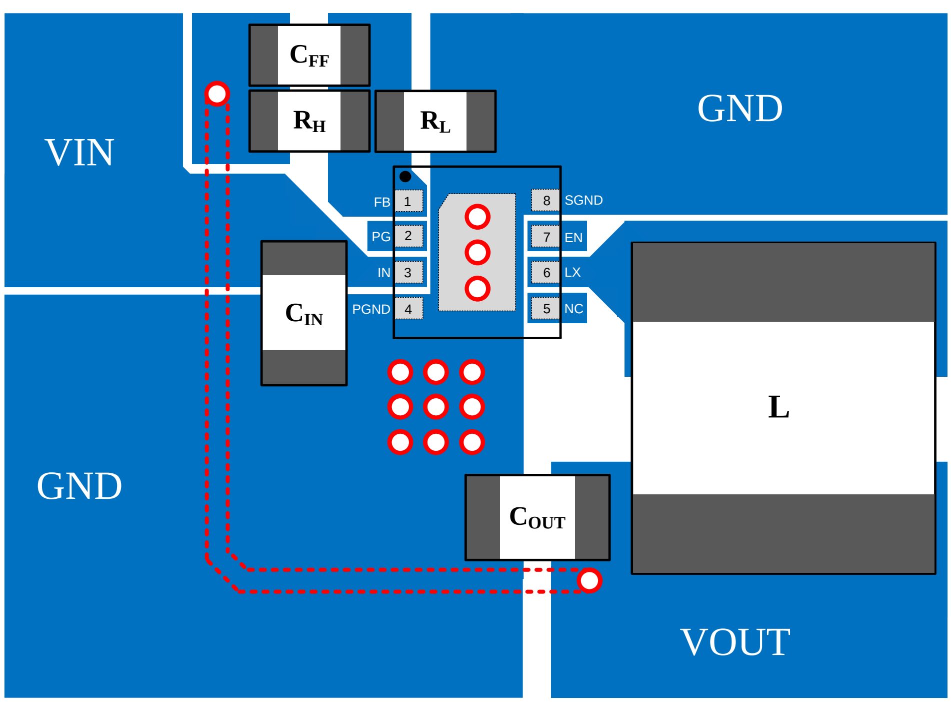
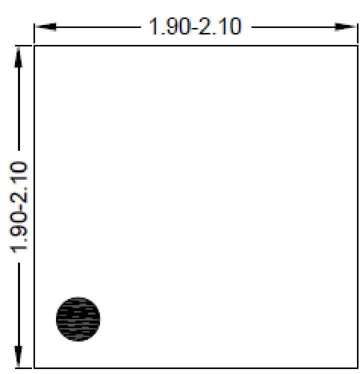
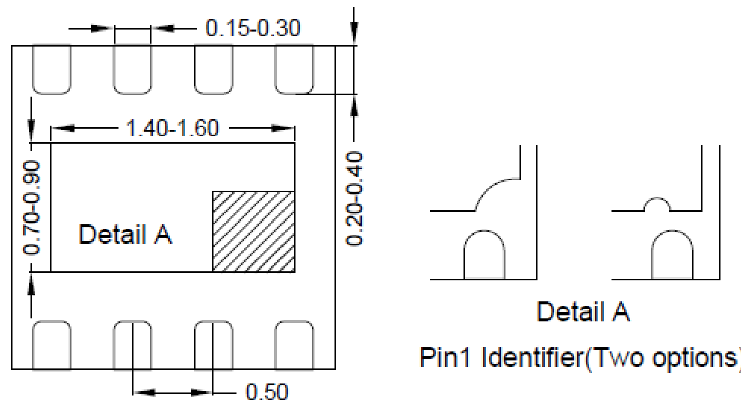


Figure4. PCB Layout Suggestion

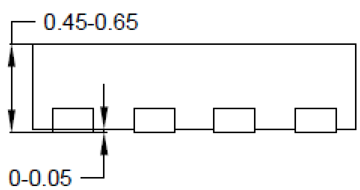
DFN2×2-8 Package Outline Drawing



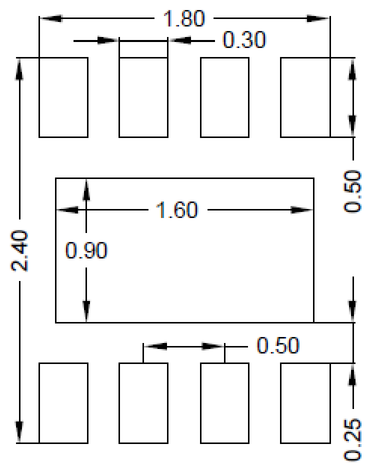
Top View



Bottom View



Side View

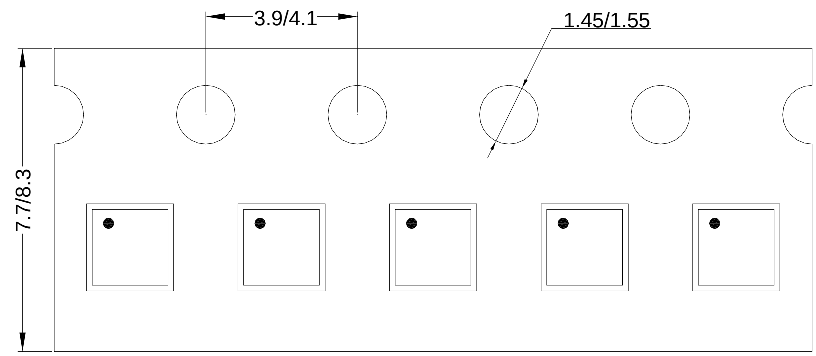


Recommended PCB Layout (Reference)

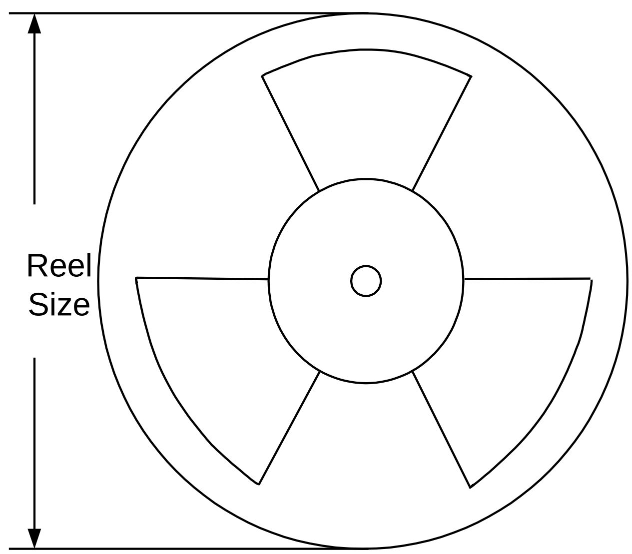
Notes: All dimensions are in millimeters and don’t include mold flash & metal burr.

Taping & Reel Specification

1. DFN2×2



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2×2	8	4	7"	400	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Mar.30, 2022	Revision 1.0	Production Release
Mar.30, 2021	Revision 0.9	Initial Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. **Applications.** Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com