SY20124E

High Efficiency 1.5MHz, 3A Ultra Fast Dynamic Response Synchronous Step Down Regulator

General Description

The SY20124E is a high efficiency 1.5MHz synchronous step down DC/DC regulators, which is capable of delivering up to 3A output current. The SY20124E can operate over a wide input voltage range from 2.7V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Low output voltage ripple, small external inductor and capacitor sizes are achieved with 1.5MHz switching frequency.

Ordering Information

SY20124□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20124EQWC	QFN1.5×1.5-7	--

Features

- 2.7~5.5V Input Voltage Range
- Ultra Fast Load Transient Speed
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom) 85mΩ /50mΩ
- High Switching Frequency 1.5MHz Minimizes the External Components
- External Soft-start Limits the Inrush Current
- CCM Only Operation
- Reliable Short Circuit Protection: Hic-cup Mode
- Output Auto Discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: QFN1.5×1.5-7

Applications

- Smart Phone
- LCD TV
- Set Top Box
- Mini-notebook PC
- Access Point Router

Typical Applications

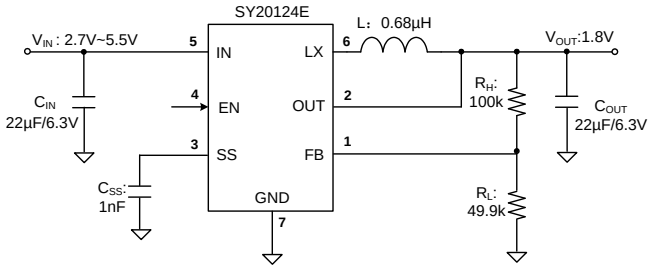


Figure1. Schematic Diagram

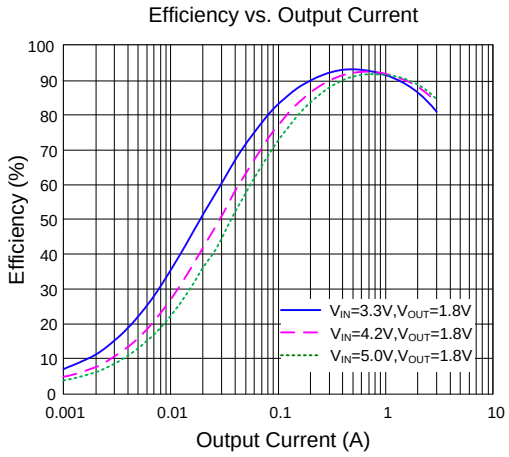
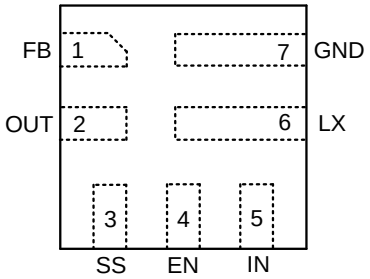


Figure2. Efficiency vs. Output Current

Pinout (Top View)



(QFN1.5×1.5-7)

Top Mark: A6*xyz* for SY20124EQWC **(**device code: A6, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
FB	1	Feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6V\times(1+R_H/R_L)$
OUT	2	Output feedback pin, connect to the output capacitor side.
SS	3	Soft-start program pin. Do not leave it floating. Connect a capacitor from this to ground to program the soft-start time. $t_{SS}=C_{SS}\times0.6V/0.6\mu A$
EN	4	Enable control. Pull high to turn on. Do not leave it floating
IN	5	Input pin. Decouple this pin to the GND pin with at least a 22μF ceramic capacitor.
LX	6	Inductor pin. Connect this pin to the switching node of inductor.
GND	7	Ground pin.

Block Diagram

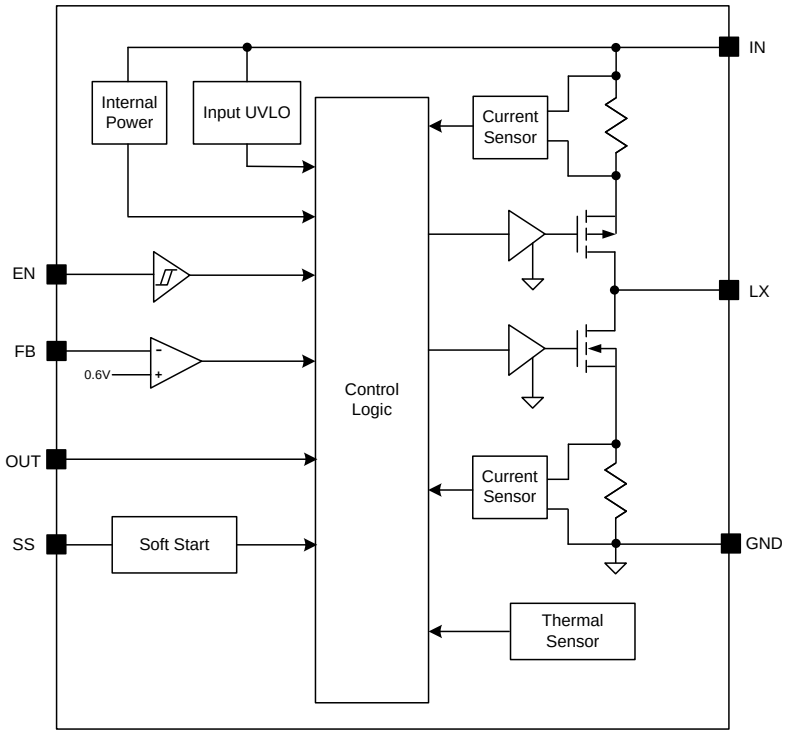


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 6.0V
EN, FB, SS, OUT Voltage---------- -0.3V to VIN + 0.6V
LX Voltage---------- -0.3V (*1) to 6V (*2)
Power Dissipation, P_D @ T_A = 25°C,
QFN1.5×1.5-7 ---------- 1.5W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 66°C/W
θ_{JC} ---------- 5°C/W
Junction Temperature Range ----------150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
(*1) LX Voltage Tested Down to -3V <20ns
(*2) LX Voltage Tested Up to +7V <20ns

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.7V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5.0V, V_{OUT} = 1.8V, L = 0.68μH, C_{OUT} = 22μF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.7		5.5	V
Input UVLO Threshold	V_{UVLO}				2.7	V
Input UVLO Hysteresis	V_{HYS}			0.18		V
Shutdown Current	I_{SHDN}	V_{EN}=0V		0.1	1	μA
Feedback Reference Voltage	V_{REF}	I_{OUT}=0A	594	600	606	mV
Output Discharge Resistance	R_{DIS}			75		Ω
Top FET R_{ON}	$R_{DS(ON)1}$			85		mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$			50		mΩ
EN Input Voltage High	$V_{EN,H}$		1.1			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
Min ON Time	$t_{ON,MIN}$			100		ns
Maximum Duty Cycle	D_{MAX}		100			%
Soft-start Charge Current	I_{SS}			0.6		μA
Turn On Delay	$t_{ON,DLY}$	C_{SS}=1nF, from EN high to LX start switching		150		μs
Switching Frequency	f_{SW}	I_{OUT}=0A		1.5		MHz
Top FET Current Limit	$I_{LMT,TOP}$		4			A
Bottom FET Current Limit	$I_{LMT,BOT}$		3			A
Output Under Voltage Protection Threshold	V_{UVP}			40		%V_{REF}
Output UVP Delay	$t_{UVP,DLY}$			15		μs
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			15		℃

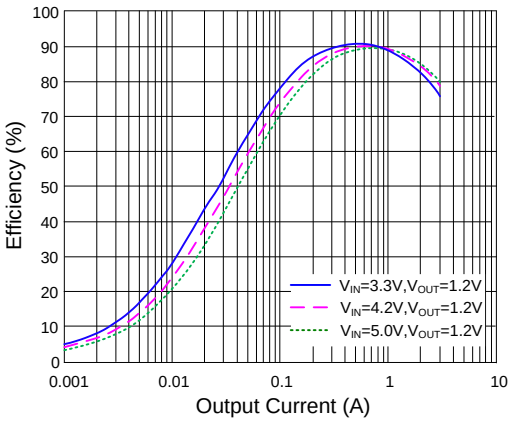
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note2: θ_{JA} of SY20124E is measured in the natural convection at T_A = 25°C on 2OZ two-layer Silergy evaluation board. Pin 6 is the case position for SY20124E θ_{JC} measurement.

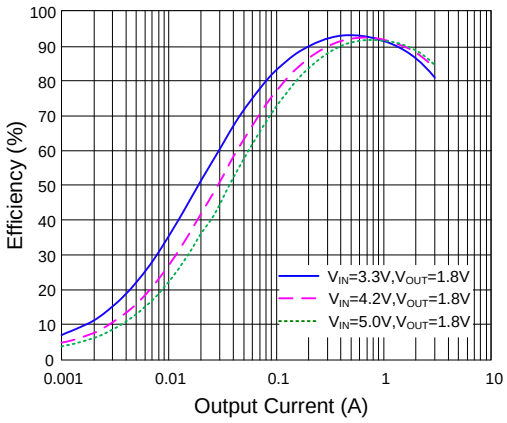
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

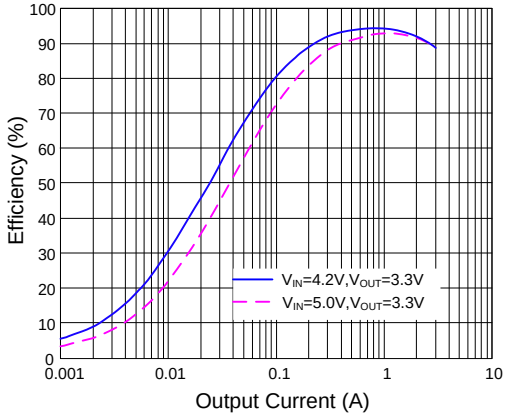
Efficiency vs. Output Current



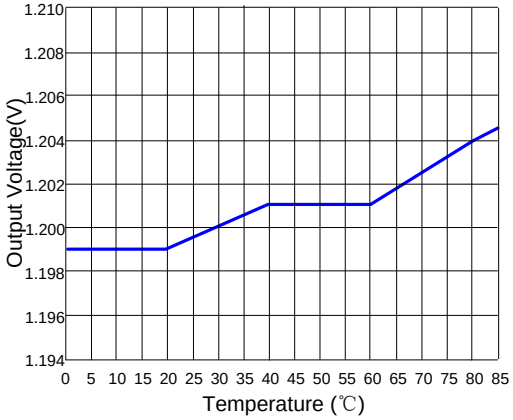
Efficiency vs. Output Current



Efficiency vs. Output Current

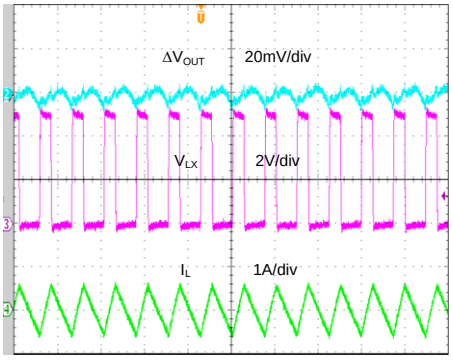


VOUT vs. Temperature



Output Ripple

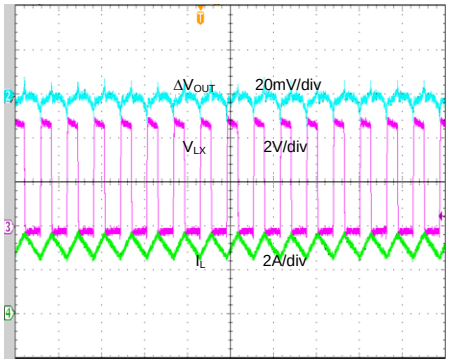
(VIN=5.0V, VOUT=1.8V, IO=0A)



Time (1μs/div)

Output Ripple

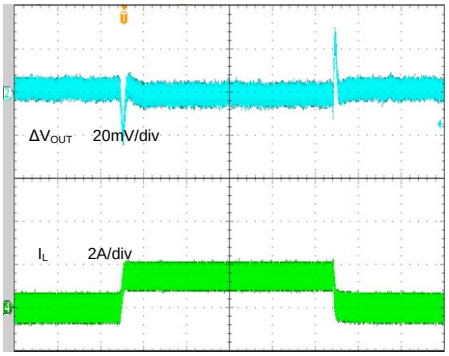
(VIN=5.0V, VOUT=1.8V, IO=3A)



Time (1μs/div)

Load Transient

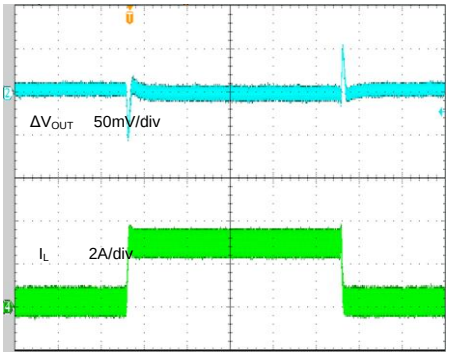
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A~1.5A~0A)



Time (100μs/div)

Load Transient

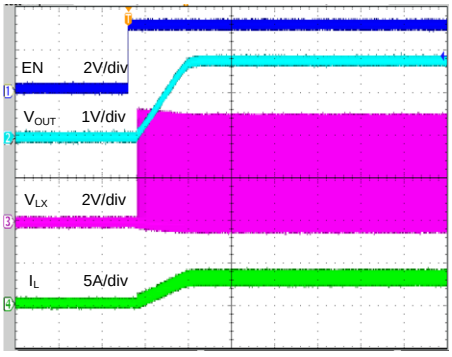
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0.3A~3A~0.3A)



Time (100μs/div)

Startup from Enable

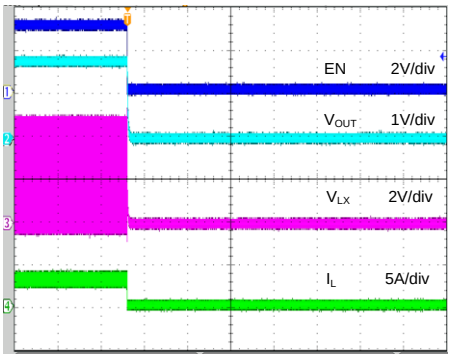
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=3.0A)



Time (800μs/div)

Shutdown from Enable

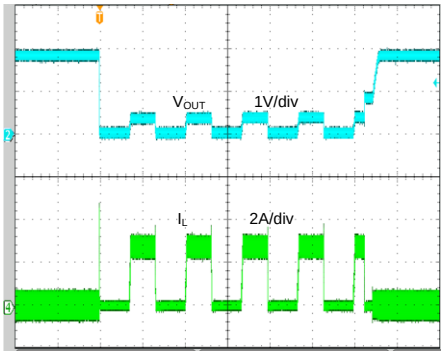
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=3.0A)



Time (800μs/div)

Short Circuit Protection

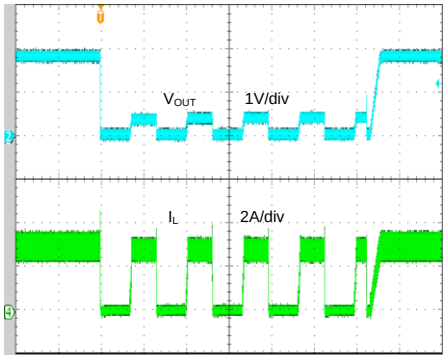
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A ~ Short ~ 0A)



Time (4ms/div)

Short Circuit Protection

(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=3.0A ~ Short ~ 3.0A)



Time (4ms/div)

Operation

The SY20124E is high efficiency 1.5MHz synchronous step down DC/DC regulators, which is capable of delivering up to 3A output current. The SY20124E can operate over a wide input voltage range from 2.7V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Low output voltage ripple, small external inductor and capacitor sizes are achieved with 1.5MHz switching frequency.

Applications Information

Because of the high integration in the SY20124E, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L and the feedback resistors (R_H and R_L) need to be selected for the targeted application specifications.

Feedback Resistor Dividers R_H and R_L

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value of between 100kΩ and 1MΩ is highly recommended for both resistors. If R_L =120kΩ is chosen, then R_H can be calculated to be:

$$R_H = \frac{(V_{OUT} - 0.6\,V) \times R_L}{0.6V}$$

Input Capacitor C_{IN}

A typical X5R or better grade ceramic capacitor with 6.3V rating and greater than 22μF capacitance is recommended. To minimize the potential noise problem, we place this ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins.

Output Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where f_{SW} is the switching frequency and I_{OUT}, max is the maximum load current.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{OUT,\,MAX} + \frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<25mΩ to achieve a good overall efficiency.

Inductor vs. Output Capacitor

The ripple base control strategy need very little C_{OUT} to confirm stability. Too large inductor and C_{OUT} will lead to be unstable. The recommend inductance and output capacitor is shown as below.

Inductance vs. Output Capacitor Selection Table

L	C_{OUT}					
	22μF	44μF	88μF	120μF	180μF	220μF
0.47μH	Note4	√	√	√	√	√
0.68μH	Note4	√	√	√	√	×
1.0μH	√	√	√	√	×	×

Note 4: Only suitable for V_{OUT}<2.0V application.

Over Current Protection

With load current increasing, as soon as the high side power FET current gets higher than peak current limit threshold, the high side power FET will turn off and the low side power FET will keep turning on until low side power FET current decrease below the valley current limit threshold. If the load current continues to increase, the output voltage will drop.

Short Circuit Protection

When the output voltage falls below 40% of the regulation level for more than 15μs, the output UVP is detected and the SY20124E will operate in hip-cup mode. The hip-cup frequency is 600Hz, the hip-cup duty cycle is 50%. If the hard short is removed, the IC will auto retry to normal operation.

Thermal Shutdown Protection

If the junction temperature of the SY20124E is higher than the thermal shutdown temperature (typical 150℃), the IC will turn off both high side power FET and low side power FET, and then enters thermal shutdown protection mode. It will remain in this state until the junction temperature decreases below 135℃. After exiting this state, the IC auto retries to normal operation.

Layout Design

The layout design of the SY20124E regulator is relatively simple. For the best efficiency and to minimum noise problems, the following components should be placed close to the IC: C_{IN}, L, R_H and R_L.

1) It is desirable to maximize the PCB copper area connected to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable. Reasonable paths are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

2) C_{IN} must be close to the pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.

4) The components R_H and R_L, and the trace connected to the FB pin and OUT pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

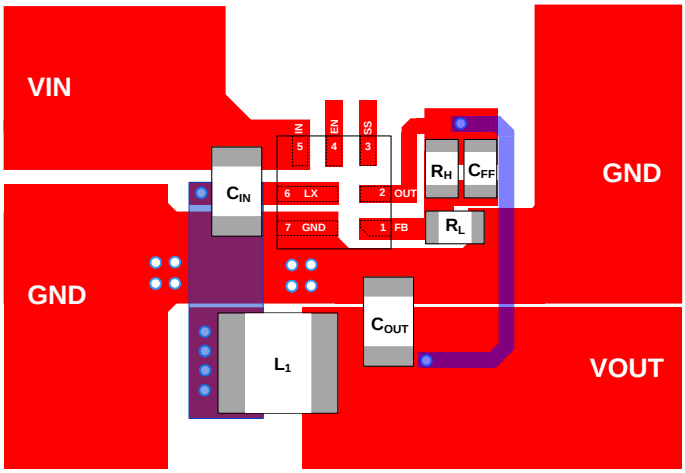
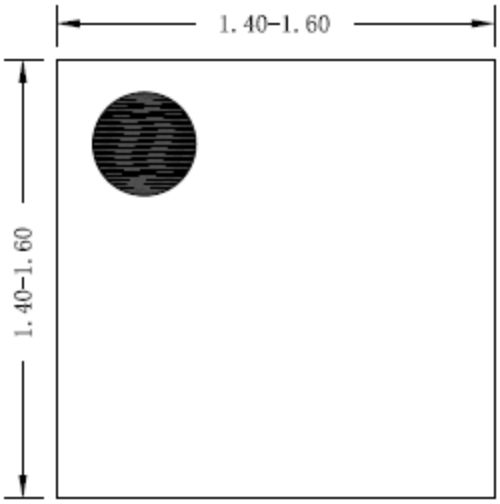
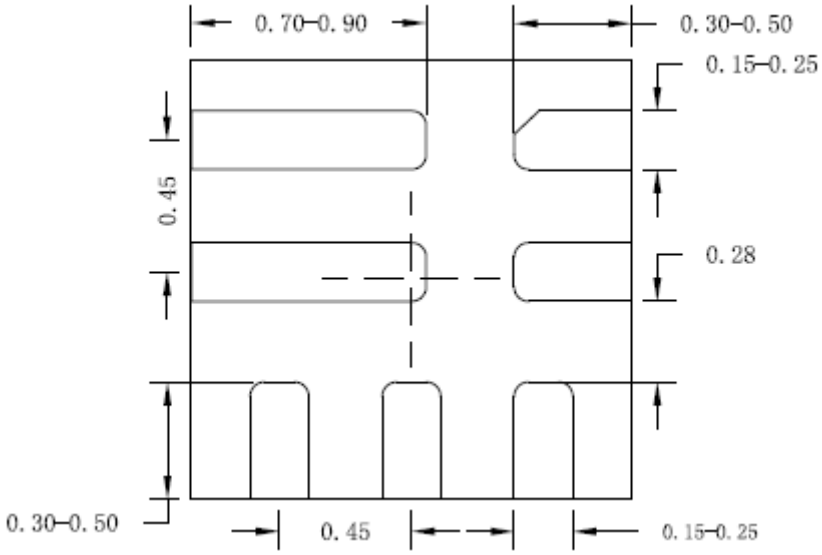


Figure4. PCB Layout Suggestion

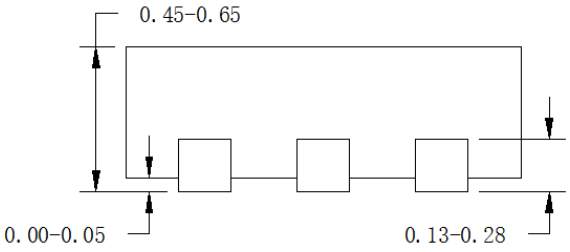
QFN1.5×1.5-7 Package Outline Drawing



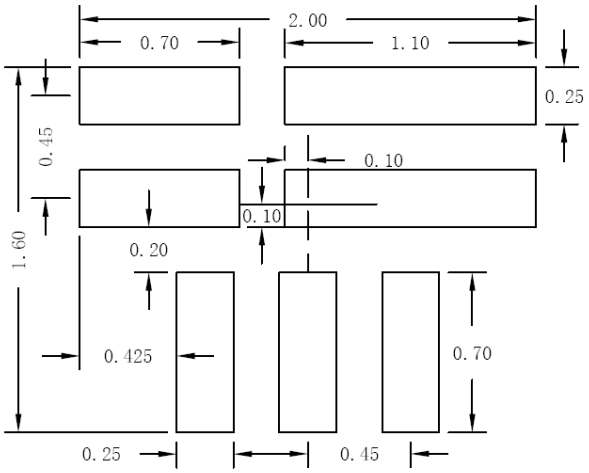
Top View



Bottom View



Side View

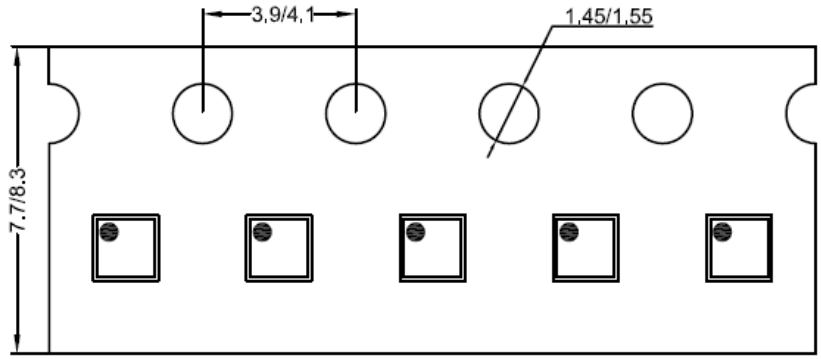


Recommended PCB layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

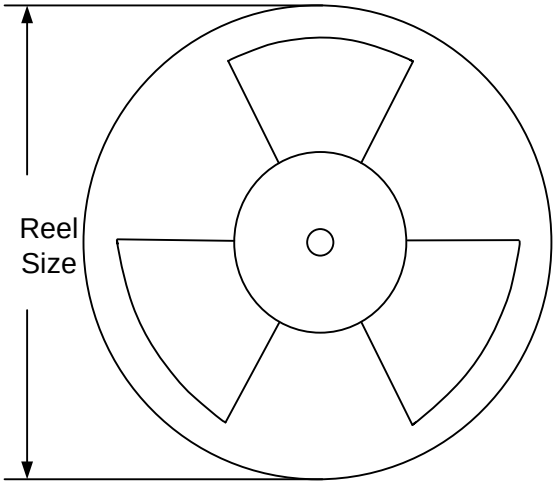
Taping & Reel Specification

1. QFN1.5×1.5 taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN1.5×1.5	8	4	7"	400	160	3000

3. Others: NA

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