SY20212C

4A, 1.8MHz, I²C Programmable Synchronous Step Down Regulator

General Description

SY20212C is a high efficiency 1.8MHz synchronous step down DC-DC regulator IC capable of delivering up to 4A output current. It can operate over a wide input voltage range from 2.6V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS\ (ON)}$ to minimize the conduction loss. The output voltage can be programmed from 0.7625V to 1.55V through I²C interface.

SY20212C is available in TSOT23-8 package.

Ordering Information

SY20212 □(□,□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package Type	Note
SY20212CAIC	TSOT23-8	--

Features

- 2.6V to 5.5V Input Voltage Range
- Fixed Frequency Operation: 1.8MHz
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 70mΩ/40mΩ
- Programmable Output Voltage: 0.7625V to 1.55V in 12.5mV Steps
- Default 1.05V Output Voltage
- 4A Output Current Capability
- Capable for 0.33µH Inductor and 22µF Ceramic Capacitor
- PFM/PWM Operation for Optimum Increased Efficiency
- OVP/OCP/UVLO/OTP Protections
- RoHs Compliant and Halogen Free
- Compact Package: TSOT23-8

Applications

- Smart Phone
- MID

Typical Applications

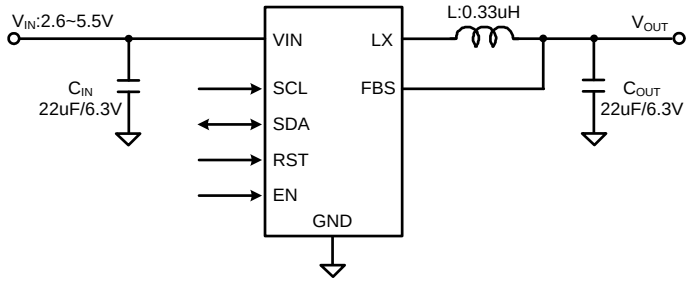


Figure 1. Schematic Diagram

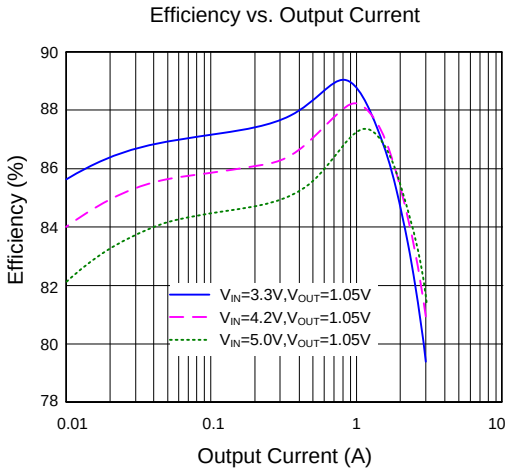
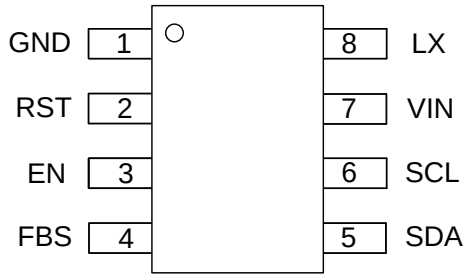


Figure 2. Efficiency vs. Output Current

Pinout (top view)



(TSOT23-8)

Top Mark: Ur***xyz***, (Device code: Ur, ***x=year code, y=week code, z= lot number code***)

Pin Number	Pin Name	Pin Description
1	GND	Ground pin.
2	RST	Pulling this pin high will reset the register to default value. Do not leave it floating.
3	EN	Enable control pin. Active high. Do not leave it floating. If EN pin is low, the DC-DC converter will be turned off, and all I^2C registers will be reset to default values.
4	FBS	Feedback pin. Must be connected to the output capacitor positive terminal with a separated trace to avoid noise.
5	SDA	Data line for the I^2C interface. Open-drain output.
6	SCL	Clock input for the I^2C interface. Open-drain input.
7	VIN	Power input pin. This pin must be decoupled to ground by a 22µF ceramic capacitor. It should be placed as close as possible between IN and GND pins.
8	LX	Switching node pin. Connect this pin to the switching of inductor.

Absolute Maximum Ratings (Note 1)

VIN---------- 6.0V
All Other Pins---------- -0.3V~V_{IN} + 0.6V
Power Dissipation, P_D @ T_A = 25°C TSOT23-8 ---------- 1.7W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 58°C /W
θ_{JC} ---------- 5.5°C /W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.6V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.05V, L = 0.33µH, C_{OUT} = 22uF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.6		5.5	V
V_{IN} UVLO	V_{UVLO}	V_{IN} rising		2.4	2.55	V
V_{IN} UVLO Hysteresis	V_{UVHYST}			120		mV
Quiescent Current	I_Q	I_{OUT}=0, EN=1, FB=105%×V_{REF}		80		µA
Shut-down Current	$I_{SHDN\_H/W}$	EN=0		0.1	1	µA
	$I_{SHDN\_S/W}$	EN=V_{IN}, Buck_EN=0		30		
EN, RST						
Rising Threshold	V_{IH}		1.1			V
Falling Threshold	V_{IL}				0.4	V
SDA, SCL						
Rising Threshold	V_{IH}		1.5			V
Falling Threshold	V_{IL}				0.4	V
V_{OUT} Accuracy	V_{REG}	Forced PWM, default value	-1		+1	%
NFET $R_{DS(ON)}$	$R_{DS(ON)N}$			40		mΩ
PFET $R_{DS(ON)}$	$R_{DS(ON)P}$			70		mΩ
PMOS Peak Current Limit	I_{LIM_PEAK}		5.5			A
NMOS Valley Current Limit	I_{LIM_VALLEY}		4			A
Internal Soft-start Time	t_{SS}			300		µs
Min On Time	t_{ON}			40		ns
Oscillator Frequency	F_{OSC}			1.8		MHz
Thermal Shut-down Temperature	T_{SD}			150		°C
Thermal Shut-down Hysteresis	T_{HYS}			15		°C
FBS Node Discharge Resistor	R_{DSH}			10		Ω
Input OVP Shut-down	V_{OVP}	Rising threshold		6.15		V
		Falling threshold	5.5	5.85		V
Over Voltage Protection Blanking Time	$t_{BLANKING}$			20		µs
SDA Pull Down Resistor	R_{SDA}			25		Ω
Dynamic Voltage Scaling Slew Rate	dv/dt			100		mV/µs

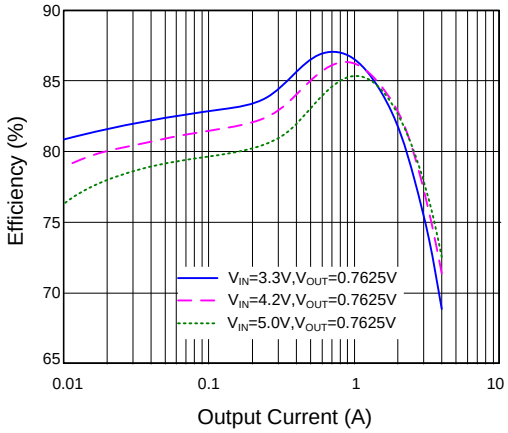
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note2: θ_{JA} of SY20212CAIC is measured in the natural convection at TA = 25°C on 2OZ four-layer Silergy evaluation board of JEDEC 51-3 thermal measurement standard. Paddle of TSOT23-8 package is the case position for SY20212CAIC.

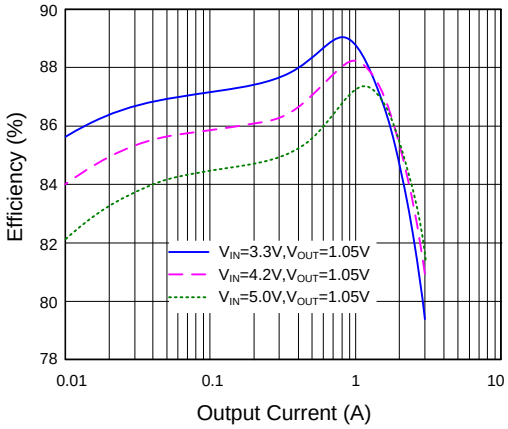
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

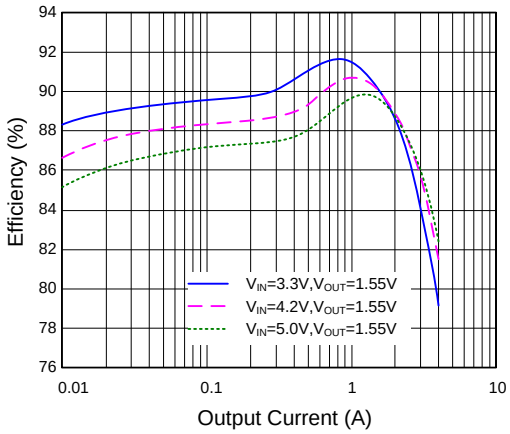
Efficiency vs. Output Current



Efficiency vs. Output Current

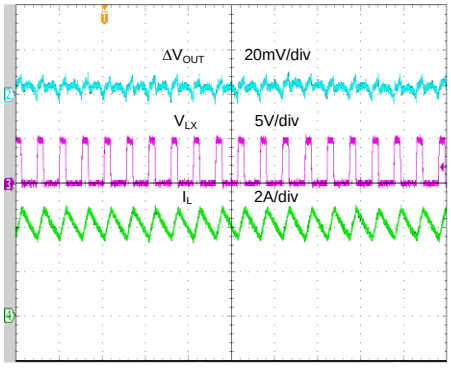


Efficiency vs. Output Current



Output Ripple

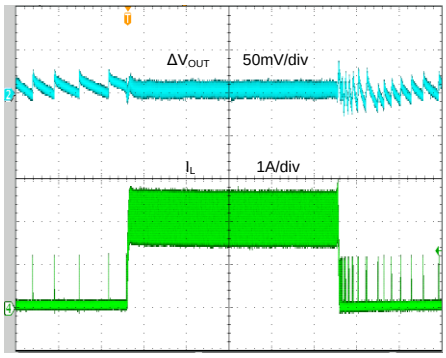
(V_{IN}=5.0V, V_{OUT}=1.05V, I_O=4.0A)



Time (1μs/div)

Load Transient

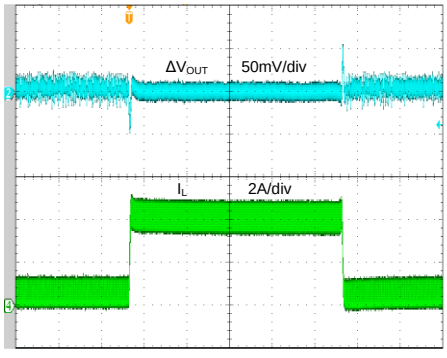
(V_{IN}=5.0V, V_{OUT}=1.05V, I_O=0 ~ 2.0A)



Time (100μs/div)

Load Transient

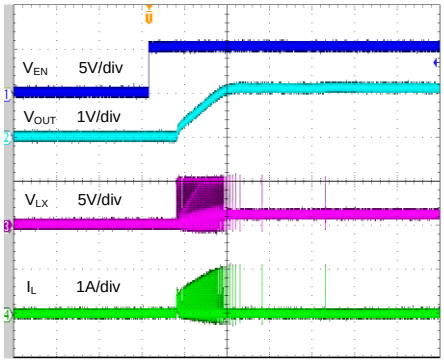
(V_{IN}=5.0V, V_{OUT}=1.05V, I_O=0.4 ~ 4.0A)



Time (100μs/div)

Start up from EN

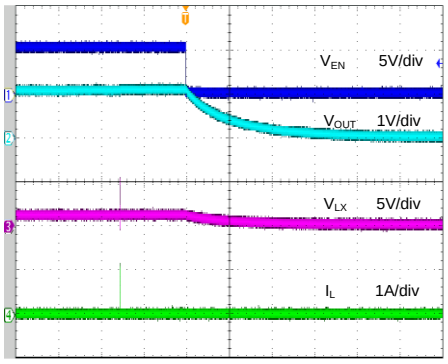
(V_{IN}=5.0V, V_{OUT}=1.05V, I_O=0A)



Time (200μs/div)

Shutdown from EN

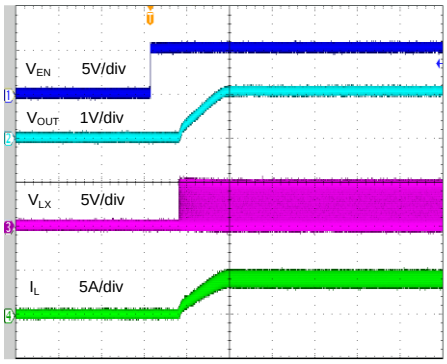
(V_{IN}=5.0V, V_{OUT}=1.05V, I_O=0A)



Time (200μs/div)

Start up from EN

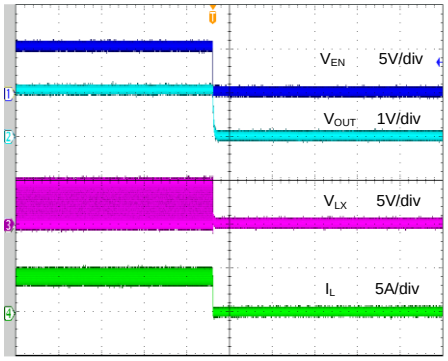
(V_{IN}=5.0V, V_{OUT}=1.05V, I_O=4A)



Time (200μs/div)

Shutdown from EN

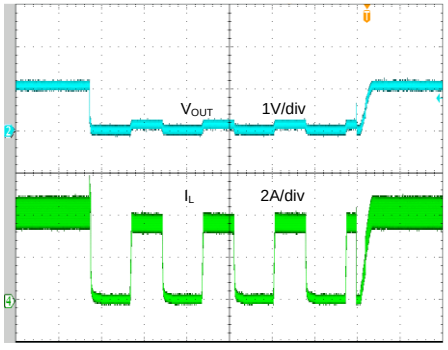
(V_{IN}=5.0V, V_{OUT}=1.05V, I_O=4A)



Time (200μs/div)

Short Circuit Protection

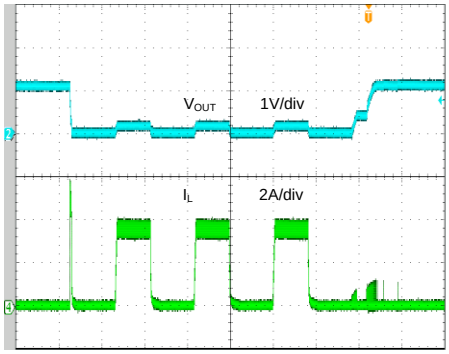
(V_{IN}=5.0V, V_{OUT}=1.05V, I_O=0A ~ short)



Time (800μs/div)

Short Circuit Protection

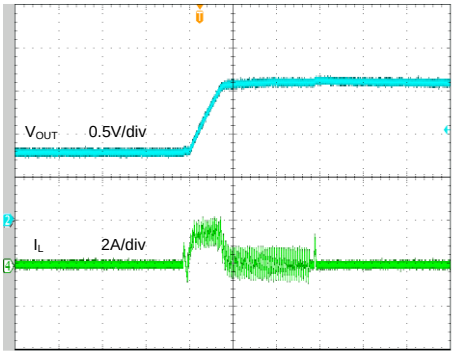
(V_{IN}=5.0V, V_{OUT}=1.05V, I_O=4A ~ short)



Time (800μs/div)

Dynamic Voltage Scale

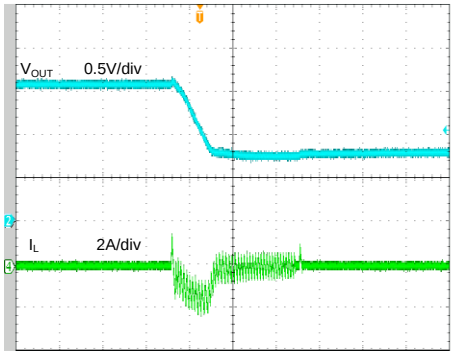
(V_{IN}=5V,V_{OUT}=0.7625V~1.55V,I_{OUT}=0A)



Time (10μs/div)

Dynamic Voltage Scale

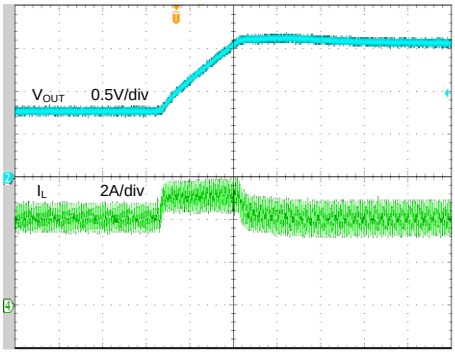
(V_{IN}=5V,V_{OUT}=1.55V~0.7625V,I_{OUT}=0A)



Time (10μs/div)

Dynamic Voltage Scale

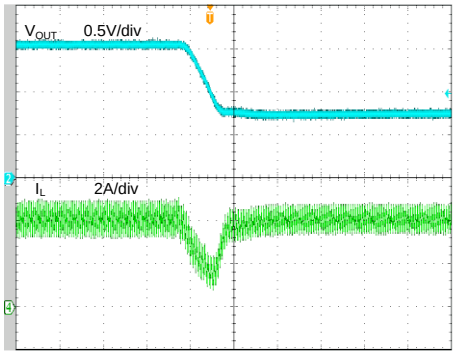
(V_{IN}=5V,V_{OUT}=0.7625V~1.55V,I_{OUT}=4A)



Time (10μs/div)

Dynamic Voltage Scale

(V_{IN}=5V,V_{OUT}=1.55V~0.7625V,I_{OUT}=4A)



Time (10μs/div)

I²C Interface

I²C address of the SY20212C is set to 0xCCh at the factory.

SY20212C features an I²C interface that allows the HOST processor to control the output voltage achieve the DVS function. The I²C interface supports clock in speeding up to 3.4MHz and uses standard I²C commands. SY20212C always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation.

START and STOP Conditions:

SY20212C is controlled via an I²C compatible interface. The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.

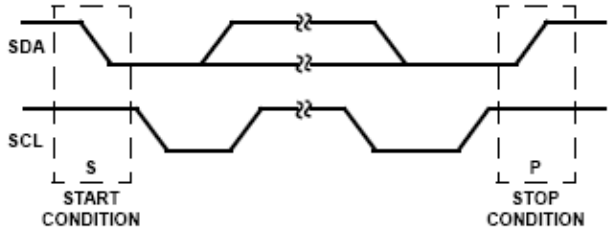


Figure3. START and STOP Conditions

Data Validity:

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

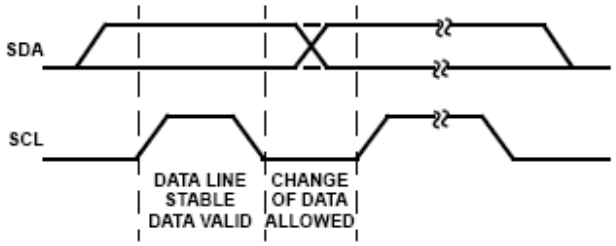


Figure4. Data Validity

Acknowledge:

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

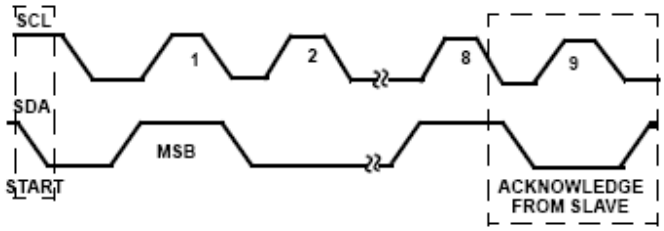


Figure5. Complete Data Transfer

Data Transactions:

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bits of slave address (1100110x) for the SY20212C (this address can be changed if necessary) followed by the 8th bit, R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and SY20212C acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the SY20212C which register the master will write or read. Once the SY20212C receives a register address byte it responds with an acknowledge.

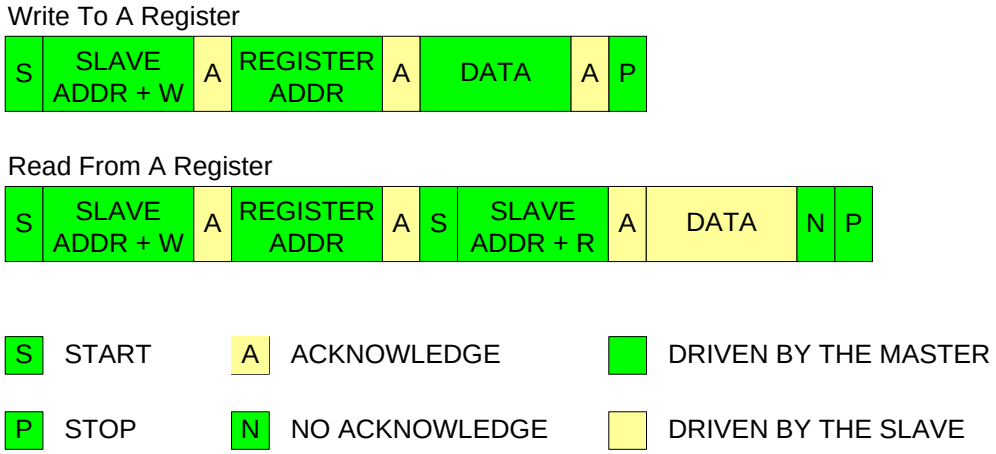


Figure 6. Data Transactions

Register Settings:

Register Name				VSEL0
Address				0x00
Field	**Bit**	**R/W**	**Default**	**Description**
BUCK_EN	7	R/W	1	Software buck enable. When EN pin is low, the regulator is off. When EN pin is high, BUCK_EN bit takes precedent.
MODE	6	R/W	0	0=Allow auto-PFM mode during light load. 1=Forced PWM mode
NSEL	5:0	R/W	010111 = 1.05V	000000 = 0.7625V 000001 = 0.775V …… 010111= 1.05V …… 111111=1.55V

Operation

SY20212C is a high efficiency 1.8MHz synchronous step down DC-DC regulator IC capable of delivering up to 4A output current. It can operate over a wide input voltage range from 2.6V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS\ (ON)}$ to minimize the conduction loss. The output voltage can be programmed from 0.7625V to 1.55V through I^2C interface.

Enabling Function

The EN pin controls SY20212C start up. EN pin low to high transition starts up the power up sequencer. If EN pin is low, the DC-DC converter will be turned off, and all registers are reset to default values.

SY20212C allows software enable of the regulator. BUCK_EN is initialized HIGH in the registers.

Table1. Hardware and Software Enable Control

Pin	Soft-ware bit	Output
EN	BUCK_EN	
0	x	OFF
1	0	OFF
1	1	ON

Input Over Voltage Protection Function

When the V_{IN} exceeds over voltage protection threshold, SY20212C will stop switching to protect the circuitry. An internal 20μs blanking time filter helps to prevent the circuit from shutting down due to noise spikes.

Applications Information

Because of the high integration in SY20212C, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L need to be selected for the targeted applications.

Input capacitor C_{IN}

This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS}=I_{OUT}\times\sqrt{D(1\text{-}D)}\ (A)$$

This formula has a maximum at $V_{IN}=2\times V_{OUT}$ condition, where $I_{CIN\_RMS}=I_{OUT}/2$.

With the maximum load current at 4A, a typical X5R or better grade ceramic capacitor with 6.3V rating and greater than 22uF capacitance can handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the VIN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and VIN/GND pins.

Output inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L=\frac{V_{OUT}(1-V_{OUT}/V_{IN\_MAX})}{F_{SW}\times I_{OUT\_MAX}\times 40\%}\ (H)$$

where F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

SY20212C is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT,\,MIN}>I_{OUT,\,MAX}+\frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{2\cdot F_{SW}\cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<15mΩ to achieve a good overall efficiency.

Inductor vs. Output Capacitor

The ripple base control strategy need very little C_{OUT} to confirm stability. Too large inductor and C_{OUT} will lead to unstable. The recommend inductance and output capacitor is shown as below.

Table2. Inductance vs. Output Capacitor Selection (Note4)

L	C_{OUT}					
	10uF	22uF	22uFx2	22uFx3	22uFx4	22uFx5
0.33uH	×	√	√	√	√	×
0.47uH	×	√	√	√	×	×
0.68uH	×	√	√	×	×	×

Note 4: Use electrolytic capacitor will help stability because electrolytic capacitor has large ESR.

Layout Design

To achieve the higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, L and C_{OUT}.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance

2) The decoupling capacitor of VIN and GND must be placed close enough to the pins. The loop area formed by the capacitors and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to improve the noise immunity.

4) The feedback trace connecting C_{OUT} to the FBS pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to the FBS pin.

5) The PCB copper area associated with VIN pin must be routed across pin1 and pin8 to get better noise immunity and thermal performance.

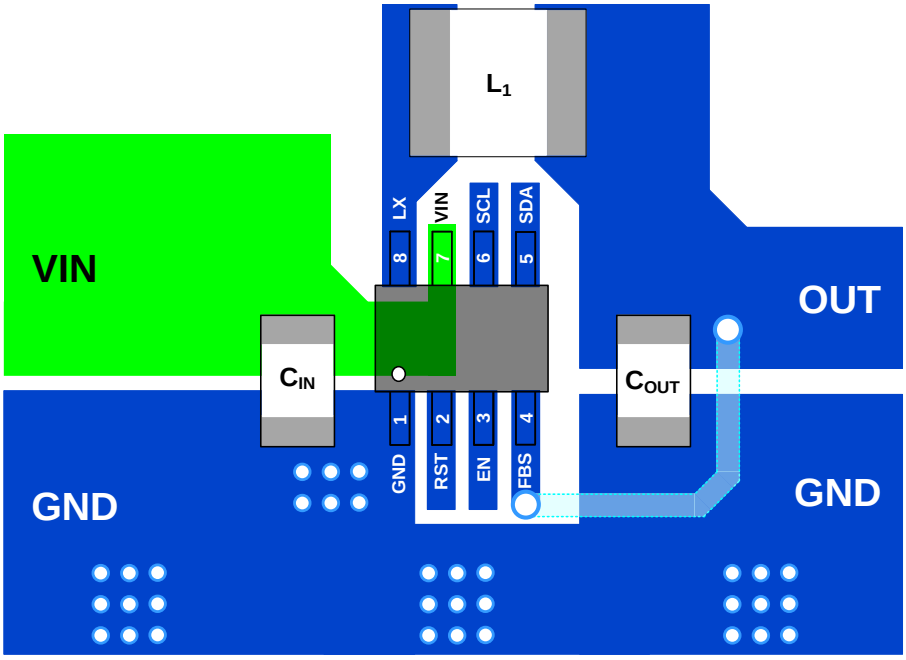
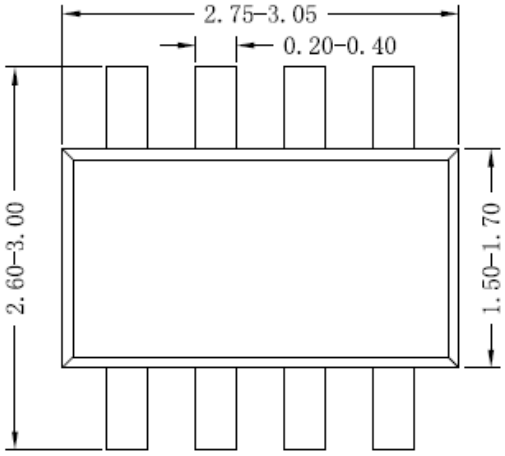
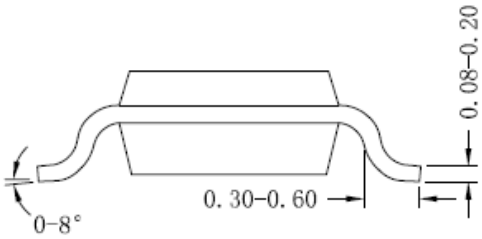


Figure7. SY20212CAIC PCB layout Suggestion

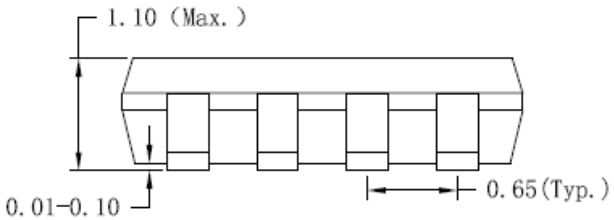
TSOT23-8 Package Outline Drawing



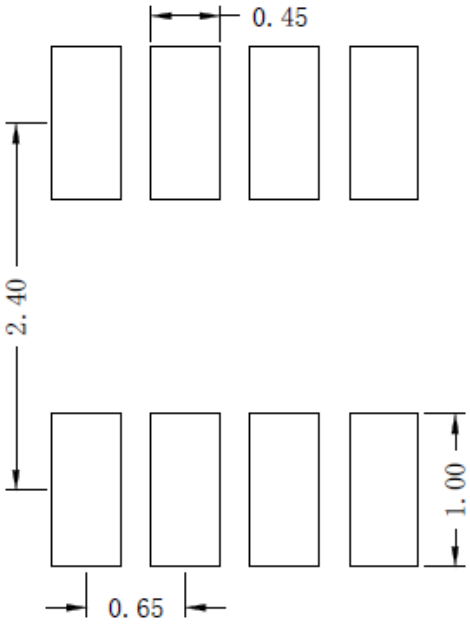
Top view



Side view A



Side view B



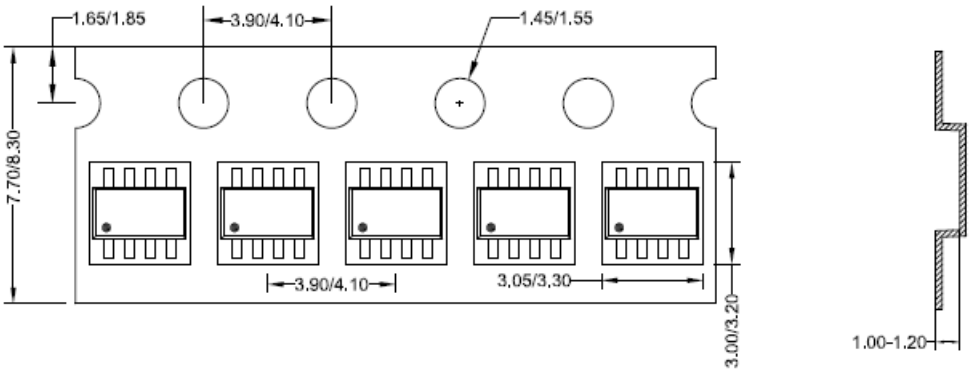
Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr**

Taping & Reel Specification

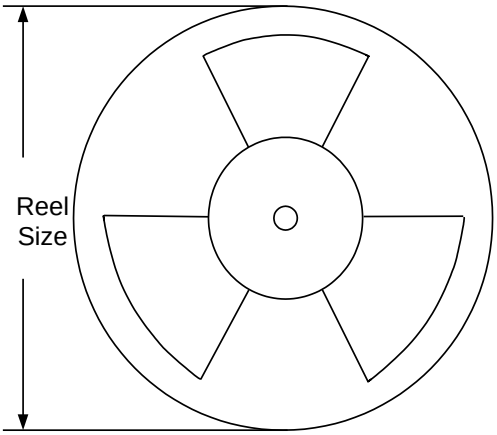
1. Taping orientation

TSOT23-8



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
TSOT23-8	8	4	7	400	160	3000

3. Others: NA

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