

## High Efficiency 6V, 6A, 1.2MHz Synchronous Step Down Regulator

### General Description

SY20228 is a high efficiency high frequency synchronous step down DC/DC regulator capable of delivering up to 6A output current. It operates over a wide input voltage range from 2.75V to 6V. It integrates main switch and synchronous switch with very low  $R_{DS(ON)}$  to minimize the conduction loss. High integrated solution and DFN2x2-8 package perform the optimized BOM cost and reduce external component part count. Low input and output voltage ripple, small external inductor and capacitor sizes, small PCB layout space are achieved.

### Ordering Information

SY20228 □(□□)□  
 □ Temperature Code  
 □□ Package Code  
 □ Optional Spec Code

Ordering Number	Package type	Note
SY20228DFC	DFN2x2-8	--

### Features

- Low  $R_{DS(ON)}$  for Internal Switches (Top/Bottom): 35/15 mΩ
- 2.75-6V Input Voltage Range
- 1.2 MHz Switching Frequency Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- Up to 94% Efficiency
- 6A Continuous Output Current Capability
- Shutdown Mode Draws <math><0.1\mu A</math> Supply Current
- 100% Dropout Operation
- Power Good Indicator
- OCP/UVLO/OTP Protections
- RoHS Compliant and Halogen Free
- Compact Package: DFN2x2-8

### Applications

- High Definition Set Top Box
- LCD TV
- Notebook PC

### Typical Applications

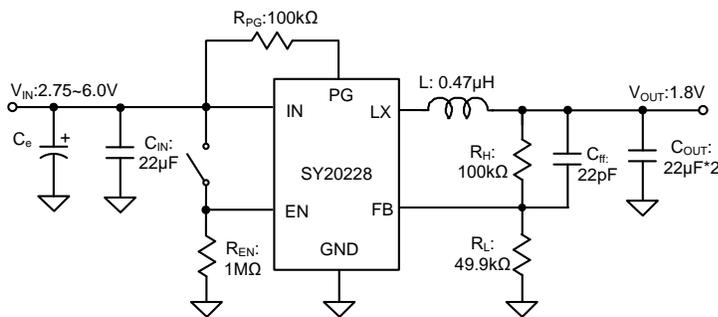


Figure 1. Schematic Diagram

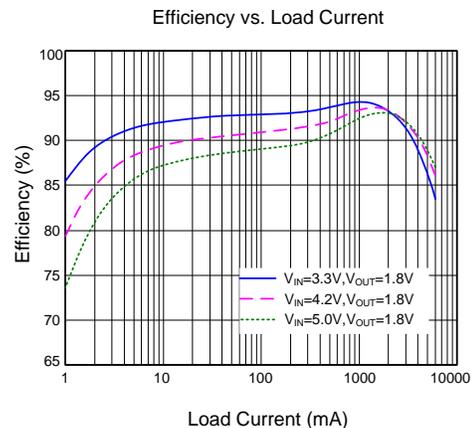
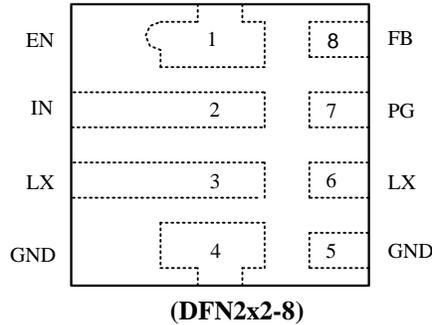


Figure 2. Efficiency vs. Load Current

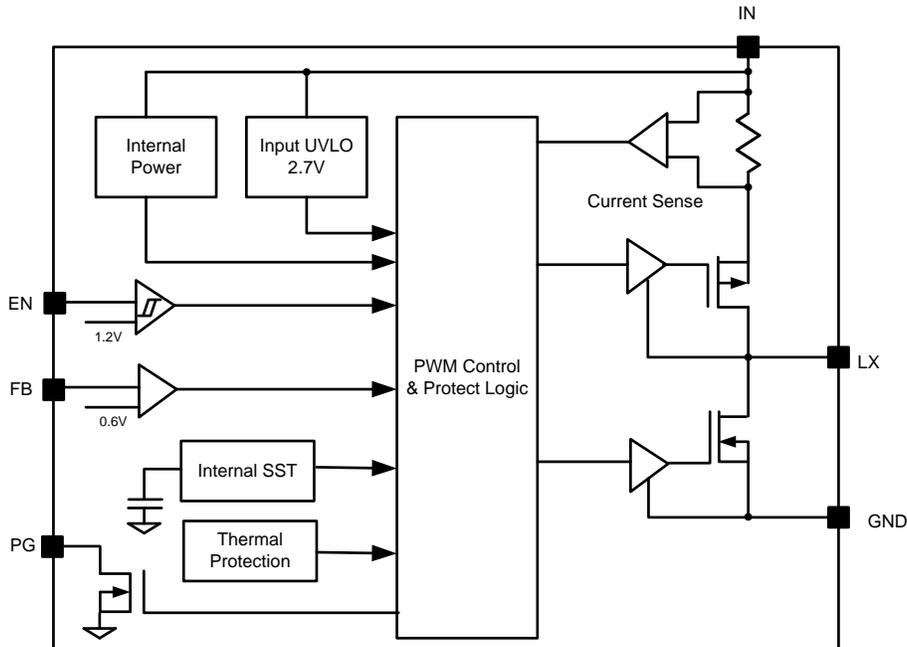
**Pinout (top view)**



**Top Mark:** VWxyz for SY20228DFC (device code: VW, x=year code, y=week code, z=lot number code)

Pin Name	Pin Number	Description
EN	1	Enable control. Pull high to turn on. Do not leave it floating.
GND	4,5	Ground pin.
LX	3,6	Inductor pin. Connect this pin to the switching node of the inductor.
IN	2	Power input pin.
FB	8	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure.1) to program the output voltage: $V_{OUT}=0.6 \times (1+R_1/R_2)$
PG	7	Power good indicator. When the output voltage exceeds 90% of regulation point, it becomes open drain. Low otherwise.

**Block Diagram**



**Figure 3. Block Diagram**



**Absolute Maximum Ratings** (Note 1)

IN, LX -----	6.5V
All Other Pins-----	V <sub>IN</sub> + 0.6V
Power Dissipation, P <sub>D</sub> @ T <sub>A</sub> = 25°C DFN2x2 -----	2W
Package Thermal Resistance (Note 2)	
θ <sub>JA</sub> -----	62.5°C/W
θ <sub>JC</sub> -----	10°C/W
Junction Temperature Range -----	150°C
Lead Temperature (Soldering, 10 sec.) -----	260°C
Storage Temperature Range -----	-65°C to 150°C

**Recommended Operating Conditions** (Note 3)

Supply Input Voltage -----	2.75V to 6.0V
Junction Temperature Range -----	-40°C to 125°C
Ambient Temperature Range -----	-40°C to 85°C

## Electrical Characteristics

( $V_{IN} = 5V$ ,  $V_{OUT} = 2.5V$ ,  $L = 0.47\mu H$ ,  $C_{OUT} = 22\mu F \times 2$ ,  $T_A = 25^\circ C$ ,  $I_{OUT} = 1A$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	$V_{IN}$		2.75		6	V
Quiescent Current	$I_Q$	$I_{OUT}=0$ , $EN=1$ , $FB=105\% \times V_{REF}$		60		$\mu A$
Shutdown Current	$I_{SHDN}$	$EN=0$		0.1	1	$\mu A$
Feedback Reference Voltage	$V_{REF}$		0.591	0.6	0.609	V
NFET $R_{DS(ON)}$	$R_{DS(ON)N}$			15		$m\Omega$
PFET $R_{DS(ON)}$	$R_{DS(ON)P}$			35		$m\Omega$
PFET Current Limit	$I_{LIM}$		7.5			A
Internal Soft-start Time	$t_{SS}$			0.8		ms
PGOOD Under-voltage Threshold	$V_{FB,LV}$			0.54		V
Short Circuit Protection Threshold	$V_{SCP}$			0.25		V
Min ON Time				60		ns
Max Duty Cycle			100			%
EN Rising Threshold	$V_{ENH}$		1.2			V
EN Falling Threshold	$V_{ENL}$				0.4	V
Input UVLO Threshold	$V_{UVLO}$				2.7	V
UVLO Hysteresis	$V_{HYS}$			0.3		V
Oscillator Frequency	$F_{OSC}$			1.2		MHz
Thermal Shutdown Temperature	$T_{SD}$			150		$^\circ C$
Thermal Shutdown Hysteresis	$T_{HYS}$			15		$^\circ C$
LX Node Discharge Resistance	$R_{DISCHG}$			50		$\Omega$

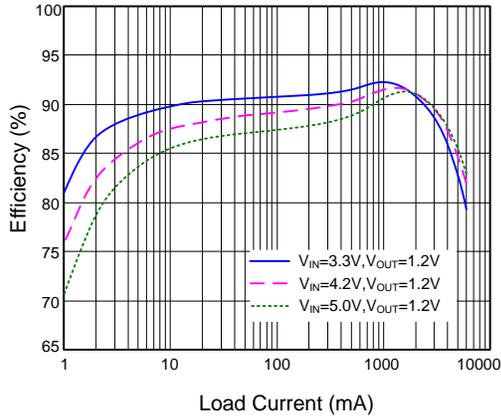
**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ C$  on 2OZ four-layer Silergy evaluation board of JEDEC 51-3 thermal measurement standard. Paddle of DFN2x2-8 package is the case position for  $\theta_{JC}$  measurement.

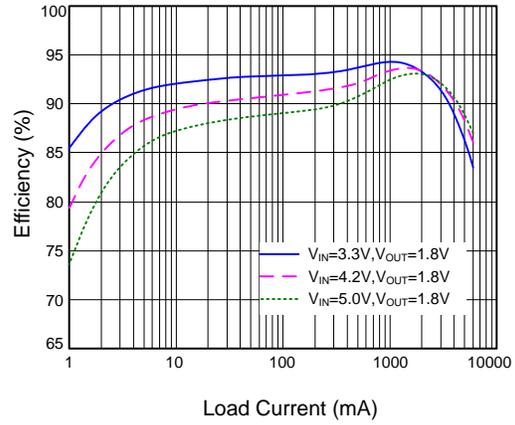
**Note 3:** The device is not guaranteed to function outside its operating conditions.

## Typical Performance Characteristics

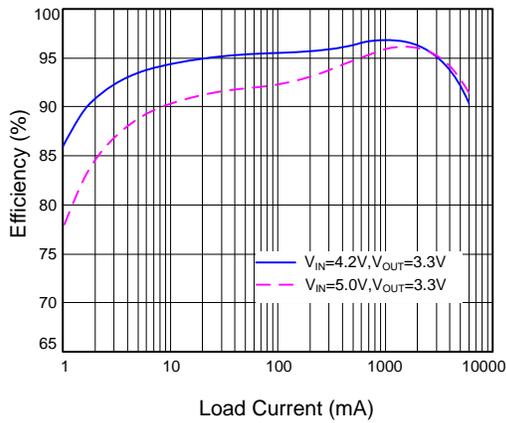
Efficiency vs. Load Current



Efficiency vs. Load Current

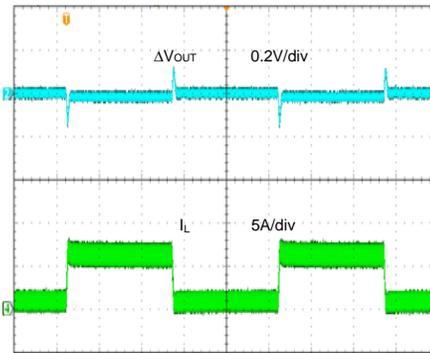


Efficiency vs. Load Current



Load Transient

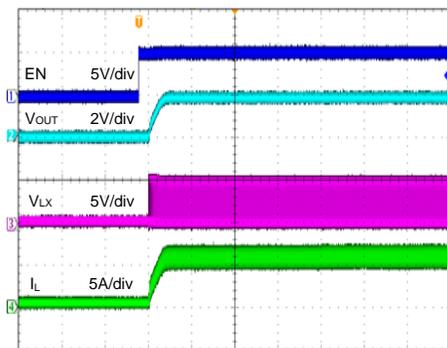
( $V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0.6-6A$ )



Time (200 $\mu$ s/div)

Startup from Enable

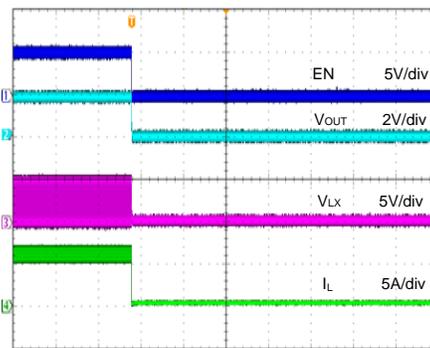
( $V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=6A$ )



Time (2ms/div)

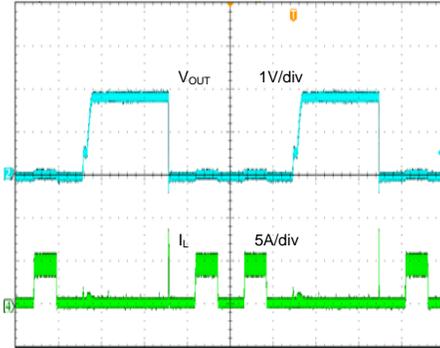
Shutdown from Enable

( $V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=6A$ )



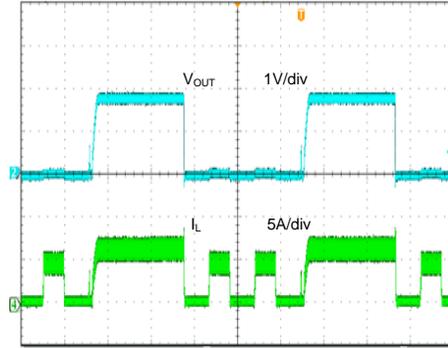
Time (2ms/div)

**Short Circuit Protection**  
( $V_{IN}=5V$ ,  $V_{OUT}=1.8V$ , 0A to Short)



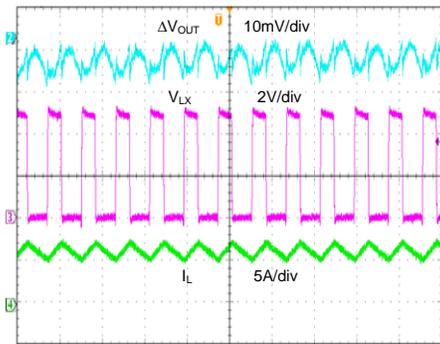
Time (4ms/div)

**Short Circuit Protection**  
( $V_{IN}=5V$ ,  $V_{OUT}=1.8V$ , 6A to Short)



Time (4ms/div)

**Output Ripple**  
( $V_{IN}=5V$ ,  $V_{OUT}=1.8V$ ,  $I_{OUT}=6A$ )



Time (1μs/div)

## Operation

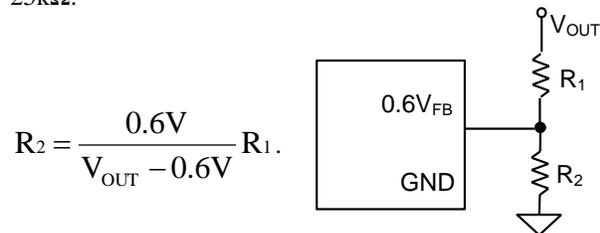
SY20228 is a high efficiency high frequency synchronous step down DC/DC regulator capable of delivering up to 6A output current. It operates over a wide input voltage range from 2.75V to 6V. It integrates main switch and synchronous switch with very low  $R_{DS(ON)}$  to minimize the conduction loss. High integrated solution and DFN2x2-8 package perform the optimized BOM cost and reduce external component part count. Low input and output voltage ripple, small external inductor and capacitor sizes, small PCB layout space are achieved.

## Applications Information

Because of the high integration in the SY20228, the application circuit based on this regulator is rather simple. Only the input capacitor  $C_{IN}$ , the output capacitor  $C_{OUT}$ , the output inductor  $L$  and the feedback resistors ( $R_1$  and  $R_2$ ) need to be selected for the targeted applications specifications.

### Feedback Resistor Dividers $R_1$ and $R_2$ :

Choose  $R_1$  and  $R_2$  to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both  $R_1$  and  $R_2$ . A value of between  $10k\Omega$  and  $1M\Omega$  is highly recommended for both resistors. If  $V_{OUT}$  is 1.8V,  $R_1=50k\Omega$  is chosen, then  $R_2$  can be calculated to be  $25k\Omega$ :



$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1.$$

### Input Capacitor $C_{IN}$ :

This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

This formula has a maximum at  $V_{IN}=2V_{OUT}$  condition, where  $I_{CIN\_RMS}=I_{OUT}/2$ . This simple worst-case condition is commonly used for DC/DC design.

With the maximum load current at 6A, a typical X5R or better grade ceramic capacitor with 6.3V rating and at least one  $22\mu F$  ceramic capacitor can handle this ripple current well. To minimize the potential noise

problem, this ceramic capacitor should be placed really close to the IN and GND pins. Care should be taken to minimize the loop area formed by the  $C_{IN}$ , and IN/GND pins.

### Output Capacitor $C_{OUT}$ :

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor with 6.3V rating and more than two  $22\mu F$  capacitances.

### Output Inductor $L$ :

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where  $F_{sw}$  is the switching frequency and  $I_{OUT,MAX}$  is the maximum load current.

The SY20228 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance

- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT, MIN} > I_{OUT, MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times F_{SW} \times L}$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with  $DCR < 15m\Omega$  to achieve a good overall efficiency.

**Enable Operation**

Pulling the EN pin low (<0.4V) will shut down the device. During shut down mode, the SY20228 shutdown current drops to lower than 0.1μA. Driving the EN pin high (>1.2V) will turn on the IC again.

**PG (Power Good):**

The power good is an open-drain output. Connect an above 100k pull up resistor to VIN to obtain an output voltage. The power good will output high immediately after the output voltage within 90% of normal output voltage.

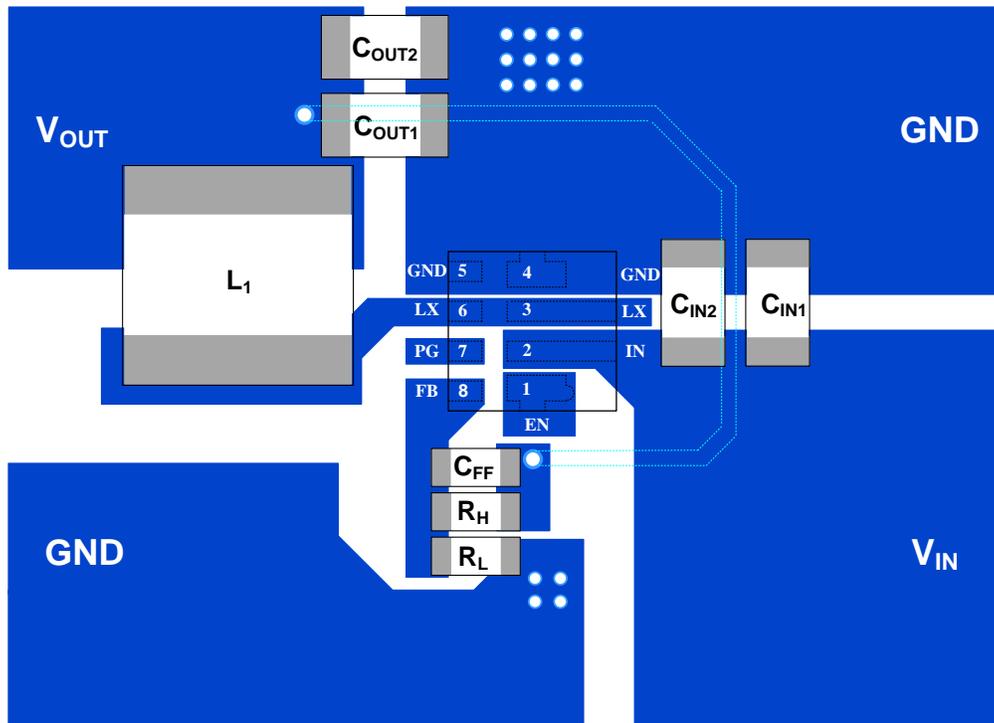
**Load Transient Considerations:**

The SY20228 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF~220pF ceramic capacitor in parallel with R<sub>H</sub> may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

**Layout Design:**

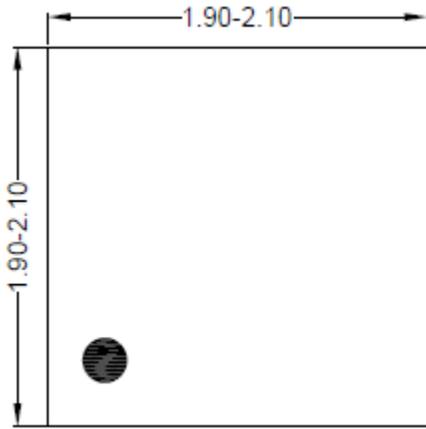
The layout design of SY20228 is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C<sub>IN</sub>, L, R<sub>H</sub> and R<sub>L</sub>.

- (1) Multi-layer board is suggested for SY20228 6A output current application. It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. Reasonable vias are suggested to be placed around GND pins to enhance the soldering quality and thermal performance.
- (2) C<sub>IN</sub> must be close to Pins IN and GND. The loop area formed by C<sub>IN</sub> and GND must be minimized.
- (3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
- (4) The components R<sub>H</sub> and R<sub>L</sub> and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

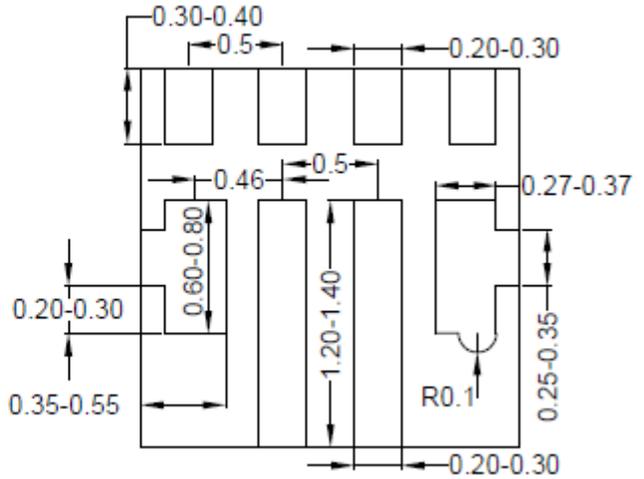


**Figure4. PCB Layout Suggestion**

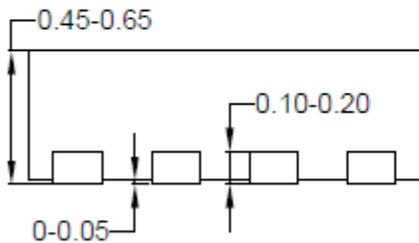
**DFN2x2-8 Package Outline**



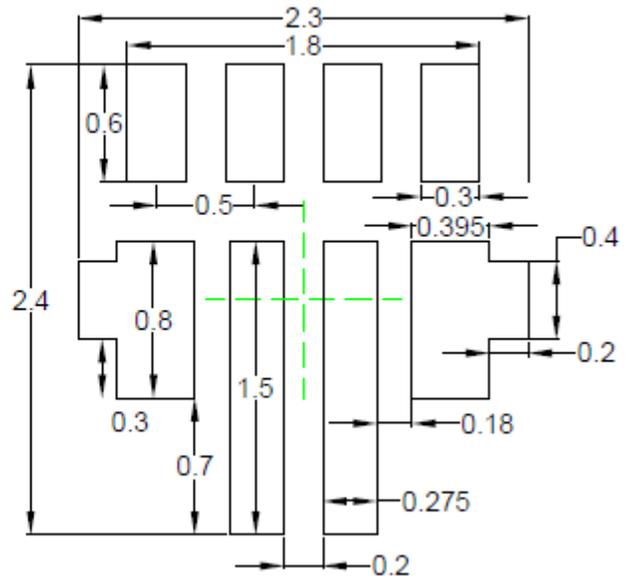
**Top View**



**Bottom View**



**Side View**

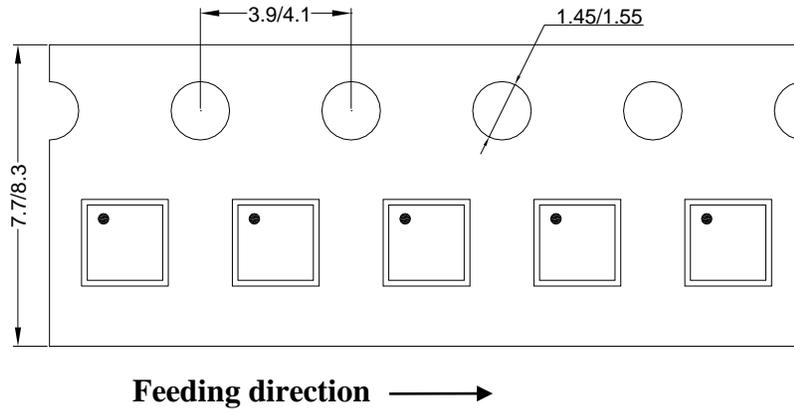


**Recommended PCB Layout  
(Reference only)**

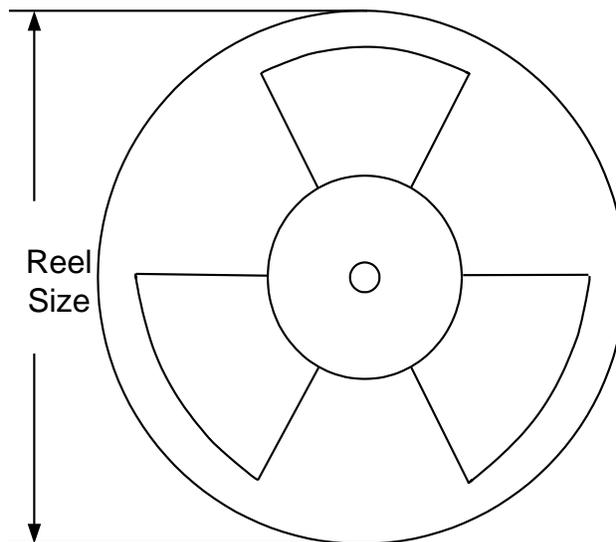
**Notes: All dimension in millimeter and exclude mold flash & metal burr.**

## Taping & Reel Specification

### 1. DFN2x2



### 2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2x2	8	4	7"	400	160	3000

### 3. Moisture Sensitive Level: MSL1

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