SY20313A

High Efficiency 5.5V, Dual 1A, 2MHz Synchronous Step Down Regulator

General Description

The SY20313A is a dual-output, high efficiency 2MHz synchronous step down DC-DC regulator IC, capable of delivering up to 1A output current each output channel. The SY20313A operates over a wide input voltage range from 2.5V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY20313A can operate in two different modes by controlling the MODE pin. For low noise applications SY20313A can be forced into fixed frequency PWM mode by pulling this pin high. For power saving applications, SY20313A can enter the variable frequency operation to maintain high efficiency at light load by pulling this pin low.

Features

- Input range: 2.5V to 5.5V
- 2MHz switching frequency
- 180° out of phase operation
- Output current: 1A per channel
- +/-1% DC output voltage accuracy at forced PWM mode
- Low Quiescent Current: <35uA when both channels are enabled
- Low $R_{DS(ON)}$ for internal switches (PFET/NFET): 220mΩ/180mΩ
- Internal softstart
- 100% dropout operation
- RoHS Compliant and Halogen Free
- Compact package: DFN3x3-10

Ordering Information

SY20313□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20313ADBC	DFN3x3-10	1A

Applications

- SSD
- Cell Phones
- Digital Cameras
- PDAs
- Portable Media Players

Typical Applications

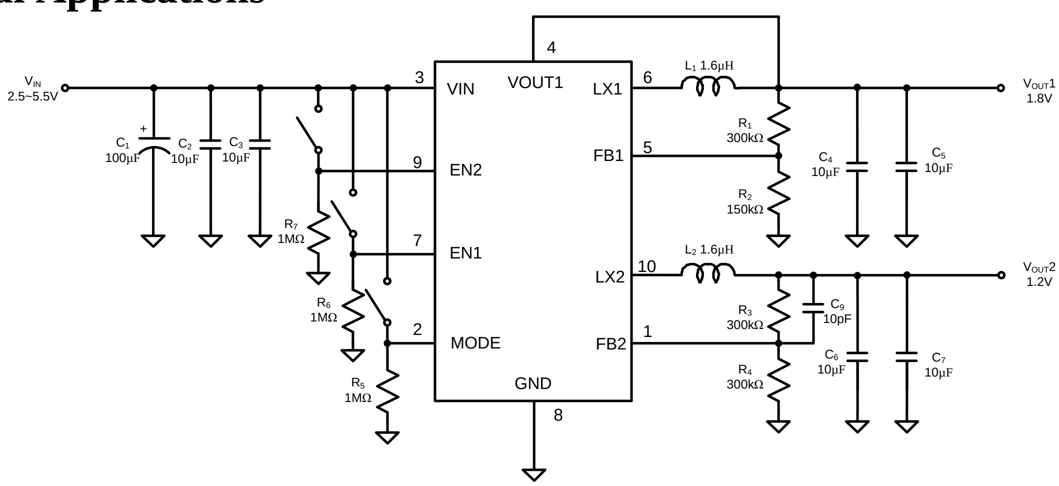
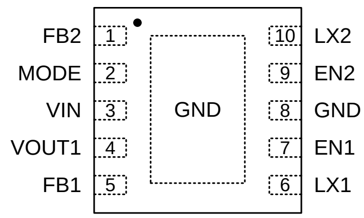


Figure 1.Schematic diagram

Pinout (top view)



Top mark: **EZ*xyz*** (Device code: EZ, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
FB2	1	Feedback pin for output2. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output2 voltage: $V_{OUT2}=0.6V\times(1+R_{H2}/R_{L2})$
Mode	2	Mode control pin. Pull this pin high to operate in fixed frequency mode and pull this pin low to allow variable frequency operation. Do not float this pin.
VIN	3	Power input pin.
VOUT1	4	Connect this pin to the output1. An internal feedforward capacitor of about 25pF is put between this pin and FB1 pin.
FB1	5	Feedback pin for output1. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output1 voltage: $V_{OUT1}=0.6V\times(1+R_{H1}/R_{L1})$
LX1	6	Inductor pin for output1. Connect this pin to the switching node of inductor.
EN1	7	Enable pin for output1.Do not float this pin.
GND	8, paddle	Ground.
EN2	9	Enable pin for output2. Do not float this pin.
LX2	10	Inductor pin for output2. Connect this pin to the switching node of inductor.

Absolute Maximum Ratings (Note 1)

All pins -- -0.3V to 6.5V
Power Dissipation, P_D @ T_A = 25°C DFN3X3 --- 3.3W
Package Thermal Resistance (Note 2)
θ_{JA} -- 38°C/W
θ_{JC} -- 8°C/W
Junction Temperature Range --- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) --- 260°C
Storage Temperature Range -- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage -- 2.5V to 5.5V
Junction Temperature Range -- -40°C to 125°C
Ambient Temperature Range -- -40°C to 85°C

Electrical Characteristics

(V_{IN}= 3.6V, V_{OUT1}=V_{OUT2}=1.8V, L_1=L_2=2.2µH, C_{OUT1}=C_{OUT2}=10µF, T_A = 25°C unless otherwise specified)

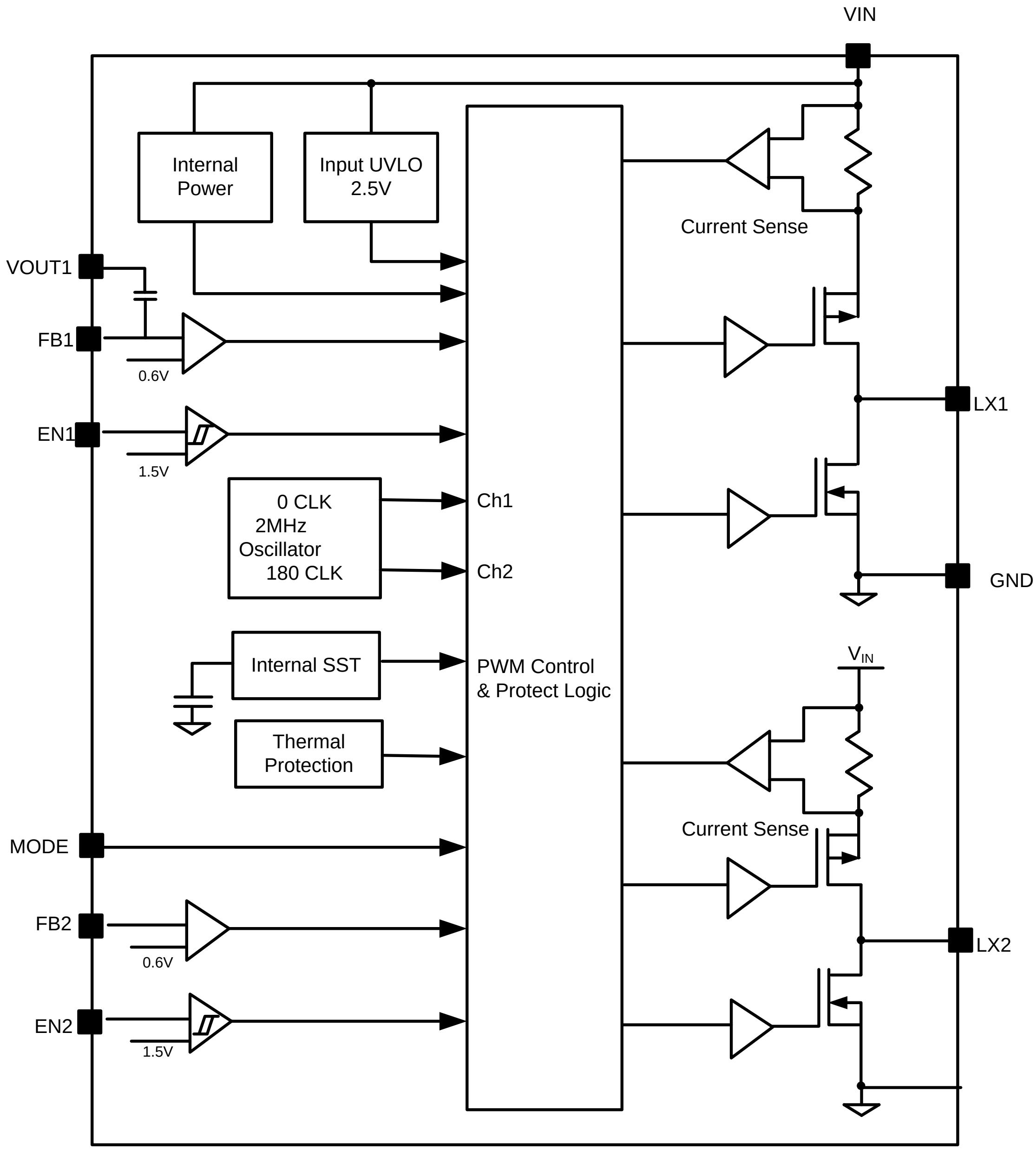
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Shutdown Current	I_{SHDN}	EN1=EN2=0			1	µA
Quiescent Current	I_Q	EN1=1 or EN2=1, MODE=0, I_{OUT1}= I_{OUT1}=0, no switching			25	µA
		EN1=1 and EN2=1, MODE=0, I_{OUT1}= I_{OUT1}=0, no switching			35	µA
		EN1=1 or EN2=1, MODE=0, I_{OUT1}= I_{OUT1}=0, switching		23		µA
		EN1=1 or EN2=1, MODE=1, I_{OUT1}= I_{OUT1}=0, switching		10		mA
Input UVLO Threshold	V_{UVLO1}				2.5	V
UVLO Hysteresis	V_{HYS1}			0.15		V
MODE Rising Threshold	V_{MODEH}		1.2			V
MODE Falling Threshold	V_{MODEL}				0.4	V
MODE Input Current	I_{MODE}			0.01	1.0	µA
Oscillator Frequency	F_{OSC}	I_{OUT1} = 0.1A, I_{OUT2} = 0.1A		2		MHz
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C
Feedback Reference Voltage	V_{REF}		0.594	0.6	0.606	V
PFET R_{ON}	$R_{DS(ON),P1}$ $R_{DS(ON),P2}$			0.22		Ω
NFET R_{ON}	$R_{DS(ON),N1}$ $R_{DS(ON),N2}$			0.18		Ω
PFET Current Limit	I_{LIM1}, I_{LIM2}		1.4			A
EN Rising Threshold	V_{ENH1},V_{ENH2}		1.2			V
EN Falling Threshold	V_{ENL1}, V_{ENL2}				0.4	V
Internal Soft Start Time	T_{SS1}, T_{SS2}			1000		µs

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via bottom layer ground plane

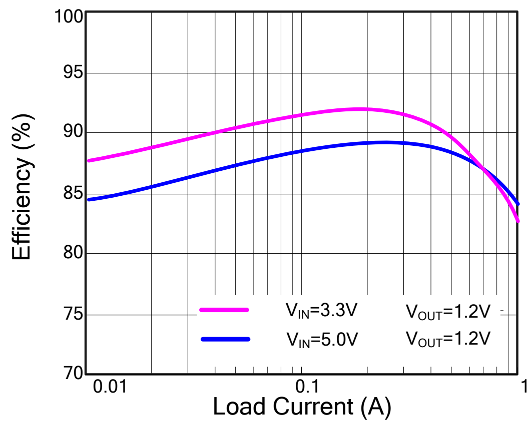
Note 3: The device is not guaranteed to function outside its operating conditions.

Function Block

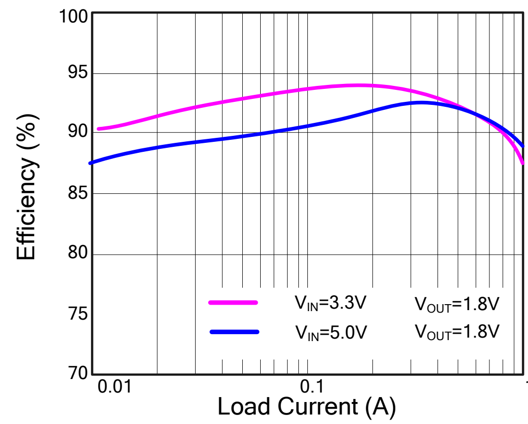


Typical Performance Characteristics

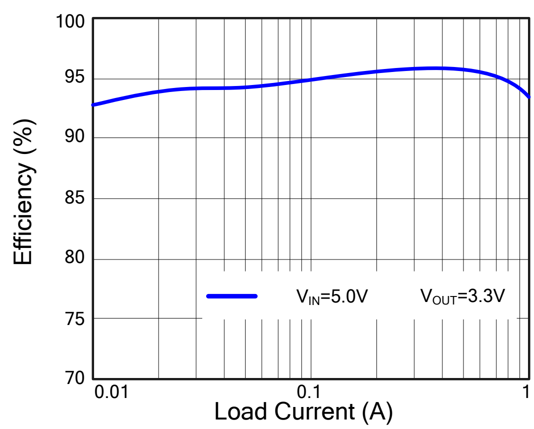
Efficiency vs. Load Current



Efficiency vs. Load Current

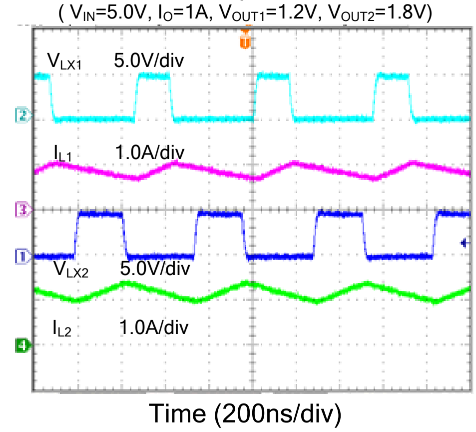


Efficiency vs. Load Current



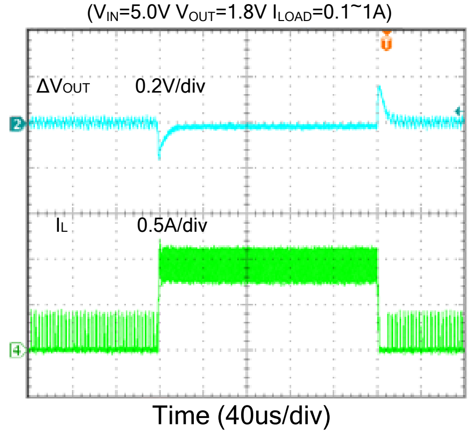
Steady State

(V_{IN}=5.0V, I_O=1A, V_{OUT1}=1.2V, V_{OUT2}=1.8V)



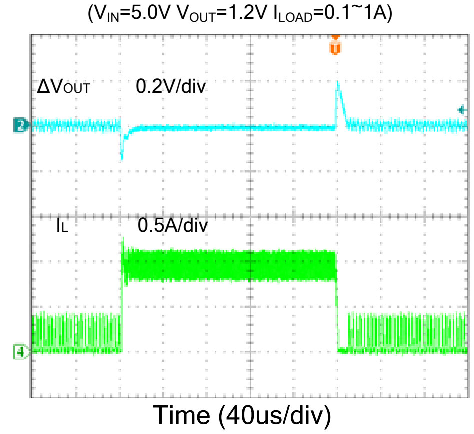
Load Transient

(V_{IN}=5.0V V_{OUT}=1.8V I_{LOAD}=0.1~1A)



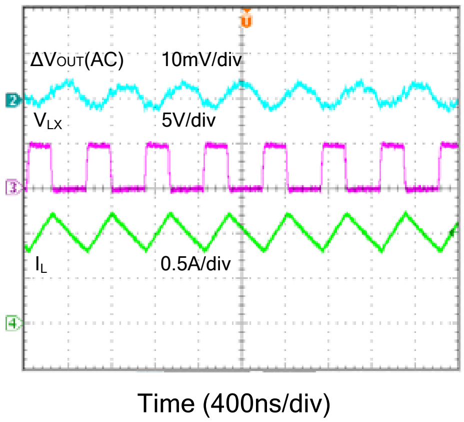
Load Transient

(V_{IN}=5.0V V_{OUT}=1.2V I_{LOAD}=0.1~1A)



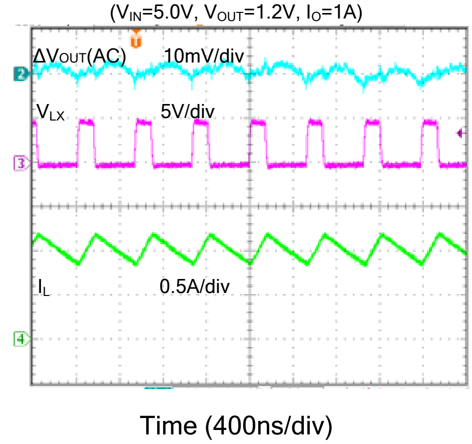
Output Ripple

(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=1A)



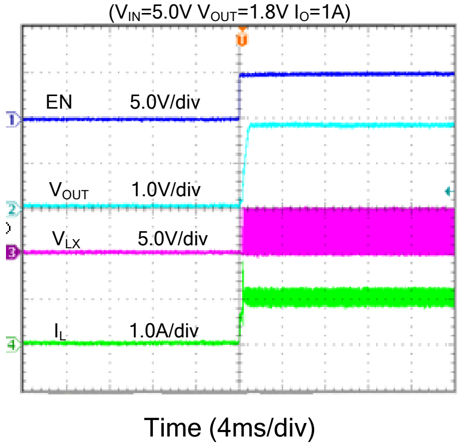
Output Ripple

(V_{IN}=5.0V, V_{OUT}=1.2V, I_O=1A)



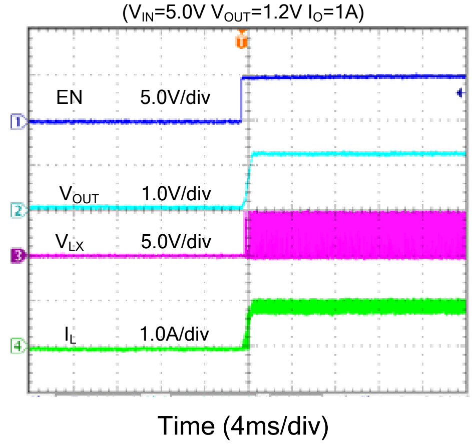
Startup from Enable

(V_{IN}=5.0V V_{OUT}=1.8V I_O=1A)



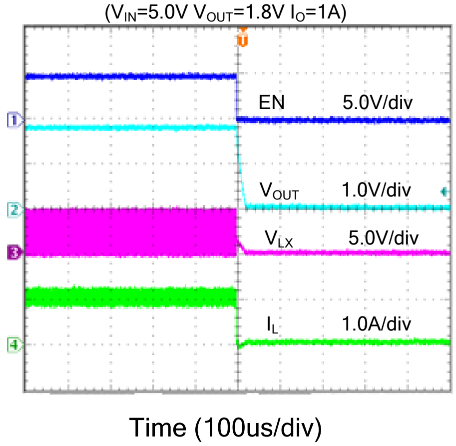
Startup from Enable

(V_{IN}=5.0V V_{OUT}=1.2V I_O=1A)



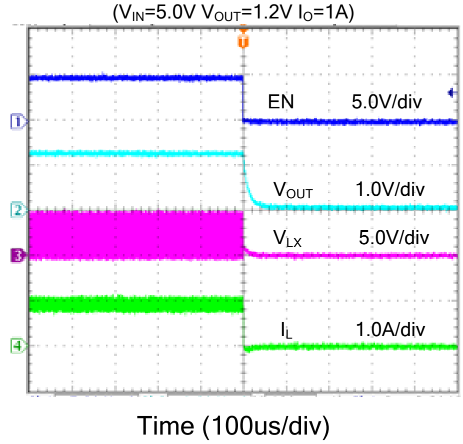
Shutdown from Enable

(V_{IN}=5.0V V_{OUT}=1.8V I_O=1A)



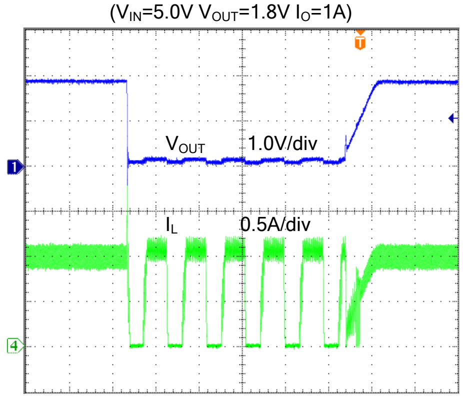
Shutdown from Enable

(V_{IN}=5.0V V_{OUT}=1.2V I_O=1A)



Short Protect

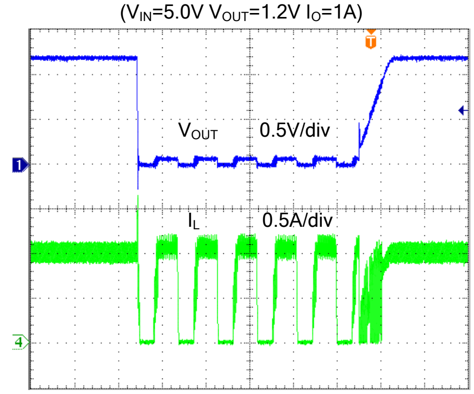
(V_{IN}=5.0V V_{OUT}=1.8V I_O=1A)



Time (1ms/div)

Short Protect

(V_{IN}=5.0V V_{OUT}=1.2V I_O=1A)



Time (1ms/div)

Operation

SY20313A is a high efficiency dual synchronous step down regulator IC that integrates the PWM control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low $R_{DS(ON)}$ power switches and proprietary PWM control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

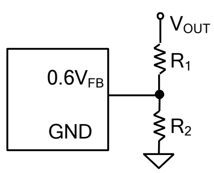
Applications Information

Because of the high integration in the SY20313A IC, only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors R need to be selected for the targeted applications specifications.

Feedback resistor dividers R1 and R2:

Choose R1 (R3) and R2 (R4) to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 (R3) and R2 (R4). A value of between 10k and 1M is highly recommended for both resistors. If R1 (R3) =100k is chosen, then R2 (R4) can be calculated to be:

$$R_2 = \frac{0.6V \times R_1}{(V_{OUT} - 0.6V)}$$



Input capacitor C_{IN}:

This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

This formula has a maximum at $V_{IN}=2V_{OUT}$ condition, where $I_{CIN\_RMS}=I_{OUT}/2$. This simple worst-case condition is commonly used for DC/DC design.

With the maximum load current at 1.0A. A typical X5R or better grade ceramic capacitor with 6.3V rating and greater than 22uF capacitance can handle this ripple current well. To minimize the potential noise problem, ceramic capacitor should be placed really close to the V_{IN} and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and V_{IN}/GND pins.

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6.3V rating and greater than 22uF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{40\% \times F_{SW} \times I_{OUT,MAX}}$$

Where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY20313A regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<30mohm to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY20313A shutdown current drops to about 0.1uA. Driving the EN pin high (>1.2V) will turn on the IC again.

Soft-start

The SY20313A has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during IC start-up. The typical soft-start time is 1ms.

Load Transient Considerations:

The SY20313A regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 10pF ceramic cap in parallel with R3 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

Layout Design:

The layout design of SY20313A regulator is relatively simple.

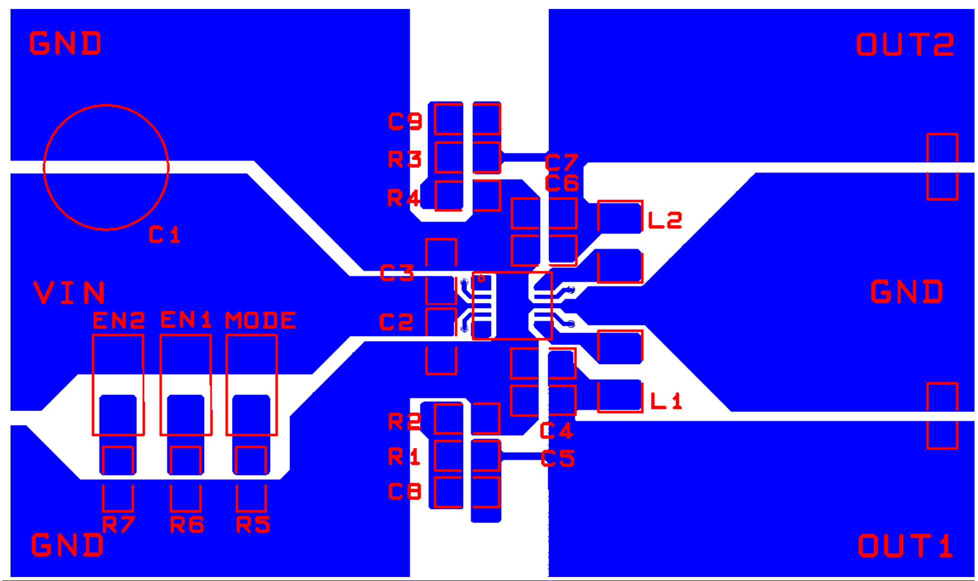
1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space is allowed, a ground plane is highly desirable.

2) Input cap C2 and C3 must be close to Pins V_{IN} and GND. The loop area formed by input cap, V_{IN}, GND must be minimized.

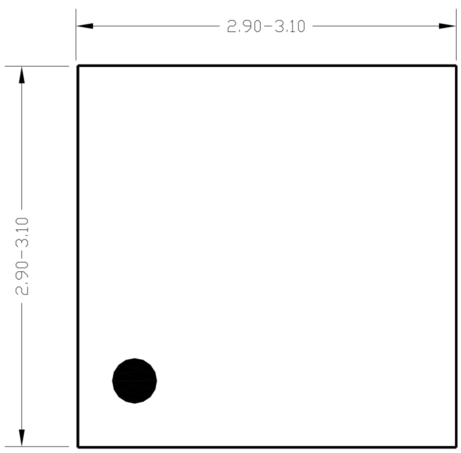
3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the V_{IN} pin is connected directly to a power source such as a LiIon battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

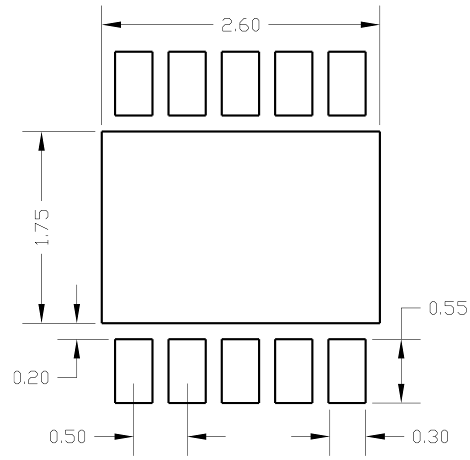
PCB Layout Guideline



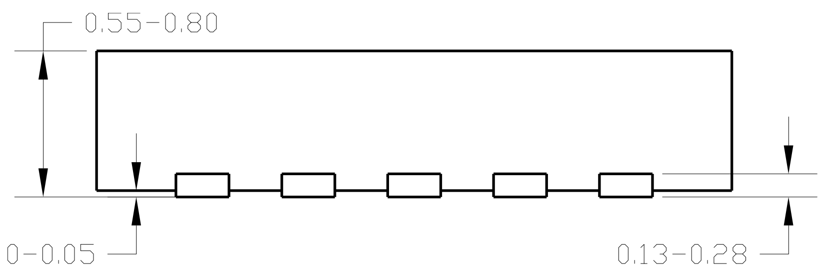
DFN3x3-10 Package outline



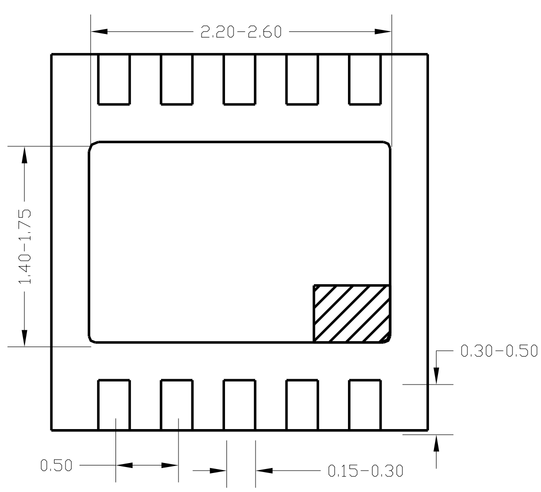
Top View

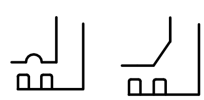


PCB layout (recommended)



Side View





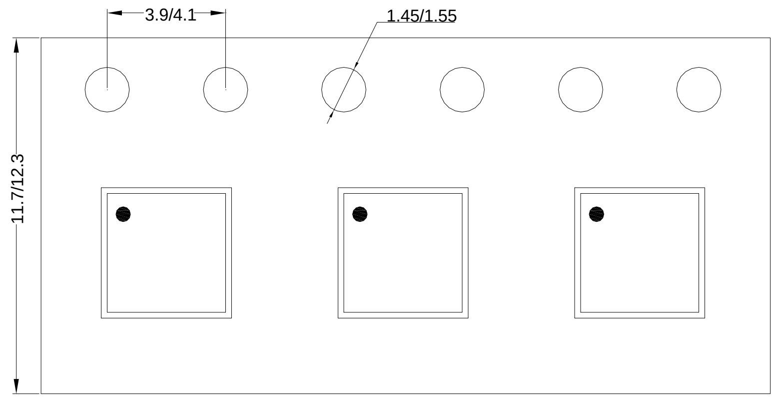
Detail A
Pin1 identifier: two options

Bottom View

Notes: All dimensions are in millimeters and exclude mold flash & metal burr.

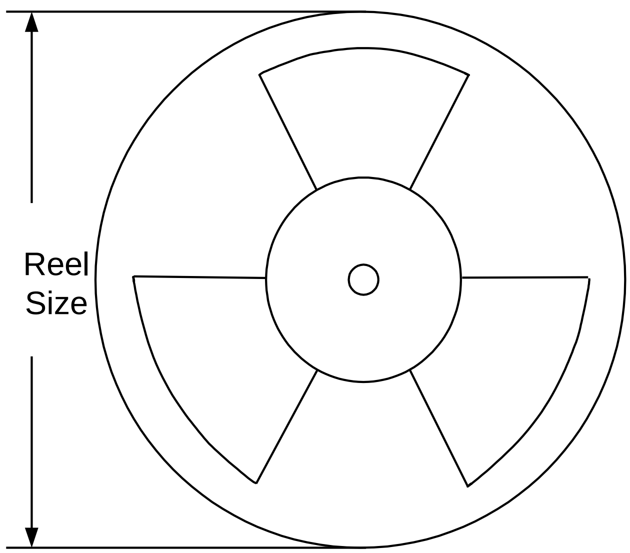
Taping & Reel Specification

1. DFN3x3-10 taping orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3x3	10	8	13"	400	400	5000

3. Others: NA

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