SY20341B

High Efficiency 2MHz, Dual 1.0A Synchronous Step Down Regulator

General Description

The SY20341B is a dual output, high efficiency 2MHz synchronous step down DC/DC regulator capable of delivering up to 1.0A for each output channel. The SY20341B operates over a wide input voltage range from 2.3V to 5.5V and integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Ordering Information

SY20341 □(□,□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20341BSAC	DFN2×1.5-8	--

Features

- 2.3V to 5.5V Input Voltage
- 2MHz Switching Frequency
- 180° Out of Phase Operation
- Output Current: 1.0A for Each Channel
- Low Quiescent Current: Typical 45μA for Both Channels
- Low $R_{DS(ON)}$ for Internal Switches (PFET/NFET): 125mΩ/100mΩ
- Internal Soft-start
- 100% Dropout Operation
- RoHS Compliant and Halogen Free
- Compact Package: DFN2x1.5-8

Applications

- SSD
- Cell Phones
- Digital Cameras
- PDAs
- Portable Media Players

Typical Applications

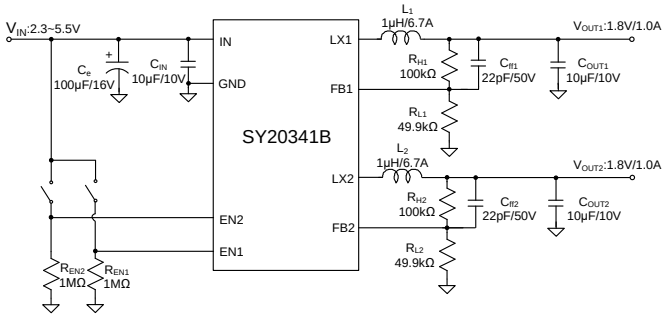


Figure1. Schematic Diagram

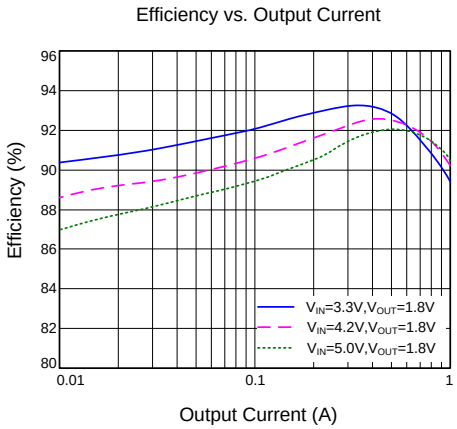
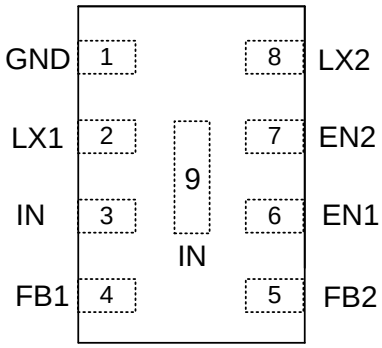


Figure2. Efficiency vs. Output Current

Pinout (top view)



(DFN2x1.5-8)

Top Mark: **Xd*xyz* for SY20341BSAC (**device code: Xd, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
GND	1	Ground pin.
LX1	2	Inductor pin for output1. Connect this pin to the switching node of the inductor.
IN	3	Power input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.
FB1	4	Feedback pin for output1. Connect this pin to the center point of the output resistor divider (as shown in figure 1) to program the output1 voltage: $V_{OUT1}=0.6V\times(1+R_{H1}/R_{L1})$
FB2	5	Feedback pin for output2. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output2 voltage: $V_{OUT2}=0.6V\times(1+R_{H2}/R_{L2})$
EN1	6	Enable pin for output1. Do not leave it floating.
EN2	7	Enable pin for output2. Do not leave it floating.
LX2	8	Inductor pin for output2. Connect this pin to the switching node of the inductor.
IN	9	Power input pin. Connect this pin to the IN pin. Do not leave it floating.

Block Diagram

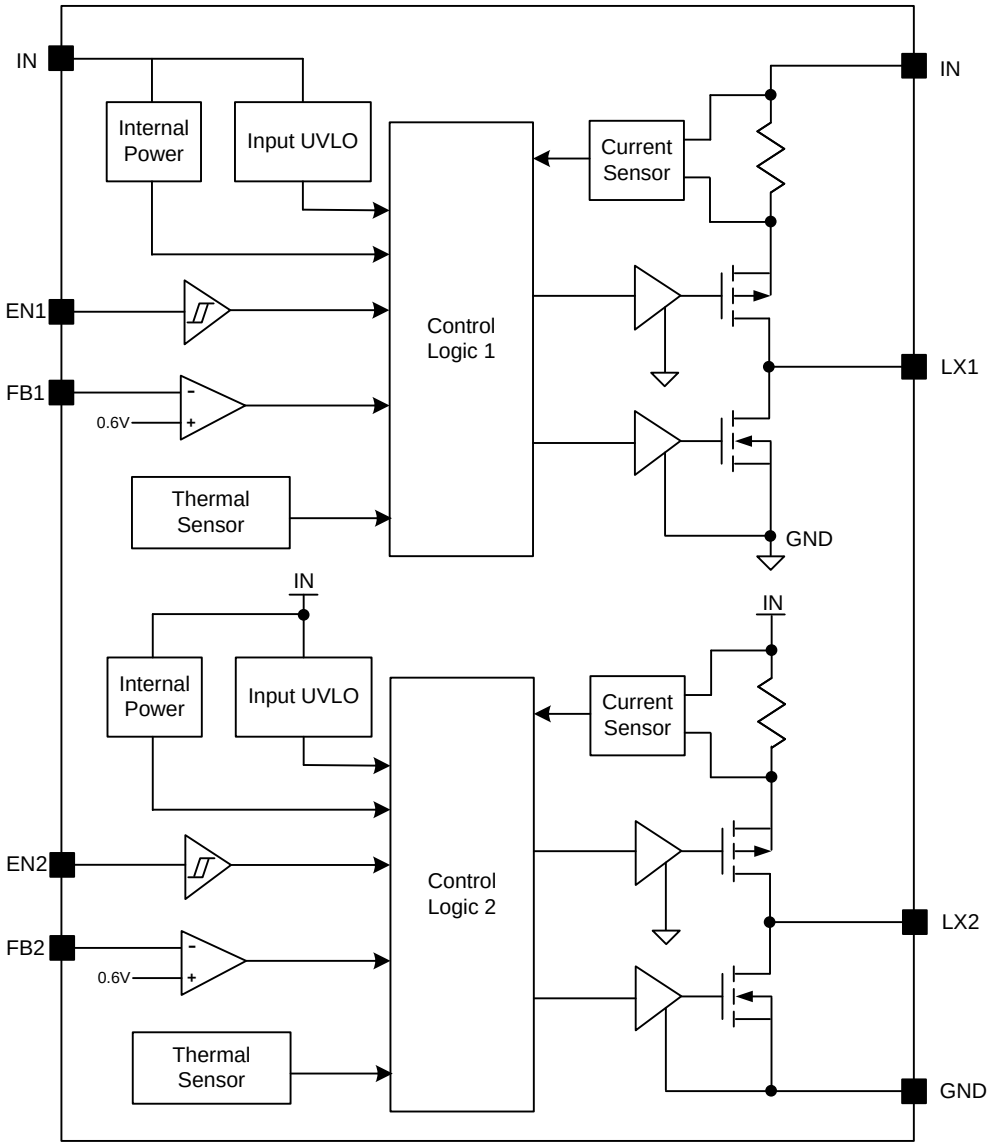


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

All Pins ---------- 6V
LX Voltage ---------- -0.3V (*1) to 6V (*2)
Power Dissipation, P_D @ T_A = 25°C, DFN2×1.5-8---------- 1.2W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 80°C/W
θ_{JC} ---------- 15°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
(*1) LX Voltage Tested Down to -3V<40ns
(*2) LX Voltage Tested Up to +7V<40ns

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.3V to 5.5V
Enable, FB Voltage ---------- V_{IN}+0.3V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN}= 5V, V_{OUT1}=V_{OUT2}=2.5V, L_1=L_2=1.0μH, C_{OUT1}=C_{OUT2}=10μF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.3		5.5	V
Input UVLO Rising Threshold	$V_{UVLO,RISING}$				2.3	V
Input UVLO Falling Threshold	$V_{UVLO,FALLING}$				2.0	V
Quiescent Current	I_Q	EN1=1 or EN2=1, I_{OUT1}=I_{OUT2}=0, no switching		35		μA
		EN1=1 and EN2=1, I_{OUT1}=I_{OUT2}=0, no switching		45		μA
Shutdown Current	I_{SHDN}	V_{EN1}=V_{EN2}=0V		0.1	1	μA
Feedback Reference Voltage	V_{REF1}, V_{REF2}		588	600	612	mV
Top FET R_{ON}	$R_{DS(ON),TOP1}$ $R_{DS(ON),TOP2}$			125		mΩ
Bottom FET R_{ON}	$R_{DS(ON),BOT1}$ $R_{DS(ON),BOT2}$			100		mΩ
EN1,EN2 Input Voltage High	$V_{EN1,H}$, $V_{EN2,H}$		1.2			V
EN1,EN2 Input Voltage Low	$V_{EN1,L}$, $V_{EN2,L}$				0.4	V
Soft-start Time	t_{SS1}, t_{SS2}			1.0		ms
Switching Frequency	F_{SW}	I_{OUT1}=0.5A, I_{OUT2}=0.5A		2.0		MHz
CH1 Top FET Current Limit	$I_{LMT,TOP1}$		1.3			A
CH2 Top FET Current Limit	$I_{LMT,TOP2}$		1.3			A
Thermal Shutdown Temperature	T_{SD}			150		˚C
Thermal Shutdown Hysteresis	T_{HYS}			20		˚C

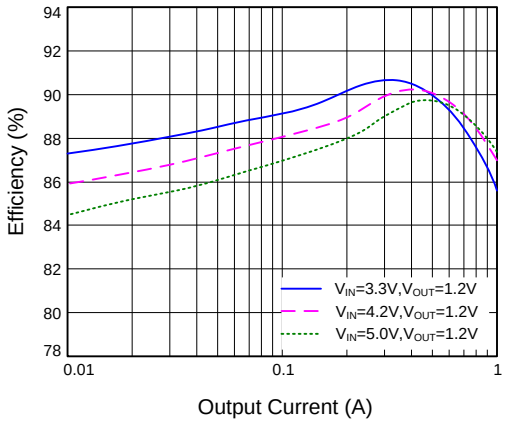
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} of SY20341BSAC is measured in the natural convection at T_A = 25°C on 2OZ two-layer Silergy evaluation board. Paddle of QFN2x1.5-8 package is the case position for SY20341BSAC θ_{JC} measurement.

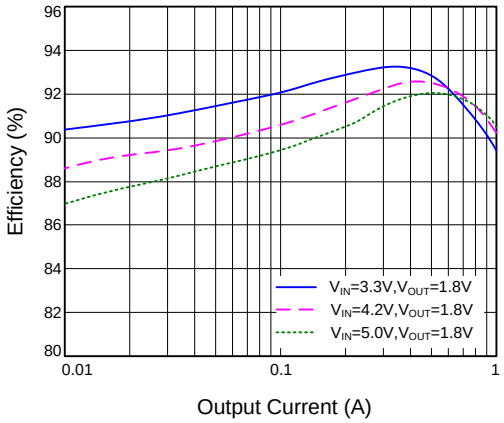
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

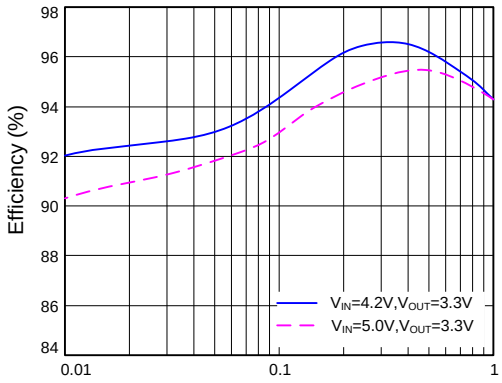
Efficiency vs. Output Current



Efficiency vs. Output Current

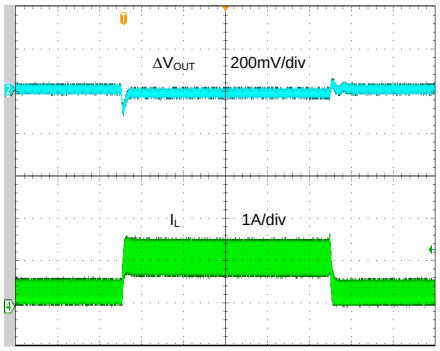


Efficiency vs. Output Current



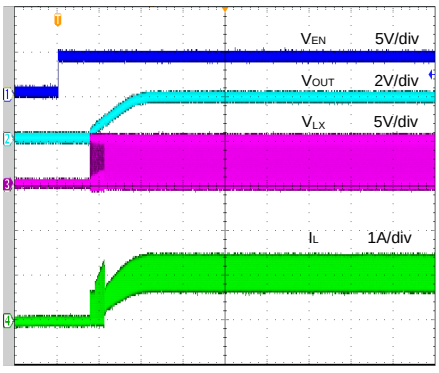
Load Transient

(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0.1~1A)



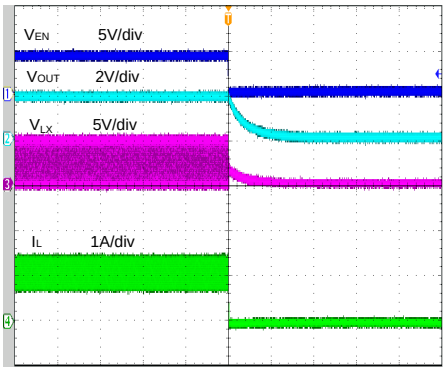
Startup from Enable

(V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=1.0A)



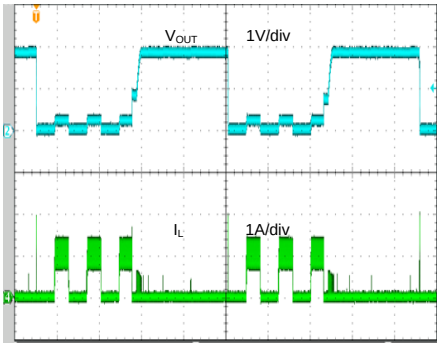
Shutdown from Enable

(V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=1.0A)



Short Circuit Protection

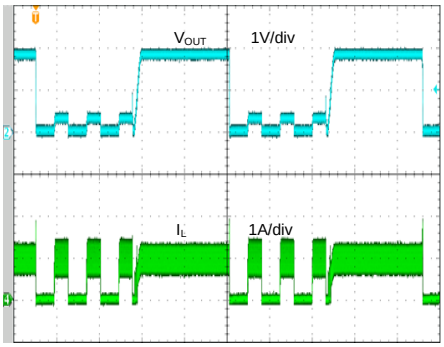
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A ~ short)



Time (4ms/div)

Short Circuit Protection

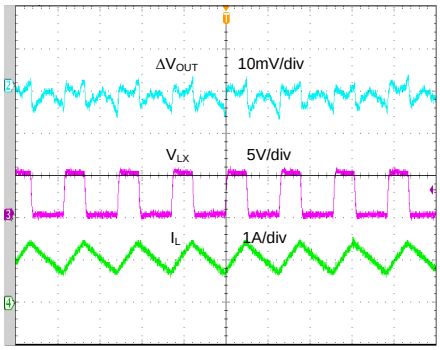
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=1A ~ short)



Time (4ms/div)

Output Ripple

(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=1.0A)



Time (400ns/div)

Operation

The SY20341B is a dual output, high efficiency 2MHz synchronous step down DC/DC regulator capable of delivering up to 1.0A for each output channel. The SY20341B operates over a wide input voltage range from 2.3V to 5.5V and integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Applications Information

Because of the high integration in the SY20341B, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L and the feedback resistors (R_H and R_L) need to be selected for the targeted applications.

Feedback Resistor Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_H and R_L. A value of between 100kΩ and 1MΩ is highly recommended for both resistors. If R_H=120kΩ is chosen, then R_L can be calculated to be:

$$R_L = \frac{0.6V \times R_H}{(V_{OUT}-0.6V)}$$

Input Capacitor C_{IN}

This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

This formula has a maximum at V_{IN}=2V_{OUT} condition, where I_{CIN_RMS}=I_{OUT}/2. This simple worst-case condition is commonly used for DC/DC design.

With the maximum load current of 1.0A, a typical X5R or a better grade ceramic capacitor with 10V rating and larger than 10µF capacitance can handle this ripple current well. To minimize the potential noise problem, a ceramic capacitor should be placed really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} and V_{IN}/GND pins.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X7R or better grade ceramic capacitor with 6V rating and larger than 10µF capacitance.

Output Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY20341B is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load condition.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

Load Transient Considerations:

The SY20341B integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF ceramic capacitor in parallel with R_H may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

Layout Design:

The layout design of SY20341B regulator is relatively simple. For the best efficiency and minimum noise problems, the following components should be placed close to the IC: C_{IN}, L, R_H and R_L.

1) It is desirable to maximize the PCB copper area connected to GND pin to achieve the best thermal and noise performance. If the board

space allowed, a ground plane is highly desirable. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

2) Input capacitor must be close to the IN and GND pins. The loop area formed by input capacitor，IN and GND must be minimized.

3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem. For the smallest loop area of C_{IN}, IN and GND, the LX pin copper can pour area on internal or bottom layer.

4) The components R_H and R_L and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

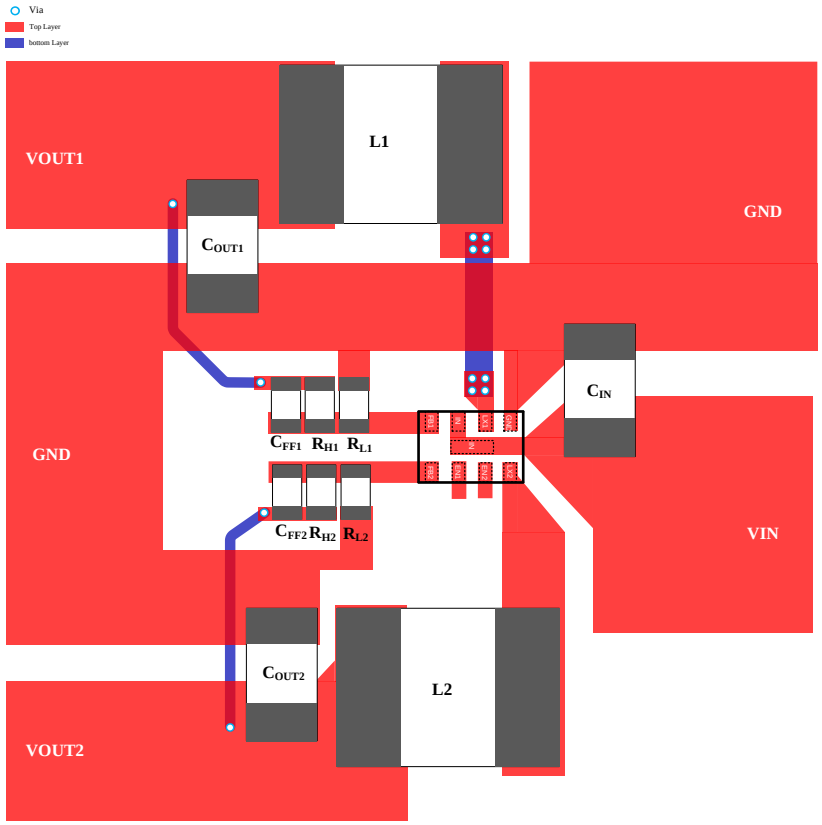
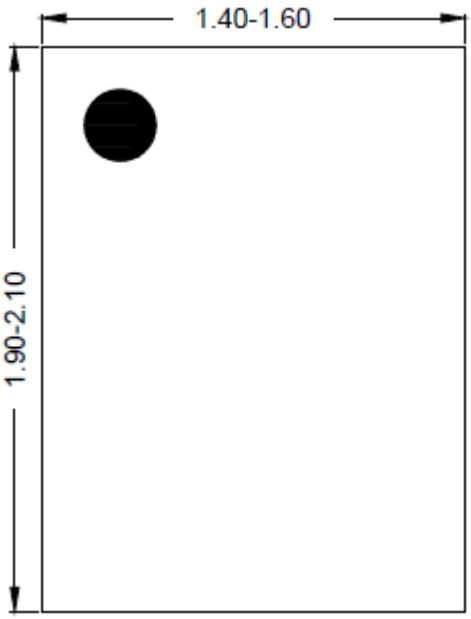
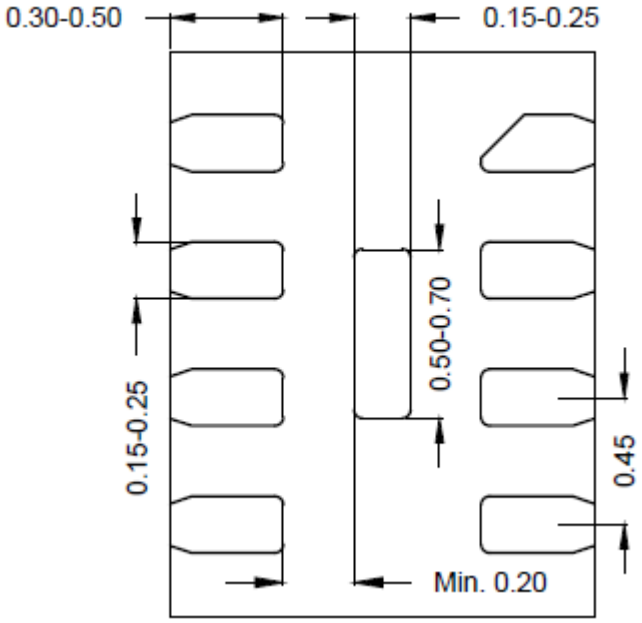


Figure4. PCB Layout Suggestion

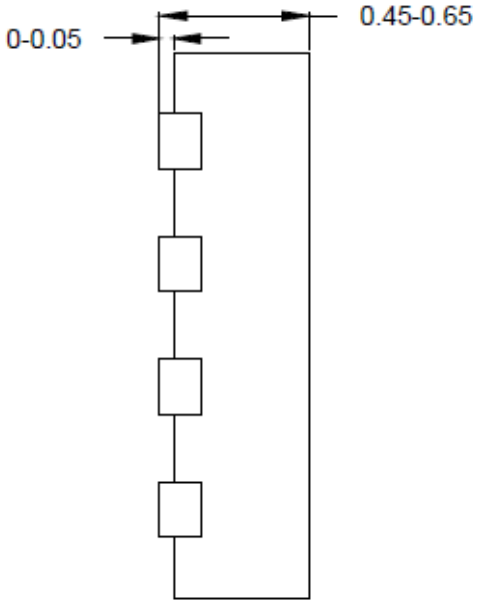
DFN2×1.5-8 Package Outline Drawing



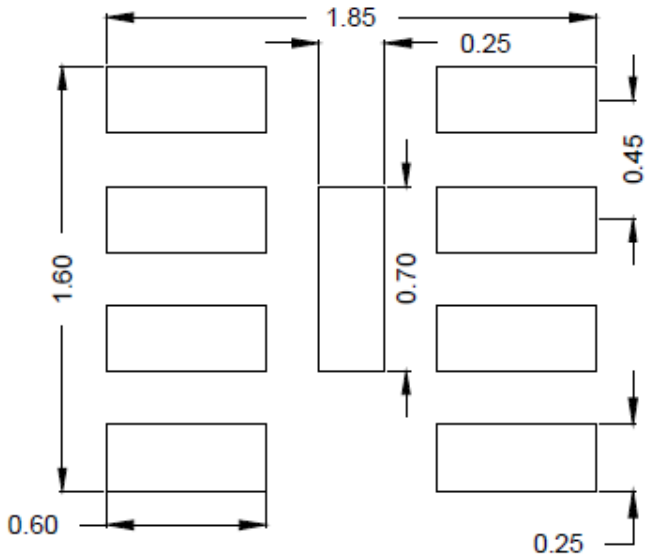
Top view



Bottom view



Side view



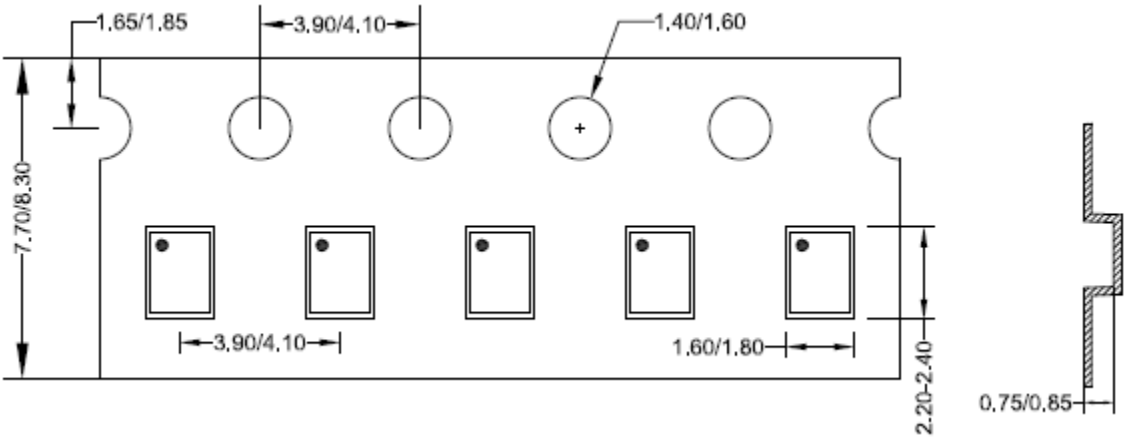
Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr**

Taping & Reel Specification

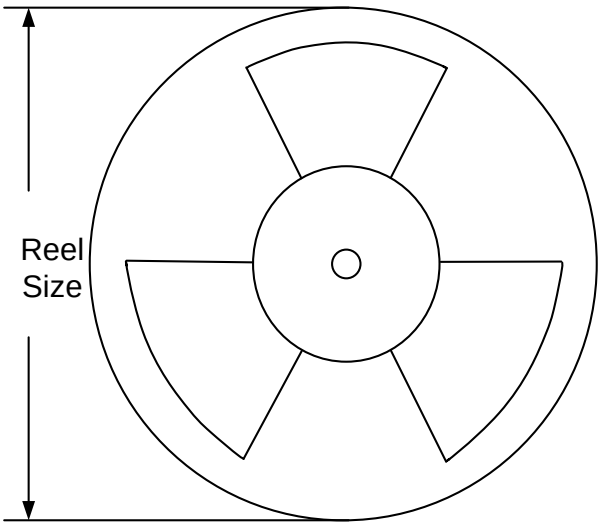
1. Taping orientation

DFN2x1.5



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2x1.5	8	4	7	400	160	3000

3. Others: NA

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com