SY87004

5.5V, High Efficiency Synchronous Boost Regulator with Bypass Mode

General Description

The SY87004 is a high efficiency, synchronous boost converter with bypass mode. The device is designed to operate in bypass mode by providing a low resistance path between the output and input when the input voltage is higher than the target voltage. It transition automatically into boost mode when the input voltage is lower than the desired output.

The SY87004 operates over a wide input voltage range from 1.9V to 5.5V and supports up to 6A maximum load current in bypass mode.

Overtemperature, overcurrent, as well as output undervoltage and input overvoltage protections are provided reliable operation.

The device operation and parameters can be configured using the I²C bus.

The SY87004 is available in a compact CSP 1.65mm×1.65mm-16 bump package.

Features

- Input Voltage Range: 1.9V to 5.5V
- Program Output Range: 2.85V to 5.5V
- Maximum Bypass Continuous Load Current :6A
- Up to 95% Efficiency
- Supports 0.9V signaling for SCL/SDA/EN Pins
- Programmable Valley Inductor Current Limit and Output Voltage
- I²C Configurable Auto Bypass Operation And Forced Bypass Mode
- I²C configurable FCCM and PFM Modes
- Low Operating Quiescent Current
- Shutdown Current 0.1 µA (Typ.)
- Load Disconnect During Shutdown
- Compact Package CSP1.65×1.65-16

Applications

- Single-Cell Li-Ion, LiFePO4 Smart-Phones or Tablet PCs
- 2.5G/3G/4G Data Cards

Typical Application

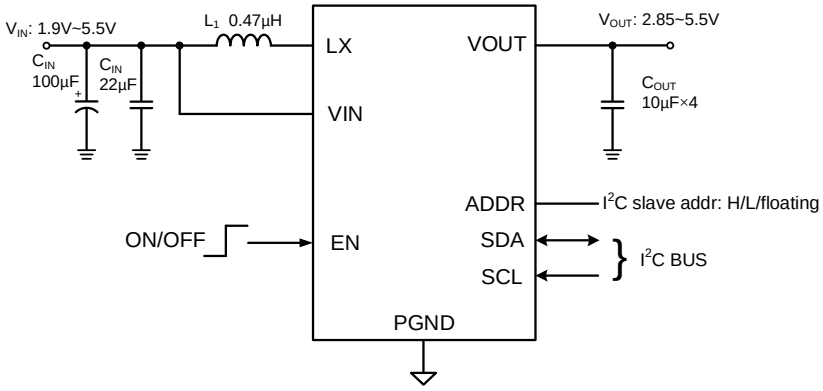


Figure 1. Schematic Diagram

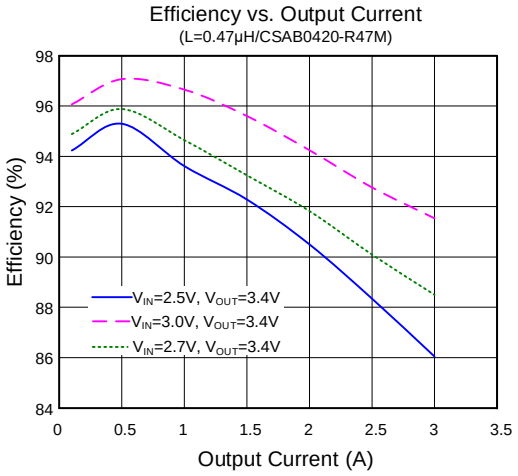


Figure 2. Efficiency vs. Output Current

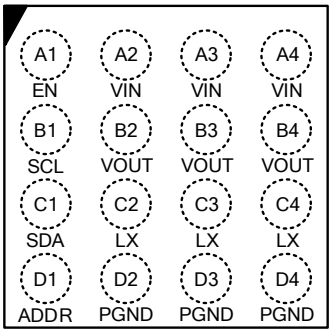
Ordering Information

Ordering Part Number	Package Type	Top Mark
SY87004WUS	**CSP1.65×1.65-16** RoHS-Compliant, Halogen-Free	**HFCxyz**

Device code: HFC

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Description

Pin Name	Pin Number	Pin Description
EN	A1	Enable pin. Active high, do not leave floating.
VIN	A2, A3, A4	Input pin. Decouple this pin to the GND with at least a 4.7μF ceramic capacitor.
SCL	B1	I²C interface serial clock line. Logic level input.
VOUT	B2, B3, B4	Output voltage pin. Decouple this pin to PGND with at least 4x10μF ceramic capacitors.
SDA	C1	I²C interface serial data line. Logic level input/output.
LX	C2, C3, C4	Switching node pin. Connect these pins to the switching node of inductor.
ADDR	D1	I²C slave address pin. This pin can be pulled high, low or left floating to change the peripheral address.
PGND	D2, D3, D4	Power ground.

Function Block

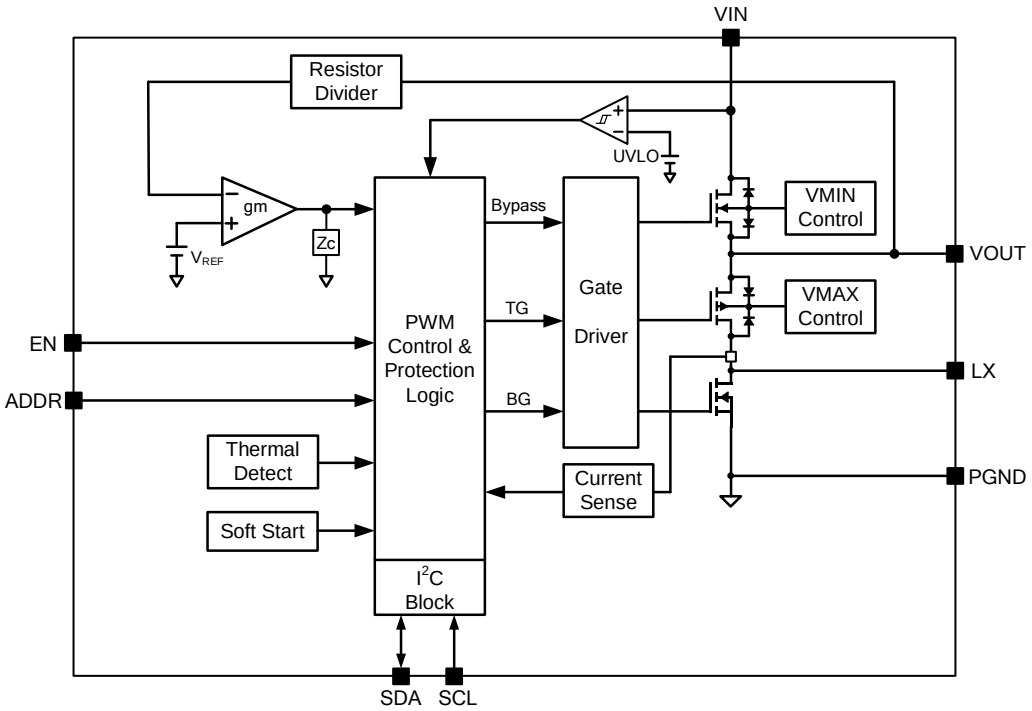


Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)		Min	Max	Unit
VIN		-0.3	6	V
SCL, SDA, ADDR		-0.3	6	
EN, VOUT, LX		-0.3	6	
Lead Temperature (Soldering, 10 sec.)			260	°C
Junction Temperature, Operating		-40	150	
Storage Temperature		-65	150	
V_{ESD} Electrostatic Discharge	Human Body Model(HBM)		±2000	V
	Charged Device Model(CDM)		±500	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	50	°C/W
θ_{JC} Junction-to-case Thermal Resistance	1	
P_D Power Dissipation T_A=25°C	2	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VIN	1.9	5.5	V
VOUT	2.85	5.5	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 2.7V, V_{OUT}=3.4V, schematic of Figure 1, T_J=-40°C to +85°C. Typical values are at T_J=25°C, unless otherwise specified. (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range		V_{IN}		1.9		5.5	V
Input UVLO Threshold		V_{UVLO}			1.65	1.75	V
Input UVLO Hysteresis		V_{HYS}			0.1		V
Output Voltage Range		V_{OUT}		2.85		5.5	V
Quiescent Current	V_{IN} (Boost)	I_Q	I_{LOAD}= 0A, V_{IN}= V_{EN}= 2.7V, V_{OUT}=3.6V, Device not switching		3	5	µA
	V_{OUT} (Boost)				24	33	µA
	V_{IN}(Auto Bypass)		V_{EN}=1.9V, V_{IN}=3.6V		33	47	µA
	V_{IN}(Forced Bypass)				18	28	µA
	V_{IN}(low I_Q Bypass)				13	20	µA
Shutdown Current		I_{SHDN}	V_{EN}=0V,V_{IN}=3.6V		0.1	3	µA
EN Input Voltage High		V_{IH}		0.9			V
EN Input Voltage Low		V_{IL}				0.4	V
EN Leakage Current		$I_{EN,LK}$	V_{EN}=3.3V	-1		1	uA
Output Voltage Accuracy		V_{OUT_AC}	I_{LOAD}=1A, 0x02[5:0]='001011'	-1.5		1.5	%
Output Discharge Resistance		R_{DIS}			75	110	Ω
Low Side Main FET R_{ON}		$R_{DS(ON)1}$			17	30	mΩ
Synchronous FET R_{ON}		$R_{DS(ON)2}$			17	28	mΩ
Bypass FET R_{ON}		$R_{DS(ON)3}$			14	22	mΩ
Main FET Leakage Current		I_{LKG_LS}	V_{EN}=0V, V_{IN}=V_{OUT}=V_{SW}=3.5V		0.1	1	µA
Synchronous FET Leakage Current		I_{LKG_HS}	V_{EN}=0V, V_{IN}=V_{OUT}=4.5V, V_{SW}=0V		0.1	1.5	µA
BYP FET Leakage Current		I_{LKG_BYP}	V_{EN}=0V, V_{IN}=3.5V, V_{OUT}=0V		0.1	2	µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Min ON Time	$t_{ON,MIN}$	**(Note 5)**		60		ns
Min OFF Time	$t_{OFF,MIN}$			160		ns
Switching Frequency	f_{SW}	I_{OUT}=1A	1.9	2.1	2.3	MHz
Boost Mode Valley Current Limit	$I_{LMT,Valley}$	0x03[3:0]='0110'(default)	5.5	7	8.5	A
Boost Mode Negative Current Limit	$I_{LMT,Negative}$			-2		A
Pass Through Mode Current Limit	$I_{LMT,BYP}$	V_{IN}=3.6V		9		A
Input Over Voltage Threshold	$V_{OVP,IN}$			5.8		V
Input Over Voltage Hysteresis	$V_{OVP,HYS}$			0.3		V
Linear Charge Current Limit I	$I_{CHARGE1}$	V_{IN}-V_{OUT}＞300mV		1		A
Linear Charge Current Limit II	$I_{CHARGE2}$			2		A
Thermal Shutdown Temperature	T_{SD}			150		˚C
Thermal Shutdown Hysteresis	T_{HYS}			20		˚C
SCL, SDA Input Voltage High	V_{IH}		0.9			V
SCL, SDA Input Voltage Low	V_{IL}				0.4	V
SCL Clock Frequency	F_{SCL}		100		1000	kHz

Note 1: Stresses beyond the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A=25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

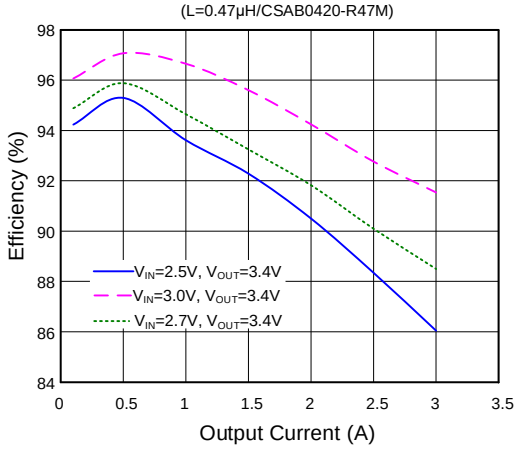
Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test , or statistical correlation.

Note 5: Guaranteed by design.

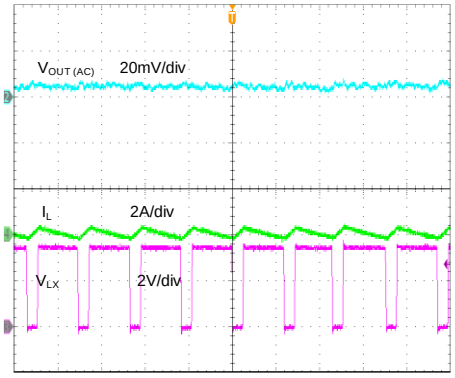
Typical Performance Characteristics

(T_A=25ºC, V_{IN}=2.7V, V_{OUT}=3.4V; L=0.47µH, unless otherwise specified.)

Efficiency vs. Output Current
(L=0.47µH/CSAB0420-R47M)

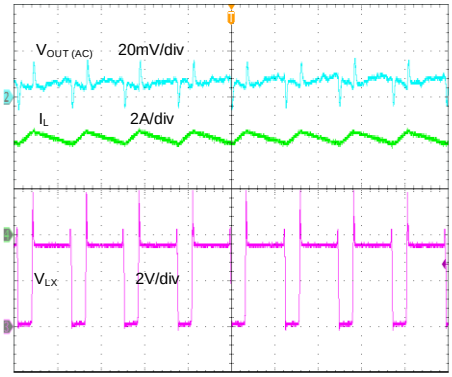


Output Ripple
(V_{IN}=2.7V, V_{OUT}=3.4V, I_{OUT}=0A, FCCM)



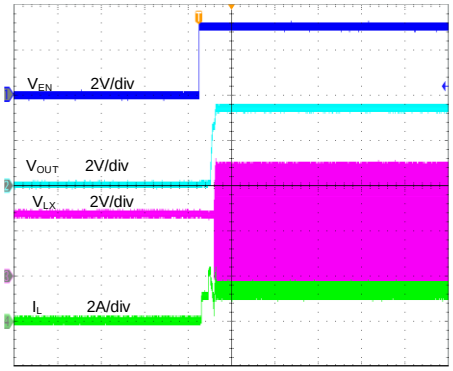
Time (400ns/div)

Output Ripple
(V_{IN}=2.7V, V_{OUT}=3.4V, I_{OUT}=3A, FCCM)



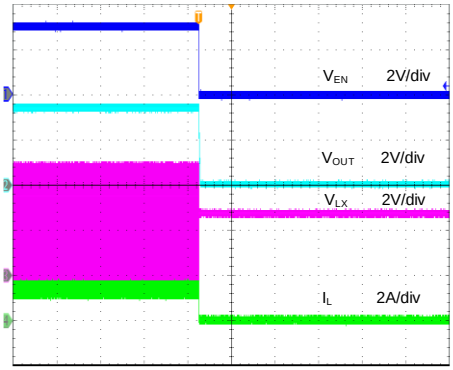
Time (400ns/div)

Startup from Enable
(V_{IN}=2.7V, V_{OUT}=3.4V, I_{OUT}=1A)



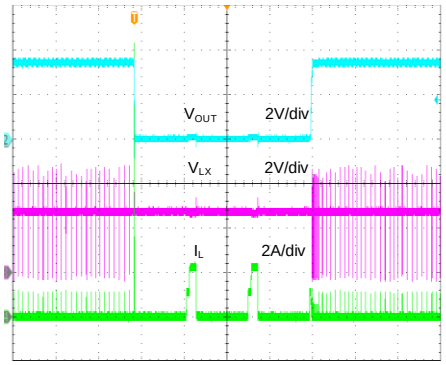
Time (4ms/div)

Shutdown from Enable
(V_{IN}=2.7V, V_{OUT}=3.4V, I_{OUT}=1A)



Time (4ms/div)

Short Circuit Protection
(V_{IN}=2.7V, V_{OUT}=3.4V, I_{OUT}=0A~short)



Time (10ms/div)

Applications Information

The SY87004 is a boost converter with adaptive contant on time control, which is designed for one-cell Li-Ion or LiFeP04 battery powered applications. It enters bypass mode when the battery is charged. The boost mode is automatically enabled when the battery voltage drops below the target voltage, so that the battery capacity can be fully utilized to provide power to blocs that require higher operating voltage.

The SY87004 operates over a wide input voltage range from 1.9V to 5.5V and integrates low $R_{DS(ON)}$ power MOSFETs.

Operating parameters including minimum output, current limit, operating mode can be configured using the I²C interface.

Input Capacitor C_{IN}

For the best performance, select a typical X5R or better grade ceramic capacitor. The component should be placed as close as possible to the VIN and PGND pins, while also minimizing the loop area formed by C_{IN} and the VIN/PGND pins. A 22µF low ESR ceramic capacitor is recommended for most applications.

Output Capacitor C_{OUT}

Both steady state ripple and transient requirements must be taken into account when selecting this capacitor. Using four X5R or better grade ceramic capacitors in parallel, with a 6.3V voltage rating and a capacitance higher than 10µF is recommended for most applications.

Boost Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{f_{SW} \times I_{OUT\_MAX} \times 40\%}$$

Where f_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

The SY87004 is tolerant to different ripple current amplitudes. Consequently, the final choice of the inductance can be slightly different than the calculated value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN} \times \eta}\right) \times I_{OUT\_MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<30mΩ to achieve a good overall efficiency.

Enable Operation

The EN pin controls SY87004 start up. The EN pin low to high transition starts the power up sequence. If the EN pin is low, the DC/DC converter will be turned off.

When EN is high, the SY87004 allows software to enable the regulator, through the DEV_EN bit.

Hardware and Software Enable control table as follows:

EN PIN	DEV_EN (0x01[6])	OUTPUT
0	x	OFF
1	0	OFF
1	1	ON

Discharge Operation

The VOUT_DISCHG bit allows SY87004 to discharge output voltage through an internal pull-down resistor. The control strategy is as follows:

VOUT_DISCHG (0x01[3])	EN PIN	DEV_EN (0x01[6])	STATUS
1	L	x	Discharge
	H	0	Discharge
0	L	x	Discharge
	H	0	No discharge

The discharge circuit is enabled when an output overvoltage condition is detected. The overvoltage threshold is 120% the target output voltage.

Start Up Operation

When V_{IN} > UVLO and EN transitions from low to high, the SY87004 initiates the startup sequence where the output voltage gradually ramps until V_{OUT} > 0.9×V_{IN}. The linear startup period includes two different states: LIN1 and LIN2. During LIN1, the current limit is set to 1A for a 800us duration. If V_{OUT} is still lower than 0.9×V_{IN} after this duration, the converter enters LIN2 state where 2A current limit is used for 1600µs. If V_{OUT} is still lower than 0.9×V_{IN} after the

LIN2 duration, the device enters fault mode. Otherwise, it will enter soft-start operation to reach the V_{OUT} setting. During the soft-start state, if the target V_{OUT} is not reached in 2ms, the device also enters fault mode.

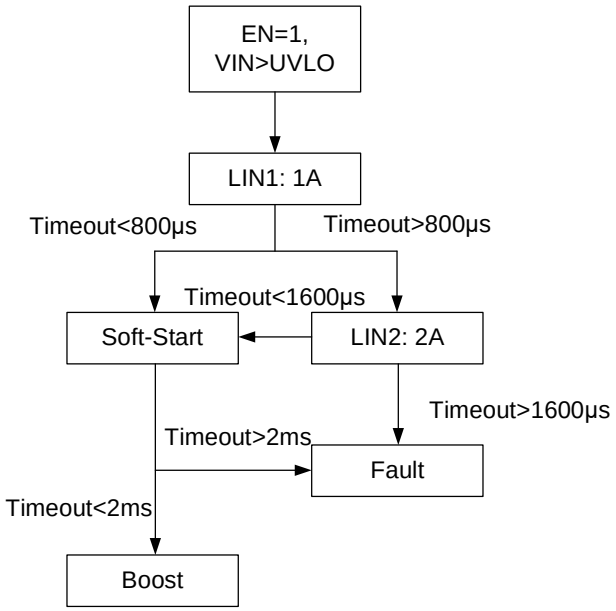


Figure4. Start Up Operation

Spread Spectrum Function

The spread spectrum function is enabled by 0x01[1] to optimize EMI performance. The operating frequency is varied ±15% centered on frequency. The modulation signal is a triangular wave with a period of 100µs. When spread spectrum is enabled , fsw ramps down 15% and back to the center frequency in 50µs, followed by a ramp up 15% and back to the center frequency in 50µs.

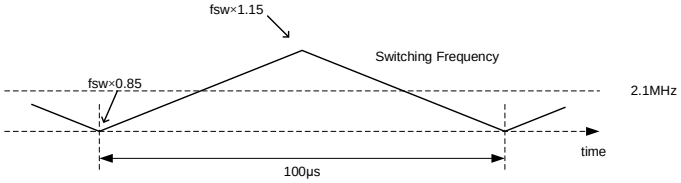


Figure5. Spread Spectrum

Eliminating the 10kHz ripple caused by the spread spectrum can be obtained by enabling a ripple cancellation feature by writing to setting bit [2] at register address 0x01.

Forced Bypass Operation

The SY87004 can operate in forced bypass mode, which can be enabled programming bits [5:4] at register address 0x01. In forced bypass mode, the output is connected to input directly, while the quiescent current is reduced.

Light Load Operation

The SY87004 can operate in burst mode during light load conditions to maintain high-efficiency. PFM operation is automatically initiated when the inductor current falls to zero. As the load decreases further the resulting switching frequency will also decrease in order to keep the output close to the target value.

Overcurrent Protection

The SY87004 provides cycle by cycle overcurrent protection and turns off the power MOSFET once the inductor valley current reaches the current setting limit configured by bits [3:0] at register address 0x03. Fault events can be detected by reading the fault flag, located at bit[1] register address 0x04.

Input Overvoltage Protection

The SY87004 includes input over voltage protection. If the input voltage exceeds $V_{OVP,IN}$ (typ. 5.8V), the device will stop switching, and trigger a fault flag. When the input voltage returns to the normal operating range, the device resumes operation.

Output Undervoltage Protection

The SY87004 includes output under voltage protection. If the output voltage drops below 88% of input voltage, the device will shutdown and trigger a fault flag.

Thermal Protection

The SY87004 includes over temperature protection circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the thermal protection threshold.

I²C Interface

Peripheral Address List

State	V_{ADDR}	Peripheral Address
1	LOW	1110101x
2	HIGH	1110110x
3	FLOAT	1110111x

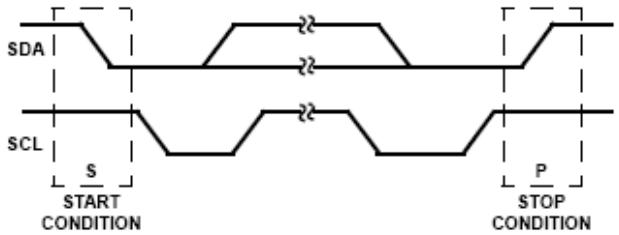
Register Memory Map

Name	Address	Description
DEVICE ID	0x00	Device ID information
CONFIG	0x01	Set several configures
VOUT	0x02	Set output voltage.
ILIMSET	0x03	Set input current valley limit and soft-start current limit.
STATUS	0x04	Device status.

The SY87004 features an I²C interface that allow a host processor to configure the operation and control the output voltage. The I²C interface supports clock speeds of up to 1MHz and uses standard I²C commands. The SY87004 always operates as a peripheral device, and it is addressed using a 7-bit slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation.

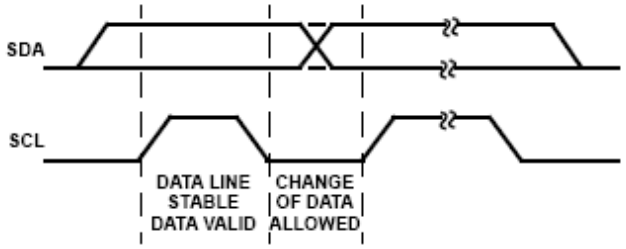
START and STOP Conditions:

The SY87004 is controlled via an I²C compatible interface. The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C controller always generates the START and STOP conditions.



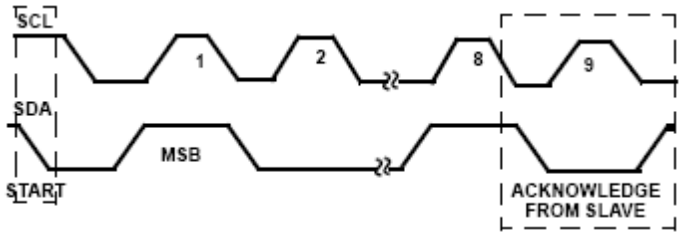
Data Validity:

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.



Acknowledge:

Each address and data transmission byte uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the controller sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the controller and the peripheral to acknowledge receipt of register addresses and data.

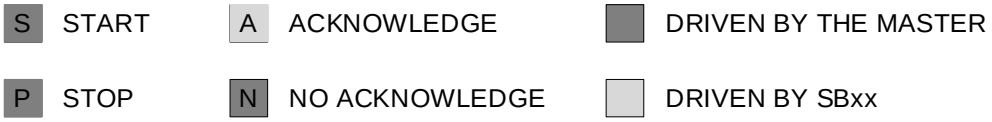


Data Transactions:

All transactions start with a control byte sent from the I²C controller device. The control byte begins with a START condition, followed by 7-bits of slave address (1110101x) for the SY87004 (this address can be set by R_{ADDR}), followed by the 8th bit, R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any peripheral devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no peripheral exists at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the SY87004 acknowledges it, the 2nd byte sent by the controller must be a register address byte. The register address byte tells the SY87004 which register the master will write to or read from. Once the SY87004 receives the register address byte, it responds with an acknowledge.

Write To A Register

Read From A Register



Register Settings

1. DEVICE ID (0x00) , the default value is 0x10.

Register Name	Bit	R/W	Default	Description
Manufacturer	7:4	R	0001	Device identity
DEV_VER	3:0	R	0000	Device version

2. CONFIG (0x01) , the default value is 0x68.

Register Name	Bit	R/W	Default	Description
RESET	7	R/W	0	Device reset bit. 0: Keep current register setting. 1: Reset to default register value. This bit returns to 0 after register reset is completed. The device operation is cycled (ON-OFF-ON), which means the converter is disabled for a short time and restarts with default parameters.
DEV_EN	6	R/W	1	Device enable bits. 0: Disable the device. 1: Device Enable.
AUTO_BYPASS	5:4	R/W	10	Device auto bypass bit. 00: Device operates in forced bypass mode with low iq. 01: Device operates in forced bypass mode (Only bypass mode). 10~11: Device operates in auto bypass mode (Auto transition between DC/DC boost and bypass).
VOUT_DISCHG	3	R/W	1	Output discharge control bit. 0: When the regulator is disabled, VOUT is not discharged. 1: When the regulator is enabled, VOUT discharges through an internal pull-down resistor.
SSFM_COMP	2	R/W	0	Spread spectrum ripple cancellation control bit. 0: Disable SSFM ripple cancellation. 1: Enable SSFM ripple cancellation.
SSFM	1	R/W	0	Spread spectrum control bit. 0: Spread spectrum modulation is disabled. 1: Spread spectrum modulation is enabled in PWM mode.
MODE_CTRL	0	R/W	0	Light load mode 0: PFM with automatic transition into PWM operation. 1: Forced PWM operation.

3. VOUT (0x02), the default value is 0x4B.

Register Name	Bit	R/W	Default	Description
VC_GM	7:6	R/W	01	00: 6uS; 01:12uS; 10:18uS; 11:24uS
VOUT	5:0	R/W	001011	Output voltage setting, DC/DC boost/bypass mode change. It has an offset of 2.85V and a range from 2.85V to 5.5V with 50mV voltage step for VOUT. It is set to 3.4V by default. 000000: 2.850V 000001: 2.900V 000010: 2.950V …… 001011: 3.400V(Default) …… 101011: 5.000V …… 110100: 5.450V 110101~111111: 5.500V

4. ILIMSET (0x03), the default value is 0x16.

Register Name	Bit	R/W	Default	Description
RESERVED	7	R/W	0	Always reads back 0
BYPASS_WAY	6	R/W	0	Bypass path selection bit. 0: Only the Bypass switch opens. 1: The Bypass and High side MOSFETs open together.
ILIM_OFF	5	R/W	0	Enable/Disable Valley Inductor Current Limit in DC/DC boost mode. 0: Current Limit Enabled 1: Current Limit Disabled
SOFT-START	4	R/W	1	Soft-start current limit selection bit. 0: Boost soft-start current is limited according to ILIM bit settings 1: Boost soft-start current is limited to 2A inductor valley current
ILIM	3:0	R/W	0110	Inductor valley current limit in DC/DC boost mode. 0000: 4A 0001: 4.5A 0010: 5A 0011: 5.5A 0100: 6A 0101: 6.5A 0110: 7A(Default) 0111: 7.5A 1000: 8A 1001: 8.5A 1010~1111: 9A

5. STATUS (0x04), the default value is 0x00.

Register Name	Bit	R/W	Default	Description
TSD	7	R	0	0: Normal operation. 1: Thermal shutdown triggered. This flag is reset after readout.
RESERVED	6	R	0	Always reads back 0
DCDCMODE	5	R	0	Real-time detection the working states. 0: Device operates in PWM mode. 1: Device operates in PFM mode.
OPMODE	4	R	0	Real-time detection the operation mode. 0: Device operates in bypass mode. 1: Device operates in DC/DC mode.
ILIM_BYP	3	R	0	0: Normal operation. 1: Indicates that the bypass FET current limit has triggered in bypass mode. This flag is reset after readout.
ILIM_BST	2	R	0	0: Normal operation. 1: Indicates that the valley inductor current limit has triggered in DC/DC boost mode. This flag is reset after readout.
FAULT	1	R	0	0: Normal operation. 1: Indicates that a fault condition has occurred, including OTP, OCP, start-up fail, UVP and VIN OVP function This flag is reset after readout.
PGOOD	0	R	0	0: Indicates the output voltage is out of regulation. 1: Indicates the output voltage is within its nominal range. This bit is set if the converter is forced in bypass mode.

Layout Design

The layout design of SY87004 regulator is highly simplified. To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN} , C_{OUT}, L.

1) It is desirable to maximize the PCB copper area connecting to PGND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins VIN and PGND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the VIN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and PGND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

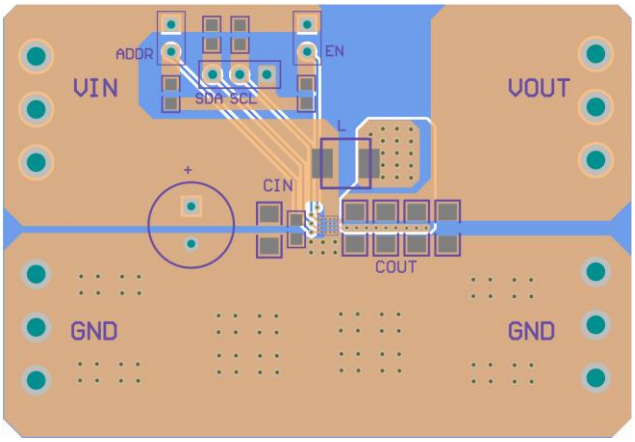
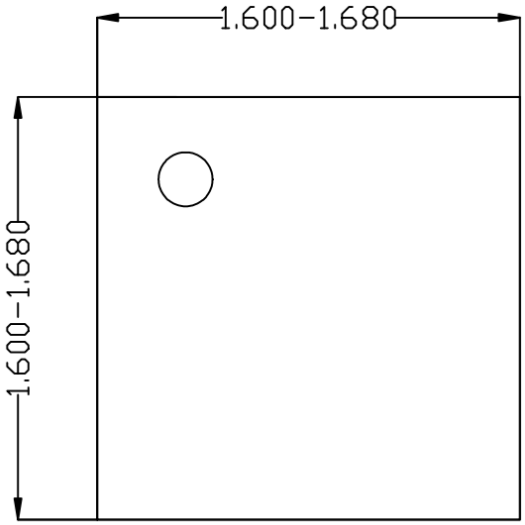
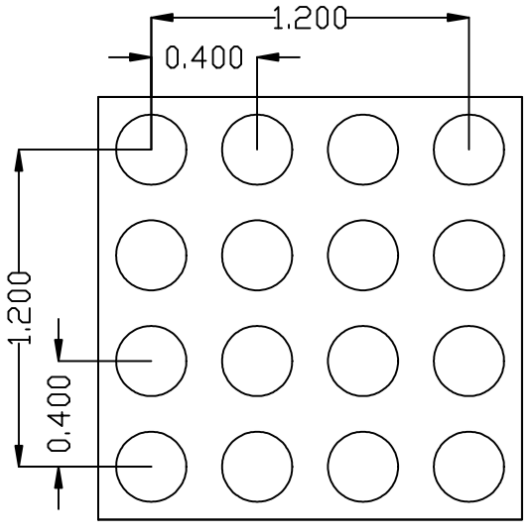


Figure 6. PCB Layout Suggestion

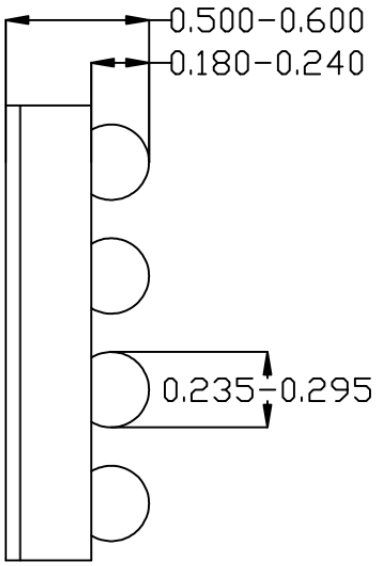
CSP1.65×1.65-16 Package Outline Drawing



Top View



Bottom View



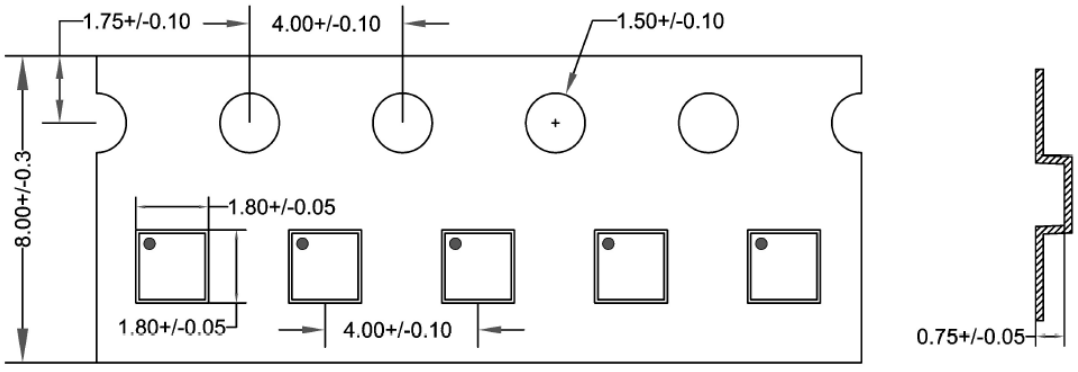
Side View

Notes: *All dimension in millimeter and exclude mold flash & metal burr.*

Tape and Reel Information

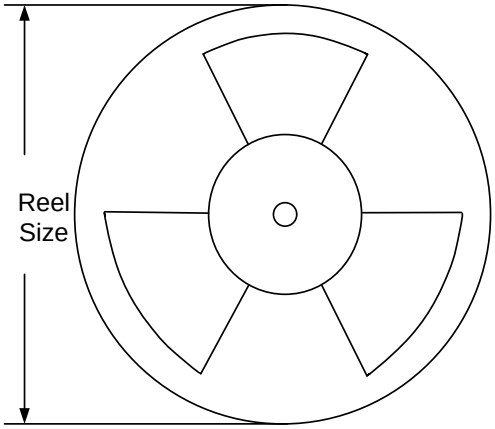
1. Tape Dimensions and Pin1 Orientation

CSP1.65×1.65-16



Feeding Direction ⟶

2. Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
CSP1.65×1.65-16	8	4	7"	400	160	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Sep. 17, 2025	Revision 1.0A	The Absolute Maximum Ratings of SCL, SDA, ADDR changed from (-0.3V to 3.6V) to (-0.3V to 6V) –(Page 3)
July 28, 2025	Revision 1.0	Initial Release

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